



## Product Change Notification / SYST-09AZKK894

---

### Date:

12-Apr-2024

### Product Category:

8-Bit Microcontrollers

### PCN Type:

Document Change

### Notification Subject:

PIC18F27/47/57Q84 Silicon Errata and Data Sheet Clarifications

### Affected CPNs:

[SYST-09AZKK894\\_Affected\\_CPN\\_04122024.pdf](#)

[SYST-09AZKK894\\_Affected\\_CPN\\_04122024.csv](#)

### Notification Text:

SYST-09AZKK894

Microchip has released a new Document for the PIC18F27/47/57Q84 Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at [PIC18F27/47/57Q84 Silicon Errata and Data Sheet Clarifications](#).

**Notification Status:** Final

#### Description of Change:

Removed data sheet clarifications, updated data sheet revision to current revision, added silicon revision C0.

**Impacts to Data Sheet:** None

**Reason for Change:** To improve productivity

**Change Implementation Status:** Complete

**Estimated First Ship Date:** 17 May 2024

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

[PIC18F27/47/57Q84 Silicon Errata and Data Sheet Clarifications](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

## Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our [PCN home page](#) select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the [PCN FAQ](#) section.

If you wish to change your PCN profile, including opt out, please go to the [PCN home page](#) select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

PIC18F27Q84-E/5N  
PIC18F27Q84-E/SO  
PIC18F27Q84-E/SP  
PIC18F27Q84-E/SS  
PIC18F27Q84-E/SSVAO  
PIC18F27Q84-I/5N  
PIC18F27Q84-I/SO  
PIC18F27Q84-I/SP  
PIC18F27Q84-I/SS  
PIC18F27Q84T-E/5N  
PIC18F27Q84T-E/5NV01  
PIC18F27Q84T-E/SSVAO  
PIC18F27Q84T-I/5N  
PIC18F27Q84T-I/SO  
PIC18F27Q84T-I/SS  
PIC18F47Q84-E/NHX  
PIC18F47Q84-E/P  
PIC18F47Q84-E/PT  
PIC18F47Q84-E/PTVAO  
PIC18F47Q84-I/NHX  
PIC18F47Q84-I/P  
PIC18F47Q84-I/PT  
PIC18F47Q84T-E/NHX  
PIC18F47Q84T-E/PT  
PIC18F47Q84T-E/PTVAO  
PIC18F47Q84T-I/NHX  
PIC18F47Q84T-I/PT  
PIC18F57Q84-E/6MX  
PIC18F57Q84-E/6MXVAO  
PIC18F57Q84-E/PT  
PIC18F57Q84-I/6MX  
PIC18F57Q84-I/PT  
PIC18F57Q84T-E/6MX  
PIC18F57Q84T-E/6MXVAO  
PIC18F57Q84T-I/6MX  
PIC18F57Q84T-I/PT

# PIC18F27/47/57Q84 Silicon Errata and Data Sheet Clarifications

## PIC18F27/47/57Q84



The PIC18F27/47/57Q84 devices that you have received conform functionally to the current device data sheet (DS40002213F), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F27/47/57Q84 silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

**Table 1.** Silicon Device Identification

Part Number	Device ID	Revision ID			
		B3	B4	B5	C0
PIC18F27Q84	0x9903	0xA043	0xA044	0xA045	0xA080
PIC18F47Q84	0x9904	0xA043	0xA044	0xA045	0xA080
PIC18F57Q84	0x9905	0xA043	0xA044	0xA045	0xA080



**Important:** Refer to the **Device/Revision ID** section in the current “**PIC18FXXQ84 Family Programming Specification**” (DS40002137) for more detailed information on Device Identification and Revision IDs for your specific device.

**Table 2. Silicon Issue Summary**

Module	Feature	Item No.	Issue Summary	Affected Revisions			
				B3	B4	B5	C0
UTMR	Hardware Reset condition	1.1.1	Reset does not happen at period match when the prescaler > 0	X			
	Level-triggered ERS Start/Reset condition	1.1.2	Dead zone exists in level-triggered Start/Reset condition when an ERS signal is generated due to an SFR access	X	X	X	X
	Hardware Reset condition	1.1.3	Reset does not happen at period match when the prescaler > 0 and the timer stops at period match (includes One Shot mode)	X	X	X	X
	Pulse output	1.1.4	Pulse output does not occur at period match when the prescaler = 1		X	X	X
	Clear Command	1.1.5	Clear Command May not Work Properly	X	X	X	X
I <sup>2</sup> C	Start and Stop Interrupt Function	1.2.1	The I <sup>2</sup> C Start and/or Stop flags may be set when I <sup>2</sup> C is enabled	X	X	X	X
SMT	Reset Bit	1.3.1	SMT Stops working if RST is set while prescaler setting is not zero	X	X	X	X
ADCC with Context	Double Sample Conversions	1.4.1	An unexpected acquisition time is added between the first and second conversion	X	X	X	X
PIC18 Core	FSR Shadow Registers	1.5.1	FSR shadow registers are not writable	X	X	X	X
UART	Stop bit	1.6.1	TXDE signal may go low before the STOP bit has been entirely transmitted	X	X	X	X
ICD	Single-Step Function (SSTEP)	1.7.1	Single Step function does not execute at Software Breakpoint.	X	X	X	X
PWM	PWM Mode	1.8.1	Wrong Duty Cycle for CCP Module	X	X	X	X
ICSP™	Low-Voltage Programming (LVP)	1.9.1	Low Voltage Programming is not possible when VDD is below BORV while BOR is enabled.	X	X	X	X
CAN FD	Masks/Filters	1.10.1	Filters 8-11 will erroneously accept incoming messages with SID of 0x000	X	X	X	
<b>Note:</b> Only those issues indicated in the last column apply to the current silicon revision.							

# 1. Silicon Errata Issues

## NOTICE

This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

## 1.1 Module: Universal Timer (UTMR) Module

### 1.1.1 Reset Does Not Happen at Period Match When the Prescaler > 0

When the prescaler > 0 and a hardware-based Reset event is selected (RESET = 'b01 or 'b10 or 'b11), the timer does not reset at period match.

#### Work around

1. Use prescaler = 0, or
2. When using prescaler > 0, clear the timer in software using the CLR command at every PR match interrupt.

#### Affected Silicon Revisions

B3	B4	B5	C0
X			

### 1.1.2 Dead Zone Exists in Level-Triggered Start/Reset Condition When an ERS Signal Is Generated Due to an SFR Access

When a level-triggered Start/Reset condition (START = 'b11 or RESET = 'b01) is triggered by an ERS signal generated by an SFR access such as TUxyPRL\_Write or TUxyTMRL\_Read or TUxyCRL\_Read (TUxyERS = 0x3E or 0x3F), there exists a dead zone in which subsequent SFR accesses will be missed. This dead zone is the period between the ZIF flag being set and the timer starting to count again. This can be monitored by checking either the RUN status bit or the level output of the timer.

#### Work around

The user must wait for the timer to start counting before accessing the period, counter and capture registers again.

#### Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

### 1.1.3 Reset Does Not Happen at Period Match When the Prescaler > 0 and the Timer Stops at Period Match

When the prescaler > 0 and the timer is configured to reset at a hardware-based event (RESET = 'b01 or 'b10 or 'b11) and stop at period match (STOP = 'b11), the timer stops at period match but does not reset (no pulse output occurs and ZIF interrupt is not generated).

#### Work around

1. Use prescaler = 0, or
2. When using prescaler > 0, clear the timer in software using the CLR command at every PR match interrupt.

**Affected Silicon Revisions**

B3	B4	B5	C0
X	X	X	X

**1.1.4 Pulse Output Does Not Occur at Period Match When the Prescaler = 1**

The timer output pulse will not occur at period match when prescaler = 1.

**Work around**

Use prescaler = 0 or prescaler > 1 when a pulse output is desired.

**Affected Silicon Revisions**

B3	B4	B5	C0
	X	X	X

**1.1.5 Clear Command May Not Work Properly in Asynchronous Mode**

When operating in asynchronous mode (CSYNC = 0), setting the Clear Command bit (CLR = 1) may not clear the Timer Counter register value.

**Work around**

Use the Universal Timer module in synchronous mode (CSYNC = 1) when Clear Command bit (CLR) is being used.

**Affected Silicon Revisions**

B3	B4	B5	C0
X	X	X	X

**1.2 Module: Inter-Integrated Circuit (I<sup>2</sup>C)****1.2.1 The I<sup>2</sup>C Start and/or Stop Flags May Be Set When I<sup>2</sup>C Is Enabled**

When I<sup>2</sup>C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I<sup>2</sup>C interrupts if enabled.

**Work around**

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I<sup>2</sup>C module.
3. Wait 250 ns + six instruction cycles ( $F_{OSC}/4$ ).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions if used.

```

I2CxPIEBits.SCIE = 0;           // Disable Start condition interrupt
I2CxPIEBits.PCIE = 0;           // Disable Stop condition interrupt
I2CxCON0bits.EN = 1;            // Enable I2C
Delay();                         // Wait for 250 ns + 6 instruction cycles ( $F_{OSC}/4$ )
I2CxPIRbits.SCIF = 0;           // Clear the Start condition interrupt flags
I2CxPIRbits.PCIF = 0;           // Clear the Stop condition interrupt flags
I2CxPIEBits.SCIE = 1;           // Enable Start condition interrupt if used
I2CxPIEBits.PCIE = 1;           // Enable Stop condition interrupt if used

```

**Affected Silicon Revisions**

B3	B4	B5	C0
X	X	X	X

## 1.3 Module: Signal Measurement Timer (SMT)

### 1.3.1 Reset Bit

If the SMT clock prescaler is set to any value other than '00', setting the RST bit will cause the module to stop working. The RST bit will remain at the value '1', the counter will not increment, and no interrupts will be generated. The problem is cleared by turning the module off and on or by performing a device reset.

#### Work around

##### Method 1:

Do not set the RST bit; manual reset is usually not required for typical operation because the measurement logic will reset the counter automatically.

##### Method 2:

Write zero to the counter manually. Either disable the module or the clock before using this method.

##### Method 3:

Use 1:1 prescaler (PS = 00).

##### Method 4:

Use the CLKREF subsystem to provide a prescaled clock and set PS = 00.

#### Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

## 1.4 Module: Analog-to-Digital Converter with Computation and Context Switching (ADC)

### 1.4.1 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = 1) with no Precharge time (ADPRE = 0) and no Acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

#### Work around

##### Method 1:

Disable Double Sample Conversion (DSEN = 0) and perform two single conversions back to back.

##### Method 2:

If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

#### Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X



## 1.5 Module: PIC18 Core

### 1.5.1 FSR Shadow Registers Are Not Writable

Writing to the FSR Shadow Registers does not result in accurate values being stored in the registers. Consequently, reading the FSR Shadow Registers after they have been written will return inaccurate data.

#### Work around

Writes to the FSR shadow registers can be performed safely using the following steps:

1. Save regular FSR2 value into RAM.
2. Write the regular FSR2 with the targeted value minus the computed offset ( $IR[6:0] + 1$ , see below).
3. Write the shadow FSRxL (data doesn't matter); this will clock the shadow FSR with the FSR computed offset value.
4. Decrement FSR2 value by 1 since FSRxH increments the address by 1 ( $IR[6:0]$ ).
5. Write FSRxH.
6. Restore the regular FSR2 from the stored RAM value.

The FSR shadow should have the value desired and the regular FSR should have the original value.

#### Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

## 1.6 Module: Universal Asynchronous Receiver Transmitter (UART)

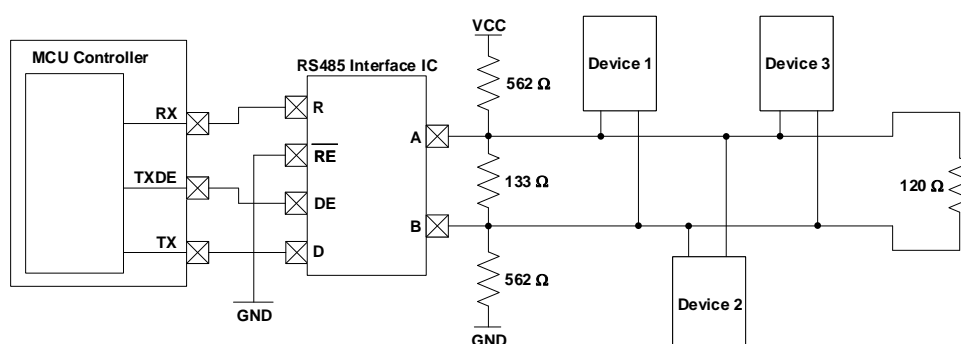
### 1.6.1 UART TXDE Signal May Go Low before the STOP Bit Has Been Entirely Transmitted

The UART Transmit Drive Enable (TXDE) signal could potentially transition into a low state before the UART STOP bit has been entirely transmitted due to the effects of parasitic capacitance on the TX line. In some applications, this could result in communication being prematurely terminated due to the TXDE bit going low before the STOP bit has had enough time to settle.

#### Work around

To ensure that the STOP bit settles into its final logic state before the TXDE signal transitions low, a biasing circuit can be implemented. A biasing circuit allows the TX line to either be driven high or low, rather than being left in a floating tri-state mode where prolonged rise or fall times could lead to communication being disrupted. This bias circuit should only be implemented on one end of the serial bus, and a termination resistor should be used on the other end. The figure below shows an example of a bias circuit that can be used to achieve this.

Please note that the resistor values used in this circuit are recommendations and that the actual resistor values required may vary based on the application.



**Affected Silicon Revisions**

B3	B4	B5	C0
X	X	X	X

**1.7 Module: In-Circuit Debug****1.7.1 Single Step Function Does Not Execute at SW Breakpoint**

The SW breakpoint occurs, but the SSTEP function does not execute at the breakpoint.

**Work around**

None.

**Affected Silicon Revisions**

B3	B4	B5	C0
X	X	X	X

**1.8 Module: Pulse-Width Modulation (PWM)****1.8.1 Wrong Duty Cycle for CCP Module**

While in PWM mode and the Timer2 prescaler is configured to 1:1, the duty cycle of the PWM output is as expected. When the Timer2 prescaler is changed to a value other than 1:1 while T2PR = 0 (PWM resolution of two bits), the expected duty cycle is wrong. The corrected duty cycle values are shown in the table below.

**Table 1-1.** Corrected Duty Cycle Values

Prescaler/CCPR	0	1	2	3	4
1:1	0%	25%	50%	75%	100%
1:2	50%	75%	50%	75%	100%
1:4...1:128	75%	75%	75%	75%	100%

**Work around**

None.

**Affected Silicon Revisions**

B3	B4	B5	C0
X	X	X	X

**1.9 Module: Low-Voltage In-Circuit Serial Programming™ (LVP)****1.9.1 Low-Voltage Programming Not Possible**

Low-Voltage Programming is not possible when  $V_{DD}$  is below the selected BORV voltage level while BOR is enabled.

**Work around****Method 1:**

Disable BOR to use Low-Voltage Programming.

**Method 2:**

Raise  $V_{DD}$  above the selected BORV level while using Low-Voltage Programming.

**Affected Silicon Revisions**

B3	B4	B5	C0
----	----	----	----

X	X	X	X
---	---	---	---

## 1.10 Module: Controller Area Network Flexible Data-Rate (CAN FD) Module

### 1.10.1 Filters 8-11 Will Erroneously Accept Incoming Messages With SID of 0x000

When using the CAN RX filters 8-11, any messages where the incoming message after masking is SID 0x000 will trigger a filter match, regardless of the filter ID settings. For example: an incoming message with ID of 0x350 and a mask setting of 0x00F will trigger a filter match regardless of other mask/filter settings. This will occur even if the filter is set to only accept extended IDs.

#### Work around

If using CAN RX filters 8-11, check the FILHIT bits of C1VECH (or the received message object) upon message reception. If the value of FILHIT is greater than 11, then this error has occurred and the message can be ignored and discarded.

#### Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	

## 2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (40002213F):

**Note:**

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

### 3. Appendix A: Revision History

Doc. Rev.	Date	Comments
G	04/2024	Removed data sheet clarifications, updated data sheet revision to current revision, added silicon revision C0.
F	05/2023	Added silicon issue 1.1.5 to UTMR module as well as new errata 1.2.1-1.10.1 . Added new errata entry to UTMR module. Added data sheet clarifications 2.2, 2.3, 2.4, and 2.5.
E	06/2022	Added Data Sheet Clarification 2.1.
D	03/2021	Adding silicon issue 1.1.4.
C	01/2021	Added new silicon Rev B4 and silicon issue 1.1.3. Minor editorial corrections.
B	11/2020	Changed to released silicon revision.
A	06/2020	Initial document release.

## Microchip Information

### The Microchip Website

Microchip provides online support via our website at [www.microchip.com/](http://www.microchip.com/). This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

### Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to [www.microchip.com/pcn](http://www.microchip.com/pcn) and follow the registration instructions.

### Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: [www.microchip.com/support](http://www.microchip.com/support)

### Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

### Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure

that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at [www.microchip.com/en-us/support/design-help/client-support-services](http://www.microchip.com/en-us/support/design-help/client-support-services).

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

## Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, TimeCesium, TimeHub, TimePictra, TimeProvider, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, EyeOpen, GridTime, IdealBridge, IGaT, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, MarginLink, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mSiC, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, Power MOS IV, Power MOS 7, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQL, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, Turing, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2020-2024, Microchip Technology Incorporated and its subsidiaries. All Rights Reserved.

ISBN: 978-1-6683-4273-2

## Quality Management System

For information regarding Microchip's Quality Management Systems, please visit [www.microchip.com/quality](http://www.microchip.com/quality).



# Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
<b>Corporate Office</b> 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: <a href="http://www.microchip.com/support">www.microchip.com/support</a> Web Address: <a href="http://www.microchip.com">www.microchip.com</a>	<b>Australia - Sydney</b> Tel: 61-2-9868-6733 <b>China - Beijing</b> Tel: 86-10-8569-7000 <b>China - Chengdu</b> Tel: 86-28-8665-5511 <b>China - Chongqing</b> Tel: 86-23-8980-9588 <b>China - Dongguan</b> Tel: 86-769-8702-9880 <b>China - Guangzhou</b> Tel: 86-20-8755-8029 <b>China - Hangzhou</b> Tel: 86-571-8792-8115 <b>China - Hong Kong SAR</b> Tel: 852-2943-5100 <b>China - Nanjing</b> Tel: 86-25-8473-2460 <b>China - Qingdao</b> Tel: 86-532-8502-7355 <b>China - Shanghai</b> Tel: 86-21-3326-8000 <b>China - Shenyang</b> Tel: 86-24-2334-2829 <b>China - Shenzhen</b> Tel: 86-755-8864-2200 <b>China - Suzhou</b> Tel: 86-186-6233-1526 <b>China - Wuhan</b> Tel: 86-27-5980-5300 <b>China - Xian</b> Tel: 86-29-8833-7252 <b>China - Xiamen</b> Tel: 86-592-2388138 <b>China - Zhuhai</b> Tel: 86-756-3210040	<b>India - Bangalore</b> Tel: 91-80-3090-4444 <b>India - New Delhi</b> Tel: 91-11-4160-8631 <b>India - Pune</b> Tel: 91-20-4121-0141 <b>Japan - Osaka</b> Tel: 81-6-6152-7160 <b>Japan - Tokyo</b> Tel: 81-3-6880-3770 <b>Korea - Daegu</b> Tel: 82-53-744-4301 <b>Korea - Seoul</b> Tel: 82-2-554-7200 <b>Malaysia - Kuala Lumpur</b> Tel: 60-3-7651-7906 <b>Malaysia - Penang</b> Tel: 60-4-227-8870 <b>Philippines - Manila</b> Tel: 63-2-634-9065 <b>Singapore</b> Tel: 65-6334-8870 <b>Taiwan - Hsin Chu</b> Tel: 886-3-577-8366 <b>Taiwan - Kaohsiung</b> Tel: 886-7-213-7830 <b>Taiwan - Taipei</b> Tel: 886-2-2508-8600 <b>Thailand - Bangkok</b> Tel: 66-2-694-1351 <b>Vietnam - Ho Chi Minh</b> Tel: 84-28-5448-2100	<b>Austria - Wels</b> Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 <b>Denmark - Copenhagen</b> Tel: 45-4485-5910 Fax: 45-4485-2829 <b>Finland - Espoo</b> Tel: 358-9-4520-820 <b>France - Paris</b> Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 <b>Germany - Garching</b> Tel: 49-8931-9700 <b>Germany - Haan</b> Tel: 49-2129-3766400 <b>Germany - Heilbronn</b> Tel: 49-7131-72400 <b>Germany - Karlsruhe</b> Tel: 49-721-625370 <b>Germany - Munich</b> Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 <b>Germany - Rosenheim</b> Tel: 49-8031-354-560 <b>Israel - Ra'anana</b> Tel: 972-9-744-7705 <b>Italy - Milan</b> Tel: 39-0331-742611 Fax: 39-0331-466781 <b>Italy - Padova</b> Tel: 39-049-7625286 <b>Netherlands - Drunen</b> Tel: 31-416-690399 Fax: 31-416-690340 <b>Norway - Trondheim</b> Tel: 47-72884388 <b>Poland - Warsaw</b> Tel: 48-22-3325737 <b>Romania - Bucharest</b> Tel: 40-21-407-87-50 <b>Spain - Madrid</b> Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 <b>Sweden - Gothenberg</b> Tel: 46-31-704-60-40 <b>Sweden - Stockholm</b> Tel: 46-8-5090-4654 <b>UK - Wokingham</b> Tel: 44-118-921-5800 Fax: 44-118-921-5820