Wideband, Unity-Gain Stable, Fast Settling Op Amp

**AD841**

**FEATURES**

**AC PERFORMANCE**
- Unity-Gain Bandwidth: 40 MHz
- Fast Settling: 110 ns to 0.01%
- Slew Rate: 300 V/µs
- Full Power Bandwidth: 4.7 MHz for 20 V p-p into a 500 Ω Load

**DC PERFORMANCE**
- Input Offset Voltage: 1 mV max
- Input Voltage Noise: 13 nV/√Hz typ
- Open-Loop Gain: 45 V/mV into a 1 kΩ Load
- Output Current: 50 mA min
- Supply Current: 12 mA max

**APPLICATIONS**
- High Speed Signal Conditioning
- Video and Pulse Amplifiers
- Data Acquisition Systems
- Line Drivers
- Active Filters
- Available in 14-Pin Plastic DIP Hermetic Cerdip, 12-Pin TO-8 Metal Can and 20-Pin LCC Packages
- Chips and MIL-STD-883B Parts Available

**PRODUCT DESCRIPTION**

The AD841 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This high speed/high precision family includes, among others, the AD840, which is stable at a gain of 10 or greater, and the AD842, which is stable at a gain of two or greater and has 100 mA minimum output current drive. These devices are fabricated using Analog Devices’ junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 40 MHz unity-gain bandwidth product, the AD841 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in 110 ns for a 10 volt step.

Unlike many high frequency amplifiers, the AD841 requires no external compensation. It remains stable over its full operating temperature range. It also offers a low quiescent current of 12 mA maximum, a minimum output current drive capability of 50 mA, a low input voltage noise of 13 nV/√Hz and low input offset voltage of 1 mV maximum.

The 300 V/µs slew rate of the AD841, along with its 40 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is well suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD841 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD841 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

**APPLICATION HIGHLIGHTS**

1. The high slew rate and fast settling time of the AD841 make it ideal for DAC and ADC buffers, and all types of video instrumentation circuitry.
2. The AD841 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth performance previously available only in hybrids.
3. The AD841’s thermally balanced layout and the speed of the CB process allow the AD841 to settle to 0.01% in 110 ns without the long “tails” that occur with other fast op amps.
4. Laser wafer trimming reduces the input offset voltage to 1 mV max on the K grade, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for additional versatility.
5. The AD841 is an enhanced replacement for the HA2541.
## AD841—SPECIFICATIONS

(@ +25°C and ±15 V dc, unless otherwise noted)

<table>
<thead>
<tr>
<th>Model</th>
<th>Conditions</th>
<th>AD841J</th>
<th>AD841K</th>
<th>AD841S</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INPUT OFFSET VOLTAGE(^2)</td>
<td>T(<em>{\text{MIN}})–T(</em>{\text{MAX}})</td>
<td>0.8</td>
<td>2.0</td>
<td>5.0</td>
</tr>
<tr>
<td>Offset Drift</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INPUT BIAS CURRENT</td>
<td>T(<em>{\text{MIN}})–T(</em>{\text{MAX}})</td>
<td>3.5</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>T(<em>{\text{MIN}})–T(</em>{\text{MAX}})</td>
<td>0.1</td>
<td>0.4</td>
<td>0.5</td>
</tr>
<tr>
<td>INPUT CHARACTERISTICS</td>
<td>Differential Mode</td>
<td>200</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Input Resistance</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INPUT VOLTAGE RANGE</td>
<td>Common Mode</td>
<td>±10</td>
<td>12</td>
<td>86</td>
</tr>
<tr>
<td>Common-Mode Rejection</td>
<td>V(_{\text{CM}}) = ±10 V</td>
<td>80</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INPUT VOLTAGE NOISE</td>
<td>f = 1 kHz</td>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 Hz to 10 MHz</td>
<td>47</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OPEN-LOOP GAIN</td>
<td>V(_{\text{O}}) = ±10 V</td>
<td>25</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>R(_{\text{LOAD}}) ≥ 500 Ω</td>
<td>T(<em>{\text{MIN}})–T(</em>{\text{MAX}})</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUTPUT CHARACTERISTICS</td>
<td>Voltage</td>
<td>±10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>V(_{\text{OUT}}) = ±10 V</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUTPUT RESISTANCE</td>
<td>Open Loop</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FREQUENCY RESPONSE</td>
<td>Unity Gain Bandwidth</td>
<td>V(_{\text{OUT}}) = 90 mV p-p</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Full Power Bandwidth(^3)</td>
<td>V(_{\text{O}}) = 20 V p-p</td>
<td>3.1</td>
<td>4.7</td>
</tr>
<tr>
<td></td>
<td>R(_{\text{LOAD}}) ≥ 500 Ω</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Rise Time(^4)</td>
<td>A(_{\text{V}}) = –1</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Overshoot(^4)</td>
<td>A(_{\text{V}}) = –1</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Slew Rate(^4)</td>
<td>A(_{\text{V}}) = –1</td>
<td>200</td>
<td>300</td>
</tr>
<tr>
<td></td>
<td>Settling Time – 10 V Step</td>
<td>A(_{\text{V}}) = –1</td>
<td>90</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>to 0.1%</td>
<td>110</td>
<td>110</td>
</tr>
<tr>
<td>OVERDRIVE RECOVERY</td>
<td>–Overdrive</td>
<td>200</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>+Overdrive</td>
<td>700</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIFFERENTIAL GAIN</td>
<td>f = 4.4 MHz</td>
<td>0.03</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 4.4 MHz</td>
<td>0.022</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Differential Phase</td>
<td>0.03</td>
<td></td>
<td></td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td>Rated Performance</td>
<td>V(_{\text{O}}) = ±5 V to ±18 V</td>
<td>±5</td>
<td>±18</td>
</tr>
<tr>
<td></td>
<td>Operating Range</td>
<td>T(<em>{\text{MIN}})–T(</em>{\text{MAX}})</td>
<td>11</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>Quiescent Current</td>
<td>V(_{\text{O}}) = ±5 V to ±18 V</td>
<td>86</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>Power Supply Rejection Ratio</td>
<td>T(<em>{\text{MIN}})–T(</em>{\text{MAX}})</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>TEMPERATURE RANGE</td>
<td>Rated Performance(^5)</td>
<td>0</td>
<td></td>
<td>+75</td>
</tr>
<tr>
<td></td>
<td>Package Options</td>
<td>AD841JQ</td>
<td>AD841KQ</td>
<td>AD841S</td>
</tr>
<tr>
<td></td>
<td>LCC (E-20A)</td>
<td>AD841JQ</td>
<td>AD841KQ</td>
<td>AD841S</td>
</tr>
<tr>
<td></td>
<td>Cerdip (Q-14)</td>
<td>AD841JQ</td>
<td>AD841KQ</td>
<td>AD841S</td>
</tr>
<tr>
<td></td>
<td>Plastic (N-14)</td>
<td>AD841JQ</td>
<td>AD841KQ</td>
<td>AD841S</td>
</tr>
<tr>
<td></td>
<td>TO-8 (H-12)</td>
<td>AD841JQ</td>
<td>AD841KQ</td>
<td>AD841S</td>
</tr>
<tr>
<td></td>
<td>Chips</td>
<td>AD841JQ</td>
<td>AD841KQ</td>
<td>AD841S</td>
</tr>
</tbody>
</table>

**NOTES**


\(^2\)Input offset voltage specifications are guaranteed after 5 minutes at T\(_{\text{A}}\) = +25°C.

\(^3\)Full power bandwidth = Slew Rate/2π V\(_{\text{PEAK}}\).

\(^4\)S grade T\(_{\text{MIN}}\)–T\(_{\text{MAX}}\) specifications are tested with automatic test equipment at T\(_{\text{A}}\) = –55°C and T\(_{\text{A}}\) = +125°C.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

REV. B
ABSOLUTE MAXIMUM RATINGS\(^1\)

Supply Voltage ........................................... ±18 V

Internal Power Dissipation\(^2\)
  TO-8 (H) ........................................... 1.4 W
  Plastic (N) ........................................... 1.5 W
  Cerdip (Q) ........................................... 1.3 W

Input Voltage ........................................... ±Vs

Differential Input Voltage ................................ ±6 V

Storage Temperature Range
  Q, H, E ........................................... –65°C to +150°C
  N ........................................... –65°C to +125°C

Junction Temperature ................................ +175°C

Lead Temperature Range (Soldering 60 sec) .......... +300°C

NOTES
\(^1\)Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

\(^2\)Maximum internal power dissipation is specified so that T\(_J\) does not exceed +175°C at an ambient temperature of +25°C.

Thermal Characteristics:

\(\theta_{JC}\) \(\theta_{JA}\) \(\theta_{SA}\)
Cerdip Package 35°C/W 110°C/W 38°C/W
TO-8 Package 30°C/W 100°C/W 37°C/W
Plastic Package 30°C/W 100°C/W
LCC Package 35°C/W 150°C/W

Recommended Heat Sink:
Aavid Engineering© #602B

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).
AD841—Typical Characteristics (at +25°C and \( V_S = \pm 15 \) V, unless otherwise noted)

Figure 1. Input Common-Mode Range vs. Supply Voltage

Figure 2. Output Voltage Swing vs. Supply Voltage

Figure 3. Output Voltage Swing vs. Load Resistance

Figure 4. Quiescent Current vs. Supply Voltage

Figure 5. Input Bias Current vs. Temperature

Figure 6. Output Impedance vs. Frequency

Figure 7. Quiescent Current vs. Temperature

Figure 8. Short-Circuit Current Limit vs. Temperature

Figure 9. Gain Bandwidth Product vs. Temperature
Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

Figure 11. Open-Loop Gain vs. Supply Voltage

Figure 12. Power Supply Rejection vs. Frequency

Figure 13. Common-Mode Rejection vs. Frequency

Figure 14. Large Signal Frequency Response

Figure 15. Output Swing and Error vs. Settling Time

Figure 16. Harmonic Distortion vs. Frequency

Figure 17. Slew Rate vs. Temperature

Figure 18. Input Voltage Noise Spectral Density
OFFSET NULLING
The input offset voltage of the AD841 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

Figure 21. Offset Nulling (DIP Pinout)

INPUT CONSIDERATIONS
An input resistor (RIN in Figure 20) is recommended in circuits where the input to the AD841 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into the input.

For high performance circuits it is recommended that a resistor (Rb in Figures 19 and 20) be used to reduce bias current errors by matching the impedance at each input. The output voltage error caused by the offset current is more than an order of magnitude less than the error present if the bias current error is not removed.

AD841 SETTLING TIME
Figures 22 and 24 show the settling performance of the AD841 in the test circuit shown in Figure 23.

Settling time is defined as:

The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing and (4) linear settling to within the specified error band.
Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

Measurement of the AD841’s 0.01% settling in 110 ns was accomplished by amplifying the error signal from a false summing junction with a very high speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 500 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp gains the error from the false summing junction by 10, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the “long term” stability of the settling characteristics of the AD841 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.
**USING A HEAT SINK**

The AD841 draws less quiescent power than most precision high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads, the current to the load can be 4 to 5 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

**TERMINATED LINE DRIVER**

The AD841 functions very well as a high speed line driver of either terminated or unterminated cables. Figure 26 shows the AD841 driving a doubly terminated cable in a follower configuration. The AD841 maintains a typical slew rate of 300 V/µs, which means it can drive a ±10 V, 4.7 MHz signal or a ±3 V, 15.9 MHz signal.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. A back-termination resistor (R_BT, also equal to the characteristic impedance of the cable) may be placed between the AD841 output and the cable in order to damp any stray signals caused by a mismatch between R_T and the cable’s characteristic impedance. This will result in a “cleaner” signal, but since 1/2 the output voltage will be dropped across R_BT, the op amp must supply double the output signal required if there is no back termination. Therefore the full power bandwidth is cut in half.

If termination is not used, cables appear as capacitive loads. If this capacitive load is large, it should be decoupled from the AD841 by a resistor in series with the output (see above: Driving a Capacitive Load).

**OVERDRIVE RECOVERY**

Figure 27 shows the overdrive recovery capability of the AD841. Typical recovery time is 200 ns from negative overdrive and 700 ns from positive overdrive.