Product Change Notification / SYST-24EFGB055

Date:

03-May-2024

Product Category:

8-Bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ATtiny202/204/402/404/406 Silicon Errata and Data Sheet Clarification Documents

Affected CPNs:

SYST-24EFGB055_Affected_CPN_05032024.pdf
SYST-24EFGB055_Affected_CPN_05032024.csv

Notification Text:

SYST-24EFGB055

Microchip has released a new Document for the ATtiny202/204/402/404/406 Silicon Errata and Data Sheet Clarification Documents of devices. If you are using one of these devices please read the document located at ATtiny202/204/402/404/406 Silicon Errata and Data Sheet Clarification Documents.

ERRATA - ATtiny202/204/402/404/406 Silicon Errata and Data Sheet Clarification Documents

Notification Status: Final

Description of Change:

• Document:
– Editorial updates
• Added new data sheet clarifications:
– SPI:
• 3.1.1. SPI Clock
– Electrical Characteristics:
• 3.2.1. Power Consumption. The Power Consumption in Power-Down (Max 25°C) reduced from 2 µA to 0.6 µA.
• 3.2.3. SPI - Timing Characteristics
• 3.2.4. Programming Time

Impacts to Data Sheet: None

Reason for Change: To improve productivity.

Change Implementation Status: Complete

Date Document Changes Effective: 03 May 2024

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ATtiny202/204/402/404/406 Silicon Errata and Data Sheet Clarification Documents

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

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Affected Catalog Part Numbers (CPN)

ATTINY202-SSF
ATTINY202-SSFR
ATTINY202-SSN
ATTINY202-SSNR
ATTINY202-SSNRA2
ATTINY204-SSF
ATTINY204-SSFR
ATTINY204-SSN
ATTINY204-SSNR
ATTINY402-SSF
ATTINY402-SSFR
ATTINY402-SSN
ATTINY402-SSNR
ATTINY402-SSNRA3
ATTINY404-SSF
ATTINY404-SSFR
ATTINY404-SSN
ATTINY404-SSNR
ATTINY406-MF
ATTINY406-MFR
ATTINY406-MN
ATTINY406-MNR
ATTINY406-SF
ATTINY406-SFR
ATTINY406-SN
ATTINY406-SNR

Silicon Errata and Data Sheet Clarifications

ATtiny202/204/402/404/406

The ATtiny202/204/402/404/406 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002318), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny202/204/402/404/406 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002318) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- \- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. B(1)	Rev. C
Device	2.2.1. The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)	X	-
	2.2.2. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values	X	X
	2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces	X	X
ADC	2.3.1. One Extra Measurement Performed After Disabling ADC Free-Running Mode	X	X
	2.3.2. ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	X	X
	2.3.3. ADC Performance Degrades with CLKADC Above 1.5 MHz and VDD < 2.7V	X	X
	2.3.4. Pending Event Stuck When Disabling the ADC	X	X
CCL	2.4.1. Connecting LUTs in Linked Mode Requires OUTEN Set to '1'	X	X
	2.4.2. D-latch is Not Functional	X	X
	2.4.3. The CCL Must be Disabled to Change the Configuration of a Single LUT	X	X
NVMCTRL	2.5.1. Wrong Reset Value of NVMCTRL.CTRLA Register	X	X
PORTMUX	2.6.1. Selecting Alternative Output Pin for TCA0 Waveform Output 0-2 also Changes Waveform Output 3-5	X	X
RTC	2.7.1. Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler Counter	X	X
	2.7.2. Disabling the RTC Stops the PIT	X	X
TCA	2.8.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	X
TCB	2.9.1. Minimum Event Duration Must Exceed the Selected Clock Period	X	X
	2.9.2. The TCA Restart Command Does Not Force a Restart of TCB	X	X
	2.9.3. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X	X
USART	2.10.1. TXD Pin Override Not Released When Disabling the Transmitter	X	X
	2.10.2. Frame Error on a Previous Message May Cause False Start Bit Detection	X	X
	2.10.3. Full Range Duty Cycle Not Supported When Validating LIN Sync Field	X	X
	2.10.4. Open-Drain Mode Does Not Work When TXD is Configured as Output	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)

The temperature sensor is not calibrated on parts with date code 727/728 (used on QFN packages) and 1728 (used on SOIC packages).

Work Around

If temperature sensor calibration data is required, devices with the affected date code may be returned through the Microchip RMA service. Devices with this date code are no longer shipped by Microchip.

Affected Silicon Revisions

Rev. B	Rev. C
X	-

2.2.2 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to '1' prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

Work Around

Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCKEN in CLKCTRL.MCLKLOCK to '1' when using the OSC20M oscillator as the Main Clock source.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.2.3 Write Operation Lost if Consecutive Writes to Specific Address Spaces

An ST/STD/STS instruction to address > = 64 followed by an ST/STD instruction to address < 64 or SLPCTRL.CTRLA register will cause loss of the last write.

Work Around

To avoid loss of write operation, use one of the following workarounds depending on address space:

- Insert an NOP instruction before writing to address < 64, or use the OUT instruction instead of ST/STD
- Insert an NOP instruction before writing to SLPCTRL.CTRLA register

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.3 ADC - Analog-to-Digital Converter

2.3.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work Around

Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.3.2 ADC Functionality Cannot be Ensured with CLK_{ADC} Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK_{ADC} > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'.

Work Around

If ADC is operated with CLK_{ADC} > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle).

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.3.3 ADC Performance Degrades with CLK_{ADC} Above 1.5 MHz and V_{DD} < 2.7V

The ADC INL performance degrades if CLK_{ADC} > 1.5 MHz and ADCn.CALIB.DUTYCYC is set to '0' for V_{DD} < 2.7V.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.3.4 Pending Event Stuck When Disabling the ADC

If the ADC is disabled during an event-triggered conversion, the event will not be cleared.

Work Around

Clear ADC.EVCTRL.STARTEI and wait for the conversion to complete before disabling the ADC.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.4 CCL - Configurable Custom Logic

2.4.1 Connecting LUTs in Linked Mode Requires OUTEN Set to '1'

Connecting the LUTs in linked mode requires LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

Work Around

Use an event channel to link the LUTs, or do not use the corresponding I/O pin for other purposes.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.4.2 D-latch is Not Functional

The CCL D-latch is not functional.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.4.3 The CCL Must be Disabled to Change the Configuration of a Single LUT

The CCL peripheral must first be disabled (write ENABLE in CCL.CTRLA to '0') to reconfigure a LUT. Writing ENABLE to '0' will disable all the LUTs and affect the LUTs not under reconfiguration.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.5 NVMCTRL - Nonvolatile Memory Controller

2.5.1 Wrong Reset Value of NVMCTRL.CTRLA Register

In some cases, the NVMCTRL.CTRLA reset value will not be '0x00'. Even reserved bits can be read as '1' after Reset.

Work Around

Ignore the initial value.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.6 PORTMUX - Port Multiplexer

2.6.1 Selecting Alternative Output Pin for TCA0 Waveform Output 0-2 also Changes Waveform Output 3-5

Selecting the alternative output pin for TCA0 in PORTMUX.CTRLC does not work as described when TCA0 operates in split mode.

- Writing PORTMUX.CTRLC bit 0 to '1' will shift the pin position for both WO0 and WO3
- Writing PORTMUX.CTRLC bit 1 to '1' will shift the pin position for both WO1 and WO4
- Writing PORTMUX.CTRLC bit 2 to '1'will shift the pin position for both WO2 and WO5

PORTMUX.CTRLC[5:3] are non-functional.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

Note: Not applicable to 8-pin devices.

2.7 RTC - Real-Time Counter

2.7.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler Counter

Any write to the RTC.CTRLA register resets the 15-bit prescaler counter. The next count occurs ½ prescaler period after the reset, resulting in a period length of 0.5 to 1.5 times the expected period, depending on when the reset occurs.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.7.2 Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

Work Around

Do not disable the RTC or the PIT if any of the modules are used.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.8 TCA - Timer/Counter A

2.8.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to the NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the direction to default. The default is counting upwards.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.9 TCB - Timer/Counter B

2.9.1 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement*.

Work Around

Ensure that the high/low period of input events is equal to or longer than the selected clock source (CLKSEL in TCBn.CTRLA) period.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.9.2 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force restarting the TCB when TCB is running in SYNCUPD mode. TCB is restarted only after a TCA OVF.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.9.3 CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB operates in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.10 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.10.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

Work Around

There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.10.2 Frame Error on a Previous Message May Cause False Start Bit Detection

A false start bit detection will trigger if receiving a frame with RXDATAH.FERR set and reading the RXDATAL before the RxD line goes high.

Work Around

Wait for the RXD pin to go high before reading RXDATA by, for instance, polling the bit in PORTn.IN where the RXD pin is located.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.10.3 Full Range Duty Cycle Not Supported When Validating LIN Sync Field

For the LIN sync field, the USART validates each bit to be within ±15% instead of the time between falling edges as described in the LIN specification, which allows a minimum duty cycle of 43.5% and a maximum duty cycle of 57.5%.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.10.4 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002318).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 SPI - Serial Peripheral Interface

3.1.1 SPI Clock

Clarifications regarding the SPI clock have been made in the *Operation - Client Mode* and *Operation - Client Mode - Buffer Mode* sections. Functional changes are shown in **bold**.

24.3.2.2 Client Mode

In Client mode, the SPI peripheral receives the SPI clock and Client Select from a Host. Client mode supports three operational modes: One Normal mode and two configurations for the Buffered mode. In Client mode, the control logic will sample the incoming signal on the SCK pin. ~~**To ensure correct sampling of this clock signal, the minimum low and high periods must each be longer than two peripheral clock cycles.**~~

24.3.2.2.2 Buffer Mode

To avoid data collisions, the SPI peripheral can be configured in Buffered mode by writing a '1' to the Buffer Mode Enable (BUFEN) bit in the Control B (SPIn.CTRLB) register. In this mode, the SPI has additional interrupt flags and extra buffers. The extra buffers are shown in *Figure 24-1*. There are two different modes for the Buffer mode, selected with the Buffer mode Wait for Receive (BUFWR) bit. The two different modes are described below with timing diagrams.

Note: When operating as a client in Buffered mode and the SPI clock is close to maximum frequency, the client may not be able to set up data in time for the first sample edge during back-to-back transfers. Refer to the *Electrical Characteristics - SPI* section for details.

3.2 Electrical Characteristics

3.2.1 Power Consumption

A clarification of the power consumption in the Power-Down sleep mode is made in *Table 33-5*. Functional change is shown in **bold**.

Table 33-5. Power Consumption in Power-Down, Standby and Reset Mode

Mode	Description	Condition		Typ. 25°C	Max. 25°C	Max. 85°C(1)	Max. 125°C	Unit
Standby	Standby power consumption	RTC running at 1.024 kHz from internal OSCULP32K	V_{DD} = 3V	0.7	3.0	6.0	8.0	µA
Power Down/ Standby	Power down/Standby power consumption is the same when all peripherals are stopped	All peripherals stopped	V_{DD} = 3V	0.1	**0.6**	5.0	7.0	µA
Reset	Reset power consumption	Reset line pulled down	V_{DD} = 3V	100	-	-	-	µA

Note:

1. These values are based on characterization and not covered by production test limits.

3.2.2 I/O Pin Characteristics

A clarification of the maximum value of the pull-up resistor is made in *Table 33-15* in the *Electrical Characteristics* section. Functional change is shown in **bold**.

Table 33-15. I/O Pin Characteristics (T_A = [-40, 105]°C, V_{DD} = [1.8, 5.5]V Unless Otherwise Stated)

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low-voltage, except $\overline{\text{RESET}}$ pin as I/O		-0.2	-	0.3 × V_{DD}	V
V_{IH}	Input high-voltage, except $\overline{\text{RESET}}$ pin as I/O		0.7 × V_{DD}	-	V_{DD} + 0.2V	V
I_{IH} / I_{IL}	I/O pin input leakage current, except $\overline{\text{RESET}}$ pin as I/O	V_{DD} = 5.5V, pin high	-	< 0.05	-	µA
		V_{DD} = 5.5V, pin low	-	< 0.05	-	
V_{OL}	I/O pin drive strength	V_{DD} = 1.8V, I_{OL} = 1.5 mA	-	-	0.36	V
		V_{DD} = 3.0V, I_{OL} = 7.5 mA	-	-	0.6	
		V_{DD} = 5.0V, I_{OL} = 15 mA	-	-	1	
V_{OH}	I/O pin drive strength	V_{DD} = 1.8V, I_{OH} = 1.5 mA	1.44	-	-	V
		V_{DD} = 3.0V, I_{OH} = 7.5 mA	2.4	-	-	
		V_{DD} = 5.0V, I_{OH} = 15 mA	4	-	-	
I_{total}	Maximum combined I/O sink current per pin group[1]		-	-	100	mA
	Maximum combined I/O source current per pin group[1]		-	-	100	
V_{IL2}	Input low-voltage on $\overline{\text{RESET}}$ pin as I/O		-0.2	-	0.3 × V_{DD}	V
V_{IH2}	Input high-voltage on $\overline{\text{RESET}}$ pin as I/O		0.7 × V_{DD}	-	V_{DD} + 0.2V	V
V_{OL2}	I/O pin drive strength on $\overline{\text{RESET}}$ pin as I/O	V_{DD} = 1.8V, I_{OL} = 0.1 mA	-	-	0.36	V
		V_{DD} = 3.0V, I_{OL} = 0.25 mA	-	-	0.6	
		V_{DD} = 5.0V, I_{OL} = 0.5 mA	-	-	1	
V_{OH2}	I/O pin drive strength on $\overline{\text{RESET}}$ pin as I/O	V_{DD} = 1.8V, I_{OH} = 0.1 mA	1.44	-	-	V
		V_{DD} = 3.0V, I_{OH} = 0.25 mA	2.4	-	-	
		V_{DD} = 5.0V, I_{OH} = 0.5 mA	4	-	-	
t_{RISE}	Rise time	V_{DD} = 3.0V, load = 20 pF	-	2.5	-	ns
		V_{DD} = 5.0V, load = 20 pF	-	1.5	-	
t_{FALL}	Fall time	V_{DD} = 3.0V, load = 20 pF	-	2.0	-	ns
		V_{DD} = 5.0V, load = 20 pF	-	1.3	-	
C_{PIN}	I/O pin capacitance except TWI pins		-	3	-	pF
C_{PIN}	I/O pin capacitance on TWI pins		-	10	-	pF
R_P	Pull-up resistor		20	35	**60**	kΩ

Note:

1. Pin group x (Px[7:0]). The combined continuous sink/source current for all I/O ports should not exceed the limits.

3.2.3 SPI - Timing Characteristics

A clarification regarding the SPI clock is made in *Table 33-17. SPI - Timing Characteristics*. Functional changes are shown in **bold**.

Table 33-17. SPI - Timing Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{SCK}	SCK clock frequency	Host	-	-	10	MHz
t_{SCK}	SCK period	Host	100	-	-	ns
t_{SCKW}	SCK high/low width	Host	-	0.5 × t_{SCK}	-	ns
t_{SCKR}	SCK rise time	Host	-	2.7	-	ns
t_{SCKF}	SCK fall time	Host	-	2.7	-	ns

.....continued

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
t_{MIS}	MISO setup to SCK	Host	-	10	-	ns
t_{MIH}	MISO hold after SCK	Host	-	10	-	ns
t_{MOS}	MOSI setup to SCK	Host	-	0.5 × t_{SCK}	-	ns
t_{MOH}	MOSI hold after SCK	Host	-	1.0	-	ns
f_{SSCK}	Client SCK clock frequency	Client	-	-	5	MHz
t_{SSCK}	Client SCK Period	Client	**6 × t_{CLK_PER}**	-	-	ns
t_{SSCKW}	SCK high/low width	Client	**3 × t_{CLK_PER}**	-	-	ns
t_{SSCKR}	SCK rise time	Client	-	-	1600	ns
t_{SSCKF}	SCK fall time	Client	-	-	1600	ns
t_{SIS}	MOSI setup to SCK	Client	**0.0**	-	-	ns
t_{SIH}	MOSI hold after SCK	Client	**3 x t_{CLK_PER}**	-	-	ns
t_{SSS}	SS setup to SCK	Client	**-**	**t_{CLK_PER}**	-	ns
t_{SSH}	SS hold after SCK	Client	**-**	**t_{CLK_PER}**	-	ns
t_{SOS}	MISO setup to SCK	Client	-	8.0	-	ns
t_{SOH}	MISO hold after SCK	Client	-	13	-	ns
t_{SOSS}	MISO setup after SS low	Client	-	11	-	ns
t_{SOSH}	MISO hold after SS low	Client	-	8.0	-	ns

3.2.4 Programming Time

A clarification of the *Programming Time* section is made. *Table 33-30* has been upgraded from *Programming Times* to *Memory Programming Specifications* in the *Electrical Characteristics*. Functional change is shown in **bold**.

Table 33-30. Memory Programming Specifications

Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
Data EEPROM Memory Specifications						
E_{EE}*	**Data EEPROM byte endurance**	**100k**	**—**	**—**	**Erase/Write cycles**	**-40°C ≤ T_A ≤ +105°C**
t_{EE_RET}	**Characteristic retention**	**—**	**40**	**—**	**Year**	**T_A = 55°C**
t_{EE_PBC}	Page Buffer Clear (PBC)	—	7	—	CLK_{CPU} cycles	
t_{EE_EEER}	Full EEPROM Erase (EEER)	—	4	—	ms	
t_{EE_WP}	Page Write (WP)	—	2	—	ms	
t_{EE_ER}	Page Erase (ER)	—	2	—	ms	
t_{EE_ERWP}	Page Erase-Write (ERWP)	—	4	—	ms	
Program Flash Memory Specifications						
E_{FL}*	**Flash memory cell endurance**	**10k**	**—**	**—**	**Erase/Write cycles**	**-40°C ≤ T_A ≤ +105°C**
t_{FL_RET}	**Characteristic retention**	**—**	**40**	**—**	**Year**	**T_A = 55°C**
V_{FL_UPDI}	**V_{DD} for Chip Erase operation**	**$V_{BODLEVEL0}$(1)**	**—**	**V_{DDMAX}**	**V**	
t_{FL_PBC}	Page Buffer Clear (PBC)	—	7	—	CLK_{CPU} cycles	
t_{FL_CHER}	**Chip Erase (CHER)**	**—**	**4**	**—**	**ms**	
t_{FL_WP}	Page Write (WP)	—	2	—	ms	
t_{FL_ER}	Page Erase (ER)	—	2	—	ms	
t_{FL_ERWP}	Page Erase/Write (ERWP)	—	4	—	ms	
t_{FL_UPDI}	Chip Erase with UPDI	—	50	—	ms	4 KB Flash
		—	30	—	ms	2 KB Flash

† Data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are not tested and are for design guidance only.

*** These parameters are characterized but not tested in production.**

Note:

1. **The Brown-out Detector (BOD) configured with BODLEVEL0 is forced ON during Chip Erase. The erase attempt will fail if the supply voltage V_{DD} is below V_{BOD} for BODLEVEL0.**

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
C	04/2024	• Document: – Editorial updates • Added new data sheet clarifications: – SPI: • 3.1.1. SPI Clock – Electrical Characteristics: • 3.2.1. Power Consumption. The Power Consumption in Power-Down (Max 25°C) reduced from 2 µA to 0.6 µA. • 3.2.3. SPI - Timing Characteristics • 3.2.4. Programming Time
B	08/2023	• Document: – Editorial updates • Silicon Errata Issues added: – Device: 2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces – NVMCTRL: 2.5.1. Wrong Reset Value of NVMCTRL.CTRLA Register • Silicon Errata Issues updated: – Device: 2.2.2. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values – RTC: 2.7.1. Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler Counter • Added new data sheet clarification: – Electrical Characteristics: 3.2.2. I/O Pin Characteristics
A	04/2021	• Initial document release The content of the document has been restructured from: • ATtiny202/402 Silicon Errata and Data Sheet Clarification • ATtiny204/404 Silicon Errata and Data Sheet Clarification • ATtiny406 Silicon Errata and Data Sheet Clarification to: • **ATtiny202/204/402/404/406 Silicon Errata and Datasheet Clarification document (this document)** Refer to 4.2. Appendix - Obsolete Revision History for further details. The following items are referring to changes between the latest revisions of the obsolete documents and this document: • Removed Errata: – USART: • Start-of-Frame Detection Can Unintentionally Be Triggered in 'Active Mode' • Removed old data sheet clarifications, as the corresponding data sheet has been updated with correct information

4.2 Appendix - Obsolete Revision History

Notes: Due to document structure change from pin organized documents, the following obsolete document revision history is provided as a reference.

- ATtiny202/402 Silicon Errata and Data Sheet Clarification (DS40002123C)
- ATtiny204/404 Silicon Errata and Data Sheet Clarification (DS40002124C)
- ATtiny406 Silicon Errata and Data Sheet Clarification (DS40002125C)

4.2.1 Obsolete Document DS40002123

Doc. Rev.	Date	Comments
C	12/2020	• Added silicon revision C • Added new errata: – Device: *Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values* – ADC: *Pending Event Stuck When Disabling the ADC* – CCL: *The CCL Must be Disabled to Change the Configuration of a Single LUT* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – USART: • *Full Range Duty Cycle Not Supported When Validating LIN Sync Field* • *Open-Drain Mode Does Not Work When TXD is Configured as Output* • *Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'* • Added new data sheet clarifications: – *USART* – *Package Drawings*
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten • Added clarification for ADC electrical characteristics
A	06/2019	Initial document release

4.2.2 Obsolete Document DS40002124

Doc. Rev.	Date	Comments
C	12/2020	• Added silicon revision C • Added new errata: – Device: *Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values* – ADC: *Pending Event Stuck When Disabling the ADC* – CCL: *The CCL Must be Disabled to Change the Configuration of a Single LUT* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – USART: • *Full Range Duty Cycle Not Supported When Validating LIN Sync Field* • *Open-Drain Mode Does Not Work When TXD is Configured as Output* • *Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'* • Added new data sheet clarifications: – *USART* – *Package Drawings*
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten • Added clarification for ADC electrical characteristics
A	06/2019	Initial document release

4.2.3 Obsolete Document DS40002125

Doc. Rev.	Date	Comments
C	12/2020	• Added silicon revision C • Added new errata: – Device: *Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values* – ADC: *Pending Event Stuck When Disabling the ADC* – CCL: *The CCL Must be Disabled to Change the Configuration of a Single LUT* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – USART: • *Full Range Duty Cycle Not Supported When Validating LIN Sync Field* • *Open-Drain Mode Does Not Work When TXD is Configured as Output* • *Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'* • Added new data sheet clarifications: – *USART* – *Package Drawings*
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten • Added clarification for ADC electrical characteristics

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Doc. Rev.	Date	Comments
A	06/2019	Initial document release

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