Product Change Notification / SYST-27VZEI815

## Date:

20-Apr-2024

## Product Category:

8-Bit Microcontrollers

## PCN Type:

Document Change

## Notification Subject:

PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarifications

## Affected CPNs:

SYST-27VZEI815_Affected_CPN_04202024.pdf
SYST-27VZEI815_Affected_CPN_04202024.csv

## Notification Text:

SYST-27VZEI815

Microchip has released a new Document for the PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarifications.

ERRATA - PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarifications

**Notification Status:** Final

**Description of Change:** Data Sheet Clarifications: Added Module 2.

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 29 Feb 2024

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

**Revision History:** February 29, 2024: Issued document PCN.
April 20, 2024: Re-issued document PCN to update the affected CPN list.

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Affected Catalog Part Numbers (CPN)

PIC18F25K83-E/ML
PIC18F25K83-E/MLVAO
PIC18F25K83-E/MX
PIC18F25K83-E/SO
PIC18F25K83-E/SP
PIC18F25K83-E/SS
PIC18F25K83-E/SSVAO
PIC18F25K83-I/ML
PIC18F25K83-I/MX
PIC18F25K83-I/SO
PIC18F25K83-I/SP
PIC18F25K83-I/SS
PIC18F25K83T-E/ML
PIC18F25K83T-E/SO
PIC18F25K83T-E/SS
PIC18F25K83T-E/SSVAO
PIC18F25K83T-I/ML
PIC18F25K83T-I/MX
PIC18F25K83T-I/SO
PIC18F25K83T-I/SS
PIC18F26K83-E/5NVAO
PIC18F26K83-E/ML
PIC18F26K83-E/MLV02
PIC18F26K83-E/MLVAO
PIC18F26K83-E/MX
PIC18F26K83-E/SO
PIC18F26K83-E/SP
PIC18F26K83-E/SS
PIC18F26K83-E/SSVAO
PIC18F26K83-I/ML
PIC18F26K83-I/MX
PIC18F26K83-I/SO
PIC18F26K83-I/SP
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PIC18F26K83-I/SSV01
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PIC18F26K83T-I/SO
PIC18F26K83T-I/SS
PIC18F26K83T-I/SS020
PIC18F26K83T-I/SSVAO
PIC18LF25K83-E/ML

PIC18LF25K83-E/MX
PIC18LF25K83-E/SO
PIC18LF25K83-E/SP
PIC18LF25K83-E/SS
PIC18LF25K83-I/ML
PIC18LF25K83-I/MX
PIC18LF25K83-I/SO
PIC18LF25K83-I/SP
PIC18LF25K83-I/SS
PIC18LF25K83T-I/ML
PIC18LF25K83T-I/MX
PIC18LF25K83T-I/SO
PIC18LF25K83T-I/SS
PIC18LF26K83-E/ML
PIC18LF26K83-E/MX
PIC18LF26K83-E/SO
PIC18LF26K83-E/SP
PIC18LF26K83-E/SS
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PIC18LF26K83-I/SS
PIC18LF26K83T-I/ML
PIC18LF26K83T-I/MX
PIC18LF26K83T-I/SO
PIC18LF26K83T-I/SS

# PIC18(L)F25/26K83

## PIC18(L)F25/26K83 Family
## Silicon Errata and Data Sheet Clarifications

The PIC18(L)F25/26K83 family devices that you have received conform functionally to the current Device Data Sheet (DS40001943**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F25/26K83 silicon.

| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**). |
|---|---|

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

| **Note:** | If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance. |
|---|---|

The DEVREV values for the various PIC18(L)F25/26K83 silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | Device ID<13:0>(1), (2) | Revision ID for Silicon Revision | |
|---|---|---|---|
| | | A2 | A3 |
| PIC18F25K83 | 6EE0h | A002 | A003 |
| PIC18F26K83 | 6EC0h | A002 | A003 |
| PIC18LF25K83 | 6F20h | A002 | A003 |
| PIC18LF26K83 | 6F00h | A002 | A003 |

**Note 1:** The Revision ID is located in addresses 3FFFFCh-3FFFFDh and Device ID is located in addresses 3FFFFEh-3FFFFFh.

**2:** Refer to the "PIC18(L)F25/26K83 *Memory Programming Specification*" (DS40001927) for detailed information on Device and Revision IDs for your specific device.

**TABLE 2: SILICON ISSUE SUMMARY**

| Module | Feature | Item No. | Issue Summary | Affected Revisions(1) | |
|---|---|---|---|---|---|
| | | | | A2 | A3 |
| Electrical Specifications | SMBus 3.0 | 1.1 | SMBus 3.0 logic levels. | X | X |
| | Fixed Voltage Reference (FVR) Accuracy | 1.2 | FVR output tolerance may be higher than specified at temperatures below 20°C. | X | X |
| Direct Memory Access (DMA) Specifications | DMA in Doze mode | 2.1 | DMA transfers may not work when CPU is in Doze mode. | X | |
| Analog-to-Digital Converter Computation (ADC2) | Burst Average mode Double Sampling | 3.1 | The ADC$^2$ does not trigger the second conversion when operated in non-continuous double-sampling Burst Average mode. | X | |
| Nonvolatile Memory (NVM) Control | WRERR bit Functionality | 4.1 | WRERR bit cannot be cleared in hardware after being set once. | X | |
| Windowed Watchdog Timer (WWDT) | WWDT Operation in Doze mode | 5.1 | Window violation occurs when WWDT is operated in Doze mode. | X | |
| Power-Saving Operation Modes | Low-Power Sleep mode | 6.1 | Low-Power Sleep mode does not operate at 3.1V <$V_{DD}$ <3.3V. | X | |
| Program Flash Memory | Endurance of PFM Cell for LF Devices | 7.1 | Endurance of PFM cell is lower than specified. | X | X |
| In-Circuit Debugging (ICD) | Software Breakpoints | 8.1 | Software breakpoints are not available. | X | X |
| I2C | I$^2$C Start/Stop Flags | 9.1 | I$^2$C Start and/or Stop flags may be set when I$^2$C is enabled. | X | X |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

## Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

### 1. Module: Electrical Specifications

#### 1.1 SMBus 3.0

The SMBus 3.0 $V_{IL}$ specification (Parameter D305) is temperature and $V_{DD}$ dependent. Refer to the table below.

| Temperature | $V_{DD}$ | D305 SMBus 3.0 $V_{IL}$ Specification |
|---|---|---|
| -40°C | 1.8V | 0.6V |
| -40°C | 5.5V | 0.8V |
| 25°C | 1.8V | 0.6V |
| 25°C | 5.5V | 0.8V |
| 85°C | 1.8V | 0.6V |
| 85°C | 5.5V | 0.6V |
| 125°C | 1.8V | 0.5V |
| 125°C | 5.5V | 0.6V |

**Work around**

None.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

#### 1.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

**Work around**

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 2. Module: Direct Memory Access (DMA) Specifications

#### 2.1 DMA in Doze Mode 3.0

When the CPU is operated in Doze mode, DMA transfers may not work as expected.

**Work around**

None.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 3. Module: Analog-to-Digital Converter Computation (ADC$^2$)

### 3.1 Burst Average Mode Double Sampling

When the ADC$^2$ is operated in Burst Average mode (MD = 0b011 in the ADCON2 register) while enabling non-continuous operation and double-sampling (CONT = 0 in the ADCON0 register and DSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond 0b1 toward the value in the ADRPT register.

**Work around**

When operating the ADC$^2$ in Burst Average mode with double-sampling, enable continuous operation of the module (CONT = 1 in the ADCON0 register) and set the Stop-On-Interrupt bit (SOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and re-trigger ADC$^2$ as necessary.

Alternatively, if the CPU is in Low-Power Sleep mode, the ADC$^2$ in non-continuous Burst Average mode can be operated with single ADC conversion (DSEN = 0 in the ADCON1 register), compromising noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in software.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 4. Module: Nonvolatile Memory (NVM) Control

### 4.1 WRERR Bit Functionality

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again, regardless of whether an NVM operation is in progress or not.

**Work around**

None.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 5. Module: Windowed Watchdog Timer (WWDT)

### 5.1 WWDT Operation in Doze Mode

When the CLRWDT instruction is issued in Doze mode, a window violation error occurs in WWDT, even though the window is open and armed.

**Work around**

Do not operate the WWDT in Doze mode.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 6. Module: Power-Saving Operation Modes

### 6.1 Low-Power Sleep Mode in F Devices

When the CLRWDT instruction is issued in Doze mode, a window violation error occurs in WWDT, even though the window is open and armed.

**Work around**

a) If wake-up from Sleep is needed at 3.1V < $V_{DD}$ <3.3V, operate the F device in Normal Power mode (VREGPM = 0).

b) If wake-up from Sleep is needed at 3.1V <$V_{DD}$ <3.3V, enable the Fixed Voltage Reference (EN = 1 in the FVRCON register). This increases the current in Sleep mode by typically 7 μA.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 7. Module: Program Flash Memory

### 7.1 Endurance of PFM Cell for LF Devices

The Flash memory cell endurance specification (Parameter MEM30) for this device family is 1K cycles.

**Work around**

None.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 8. Module: In-Circuit Debugging (ICD)

### 8.1 Software Breakpoints

When debugging code, software breakpoints will not be available.

**Work around**

None.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 9. Module: $I^2C$

### 9.1 $I^2C$ Start and/or Stop Flags May be Set When $I^2C$ is Enabled

When $I^2C$ is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous $I^2C$ interrupts if enabled.

**Work around**

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable Start and Stop conditions interrupt functions.
2. Enable $I^2C$ module.
3. Wait 250 ns + 6 instruction cycles (Fosc/4).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable Start and Stop conditions interrupt functions if used.

```
I2CxPIEbits.SCIE = 0;
I2CxPIEbits.PCIE = 0;
I2CxCON0bits.EN = 1;
Delay();
I2CxPIRbits.SCIF = 0;
I2CxPIRbits.PCIF = 0;
I2CxPIEbits.SCIE = 1;
I2CxPIEbits.PCIE = 1;
```

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001943**C**):

| | |
|---|---|
| **Note:** | Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity. |

### 1. Module: Nonvolatile Memory (NVM) Control

Section 13.2 incorrectly states the writing access for User IDs. The corrected Section 13.2 is shown below with changes highlighted in **bold**.

13.2.2 Writing Access

**Only the User IDs and CONFIG words have write access enabled. The user can write to these blocks by setting the REG bits to 0b01 or0b11.** The WREN bit in NVMCON1 must be set to enable writes. This prevents accidental writes to the CONFIG words due to errant (unexpected) code execution. The WREN bit should be kept clear at all times, except when updating the CONFIG words. The WREN bit is not cleared by hardware. The WR bit will be inhibited from being set unless the WREN bit is set.

**13.2.2.1 Writing to User IDs**

The user needs to load the TBLPTR and TABLAT registers with the address and data byte respectively. **Writing to the User IDs does not include an implicit erase cycle like the EEPROM/CONFIG words; hence, the user needs to clear the memory location pointed by TBLPTR, first by setting the FREE bit and executing the write command**. An unlock sequence is required before setting the **writing command**. **A single User ID byte is cleared at once (set to 0xFF). CPU execution is stalled and, at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag bit (NVMIF) is set and the CPU resumes operation.**

**Once the User ID byte is cleared, the user can now write the new value to that location. To do this, the user needs to execute TBLWT instruction, followed by executing the write command. An unlock sequence is required before setting the writing command. A single User ID byte is written at once. CPU execution is stalled and, at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag bit (NVMIF) is set. The new User ID value takes effect when the CPU resumes operation.**

**During the above operations, if TBLPTR points to an invalid address location (see Table 13-1), WR bit is cleared without any effect and WRERR is set.**

## 2. Module: Electrical Specifications

Table 45-11 incorrectly states values for RST06 and RST09. The corrected values are shown below with changes highlighted in **bold**.

TABLE 45-11: RESET, WDT, OSCILLATOR START-UP TIMER, POWER-UP TIMER, BROWN-OUT RESET AND LOW-POWER BROWN-OUT RESET SPECIFICATIONS

| Standard Operating Conditions (unless otherwise stated) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Sym. | Characteristic | Min. | Typ† | Max. | Units | Conditions |
| RST01* | TMCLR | $\overline{\text{MCLR}}$ Pulse Width Low to ensure Reset | 2 | — | — | µs | |
| RST02* | TIOZ | I/O high-impedance from Reset detection | — | — | 2 | µs | |
| RST03 | TWDT | Watchdog Timer Time-out Period | — | 16 | — | ms | 1:512 Prescaler |
| RST04* | TPWRT | Power-up Timer Period | — | 1<br>16<br>64 | — | ms<br>ms<br>ms | PWRTS = 00<br>PWRTS = 01<br>PWRTS = 10 |
| RST05 | TOST | Oscillator Start-up Timer Period(1,2) | — | 1024 | — | TOSC | |
| RST06 | VBOR | Brown-out Reset Voltage(4) | 2.7<br>2.55<br>2.3<br>2.3<br>1.8 | 2.85<br>2.7<br>2.45<br>2.45<br>1.9 | 3.0<br>2.85<br>2.6<br>2.6<br>**2.1** | V<br>V<br>V<br>V<br>V | BORV = 00<br>BORV = 01<br>BORV = 10<br>BORV = 11 (PIC18Fxxx)<br>BORV = 11 (PIC18LFxxx) |
| RST07 | VBORHYS | Brown-out Reset Hysteresis | — | 40 | — | mV | |
| RST08 | TBORDC | Brown-out Reset Response Time | — | 3 | — | µs | |
| RST09 | VLPBOR | Low-Power Brown-out Reset Voltage | 1.8 | **2.0** | **2.5** | V | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.

**2:** To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

# APPENDIX A: DOCUMENT REVISION HISTORY

## Rev F Document (02/2024)

Data Sheet Clarifications: Added Module 2.

## Rev E Document (09/2021)

Added Module 9.1 $I^2C$ Start/Stop Flags.

## Rev D Document (02/2021)

Added Module 8.1. Other minor corrections.

Data Sheet Clarifications:

Removed previous Module 1 as it was added to the data sheet and is no longer needed in this document.

Added new Module 1: Nonvolatile Memory (NVM) Control.

## Rev C Document (01/2020)

Removed Module 1.2, renumbered Module 1.3 and updated; Updated Table 2.

Data Sheet Clarifications: Added Module 1.

## Rev B Document (02/2019)

Added silicon revision A3.

Added Module 1.3: Fixed Voltage Reference (FVR) Accuracy. Added Module 2: Direct Memory Access (DMA). Added Module 3: Analog-to-Digital Converter with Computation ($ADC^2$). Added Module 4: Nonvolatile Memory (NVM) Control. Added Module 5: Windowed Watchdog Timer (WWDT). Added Module 6: Power-Saving Operation Modes. Added module 7: Program Flash Memory.

## Rev A Document (11/2017)

Initial release of this document.

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**Sweden - Gothenberg**
Tel: 46-31-704-60-40

**Sweden - Stockholm**
Tel: 46-8-5090-4654

**UK - Wokingham**
Tel: 44-118-921-5800
Fax: 44-118-921-5820

Product Change Notification / SYST-27VZEI815

## Date:

29-Feb-2024

## Product Category:

8-Bit Microcontrollers

## PCN Type:

Document Change

## Notification Subject:

PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarifications

## Affected CPNs:

SYST-27VZEI815_Affected_CPN_02292024.pdf
SYST-27VZEI815_Affected_CPN_02292024.csv

## Notification Text:

SYST-27VZEI815

Microchip has released a new Document for the PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarifications.

ERRATA - PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarifications

**Notification Status:** Final

**Description of Change:** Data Sheet Clarifications: Added Module 2.

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 29 Feb 2024

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarifications

Please contact your local Microchip sales office with questions or concerns regarding this notification.

**Terms and Conditions:**

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.

If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

PIC18LF25J10-I/SP
PIC18LF25J10-I/SS
PIC18LF25J10-I/SO
PIC18LF25J10T-I/SS031
PIC18LF25J10T-I/SS035
PIC18LF25J10T-I/SS038
PIC18LF25J10T-I/SS042
PIC18LF25J10T-I/SS043
PIC18LF25J10T-I/SS044
PIC18LF25J10T-I/SS046
PIC18LF25J10T-I/SS047
PIC18LF25J10T-I/SS
PIC18F252-E/SP
PIC18F252-E/SO
PIC18F252-I/SP
PIC18F252-I/SPREL
PIC18F252-I/SO
PIC18F2539-I/SO
PIC18F252T-I/SO
PIC18F252T-I/SOVAO
PIC18F258-E/SO
PIC18F258-I/SP
PIC18F258-I/SPREL
PIC18F258-I/SO
PIC18F258T-I/SO
PIC18F258T-E/SOC06
PIC18F252T-I/SO040
PIC18F252T-I/SO042
PIC18F252T-I/SO046
PIC18F252T-I/SO048
PIC18F252T-I/SO049
PIC18F252T-I/SOV01
PIC18F2525-E/SP
PIC18F2525-E/SO
PIC18F2525-I/SP026
PIC18F2525-I/SP
PIC18F2525-I/SO
PIC18F2525T-I/SO
PIC18F2525T-I/SOC02
PIC18F2525T-E/SO
PIC18F2515-I/SP
PIC18F2515-I/SO
PIC18F2550-I/SP
PIC18F2553-I/SP
PIC18F2553-I/SPREL
PIC18F2550-I/SO

PIC18F2553-I/SO
PIC18F2550T-I/SO
PIC18F2523-E/SP
PIC18F2520-E/SP
PIC18F2520-E/ML
PIC18F2523-E/ML
PIC18F2520-E/SO032
PIC18F2520-E/SO
PIC18F2523-E/SO
PIC18F2520-I/SP060
PIC18F2520-I/SP
PIC18F2523-I/SP
PIC18F2523-I/SPREL
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PIC18F2523-I/ML
PIC18F2520-I/SO
PIC18F2523-I/SO
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PIC18F2520T-I/SO055
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PIC18F2523T-I/SO
PIC18F2520T-I/SOC01
PIC18F2520T-I/SOV11
PIC18F2520T-E/ML051
PIC18F2520T-E/ML053
PIC18F2520T-E/SO021
PIC18F2520T-E/SO032
PIC18F2520T-E/SOC06
PIC18F2510-I/SP
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PIC18F2510-I/SO
PIC18F2585-E/SO
PIC18F2585-I/SP
PIC18F2585-I/SO
PIC18F2585T-H/SOV04
PIC18F2585T-I/SO
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PIC18F2580-E/SP
PIC18F2580-E/SO
PIC18F2580-E/SOVAO

PIC18F2580-I/ML
PIC18F2580-I/SP
PIC18F2580-I/SO
PIC18F2580-I/SOVAO
PIC18F2580T-I/ML
PIC18F2580T-I/MLVAO
PIC18F2580T-I/SO
PIC18F2580T-I/SOV01
PIC18F2580T-I/SOVAO
PIC18F2580T-E/ML
PIC18F2580T-E/SOVAO
PIC18F25Q10-E/5NVAO
PIC18F25Q10-E/SP
PIC18F25Q10-E/ML
PIC18F25Q10-E/MLVAO
PIC18F25Q10-E/SS
PIC18F25Q10-E/SSVAO
PIC18F25Q10-E/SO
PIC18F25Q10-E/STX
PIC18LF252-I/SP
PIC18LF2539-I/SP
PIC18LF252-I/SO
PIC18LF252T-I/SO
PIC18LF258-I/SP
PIC18LF258-I/SO
PIC18LF258T-I/SO
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PIC18LF2525-I/SO
PIC18LF2525-I/SOC09
PIC18LF2525-I/SOVAO
PIC18LF2525T-I/SO
PIC18LF2525T-I/SOV02
PIC18LF2525T-I/SOVAO
PIC18LF2515-I/SP
PIC18LF2515-I/SO
PIC18LF2515T-I/SO
PIC18LF2550-I/SP
PIC18LF2553-I/SP
PIC18LF2550-I/SO
PIC18LF2553-I/SO
PIC18LF2553-I/SOHLF
PIC18LF2550T-I/SO
PIC18LF2520-I/SP
PIC18LF2523-I/SP
PIC18LF2520-I/ML
PIC18LF2523-I/ML
PIC18LF2520-I/SO
PIC18LF2523-I/SO
PIC18LF2520T-I/ML

PIC18LF2520T-I/MLV02
PIC18LF2520T-I/SO
PIC18LF2520T-E/MLV06
PIC18LF2520T-E/MLVAO
PIC18LF2510-I/ML
PIC18LF2510-I/SO
PIC18LF2585-I/SP
PIC18LF2585-I/SO
PIC18LF2580-I/ML
PIC18LF2580-I/SP
PIC18LF2580-I/SO
PIC18LF2580-I/SOC01
PIC18LF25K22-E/SP
PIC18LF25K22-E/ML
PIC18LF25K22-E/MLV02
PIC18LF25K22-E/SS
PIC18LF25K22-E/SSVAO
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PIC18LF25K22-I/SP
PIC18LF25K22-I/ML
PIC18LF25K22-I/MLV01
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PIC18LF25K22-I/SO
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PIC18LF25K22T-I/MLV01
PIC18LF25K22T-I/SS
PIC18LF25K22T-E/MLV02
PIC18LF25K22T-E/SS
PIC18LF25K22T-E/SO
PIC18LF25K80-I/MM
PIC18LF25K80-I/SP
PIC18LF25K80-I/SS
PIC18LF25K80-I/SO
PIC18LF25K50-E/SP
PIC18LF25K50-E/SS
PIC18LF25K50-I/SP
PIC18LF25K50-I/ML
PIC18LF25K50-I/SS
PIC18LF25K50-I/SO
PIC18LF25K50T-I/SS
PIC18LF25K42-E/SP
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PIC18LF25K42-E/MV
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PIC18LF25K42T-I/ML
PIC18LF25K42T-I/SS
PIC18LF25K42T-I/SO
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PIC18LF25K40-E/ML
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PIC18LF25K40T-E/SSVAO
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PIC18LF25K83-E/ML
PIC18LF25K83-E/MX
PIC18LF25K83-E/SS
PIC18LF25K83-E/SO
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PIC18LF25K83T-I/MX
PIC18LF25K83T-I/SS
PIC18LF25K83T-I/SO
PIC18LF25J50-I/SO
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PIC18LF25J11-I/SO
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PIC18F25Q10-I/MLVAO
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PIC18F25Q10-I/SSVAO
PIC18F25Q10-I/SO
PIC18F25Q10-I/STX
PIC18F25Q10T-I/ML

PIC18F25Q10T-I/MLVAO
PIC18F25Q10T-I/SSC01
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PIC18F25Q10T-I/SSV01
PIC18F25Q10T-I/SSVAO
PIC18F25Q10T-I/SO
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PIC18F25Q10T-E/5NVAO
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PIC18F25Q24-E/STX
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PIC18F25Q24T-I/SS
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PIC18F25Q71-E/STX
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PIC18F25Q71-I/SS

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PIC18F25K20-E/SSVAO
PIC18F25K20-E/SO
PIC18F25K20-E/SOC12
PIC18F25K20-I/SP
PIC18F25K20-I/ML
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PIC18F25K20-I/MLVAO
PIC18F25K20-I/SS
PIC18F25K20-I/SSC01
PIC18F25K20-I/SSC15
PIC18F25K20-I/SSVAO
PIC18F25K20-I/SO
PIC18F25K20-I/SOLPR
PIC18F25K20-I/SOVAO
PIC18F25K20T-I/ML044
PIC18F25K20T-I/ML
PIC18F25K20T-I/MLC02
PIC18F25K20T-I/MLC10
PIC18F25K20T-I/MLV04
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PIC18F25K20T-I/MLV11
PIC18F25K20T-I/MLVAO
PIC18F25K20T-I/SS
PIC18F25K20T-I/SSC01
PIC18F25K20T-I/SSC15
PIC18F25K20T-I/SSC17
PIC18F25K20T-I/SSVAO
PIC18F25K20T-I/SO
PIC18F25K20T-I/SOVAO
PIC18F25K20T-E/ML036
PIC18F25K20T-E/ML037
PIC18F25K20T-E/ML038
PIC18F25K20T-E/ML
PIC18F25K20T-E/MLV03
PIC18F25K20T-E/MLV07
PIC18F25K20T-E/MLV09

PIC18F25K20T-E/MLVAO
PIC18F25K20T-E/MLV07-MB
PIC18F25K20T-E/SS023
PIC18F25K20T-E/SS025
PIC18F25K20T-E/SS033
PIC18F25K20T-E/SS035
PIC18F25K20T-E/SS039
PIC18F25K20T-E/SS043
PIC18F25K20T-E/SSC13
PIC18F25K20T-E/SSVAO
PIC18F25K20T-E/SOC12
PIC18F25K22-E/SP
PIC18F25K22-E/ML
PIC18F25K22-E/MLVAO
PIC18F25K22-E/SS
PIC18F25K22-E/SSV05
PIC18F25K22-E/SSV12
PIC18F25K22-E/SSV13
PIC18F25K22-E/SSVAO
PIC18F25K22-E/SO
PIC18F25K22-E/SOV03
PIC18F25K22-I/SP
PIC18F25K22-I/ML
PIC18F25K22-I/SS
PIC18F25K22-I/SSV10
PIC18F25K22-I/SSVAO
PIC18F25K22-I/SO
PIC18F25K22-I/SOC02
PIC18F25K22T-I/ML
PIC18F25K22T-I/MLV01
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PIC18F25K22T-I/SSV10
PIC18F25K22T-I/SSVAO
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PIC18F25K22T-I/SO
PIC18F25K22T-I/SOC02
PIC18F25K22T-E/MLV04
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PIC18F25K22T-E/MLV07
PIC18F25K22T-E/MLV08
PIC18F25K22T-E/MLV11
PIC18F25K22T-E/MLVAO
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PIC18F25K22T-E/SSV05
PIC18F25K22T-E/SSV09
PIC18F25K22T-E/SSV14
PIC18F25K22T-E/SSVAO
PIC18F25K22T-E/SOV03

PIC18F25K80-E/MM
PIC18F25K80-E/MMC01
PIC18F25K80-E/MMVAO
PIC18F25K80-E/MMVAO-MB
PIC18F25K80-E/SP
PIC18F25K80-E/SS
PIC18F25K80-E/SSV02
PIC18F25K80-E/SSVAO
PIC18F25K80-E/SO033
PIC18F25K80-E/SO
PIC18F25K80-E/SOVAO
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PIC18F25K80-I/MM032
PIC18F25K80-I/MM
PIC18F25K80-I/MMC04
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PIC18F25K80-I/SSVAO
PIC18F25K80-I/SO
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PIC18F25K80T-I/SOC03
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PIC18F25K80T-E/MMV04
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PIC18F25K50T-I/SO
PIC18F25K50T-E/ML020
PIC18F25K50T-E/ML022
PIC18F25K50T-E/ML
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PIC18F25K42-E/ML
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PIC18F25K42-E/SSVAO
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PIC18F25K42-I/SS
PIC18F25K42-I/SO
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PIC18F25K42T-I/ML
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PIC18F25K42T-I/MV
PIC18F25K42T-E/SSVAO
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PIC18F25K40-E/MLVAO
PIC18F25K40-E/SS
PIC18F25K40-E/SSV03
PIC18F25K40-E/SSVAO
PIC18F25K40-E/SO
PIC18F25K40-E/MV
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PIC18F25K40-I/SSVAO
PIC18F25K40-I/SO
PIC18F25K40-I/MV

PIC18F25K40-I/MVVAO
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PIC18F25K40T-I/SS
PIC18F25K40T-I/SSVAO
PIC18F25K40T-I/SO
PIC18F25K40T-I/MV
PIC18F25K40T-I/MVV04
PIC18F25K40T-I/MVVAO
PIC18F25K40T-E/ML
PIC18F25K40T-E/MLV02
PIC18F25K40T-E/MLVAO
PIC18F25K40T-E/SS
PIC18F25K40T-E/SSV03
PIC18F25K40T-E/SSV03-BW
PIC18F25K40T-E/SSVAO
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PIC18F25K83-E/ML
PIC18F25K83-E/MLVAO
PIC18F25K83-E/MX
PIC18F25K83-E/SS
PIC18F25K83-E/SSVAO
PIC18F25K83-E/SO
PIC18F25K83-I/SP
PIC18F25K83-I/ML
PIC18F25K83-I/MX
PIC18F25K83-I/SS
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PIC18F25K83T-I/SO
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PIC18F25K83T-E/SS
PIC18F25K83T-E/SSVAO
PIC18F25K83T-E/SO
PIC18F25J50-I/SP
PIC18F25J50-I/ML
PIC18F25J50-I/SS022
PIC18F25J50-I/SS024
PIC18F25J50-I/SS027
PIC18F25J50-I/SS028
PIC18F25J50-I/SS029
PIC18F25J50-I/SS030
PIC18F25J50-I/SS
PIC18F25J50-I/SO
PIC18F25J50T-I/ML
PIC18F25J50T-I/SS
PIC18F25J11-I/SP
PIC18F25J11-I/ML

PIC18F25J11-I/SS
PIC18F25J11-I/SO
PIC18F25J11T-I/ML
PIC18F25J11T-I/SS
PIC18F25J10-I/SP
PIC18F25J10-I/SPREL
PIC18F25J10-I/ML020
PIC18F25J10-I/ML
PIC18F25J10-I/SS
PIC18F25J10-I/SO
PIC18F25J10T-I/ML020
PIC18F25J10T-I/ML
PIC18F25J10T-I/SS
PIC18F25J10T-I/SO
PIC18LF26K83-E/SP
PIC18LF26K83-E/ML
PIC18LF26K83-E/MX
PIC18LF26K83-E/SS
PIC18LF26K83-E/SO
PIC18LF26K83-I/SP
PIC18LF26K83-I/ML
PIC18LF26K83-I/MX
PIC18LF26K83-I/SS
PIC18LF26K83-I/SO
PIC18LF26K83T-I/ML
PIC18LF26K83T-I/MX
PIC18LF26K83T-I/SS
PIC18LF26K83T-I/SO
PIC18F26K83-E/5NVAO
PIC18F26K83-E/SP
PIC18F26K83-E/ML
PIC18F26K83-E/MLV02
PIC18F26K83-E/MLVAO
PIC18F26K83-E/MX
PIC18F26K83-E/SS
PIC18F26K83-E/SSVAO
PIC18F26K83-E/SO
PIC18F26K83-I/SP
PIC18F26K83-I/ML
PIC18F26K83-I/MX
PIC18F26K83-I/SS
PIC18F26K83-I/SSV01
PIC18F26K83-I/SSVAO
PIC18F26K83-I/SO
PIC18F26K83T-I/ML
PIC18F26K83T-I/MX
PIC18F26K83T-I/SS020
PIC18F26K83T-I/SS
PIC18F26K83T-I/SSVAO

PIC18F26K83T-I/SO
PIC18F26K83T-E/5NVAO
PIC18F26K83T-E/MLV02
PIC18F26K83T-E/SSVAO

# PIC18(L)F25/26K83

## PIC18(L)F25/26K83 Family
## Silicon Errata and Data Sheet Clarifications

The PIC18(L)F25/26K83 family devices that you have received conform functionally to the current Device Data Sheet (DS40001943**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F25/26K83 silicon.

| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**). |
|---|---|

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

| **Note:** | If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance. |
|---|---|

The DEVREV values for the various PIC18(L)F25/26K83 silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | Device ID<13:0>(1), (2) | Revision ID for Silicon Revision | |
|---|---|---|---|
| | | A2 | A3 |
| PIC18F25K83 | 6EE0h | A002 | A003 |
| PIC18F26K83 | 6EC0h | A002 | A003 |
| PIC18LF25K83 | 6F20h | A002 | A003 |
| PIC18LF26K83 | 6F00h | A002 | A003 |

**Note 1:** The Revision ID is located in addresses 3FFFFCh-3FFFFDh and Device ID is located in addresses 3FFFFEh-3FFFFFh.

**2:** Refer to the "PIC18(L)F25/26K83 *Memory Programming Specification*" (DS40001927) for detailed information on Device and Revision IDs for your specific device.

**TABLE 2: SILICON ISSUE SUMMARY**

| Module | Feature | Item No. | Issue Summary | Affected Revisions(1) | |
|---|---|---|---|---|---|
| | | | | A2 | A3 |
| Electrical Specifications | SMBus 3.0 | 1.1 | SMBus 3.0 logic levels. | X | X |
| | Fixed Voltage Reference (FVR) Accuracy | 1.2 | FVR output tolerance may be higher than specified at temperatures below 20°C. | X | X |
| Direct Memory Access (DMA) Specifications | DMA in Doze mode | 2.1 | DMA transfers may not work when CPU is in Doze mode. | X | |
| Analog-to-Digital Converter Computation (ADC2) | Burst Average mode Double Sampling | 3.1 | The ADC$^2$ does not trigger the second conversion when operated in non-continuous double-sampling Burst Average mode. | X | |
| Nonvolatile Memory (NVM) Control | WRERR bit Functionality | 4.1 | WRERR bit cannot be cleared in hardware after being set once. | X | |
| Windowed Watchdog Timer (WWDT) | WWDT Operation in Doze mode | 5.1 | Window violation occurs when WWDT is operated in Doze mode. | X | |
| Power-Saving Operation Modes | Low-Power Sleep mode | 6.1 | Low-Power Sleep mode does not operate at 3.1V <$V_{DD}$ <3.3V. | X | |
| Program Flash Memory | Endurance of PFM Cell for LF Devices | 7.1 | Endurance of PFM cell is lower than specified. | X | X |
| In-Circuit Debugging (ICD) | Software Breakpoints | 8.1 | Software breakpoints are not available. | X | X |
| I2C | I$^2$C Start/Stop Flags | 9.1 | I$^2$C Start and/or Stop flags may be set when I$^2$C is enabled. | X | X |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

## Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

### 1. Module: Electrical Specifications

#### 1.1 SMBus 3.0

The SMBus 3.0 $V_{IL}$ specification (Parameter D305) is temperature and $V_{DD}$ dependent. Refer to the table below.

| Temperature | $V_{DD}$ | D305 SMBus 3.0 $V_{IL}$ Specification |
|---|---|---|
| -40°C | 1.8V | 0.6V |
| -40°C | 5.5V | 0.8V |
| 25°C | 1.8V | 0.6V |
| 25°C | 5.5V | 0.8V |
| 85°C | 1.8V | 0.6V |
| 85°C | 5.5V | 0.6V |
| 125°C | 1.8V | 0.5V |
| 125°C | 5.5V | 0.6V |

**Work around**

None.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

#### 1.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

**Work around**

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 2. Module: Direct Memory Access (DMA) Specifications

#### 2.1 DMA in Doze Mode 3.0

When the CPU is operated in Doze mode, DMA transfers may not work as expected.

**Work around**

None.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 3. Module: Analog-to-Digital Converter Computation (ADC$^2$)

### 3.1 Burst Average Mode Double Sampling

When the ADC$^2$ is operated in Burst Average mode (MD = 0b011 in the ADCON2 register) while enabling non-continuous operation and double-sampling (CONT = 0 in the ADCON0 register and DSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond 0b1 toward the value in the ADRPT register.

**Work around**

When operating the ADC$^2$ in Burst Average mode with double-sampling, enable continuous operation of the module (CONT = 1 in the ADCON0 register) and set the Stop-On-Interrupt bit (SOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and re-trigger ADC$^2$ as necessary.

Alternatively, if the CPU is in Low-Power Sleep mode, the ADC$^2$ in non-continuous Burst Average mode can be operated with single ADC conversion (DSEN = 0 in the ADCON1 register), compromising noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in software.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 4. Module: Nonvolatile Memory (NVM) Control

### 4.1 WRERR Bit Functionality

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again, regardless of whether an NVM operation is in progress or not.

**Work around**

None.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 5. Module: Windowed Watchdog Timer (WWDT)

### 5.1 WWDT Operation in Doze Mode

When the CLRWDT instruction is issued in Doze mode, a window violation error occurs in WWDT, even though the window is open and armed.

**Work around**

Do not operate the WWDT in Doze mode.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 6. Module: Power-Saving Operation Modes

### 6.1 Low-Power Sleep Mode in F Devices

When the CLRWDT instruction is issued in Doze mode, a window violation error occurs in WWDT, even though the window is open and armed.

**Work around**

a) If wake-up from Sleep is needed at 3.1V < $V_{DD}$ <3.3V, operate the F device in Normal Power mode (VREGPM = 0).

b) If wake-up from Sleep is needed at 3.1V <$V_{DD}$ <3.3V, enable the Fixed Voltage Reference (EN = 1 in the FVRCON register). This increases the current in Sleep mode by typically 7 μA.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 7. Module: Program Flash Memory

### 7.1 Endurance of PFM Cell for LF Devices

The Flash memory cell endurance specification (Parameter MEM30) for this device family is 1K cycles.

**Work around**

None.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 8. Module: In-Circuit Debugging (ICD)

### 8.1 Software Breakpoints

When debugging code, software breakpoints will not be available.

**Work around**

None.

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 9. Module: $I^2C$

### 9.1 $I^2C$ Start and/or Stop Flags May be Set When $I^2C$ is Enabled

When $I^2C$ is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous $I^2C$ interrupts if enabled.

**Work around**

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable Start and Stop conditions interrupt functions.
2. Enable $I^2C$ module.
3. Wait 250 ns + 6 instruction cycles (Fosc/4).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable Start and Stop conditions interrupt functions if used.

```
I2CxPIEbits.SCIE = 0;
I2CxPIEbits.PCIE = 0;
I2CxCON0bits.EN = 1;
Delay();
I2CxPIRbits.SCIF = 0;
I2CxPIRbits.PCIF = 0;
I2CxPIEbits.SCIE = 1;
I2CxPIEbits.PCIE = 1;
```

**Affected Silicon Revisions**

| A2 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001943**C**):

| | |
|---|---|
| **Note:** | Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity. |

### 1. Module: Nonvolatile Memory (NVM) Control

Section 13.2 incorrectly states the writing access for User IDs. The corrected Section 13.2 is shown below with changes highlighted in **bold**.

13.2.2 Writing Access

**Only the User IDs and CONFIG words have write access enabled. The user can write to these blocks by setting the REG bits to 0b01 or0b11.** The WREN bit in NVMCON1 must be set to enable writes. This prevents accidental writes to the CONFIG words due to errant (unexpected) code execution. The WREN bit should be kept clear at all times, except when updating the CONFIG words. The WREN bit is not cleared by hardware. The WR bit will be inhibited from being set unless the WREN bit is set.

**13.2.2.1 Writing to User IDs**

The user needs to load the TBLPTR and TABLAT registers with the address and data byte respectively. **Writing to the User IDs does not include an implicit erase cycle like the EEPROM/CONFIG words; hence, the user needs to clear the memory location pointed by TBLPTR, first by setting the FREE bit and executing the write command**. An unlock sequence is required before setting the **writing command**. **A single User ID byte is cleared at once (set to 0xFF). CPU execution is stalled and, at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag bit (NVMIF) is set and the CPU resumes operation.**

**Once the User ID byte is cleared, the user can now write the new value to that location. To do this, the user needs to execute TBLWT instruction, followed by executing the write command. An unlock sequence is required before setting the writing command. A single User ID byte is written at once. CPU execution is stalled and, at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag bit (NVMIF) is set. The new User ID value takes effect when the CPU resumes operation.**

**During the above operations, if TBLPTR points to an invalid address location (see Table 13-1), WR bit is cleared without any effect and WRERR is set.**

## 2. Module: Electrical Specifications

Table 45-11 incorrectly states values for RST06 and RST09. The corrected values are shown below with changes highlighted in **bold**.

TABLE 45-11: RESET, WDT, OSCILLATOR START-UP TIMER, POWER-UP TIMER, BROWN-OUT RESET AND LOW-POWER BROWN-OUT RESET SPECIFICATIONS

| Standard Operating Conditions (unless otherwise stated) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Sym. | Characteristic | Min. | Typ† | Max. | Units | Conditions |
| RST01* | TMCLR | $\overline{\text{MCLR}}$ Pulse Width Low to ensure Reset | 2 | — | — | µs | |
| RST02* | TIOZ | I/O high-impedance from Reset detection | — | — | 2 | µs | |
| RST03 | TWDT | Watchdog Timer Time-out Period | — | 16 | — | ms | 1:512 Prescaler |
| RST04* | TPWRT | Power-up Timer Period | — | 1<br>16<br>64 | — | ms<br>ms<br>ms | PWRTS = 00<br>PWRTS = 01<br>PWRTS = 10 |
| RST05 | TOST | Oscillator Start-up Timer Period(1,2) | — | 1024 | — | TOSC | |
| RST06 | VBOR | Brown-out Reset Voltage(4) | 2.7<br>2.55<br>2.3<br>2.3<br>1.8 | 2.85<br>2.7<br>2.45<br>2.45<br>1.9 | 3.0<br>2.85<br>2.6<br>2.6<br>**2.1** | V<br>V<br>V<br>V<br>V | BORV = 00<br>BORV = 01<br>BORV = 10<br>BORV = 11 (PIC18Fxxx)<br>BORV = 11 (PIC18LFxxx) |
| RST07 | VBORHYS | Brown-out Reset Hysteresis | — | 40 | — | mV | |
| RST08 | TBORDC | Brown-out Reset Response Time | — | 3 | — | µs | |
| RST09 | VLPBOR | Low-Power Brown-out Reset Voltage | 1.8 | **2.0** | **2.5** | V | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.

**2:** To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

# APPENDIX A: DOCUMENT REVISION HISTORY

## Rev F Document (02/2024)

Data Sheet Clarifications: Added Module 2.

## Rev E Document (09/2021)

Added Module 9.1 $I^2C$ Start/Stop Flags.

## Rev D Document (02/2021)

Added Module 8.1. Other minor corrections.

Data Sheet Clarifications:

Removed previous Module 1 as it was added to the data sheet and is no longer needed in this document.

Added new Module 1: Nonvolatile Memory (NVM) Control.

## Rev C Document (01/2020)

Removed Module 1.2, renumbered Module 1.3 and updated; Updated Table 2.

Data Sheet Clarifications: Added Module 1.

## Rev B Document (02/2019)

Added silicon revision A3.

Added Module 1.3: Fixed Voltage Reference (FVR) Accuracy. Added Module 2: Direct Memory Access (DMA). Added Module 3: Analog-to-Digital Converter with Computation ($ADC^2$). Added Module 4: Nonvolatile Memory (NVM) Control. Added Module 5: Windowed Watchdog Timer (WWDT). Added Module 6: Power-Saving Operation Modes. Added module 7: Program Flash Memory.

## Rev A Document (11/2017)

Initial release of this document.

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