*Click **here** to ask an associate for production status of specific part numbers.*

MAX9295D

GMSL2 Dual CSI-2 Serializer with GMSL1 Compatibility

General Description

The MAX9295D converts single- or dual-port MIPI CSI-2 data streams to GMSL2™ or GMSL1™ while sending and receiving control-channel data, enabling full-duplex single-wire transmission of forward video and bidirectional control data over cables in excess of 15m in length. In GMSL2 mode, the device operates at a fixed rate of 3Gbps or 6Gbps in the forward direction and 187.5Mbps in the reverse direction. In GMSL1 mode, the MAX9295D can be paired with first-generation 3.12Gbps or 1.5Gbps GMSL1 deserializers or operate up to 4.5Gbps with GMSL2 deserializers configured for GMSL1 mode. Operation is specified over the automotive temperature range of -40°C to +105°C and the device is AEC-Q100 Grade 2 qualified. Cable can be coaxial or shielded twisted pair (STP).

Table 1. Typical Maximum Cable Length

	3.2mm Ø 50Ω Coax, Foam Dielectric	**2.7mm Ø 50Ω Coax, Solid Dielectric**	**100Ω Shielded Twisted Pair, AWG26**
Attenuation at 3GHz (Typ, Room Temp)	0.9dB/m	1.6dB/m	1.8dB/m
Attenuation at 3GHz (Max, Aged, +105°C)	1.1dB/m	2.0dB/m	2.2dB/m
GMSL Fwd/Rev Data Rate	**Typical Maximum Cable Length at +105°**		
3Gbps/187.5Mbps	20m	10m	11m
6Gbps/187.5Mbps	15m	9m	8m

Applications

- Co-located sensors
- Stereo camera
- Side mirror
- Radar
- Lidar

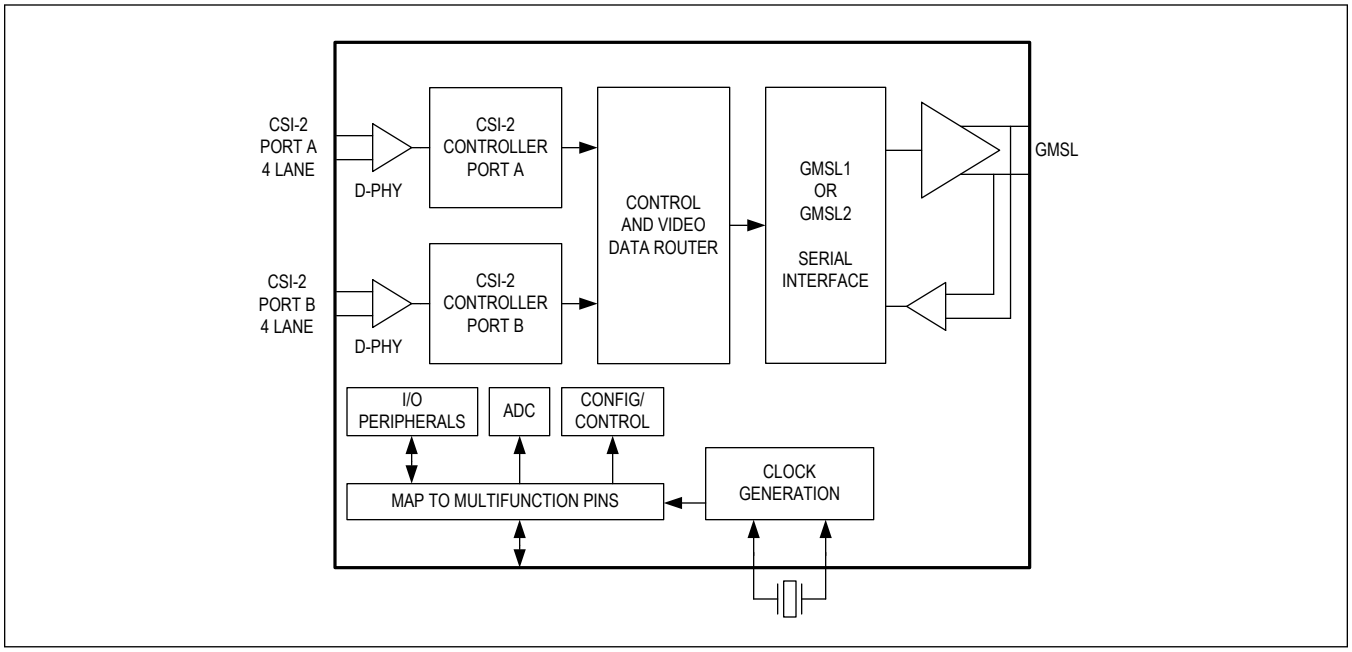
Benefits and Features

- Dual 4-Lane MIPI CSI-2 v1.3 Ports
  - MIPI D-PHY v1.2 at 80Mbps - 2.5Gbps per Lane
  - 4-Channel CSI-2 Virtual-Channel Support
  - Support for RAW8/10/12/14/16/20, RGB565/666/888 and YUV8-/10-Bit Data Types
  - CSI-2 Inputs in GMSL2 Mode Accept Cameras with Different Video Timing and Resolution
  - CSI-2 ECC and Checksum Error Detection and Flagging
  - CSI-2 Lane Reassignment and Polarity Flip
- Selectable GMSL2 at 3/6Gbps or Backward-Compatible GMSL1 Mode
  - Operates up to 4.5Gbps with GMSL2 Deserializers in GMSL1 Mode
  - 187.5Mbps Reverse Link for Reduced-Size Power-over-Cable (PoC) Filter
  - Forward- and Reverse-Channel PRBS for BER Testing of Serial Link
  - Reverse-Channel Eye-Opening Monitor for Continuous Link-Margin Diagnosis
  - Reverse-Channel Adaptive Equalization Allows Coax Cable Longer than 15m with Multiple Inline Connectors
  - Crosspoint Switch Remaps Input to Any Desired Deserializer Output Order
- ASIL-Relevant Functional Safety Features (GMSL2)
  - ASIL-B Compliant
  - 16-Bit CRC Protection of Side-Channel Data (I^2C, UART, SPI, GPIO) with Retransmission upon Error Detection
  - Optional 32-Bit CRC Protection of Video-Line Data
  - Video Watermark Insertion and Detection
- Concurrent Side Channel for Device Configuration and Communication with Peripherals
  - GMSL2: I^2C/UART, Dual Pass-Through I^2C/UART, SPI, GPIO and Register-Programmable GPIO
  - GMSL1: I^2C/UART, Tunneled GPI-GPO and CNTL Links, and Register-Programmable GPIO
  - Four Hardware-Selectable Device Addresses
- Three Internal and Three External Supply Voltage Monitors
- 50Ω Coax Cable or 100Ω STP
- Programmable Spread Spectrum for EMI Reduction
- 7mm x 7mm TQFN Package with Exposed Pad and Available Wettable Flanks
- -40°C to +105°C Operating Temperature
- AEC-Q100 Grade 2

Ordering Information appears at end of data sheet.

19-100518; Rev 6; 11/23

Simplified Block Diagram



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Absolute Maximum Ratings

(All voltages with respect to ground.) .....
V_{DDIO} ..... -0.3V to +3.9V
V_{DD18} ..... -0.3V to +2.0V
V_{DD} ..... -0.3V to +2.0V
CAP_VDD ..... -0.3V to +1.2V
SIO_ (Active State) (*Note a*)..... (V_{DD18} - 1.1V) to V_{DD18}
SIO_ (Inactive State) (*Note a*) ..... -0.3V to +1.1V
DA/B_P/N, CKA/BP/N ..... -0.3V to +1.35V
XRES, X2 ..... -0.3V to (V_{DD18} + 0.3)
All Other Pins (*Note b*) ..... -0.3V to (V_{DDIO} + 0.3)
Continuous Power Dissipation - Multilayer Board (*Note c*) 2200mW
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note a: Active state means the device is powered up and not in sleep or power-down mode. Inactive means the device is not powered up, or it is powered up in sleep or power-down mode.

Note b: Specified maximum voltage or 3.9V, whichever is lower.

Note c: Derate 40mW/°C above T_A = +70°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

48-Pin TQFN

Package Code	T4877+11C
Outline Number	21-0144
Land Pattern Number	90-0130
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1.1°C/W

48-Pin TQFN-SW (Side-Wettable)

Package Code	T4877Y+11C
Outline Number	21-100045
Land Pattern Number	90-100016
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to *www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board in still air. For detailed information on package thermal considerations, refer to *www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages*.

Electrical Characteristics

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDIO} = 1.7V to 1.9V or 3.0V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / GMSL2 FORWARD-CHANNEL SERIAL OUTPUTS (SIO_) - SEE Figure 1						
Output-Voltage Swing (Single-Ended)	V_O	R_L = 100Ω ±1%, (V_{OH} - V_{OL}) for both outputs	300	400	500	mV
Output-Voltage Swing (Differential)	V_{ODT}	R_L = 100Ω ±1%, peak-to-peak differential voltage	600	800	1000	mV_{P-P}
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	R_L = 100Ω ±1%, $\lvert V_{OD(H)}-V_{OD(L)}\rvert$			25	mV
Differential-Output Offset Voltage	V_{OS}	R_L = 100Ω ±1%, offset voltage in each output state	V_{DD18} - 0.65	V_{DD18} - 0.45	V_{DD18} - 0.25	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	R_L = 100Ω ±1%, $\lvert V_{OS(H)} - V_{OS(L)}\rvert$			25	mV
Termination Resistance (Internal)	R_T	Any pin to V_{DD18}	50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / GMSL1 FORWARD-CHANNEL SERIAL OUTPUTS (SIO_) - SEE Figure 1						
Output-Voltage Swing (Single-Ended)	V_O	R_L = 100Ω ±1%, coax mode	375	500	625	mV
Output Offset Voltage (Single-Ended)	V_{OS}	R_L = 100Ω ±1%, coax mode	V_{DD18} - 0.75	V_{DD18} - 0.55	V_{DD18} - 0.35	V
Output-Voltage Swing (Differential)	V_{ODT}	R_L = 100Ω ±1%, STP mode	600	800	1000	mV_{P-P}
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	R_L = 100Ω ±1%, $\lvert V_{OD(H)}-V_{OD(L)}\rvert$, STP mode			25	mV
Differential-Output Offset Voltage	V_{OS}	R_L = 100Ω ±1%, STP mode	V_{DD18} - 0.65	V_{DD18} - 0.45	V_{DD18} - 0.25	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	R_L = 100Ω ±1%, $\lvert V_{OS(H)} - V_{OS(L)}\rvert$, STP mode			25	mV
Termination Resistance (Internal)	R_T	Any pin to V_{DD18}	50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / GMSL1 REVERSE CONTROL-CHANNEL RECEIVER (SIO_)						
High Switching Threshold	V_{CHR}	HIM disabled			27	mV
		HIM enabled			40	
Low Switching Threshold	V_{CLR}	HIM disabled	-27			mV
		HIM enabled	-40			
DC ELECTRICAL CHARACTERISTICS / D-PHY HS RECEIVER						
Common-Mode Voltage HS Receive Mode	$V_{CMRX(DC)}$		70		330	mV
Differential Input High Threshold	V_{IDTH}				40	mV

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDIO} = 1.7V to 1.9V or 3.0V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Low Threshold	V_{IDTL}		-40			mV
Differential Input Impedance	Z_{ID}	(*Note 2*)	80	100	125	Ω
Single-Ended Input High Voltage	V_{IHHS}				460	mV
Single-Ended Input Low Voltage	V_{ILHS}		-40			mV
Single-Ended Threshold for HS Termination Enable	$V_{TERM-EN}$	(*Note 2*)			450	mV
DC ELECTRICAL CHARACTERISTICS / D-PHY LP RECEIVER						
High-Level Input Voltage	V_{IH}		740			mV
Low-Level Input Voltage	V_{IL}				550	mV
Input Hysteresis	V_{HYST}	(*Note 2*)	25			mV
Pin Leakage Current	I_{LEAK}	-0.05V to +1.35V	-10		+10	µA
DC ELECTRICAL CHARACTERISTICS / I/O PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pull-up/pull-down devices disabled, V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pull-Up/Pull-Down Resistance	R_{IN}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pull-up/pull-down devices disabled, V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pull-Up Resistance	R_{PU}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDIO} = 1.7V to 1.9V or 3.0V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DDIO}			6	µA
Input Capacitance	C_{IN}			3		pF
Internal Pull-Down Resistance	R_{PD}			1		MΩ
DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS						
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
DC ELECTRICAL CHARACTERISTICS / LINE-FAULT DETECTION INPUTS (LMN0, LMN1)						
Open Pin Voltage	V_{O0}	LMN0		1.25		V
	V_{O1}	LMN1		0.75		
DC ELECTRICAL CHARACTERISTICS / REFERENCE-CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1/OSC, X2)						
X1 Input Capacitance	C_{IN_X1}			3		pF
X2 Input Capacitance	C_{IN_X2}			1		pF
Internal X2 Limit Resistor	R_{LIM}			1.2		kΩ
Internal Feedback Resistor	R_{FB}			10		kΩ
Transconductance	g_M			28		mA/V
DC ELECTRICAL CHARACTERISTICS / REFERENCE-CLOCK REQUIREMENTS (EXTERNAL INPUT ON X1/OSC, X2 UNCONNECTED)						
High-Level Input Voltage	V_{IH}		0.9			V
Low-Level Input Voltage	V_{IL}				0.4	V
Input Impedance	R_{IN}			10		kΩ
X1 Input Capacitance	C_{IN_X1}			3		pF
DC ELECTRICAL CHARACTERISTICS / MONITOR ADC						
Resolution				10		Bits

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDIO} = 1.7V to 1.9V or 3.0V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Using internal reference, no divider, no internal buffer			0 to V_{REF}		V
		Using internal reference, 2:1 divider, no internal buffer, pin function ADC0			0 to 2 x V_{REF}		
		Using internal reference, 2:1 divider, no internal buffer, pin functions ADC1 and ADC2			0 to Lesser of 2 x V_{REF} or V_{DDIO}		
		Using internal reference, 3:1 divider, no internal buffer, pin function ADC0			0 to 3.6		
		Using internal reference, 3:1 divider, no internal buffer, pin functions ADC1 and ADC2			0 to V_{DDIO}		
		Using internal reference, 4:1 divider, no internal buffer, pin function ADC0			0 to 3.6		
		Using internal reference, 4:1 divider, no internal buffer, pin functions ADC1 and ADC2			0 to V_{DDIO}		
		No divider, internal buffer enabled			0.1 to V_{REF}		
Input Resistance	R_{IN}	Input configured for 2:1 voltage division			60		kΩ
		Input configured for 4:1 voltage division			40		
		No divider, buffered input			> 5		MΩ
Total Unadjusted Error	TUE	V_{REF} = 1.25V, no divider, buffer enabled	External voltage = 0.1V	-10		+10	mV
			External voltage = 0.625V	-12		+12	
			External voltage = 1.2V	-15		+15	
Reference-Voltage Tolerance for 1% ADC Accuracy	V_{REF_TOL}	V_{REF} = 1.2V			±1		mV
ADC Supply Current		ADC Enabled			260		µA

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDIO} = 1.7V to 1.9V or 3.0V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / POWER-SUPPLY CURRENT - GMSL2 MODE							
Supply Current (*Note 3*)	I_{DD}	3Gbps serial link, two four-lane inputs, 325Mbps/lane, RGB888	V_{DD18}		90	120	mA
			V_{DD} = 1V Range		95	330	
			V_{DD} = 1.2V Range		95	330	
		3Gbps serial link, one four-lane input, 650Mbps/lane, RGB888	V_{DD18}		90	120	
			V_{DD} = 1V Range		85	330	
			V_{DD} = 1.2V Range		85	330	
		6Gbps serial link, two four-lane inputs, 650Mbps/lane, RGB888	V_{DD18}		90	120	
			V_{DD} = 1V Range		120	360	
			V_{DD} = 1.2V Range		120	360	
		6Gbps serial link, one four-lane input, 1.3Gbps/lane, RGB888	V_{DD18}		90	120	
			V_{DD} = 1V Range		110	350	
			V_{DD} = 1.2V Range		110	350	
Maximum V_{DDIO} Supply Current (*Note 4*)	I_{DDIO}	Per toggling GPIO, C_L = 20pF	V_{DDIO} = 1.8V Range		44		µA/MHz
			V_{DDIO} = 3.3V Range		81		
DC ELECTRICAL CHARACTERISTICS / POWER-SUPPLY CURRENT - GMSL1 MODE							
Supply Current (*Note 3*)	I_{DD}	4.5Gbps serial link, one four-lane input, 900Mbps/lane, RGB888, high-bandwidth mode (HIBW = 1)	V_{DD18}		60	90	mA
			V_{DD} = 1V Range		65	295	
			V_{DD} = 1.2V Range		65	295	
Maximum V_{DDIO} Supply Current (*Note 4*)	I_{DDIO}	Per toggling GPIO, C_L = 20pF	V_{DDIO} = 1.8V Range		44		µA/MHz
			V_{DDIO} = 3.3V Range		81		
DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENT							
Maximum Power-Down Current	I_{DD}	V_{DDIO} = 3.6V	T_A = +25°C		4.5		µA
			T_A = +105°C		5		
		V_{DD18} = 1.9V	T_A = +25°C		1.3		
			T_A = +105°C		6		
		V_{DD} = 1.26V	T_A = +25°C		< 1		
			T_A = +105°C		< 1		

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDIO} = 1.7V to 1.9V or 3.0V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / SLEEP CURRENT							
Maximum Sleep Current	I_{DD}	V_{DDIO} = 3.6V	T_A = +25°C		4.5		µA
			T_A = +105°C		5		
		V_{DD18} = 1.9V	T_A = +25°C		16.5		
			T_A = +105°C		22		
		V_{DD} = 1.26V	T_A = +25°C		< 1		
			T_A = +105°C		< 1		
AC ELECTRICAL CHARACTERISTICS / GMSL2 FORWARD-CHANNEL SERIAL OUTPUTS (SIO_)							
Serial-Output Rise Time	t_R	20% to 80%, V_O = 400mV, R_L = 100Ω ±1%			50		ps
Serial-Output Fall Time	t_F	80% to 20%, V_O = 400mV, R_L = 100Ω ±1%			50		ps
Total Serial-Output Jitter	t_{TSOJ}	PRBS7, single-ended or differential output			0.15		UI (p-p)
Deterministic Serial-Output Jitter	t_{DSOJ}	PRBS7, single-ended or differential output			0.10		UI (p-p)
Lock Time	t_{LOCK}	From power-up, one-shot reset, or rising edge of PWDNB to rising edge of LOCK. See Figure 20			20		ms
Maximum Video-Initialization Time	$t_{VIDEOSTART}$	Time from video applied to input until the first video packet appears at GMSL2 outputs, assuming link is already established. See Figure 2			1.1 + 17,000 x t_{PCLK}		ms
Maximum Video Latency	t_{VL}	Time from CSI-2 input to SIO± output in GMSL2 packet. See Figure 3			120 x t_{PCLK}		s
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the chip.			1		ms
GPI-GPO Delay Reverse Path	t_{GPDR}	Delay-compensated Mode, See Table 6			15		µs
		Non-delay-compensated Mode, See Table 6			6		
GPI-GPO Skew Reverse Path	t_{SKEW}	Delay-compensated Mode			7		ns
AC ELECTRICAL CHARACTERISTICS / GMSL1 FORWARD-CHANNEL SERIAL OUTPUTS (SIO_)							
Serial-Output Rise Time	t_R	20% to 80%, R_L = 100Ω ±1%			50		ps
Serial-Output Fall Time	t_F	80% to 20%, R_L = 100Ω ±1%			50		ps
Total Serial-Output Jitter	t_{TSOJ1}	PRBS7, single-ended or differential output			0.25		UI
Deterministic Serial-Output Jitter	t_{DSOJ2}	PRBS7, single-ended or differential output			0.15		UI
Maximum Link Startup Time		Figure 4			250		µs
Maximum Video Latency		Time from high-speed signal received at input until it appears on GMSL1 output during active video (Figure 5)			100		t_{PCLK}

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDIO} = 1.7V to 1.9V or 3.0V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / D-PHY HS RECEIVER (*Note 2*)						
Common-Mode Interference Beyond 450MHz	$\Delta V_{CMRX(HF)}$	(*Note 5*)			50	mV
Common-Mode Interference 50MHz to 450MHz	$\Delta V_{CMRX(LF)}$	(*Note 6*, *Note 7*)	-25		+25	mV
Differential-Mode Reflection Coefficient (*Note 8*)	Sdd_{RX}	f < 20MHz		-22.5		dB
		f = 1.25GHz		-10		
		f = 1.875GHz		-7.5		
Common-Mode Reflection Coefficient (*Note 8*)	Scc_{RX}	450MHz < f < 1.875GHz		-5		dB
AC ELECTRICAL CHARACTERISTICS / D-PHY LP RECEIVER - SEE Figure 6 (*Note 2*)						
Input-Pulse Rejection	e_{SPIKE}				300	V-ps
Minimum Pulse-Width Response	t_{MIN-RX}		20			ns
Peak Interference Amplitude	V_{INT}				200	mV
Interference Frequency	f_{INT}		450			MHz
AC ELECTRICAL CHARACTERISTICS / D-PHY DATA-CLOCK TIMING - SEE Figure 7 (*Note 2*)						
UI Instantaneous	UI_{INST}		0.4		12.5	ns
UI Variation	ΔUI	UI ≥ 1ns, within a single burst	-10%		+10%	UI
		0.667ns < UI < 1ns, within a single burst	-5%		+5%	
Data-to-Clock Setup Time	$t_{SETUP(RX)}$	0.08Gbps to 1.0Gbps	0.15			UI_{INST}
		> 1.0Gbps to 1.5Gbps	0.20			
Data-to-Clock Hold Time	$t_{HOLD(RX)}$	0.08Gbps to 1.0Gbps	0.15			UI_{INST}
		> 1.0Gbps to 1.5Gbps	0.20			
Static Data-to-Clock Skew (Rx)	$t_{SKEW(RX)}$ Static	> 1.5Gbps	-0.20		+0.20	UI_{INST}
Dynamic Data-to-Clock Skew Window Rx Tolerance	$t_{SETUP(RX)}$ + $t_{HOLD(RX)}$ Dynamic	> 1.5Gbps	0.50			UI_{INST}
AC ELECTRICAL CHARACTERISTICS / D-PHY CSI GLOBAL OPERATION TIMING (*Note 2*)						
Time interval during which the HS receiver ignores any clock-lane HS transitions, starting from the beginning of TCLK_PREPARE	T_{CLK_SETTLE}	See Figure 8	95		300	ns

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDIO} = 1.7V to 1.9V or 3.0V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time for the clock-lane receiver to enable the HS line termination, starting from the time when Dn crosses $V_{IL,MAX}$	$T_{CLK-TERM-EN}$	See Figure 9	Time for Dn to reach $V_{TERM-EN}$		38	ns
Time for the data-lane receiver to enable the HS line termination, starting from the time when Dn crosses $V_{IL,MAX}$	$T_{D-TERM-EN}$	See Figure 10	Time for Dn to reach $V_{TERM-EN}$		35ns + 4 x UI_{INST}	ns
Time interval during which the HS receiver ignores any data-lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$.	T_{HS_SETTLE}	See Figure 10	85ns + 6 x UI_{INST}		145ns + 10 x UI_{INST}	ns
AC ELECTRICAL CHARACTERISTICS / I^2C/UART PORT TIMING						
Output Fall Time	t_F	70% to 30%, C_L = 20pF to 100pF, 1kΩ pull-up to V_{DDIO} (*Note 2*)	20 x V_{DDIO}/5.5V		150	ns
I^2C/UART Wake Time		From power-up, or rising edge of PWDNB to local register access; for remote register access, I^2C/UART wake time is the same as lock time (t_{LOCK}).		2.25		ms
AC ELECTRICAL CHARACTERISTICS / I^2C TIMING - SEE Figure 11						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2C_MST_BT = 010, I2C_SLV_SH = 10)	9.6		100	kHz
		Mid f_{SCL} range: (I2C_MST_BT = 101, I2C_SLV_SH = 01)	100		400	
		High f_{SCL} range: (I2C_MST_BT = 111, I2C_SLV_SH = 00)	400		1000	
Start-Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Repeated Start-Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDIO} = 1.7V to 1.9V or 3.0V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, low	0			ns
		f_{SCL} range, mid	0			
		f_{SCL} range, high	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, low	250			ns
		f_{SCL} range, mid	100			
		f_{SCL} range, high	50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, low			50	ns
		f_{SCL} range, mid			50	
		f_{SCL} range, high			50	
Capacitive Load On Each Bus Line	C_B	(*Note 2*)			100	pF
AC ELECTRICAL CHARACTERISTICS / SPI MAIN - SEE Figure 12 (*Note 4*)						
Operating Frequency	f_{MCK}	(*Note 2*)	0.588		50	MHz
SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}	C_L = 5pF (*Note 2*)	$t_{MCK}/2$ - 3.4	$t_{MCK}/2$		ns
MOSI Output Valid Time	t_{MOV}	After SCLK falling edge, C_L = 5pF (*Note 2*)	2.3		t_{MCK} - 2.3	ns
MISO Input Setup Time	t_{MIS}	Before programmed sampling edge (*Note 2*)	13.5			ns
MISO Input Hold Time	t_{MIH}	After programmed sampling edge (*Note 2*)	-2			ns
AC ELECTRICAL CHARACTERISTICS / SPI SUBORDINATE - SEE Figure 13 (*Note 9*)						
Operating Frequency	f_{SCK}	(*Note 2*)			50	MHz
SCLK Period	t_{SCK}			$1/f_{SCK}$		ns
MOSI Output Valid Time	t_{SOV}	After SCLK falling edge, C_L = 5pF (*Note 2*)	11.3		t_{SCK} - 1.5	ns
MOSI Input Setup Time	t_{SIS}	Before SCLK rising edge (*Note 2*)	5			ns

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDIO} = 1.7V to 1.9V or 3.0V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MOSI Input Hold Time	t_{SIH}	After SCLK rising edge (*Note 2*)	3			ns
AC ELECTRICAL CHARACTERISTICS / MONITOR ADC						
Conversion Time				430		µs
ADC Setup Time	t_{ADC_SETUP}	Excluding V_{REF} power-up time		30		µs
ADC Clock	f_{ADCCLK}			2.5		MHz
AC ELECTRICAL CHARACTERISTICS / REFERENCE-CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1/OSC, X2) (*Note 2*)						
Frequency	f_{REF}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
AC ELECTRICAL CHARACTERISTICS / REFERENCE-CLOCK REQUIREMENTS (EXTERNAL CLOCK INPUT ON X1/OSC, X2 UNCONNECTED) (*Note 2*)						
Frequency	f_{REF}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
Input Jitter		Link speed = 6Gbps/187.5Mbps sinusoidal jitter < 1MHz (falling edge) downstream deserializer using crystal reference			600	ps (p-p)
Input Duty Cycle	t_{DUTY}		40		60	%
Input Fall Time	t_F	80% to 20%			4	ns
AC ELECTRICAL CHARACTERISTICS / REFERENCE-CLOCK OUTPUT (RCLKOUT)						
Frequency	f_{REFOUT}	Crystal or reference clock input, f_{REF} / 1		25		MHz
		Crystal or reference clock input, f_{REF} / 2		12.5		MHz
		Crystal or reference clock input, f_{REF} / 4		6.25		MHz
Rise Time	t_R	20% to 80%, C_L = 10pF (*Note 2*, *Note 10*)			4	ns
Fall Time	t_F	80% to 20%, C_L = 10pF (*Note 2*, *Note 10*)			4	ns
Jitter	t_J	C_L = 10pF, rising or falling edge f_{REFOUT} = 12.5MHz		210		ps (p-p)
AC ELECTRICAL CHARACTERISTICS / DIGITAL PLL OUTPUT (DPLL_OUT)						
Frequency	f_{DPLL}	Maximum			75	MHz
		Minimum		150		kHz
Rise Time	t_R	20% to 80%, C_L = 10pF (*Note 2*, *Note 4*)			3	ns
Fall Time	t_F	80% to 20%, C_L = 10pF (*Note 2*, *Note 4*)			3	ns
Jitter	t_J	Rising or falling edge, deterministic jitter + 14 x random jitter f_{DPLL} = 27MHz (*Note 2*)			750	ps (p-p)

Note 1: Limits are 100% tested at T_A = +105°C unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: Color bar pattern.

Note 4: MFP pin speed programmed to fastest setting (TTS = 00). See Table 13 for details regarding output speed programming.

Note 5: $\Delta V_{CRMX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.

Note 6: Excluding static ground shift of 50mV.

Note 7: Voltage difference compared to the DC average common-mode potential.

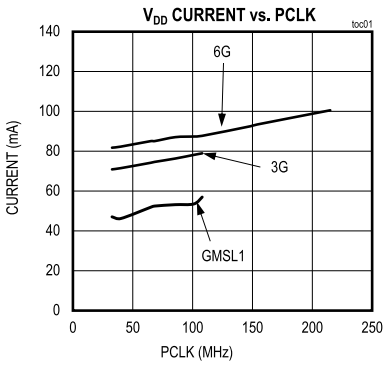
Note 8: Differential-mode and common-mode reflection coefficient are compliant with MIPI D-PHY V1.2 requirements over all specified operating frequencies.

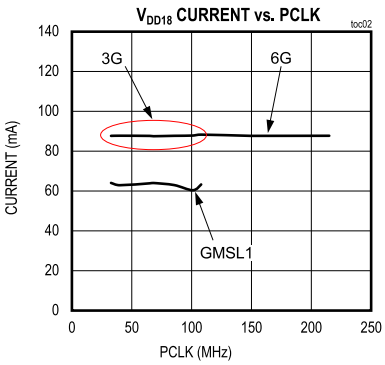
Note 9: Measured at 50MHz. For V_{DDIO} < 2.25V, Speed Group A TTS = 00 and for V_{DDIO} ≥ 2.25V, Speed Group A TTS = 01. See Table 12 for details regarding output-speed programming.

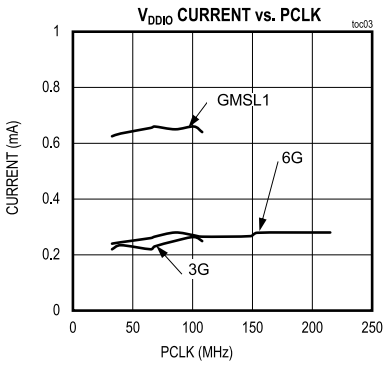
Note 10: MFP pin speed configured based on V_{DDIO}:
TTS = 01 for V_{DDIO} < 3V
TTS = 10 for V_{DDIO} ≥ 3V
See Table 13 for details regarding output speed programming.

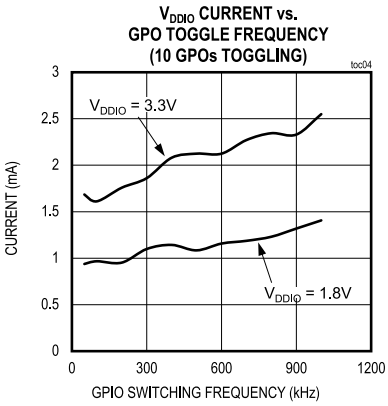
Typical Operating Characteristics

(V_{DD18} = V_{DD18_LVDS} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C. In daisy-chain applications, the streams input at SIO drive both the OLDI outputs and DCIO, and SIO and DCIO are both set to the same GMSL mode.)

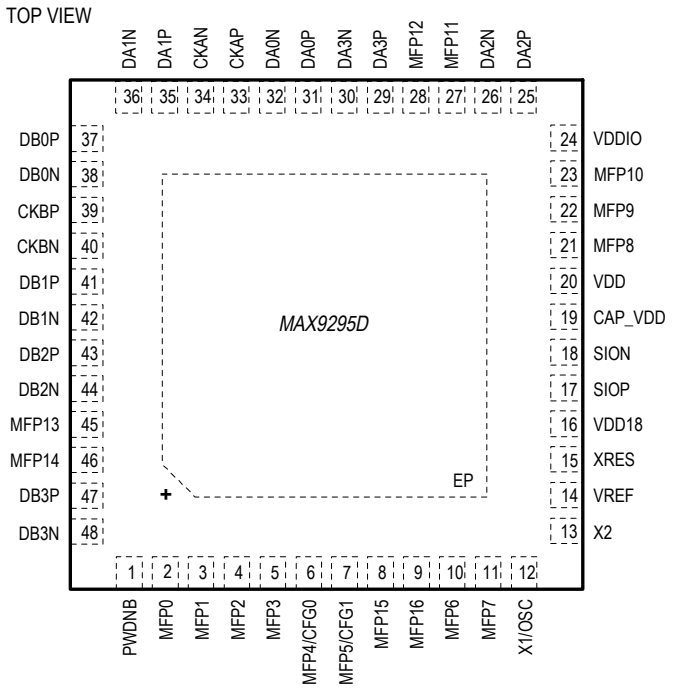








Pin Configuration



Pin Descriptions

PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
GMSL2/GMSL1 SERIAL LINK				
17	SIOP	SIOP	SIOP	Non-Inverted Coax/Twisted-Pair Serial-Data Input/ output. State of CFG1 at power-up determines configuration.
18	SION	SION	SION	Inverted Twisted-Pair Serial-Data Input/output. State of CFG1 at power-up determines configuration.
CSI INTERFACE A				
31	DA0P	DA0P	DA0P	CSI-2 Port A Data Lane 0 Non-Inverted D-PHY Input
32	DA0N	DA0N	DA0N	CSI-2 Port A Data Lane 0 Inverted D-PHY Input
35	DA1P	DA1P	DA1P	CSI-2 Port A Data Lane 1 Non-Inverted D-PHY Input
36	DA1N	DA1N	DA1N	CSI-2 Port A Data Lane 1 Inverted D-PHY Input
25	DA2P	DA2P	DA2P	CSI-2 Port A Data Lane 2 Non-Inverted D-PHY Input
26	DA2N	DA2N	DA2N	CSI-2 Port A Data Lane 2 Inverted D-PHY Input
29	DA3P	DA3P	DA3P	CSI-2 Port A Data Lane 3 Non-Inverted D-PHY Input
30	DA3N	DA3N	DA3N	CSI-2 Port A Data Lane 3 Inverted D-PHY Input
33	CKAP	CKAP	CKAP	CSI-2 Port A Clock Lane Non-Inverted D-PHY Input

PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
34	CKAN	CKAN	CKAN	CSI-2 Port A Clock Lane Inverted D-PHY Input
CSI INTERFACE B				
37	DB0P	DB0P	DB0P	CSI-2 Port B Data Lane 0 Non-Inverted D-PHY Input.
38	DB0N	DB0N	DB0N	CSI-2 Port B Data Lane 0 Inverted D-PHY Input.
41	DB1P	DB1P	DB1P	CSI-2 Port B Data Lane 1 Non-Inverted D-PHY Input.
42	DB1N	DB1N	DB1N	CSI-2 Port B Data Lane 1 Inverted D-PHY Input.
43	DB2P	DB2P	DB2P	CSI-2 Port B Data Lane 2 Non-Inverted D-PHY Input.
44	DB2N	DB2N	DB2N	CSI-2 Port B Data Lane 2 Inverted D-PHY Input.
47	DB3P	DB3P	DB3P	CSI-2 Port B Data Lane 3 Non-Inverted D-PHY Input.
48	DB3N	DB3N	DB3N	CSI-2 Port B Data Lane 3 Inverted D-PHY Input.
39	CKBP	CKBP	CKBP	CSI-2 Port B Clock Lane Non-Inverted D-PHY Input.
40	CKBN	CKBN	CKBN	CSI-2 Port B Clock Lane Inverted D-PHY Input.
MULTIFUNCTION PINS (* denotes default state after power-up) (input read or output write by register programming only) - SEE Table 3**				
2	MFP0	SCLK GPIO0*	CNTL1* GPIO0**	CNTL1: CMOS Control Input with Internal 1MΩ Pull-Down to Ground. Tunnels through to corresponding pin on deserializer. SCLK: SPI Clock. When configured as main, push-pull clock output. When configured as subordinate, clock input with internal 1MΩ pull-down to ground. GPIO0: Configurable General-Purpose Input or Output. GMSL2 power-up default is bidirectional open-drain output with CMOS input receiver and 40kΩ pull-up to V_{DDIO}.
3	MFP1	MOSI GPIO1*	CNTL2* GPIO1**	CNTL2: CMOS Control Input with Internal 1MΩ Pull-Down to Ground. Tunnels through to corresponding pin on deserializer MOSI: SPI Main Out, Subordinate In. When configured as main, push-pull output that drives data to external subordinate. When configured as subordinate, input with internal 1MΩ pull-down to ground that receives data from external main. GPIO1: Configurable General-Purpose Input or Output. GMSL2 Power-up default is high impedance with floating input receiver. User must drive pin to ground or V_{DDIO}, or enable internal pull-up or pull-down resistor.

PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
4	MFP2	MISO GPIO2*	GPO(Alt) GPIO2(*)**	MISO: SPI Main In, Subordinate Out. When configured as main, input with internal 1MΩ pull-down to ground that receives data from external subordinate. When configured as subordinate, push-pull output that drives data to an external main. GPO(Alt): Dedicated Push-Pull Output for GMSL1 GPI-GPO Sync Signal. GPIO2: Configurable General-Purpose Input or Output. Power-up default is high impedance with floating input receiver. User must drive pin to ground or V_{DDIO}, or enable internal pull-up or pull-down resistor.
5	MFP3	RCLKOUT DPLL_OUT GPIO3*	CNTL3* RCLKOUT DPLL_OUT GPIO3**	CNTL3: CMOS Control Input with Internal 1MΩ Pull-Down to Ground. Tunnels through to corresponding pin on deserializer. RCLKOUT: 25MHz Frequency Reference Divider Push-Pull Output. Divide by 2 or 4 available. In GMSL1 mode, optional crystal must be connected to use this feature. DPLL_OUT: Digital PLL Push-Pull Output. In GMSL1 mode, optional crystal must be connected to use this feature. GPIO3: Configurable General-Purpose Input or Output. GMSL2 Power-up default is high impedance with floating input receiver. User must drive pin to ground or V_{DDIO}, or enable internal pull-up or pull-down resistor.
6	MFP4/CFG0	CFG0 BNE SS1 GPO4*	CFG0 GPO4(*)**	CFG0: Configuration Pin 0. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor-divider between V_{DDIO} and ground. See Table 9 for configuration details. BNE: SPI Buffer Not Empty. When configured as subordinate, SPI BNE push-pull output. BNE = high indicates SPI data is available, Subordinate 1 select push-pull output. GPO4: General-Purpose Push-Pull Output. Disabled by default to accommodate CFG0 function.
7	MFP5/CFG1	CFG1 GPO5*	CFG1 GPO5(*)**	CFG1: Configuration Pin 1. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor-divider between V_{DDIO} and ground. See Table 10 for configuration details. GPO5: General-Purpose Push-Pull Output. Disabled by default to accommodate CFG1 function.

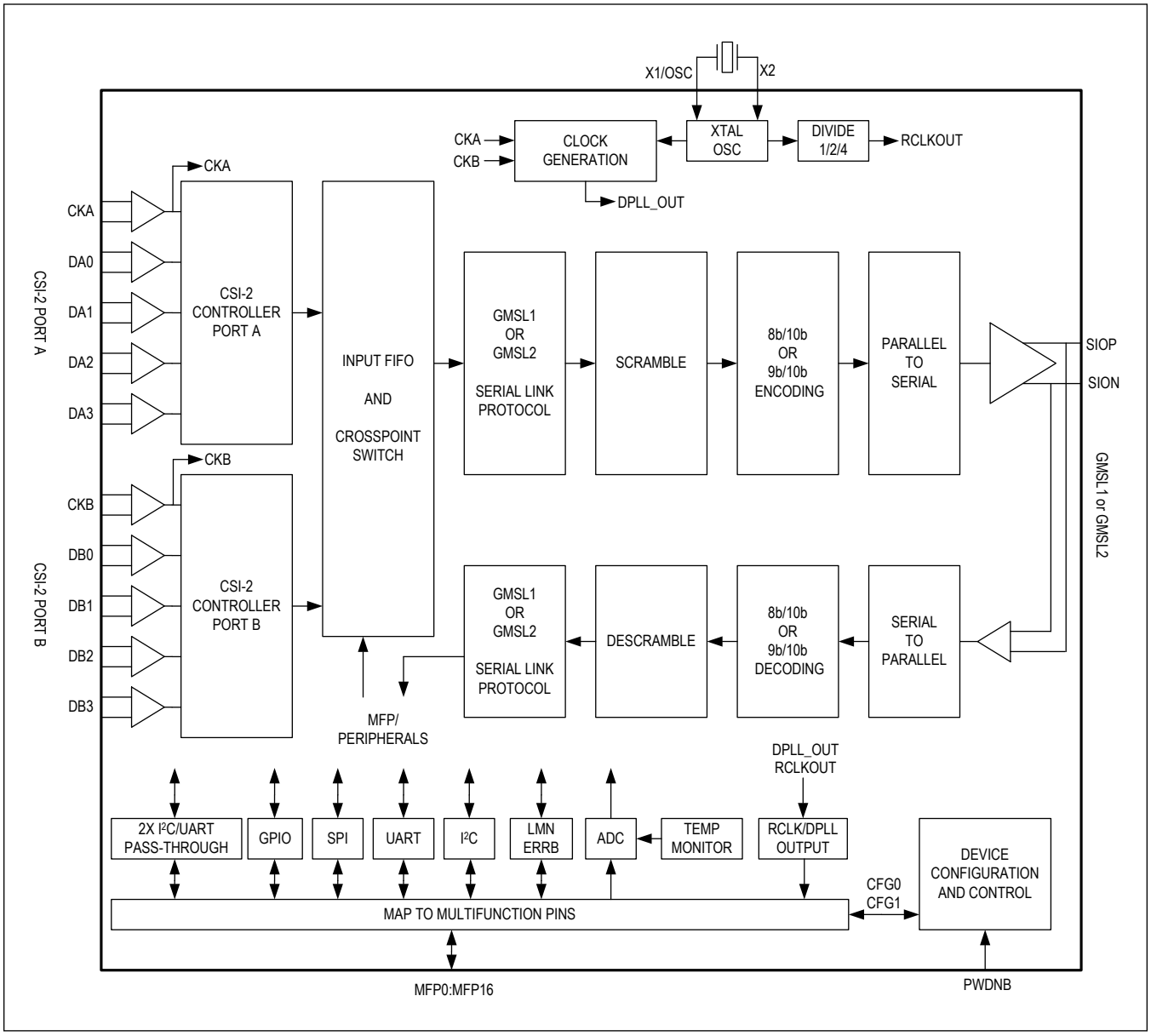
PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
10	MFP6	ERRB GPIO6*	CNTL0* ERRB GPIO6**	CNTL0: CMOS Control Input with Internal 1MΩ Pull-Down to Ground. Tunnels through to corresponding pin on deserializer. ERRB: Open-Drain Error Indication Output with Internal 40kΩ Pull-Up to V_{DDIO}. ERRB = low indicates that a data error, line fault, or interrupt has been detected. GPIO6: Configurable General-Purpose Input or Output. GMSL2 Power-up default is high impedance with floating input receiver. User must drive pin to ground or V_{DDIO}, or enable internal pull-up or pull-down resistor.
11	MFP7	ADC0 GPIO7*	ADC0 GPIO7(*)**	ADC0: Supply Voltage Monitor Input 0. GPIO7: Configurable General-Purpose Input or Output. GMSL2 power-up default is general-purpose input with internal 1MΩ pull-down to ground. GMSL1 Power-up default is high impedance with floating input receiver. User must drive pin to ground or V_{DDIO}, or enable internal pull-up or pull-down resistor when in GMSL1 mode.
21	MFP8	ADC1 GPIO8*	ADC1 GPIO8(*)**	ADC1: Supply Voltage Monitor Input 1. GPIO8: Configurable General-Purpose Input or Output. GMSL2 power-up default is bidirectional open-drain output with CMOS input receiver and 40kΩ pull-up to V_{DDIO}. GMSL1 power-up default is high impedance with floating input receiver. User must drive pin to ground or V_{DDIO}, or enable internal pull-up or pull-down resistor when in GMSL1 mode.
22	MFP9	LOCK ADC2 GPIO9*	LOCK ADC2 GPO* GPIO9**	LOCK: Open-Drain Lock Indication Output with Internal 40kΩ Pull-Up to V_{DDIO}. ADC2: Supply Voltage Monitor Input 2. GPO: Dedicated Push-Pull Output for GMSL1 GPI-GPO Sync Signal. Default output state is logic-low. GPIO9: Configurable General-Purpose Input or Output. GMSL2 Power-up default is high impedance with floating input receiver. User must drive pin to ground or V_{DDIO}, or enable internal pull-up or pull-down resistor.

PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
23	MFP10	RO SS2 MS GPIO10*	CNTL4 MS GPIO10(*)**	CNTL4: CMOS Control Input with Internal 1MΩ Pull-Down to Ground. Tunnels through to corresponding pin on deserializer. RO: When Configured as Subordinate, SPI Mode-Select Input with Internal 1MΩ Pull-Down to Ground. RO = high enables main read from MISO. RO = low enables main write to MOSI. SS2: SPI Subordinate Select. When configured as main, Subordinate 2 select push-pull output. MS: UART Mode Select with Internal 1MΩ Pull-Down to Ground. Set MS = low to select base mode. Set MS = high to select bypass mode. MS state may also be temporarily overwritten by a register write. GPIO10: Configurable General-Purpose Input or Output. Power-up default is high impedance with floating input receiver. User must drive pin to ground or V_{DDIO}, or enable internal pull-up or pull-down resistor.
27	MFP11	SDA1 RX1 ODO11/GPI11*	ODO11/GPI11(*)**	SDA1: Pass-Through Port 1 I^2C Data Input/Open-Drain Output with Internal 40kΩ Pull-Up to V_{DDIO}. RX1: Pass-Through Port 1 UART Input. ODO11/GPI11: Configurable General-Purpose Input and/or Open-Drain Output with Selectable Internal Pull-Up. Power-up default is high impedance with floating input receiver. User must drive pin to ground or V_{DDIO}, or enable internal pull-up or pull-down resistor.
28	MFP12	SCL1 TX1 ODO12/GPI12*	ODO12/GPI12(*)**	SCL1: Pass-Through Port 1 I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pull-Up to V_{DDIO}. TX1: Pass-Through Port 1 UART Output with Internal 40kΩ Pull-Up to V_{DDIO}. ODO12/GPI12: Configurable General-Purpose Input and/or Open-Drain Output with Selectable Internal Pull-Up. Power-up default is high impedance with floating input receiver. User must drive pin to ground or V_{DDIO}, or enable internal pull-up or pull-down resistor.
45	MFP13	LMN0 ODO13/GPI13*	LMN0 ODO13/GPI13(*)**	LMN0: Line-Fault Monitor Input 0. ODO13/GPI13: Configurable General-Purpose Input and/or Open-Drain Output with Selectable Internal Pull-Up. Power-up default is high impedance with floating input receiver. User must drive pin to ground or V_{DDIO}, or enable internal pull-up or pull-down resistor.

PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
46	MFP14	LMN1 ODO14/GPI14*	LMN1 ODO14/GPI14(*)**	LMN1: Line-Fault Monitor Input 1. ODO14/GPI14: Configurable General-Purpose Input and/or Open-Drain Output with Selectable Internal Pull-Up. Power-up default is high impedance with floating input receiver. User must drive pin to ground or V_{DDIO}, or enable internal pull-up or pull-down resistor.
8	MFP15	SDA* RX* SDA2 RX2 ODO15/GPI15	SDA* RX* ODO15/GPI15**	SDA: Primary I^2C Data Input/Open-Drain Output with Internal 40kΩ Pull-Up to V_{DDIO} (SDA or RX selected by CFG0 at power-up). Provides access to internal GMSL device registers and peripheral registers. RX: Main UART Input (SDA or RX selected by CFG0 at power-up). Provides access to internal GMSL device registers and peripheral registers. SDA2: Pass-Through Port 2 I^2C Data Input/Open-Drain Output with Internal 40kΩ Pull-Drain to V_{DDIO}. RX2: Pass-Through Port 2 UART Input. ODO15/GPI15: Configurable General-Purpose Input and/or Open-Drain Output with Selectable Internal Pull-Up.
9	MFP16	SCL* TX* SCL2 TX2 ODO16/GPI16	SCL* TX* ODO16/GPI16**	SCL: Primary I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pull-Up to V_{DDIO} (SCL or TX selected by CFG0 at power-up). Provides access to internal GMSL device registers and peripheral registers. TX: Main UART Open-Drain Output with Internal 40kΩ Pull-Up to V_{DDIO} (SCL or TX selected by CFG0 at power-up). Provides access to internal GMSL device registers and peripheral registers. SCL2: Pass-Through Port 2 I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pull-Up to V_{DDIO}. TX2: Pass-Through Port 2 UART Output with Internal 40kΩ Pull-Up to V_{DDIO}. ODO16/GPI16: Configurable General-Purpose Input and/or Open-Drain Output with Selectable Internal Pull-Up.
MISCELLANEOUS - SEE Table 3				
12	X1/OSC	X1/OSC	N/A	X1/OSC: Crystal/Oscillator Input. Connect either to one terminal of a ±200ppm 25MHz crystal or a 25MHz external clock source. If crystal is used, connect a load capacitor from X1/OSC to ground (load capacitor value depends on crystal used). N/A: Crystal not required in GMSL1 mode.

PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
13	X2	X2	N/A	X2: Crystal Input. Connect to one terminal of a 25MHz ±200ppm crystal. If crystal is used, connect a load capacitor from X2 to ground (load capacitor value depends on crystal used). If external oscillator is connected to X1/OSC, leave X2 floating. N/A: Crystal not required in GMSL1 mode.
1	PWDNB	PWDNB	PWDNB	Active-Low Power-Down. Apply logic-low to place device in power-down mode. Connect to V_{DDIO}/logic-high for normal operation.
15	XRES	XRES	XRES	Connect 402Ω 1% resistor between XRES and ground.
14	VREF	VREF	VREF	Optional External 1.2V Reference-Voltage Input for ADC. Leave open if external reference voltage is not used.
POWER SUPPLIES - SEE Table 3				
16	VDD18	VDD18	VDD18	1.8V Analog Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
19	CAP_VDD	CAP_VDD	CAP_VDD	Decoupling capacitor for 1V core supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
24	VDDIO	VDDIO	VDDIO	1.8V to 3.3V I/O power supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
20	VDD	VDD	VDD	1.0V Core Supply. This pin includes an optional on-chip LDO. Connect a 0.95V to 1.05V supply to bypass LDO. Connect a 1.14V to 1.26V supply to use the internal 1.0V regulator. In order to use the internal 1V regulator, first write REG_ENABLE = 1, and then write REG_MNL = 1. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
EP	EP	EP	EP	Exposed Pad. EP is internally connected to device ground. EP must be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Block Diagram



Recommended Operating Conditions, External Component Requirements, and ESD Protection

Table 2. Recommended Operating Conditions

PARAMETER	PIN	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
Supply Range	V_{DD18}		1.7	1.8	1.9	V
	V_{DD}	1.0V	0.95	1.0	1.05	
		1.2V	1.14	1.2	1.26	
	V_{DDIO}		1.7		3.6	
Maximum Supply Noise (supply noise frequency < 1MHz)	V_{DD18}			25		mVp-p
	V_{DD}	1.0V		25		
		1.2V		50		
	V_{DDIO}	1.8V		50		
		3.3V		100		
Operating Junction Temperature (T_J)			-40		125	°C

Table 3 details critical components that must be connected to the specified pins for correct functionality. Figure 21 and Figure 22 illustrate the use of R_{XRES}, R_{PD}, R_{EXT}, and C_{LINK} in typical applications.

Table 3. External Component Requirements

COMPONENT	SYMBOL	CONDITION		VALUE	UNIT
XRES	R_{XRES}	Connect R_{XRES} resistor between XRES pin and ground.		402 ±1%. Use a single resistor.	Ω
Line-Fault Pull-Down Resistor	R_{PD}	Connect to ground at far end of coax/STP cable; only required if remote line-fault detection is used.		49.9 ±1%	kΩ
Line-Fault Resistor	R_{EXT}	Connect to LMN input of serializer at near end of coax/STP cable; only required if local line-fault detection is used.	LMN0 STP mode	42.2 ±1%	kΩ
			LMN0 coax mode	48.7 ±1%	
			LMN1 STP/coax mode	48.7 ±1%	
Link-Isolation Capacitors	C_{LINK}	Place in series and in close proximity to the SIO pins (pins 17 and 18)	GMSL2 mode, GMSL1 mode with HIM enabled	0.1	µF
			GMSL1 mode, HIM disabled	0.22	
Crystal		Place as close as possible to pins X1/OSC (pin 12) and X2 (pin 13) and connect between these two pins. GMSL2 mode only; not required for GMSL1 mode operation.		25MHz ±200ppm	
Crystal Load Capacitors		Use crystal-loading capacitor guidance from the crystal manufacturer. Select values which compensate for the X1 and X2 input and PCB node capacitances. Place the capacitors as close as possible to pins X1/OSC (pin 12) and X2 (pin 13).			
V_{DDIO} Decoupling Capacitors		Place 0.01µF capacitor as close as possible to pin V_{DDIO} (pin 24). Include a minimum of 10µF bulk decoupling on the PCB.		0.01µF + 10µF	
V_{DD18} Decoupling Capacitors		Place 0.01µF capacitor as close as possible to pin V_{DD18} (pin 16). Include a minimum of 10µF bulk decoupling on the PCB.		0.01µF + 10µF	

Table 3. External Component Requirements (continued)

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
V_{DD} Decoupling Capacitors		Place a 0.1µF capacitor as close as possible to pin V_{DD} (pin 20). Include a minimum of 10µF bulk decoupling on the PCB. See configuration information in the *Power Supplies* section.	0.1µF + 10µF	
CAP_VDD Decoupling Capacitors		Place a 0.1µF capacitor as close as possible to pin CAP_VDD (pin 19). Include a minimum of 10µF bulk decoupling on the PCB.	0.1µF + 10µF	
Open-Drain Pull-Up Resistors		Application-specific. Quantity and values depend on multifunction GPIO pin configurations. I^2C/UART MFP functions require appropriate external pull-up resistors in all cases. A 1MΩ pull-down resistor is recommended on MFP6 if the ERRB function is enabled.		
Resistors for Configuration Pin Resistor-Divider	R1, R2	Place resistor-divider close to pin 6 (MFP4/CFG0). Resistor value depends on desired configuration.	Use ±1% Tolerance Resistors. See Table 9.	Ω
	R1, R2	Place resistor-divider close to pin 7 (MFP5/CFG1). Resistor value depends on desired configuration.	Use ±1% Tolerance Resistors. See Table 10.	Ω

Table 4. ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SIO__	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, CS = 100pF		±8		kV
		ISO10605, R_D = 330Ω, CS = 150pF, Contact Discharge, Coax Configuration		±6		
		ISO10605, R_D = 330Ω, CS = 150pF, Contact Discharge, STP Configuration		±4		
		ISO10605, R_D = 330Ω, CS = 150pF, Air Discharge		±8		
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V
All Other Pins	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±4		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

Functional Diagrams

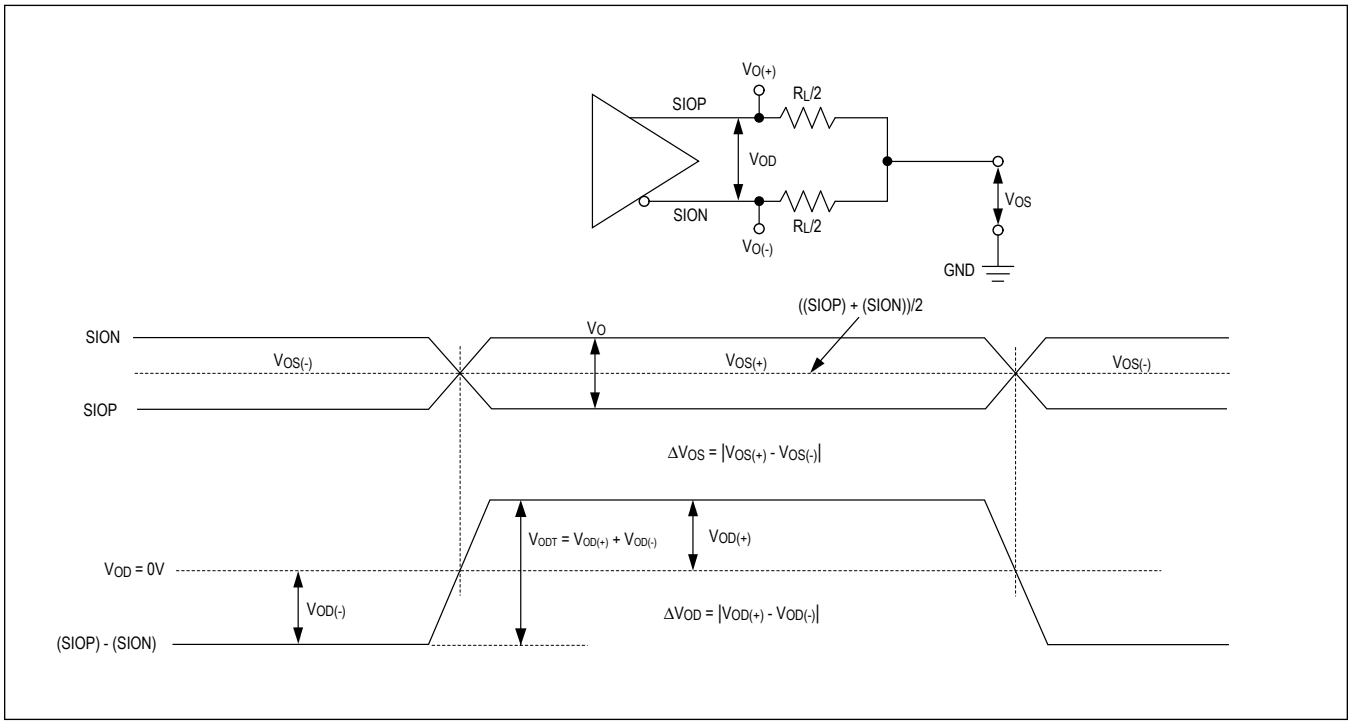


Figure 1. Serial Output Parameters

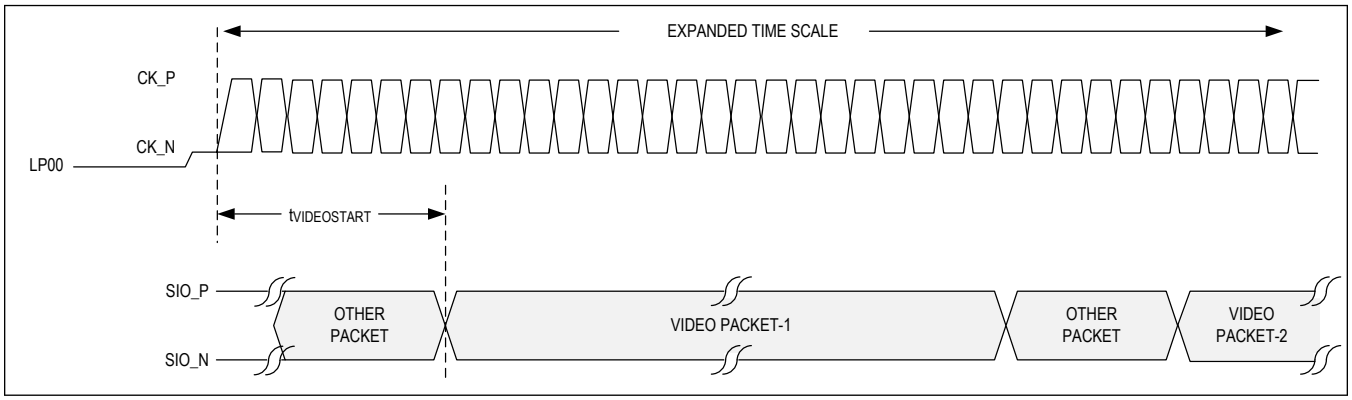


Figure 2. GMSL2 Video Initialization Time

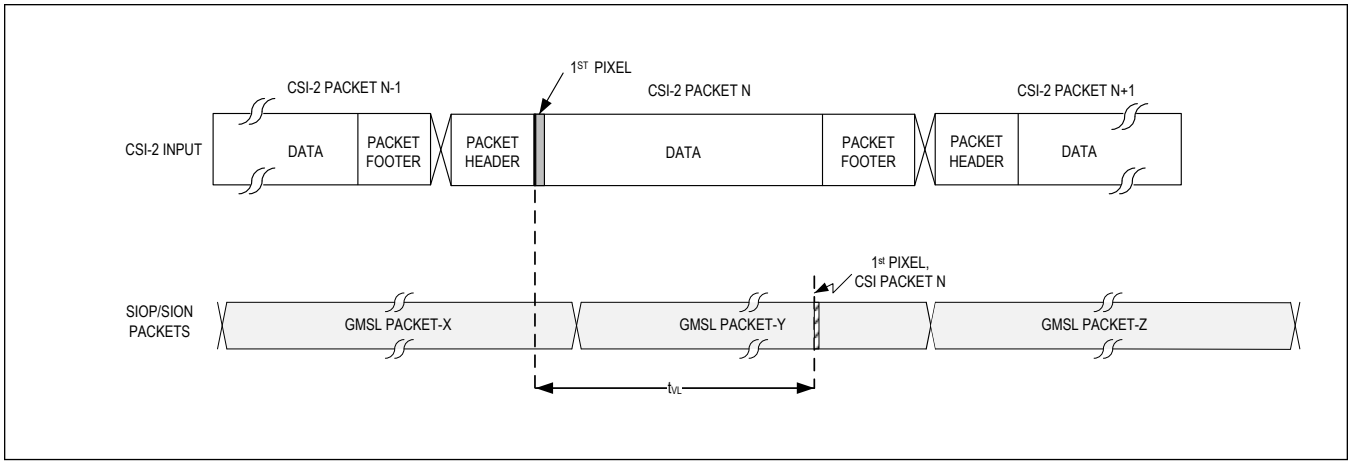


Figure 3. GMSL2 Video Latency

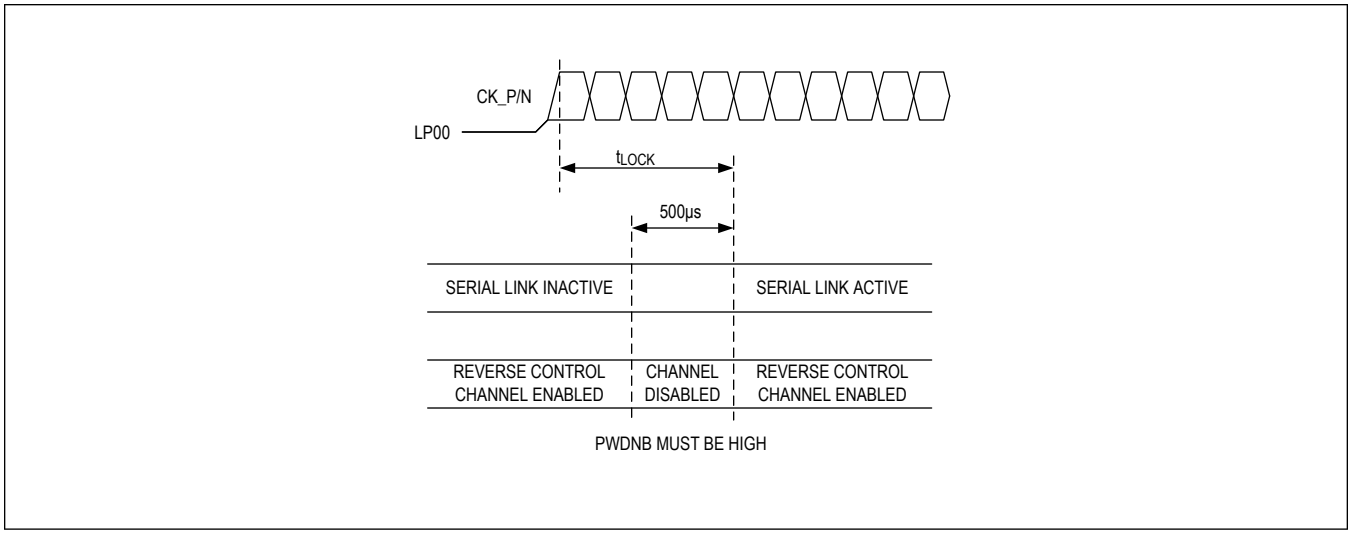


Figure 4. GMSL1 Link Startup Time

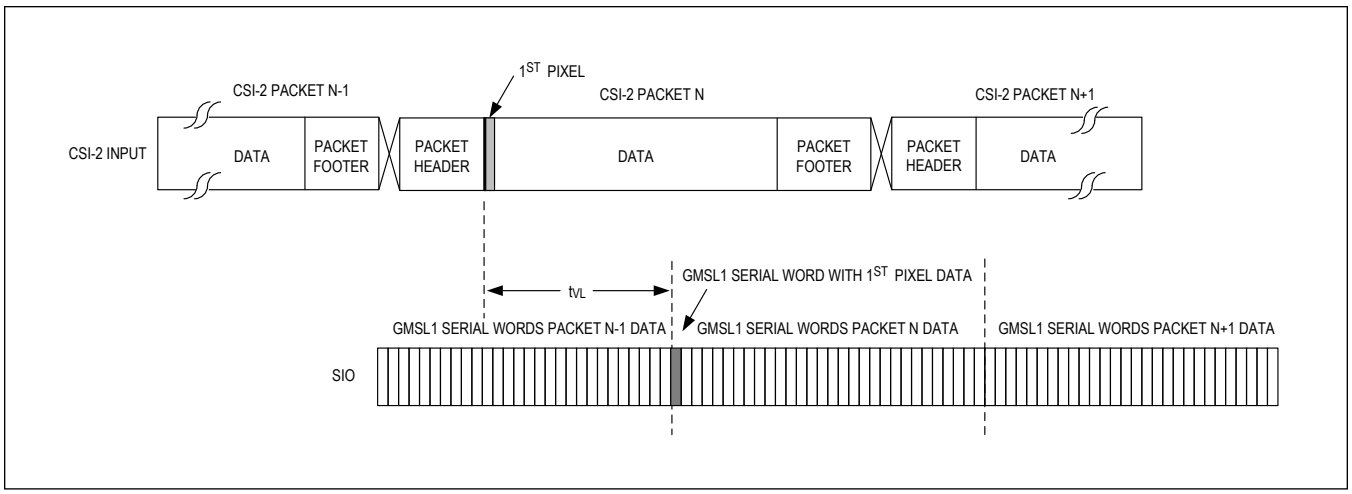


Figure 5. GMSL1 Video Latency

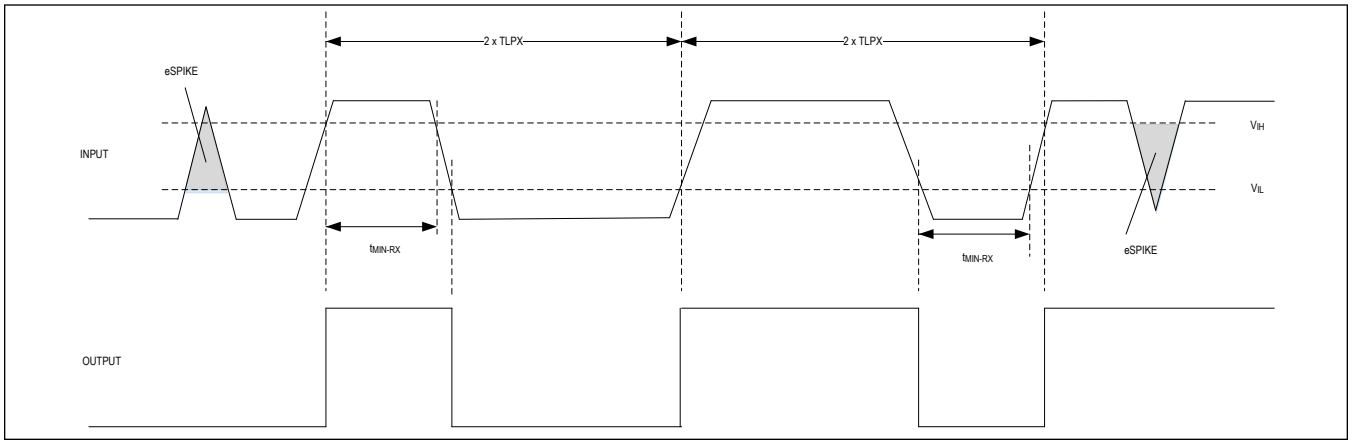


Figure 6. D-PHY LP Receiver Pulse

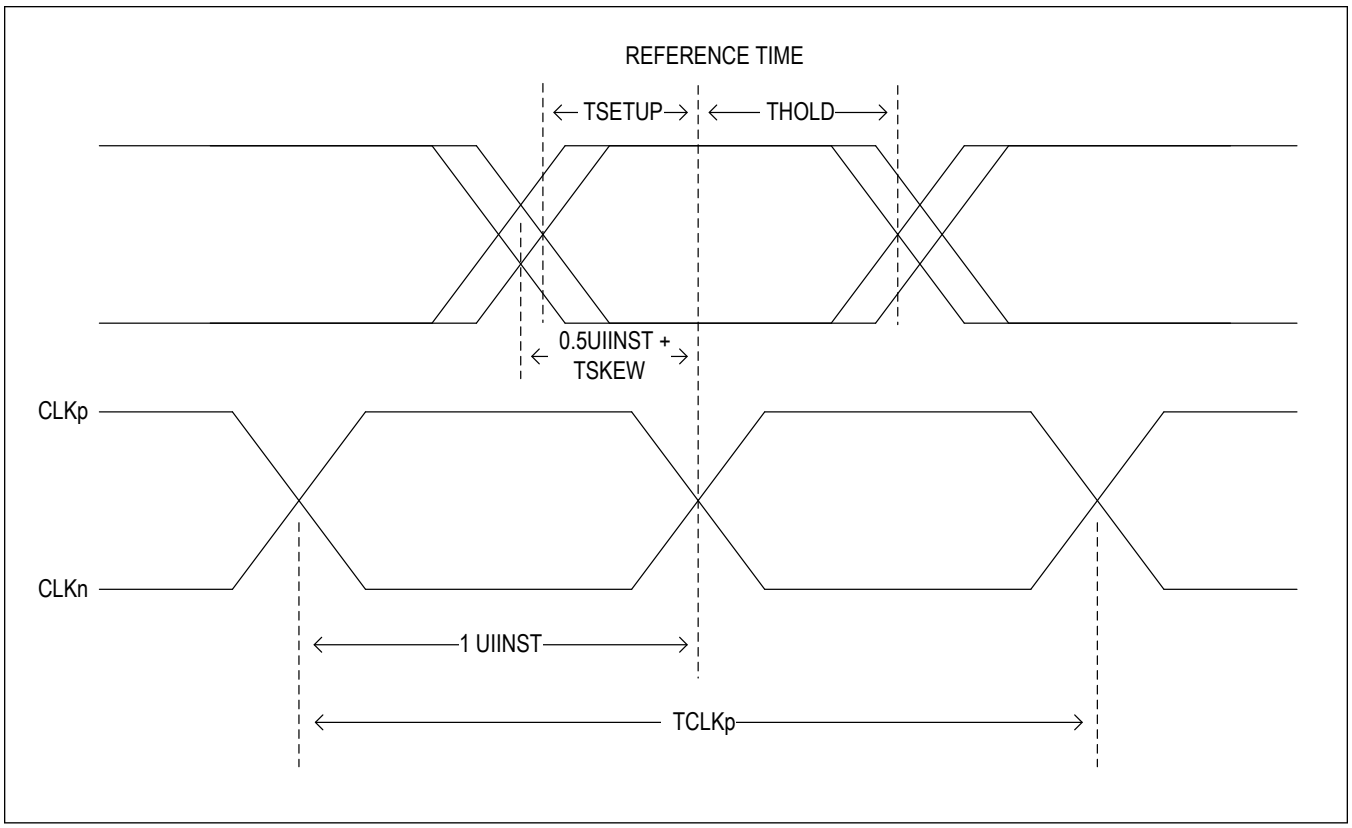


Figure 7. D-PHY Data Clock Timing

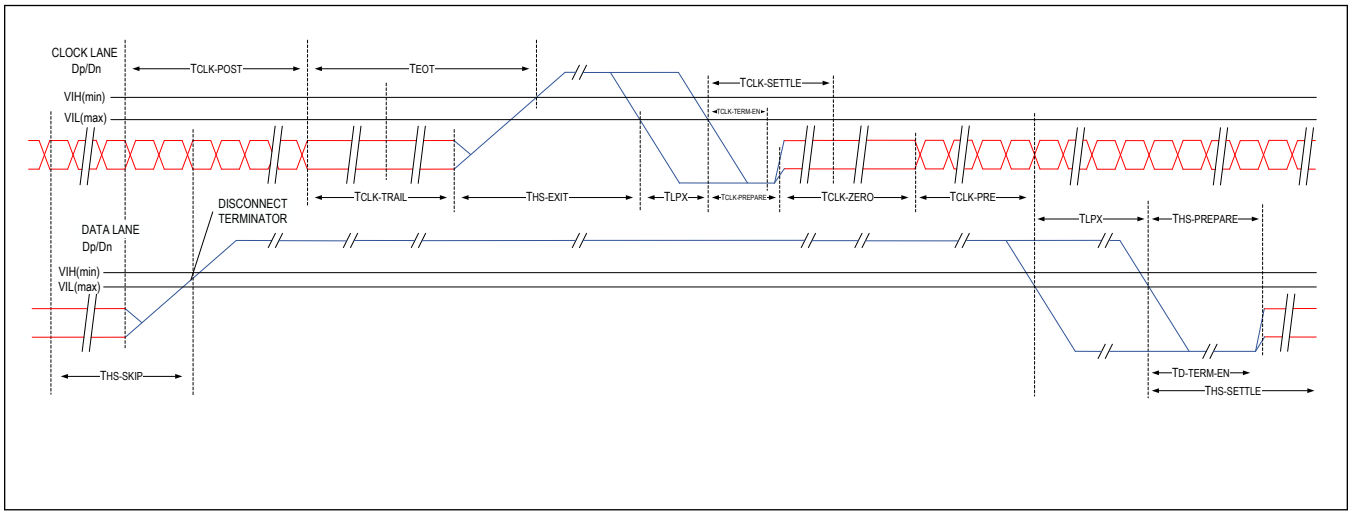


Figure 8. D-PHY Switching Clock Lane From Active Transmission to Low-Power Mode

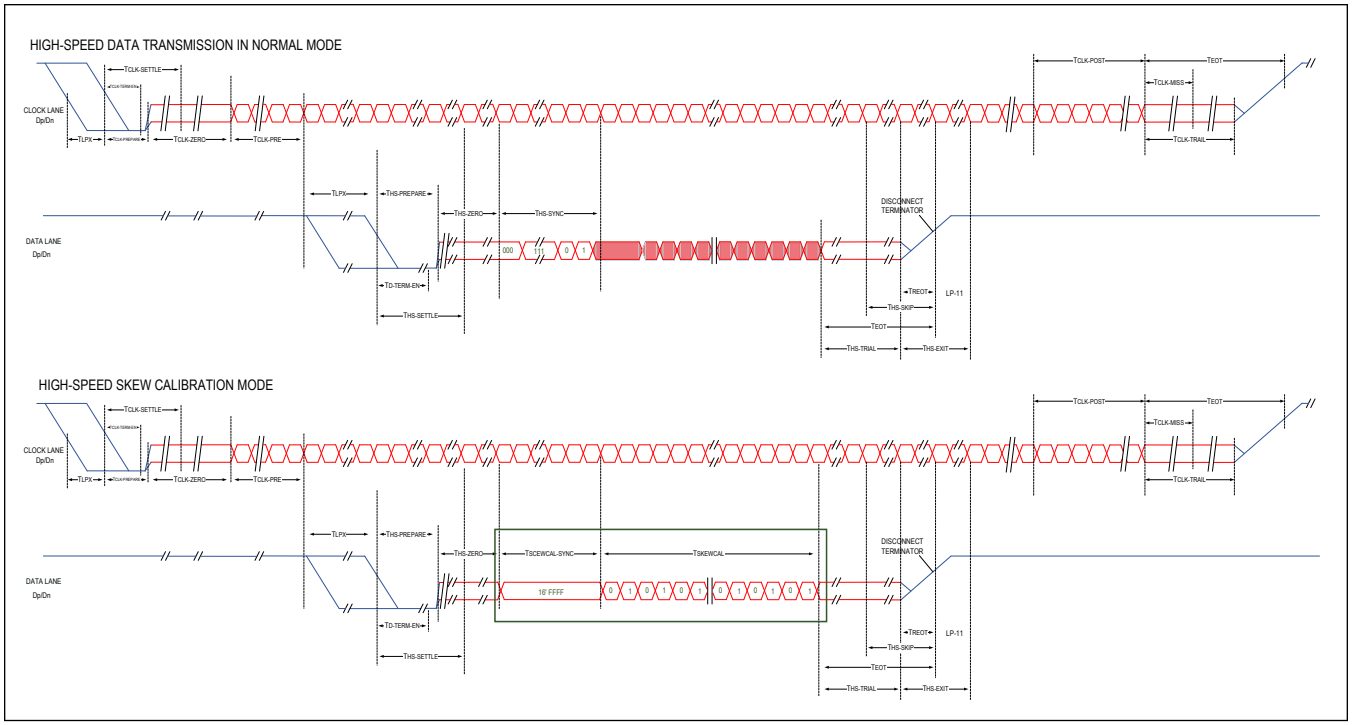


Figure 9. D-PHY Normal Transmission Mode vs Skew Calibration

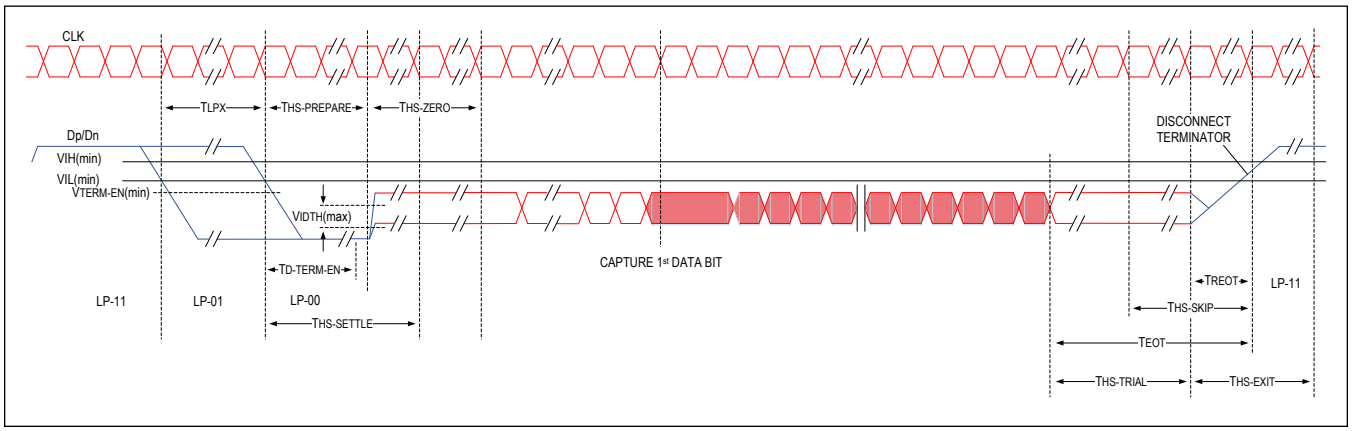


Figure 10. D-PHY HS Burst Data Transmission

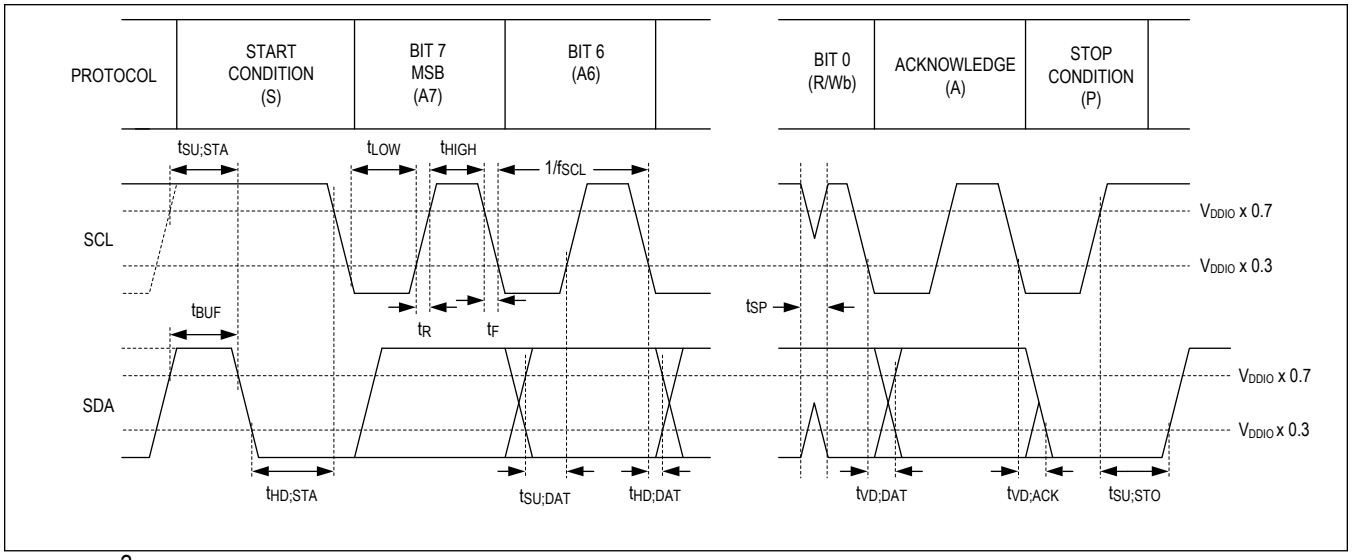


Figure 11. I²C Timing Parameters

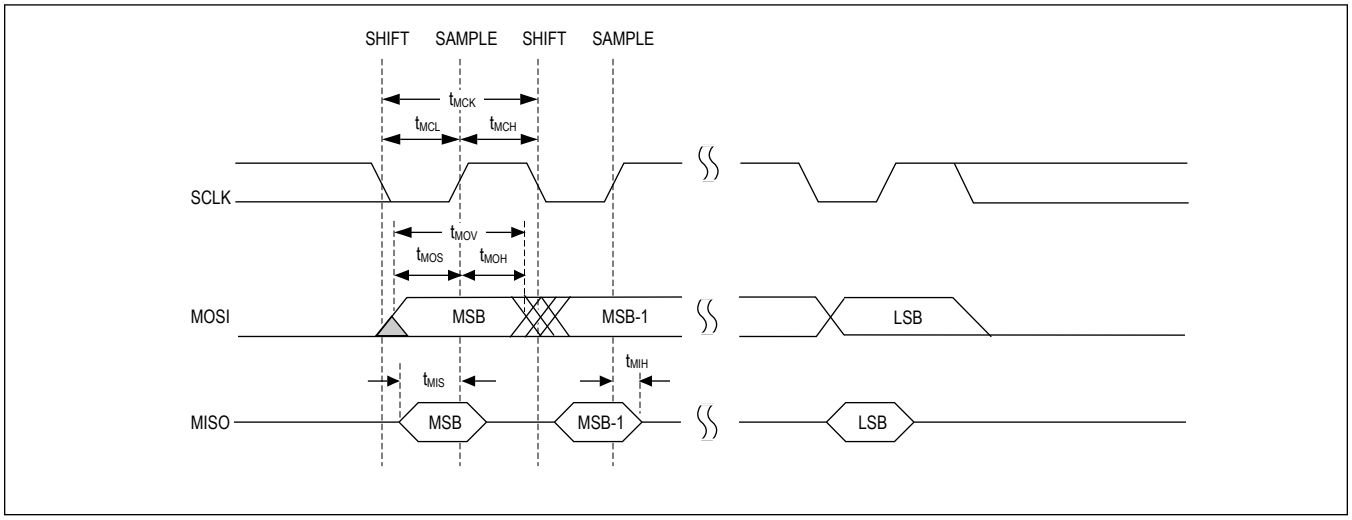


Figure 12. SPI Main Mode Timing Parameters

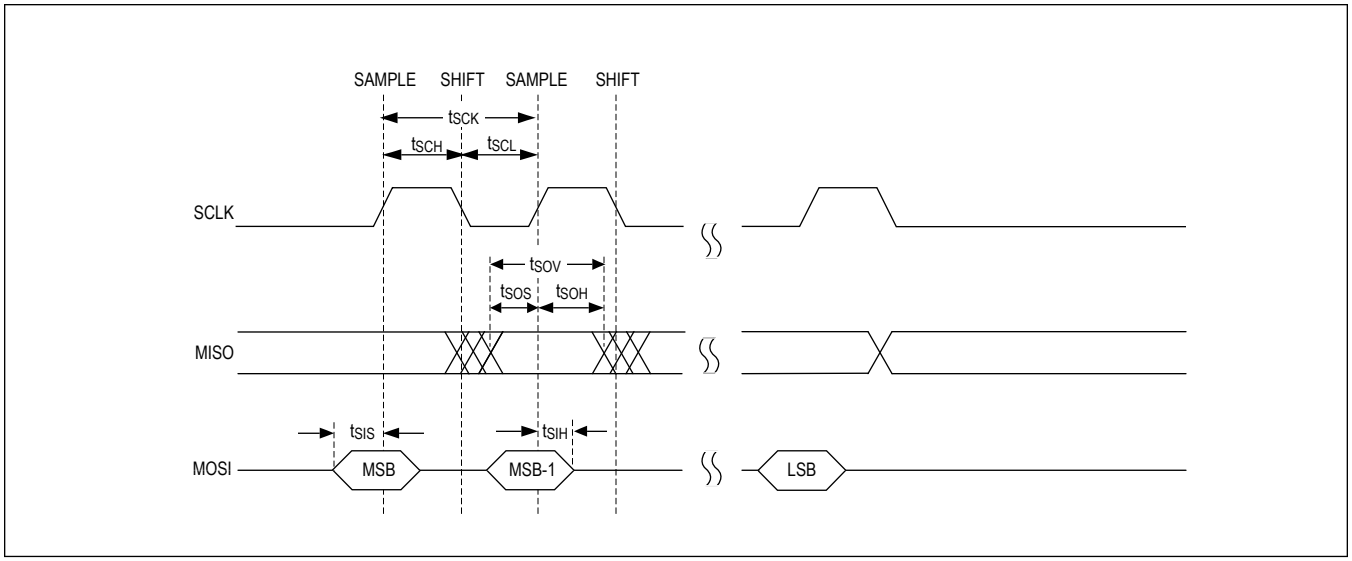


Figure 13. SPI Subordinate Mode Timing Parameters

Detailed Description

Additional Documentation

In addition to the provided information, designers must also use the following information to correctly design systems using the MAX9295D.

- GMSL2 Channel Specification User Guide
- GMSL2 Hardware Design Guide
- GMSL2 General User Guide
- MAX9295D User Guide
- Errata for MAX9295D

The Channel Specification contains physical layer requirements for the PCB traces, cables, and connectors that constitute the GMSL link. The Hardware Design Guide contains recommendations for PCB design, applications circuits, selection of external components, and guidelines for use of GMSL signal integrity tools. The User Guide contains detailed programming guidelines for GMSL device features. Errata sheets contain deviations from published device specifications and are specific to part number and revision ID. Contact the factory for these documents.

Introduction

Analog Devices' GMSL2 serializers and deserializers provide sophisticated link management for transporting high-speed, low bit-error-rate, serial data. GMSL2 serializers and deserializers support a comprehensive suite of display, camera, and communication interfaces over a single wire. GMSL2 provides up to 6Gbps forward and 187.5Mbps reverse packetized data transmission over each fixed-speed link. GMSL1 operation is also supported for pairing with GMSL1 deserializers at 1.5Gbps or 3.12Gbps or up to 4.5Gbps with GMSL2 deserializers operating in GMSL1 mode.

The following sections provide a brief overview of the device functions and features. Contact factory for additional information and details on configuration of each function and feature.

Product Overview

The MAX9295D serializer converts dual MIPI CSI-2 ports to single-link GMSL2 or GMSL1. It also sends and receives side-channel data, enabling full-duplex transmission of forward-path video at 3/6Gbps and bidirectional control data over low-cost 50Ω coax or 100Ω STP cables that meet the GMSL2 channel specification. In backward-compatible GMSL1 mode, the MAX9295D can be paired with 3.12Gbps or 1.5Gbps GMSL1 deserializers, or operate up to 4.5Gbps with GMSL2 deserializers in GMSL1 mode.

The MAX9295D has dual 4-lane CSI-2 v1.3 input ports which support data rates of 80Mbps to 2.5Gbps per lane. The number of active D-PHY v1.2 data lanes in each CSI-2 port is programmable with support for 1-, 2-, or 4-lane configurations. The device supports up to 4 virtual channels and accommodates multiple data types, including RAW8/10/12/14/16/20, RGB565/666/888/YUV422 8/10-bit, user defined, and generic long packet.

The MAX9295D is intended to be paired with GMSL2 deserializers or legacy GMSL1 deserializers. When used with a GMSL2 deserializer, several common multisensor use cases are supported. One scenario features a pair of co-located independent sensors that are routed to independent camera inputs of the SoC. Use of separate CSI-2 inputs on the SoC may be beneficial if the SoC inputs have bandwidth limitations. In this case, the MAX9295D provides two fully independent 1-, 2-, or 4-lane CSI-2 inputs, while the deserializer interface is similar to the SoC, with two independent 1-, 2-, 3-, or 4-lane CSI-2 outputs. The total combined video throughput shared by the two sensors is 6Gbps, and the two sensors can have different video data rates/formats (GMSL2 mode only). This application is detailed in Figure 14.

Some GMSL2 deserializers also support data aggregation as detailed in Figure 15. This enables simultaneous input of multiple sensor data streams using a single CSI-2 port on the SoC, which may result in more efficient utilization of the SoC's input resources. As above, the sensors can have different video timing and resolution. The SoC identifies the video source by reading each packet's virtual channel ID. If both sources initially use the same virtual channel, the MAX9295D can assign a different virtual channel (a total of 4 virtual channels, shared by the two CSI ports, are available). Reassignment of up to 16 data types is also possible.

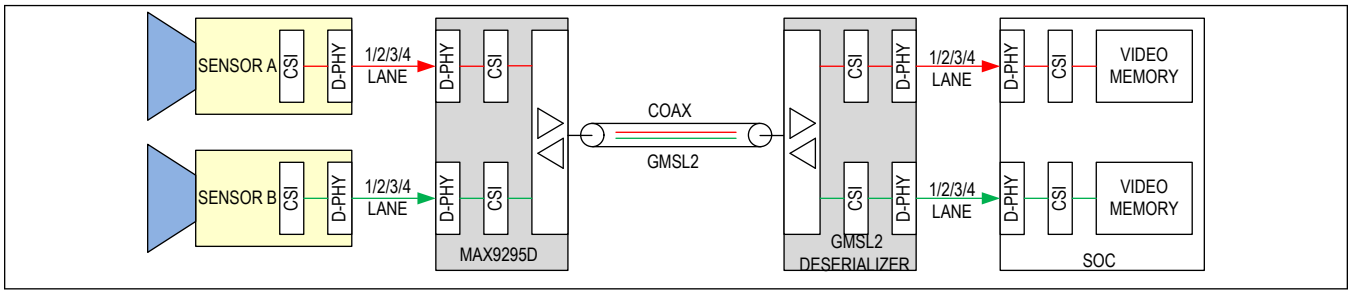


Figure 14. Dual Sensors, Dual Port

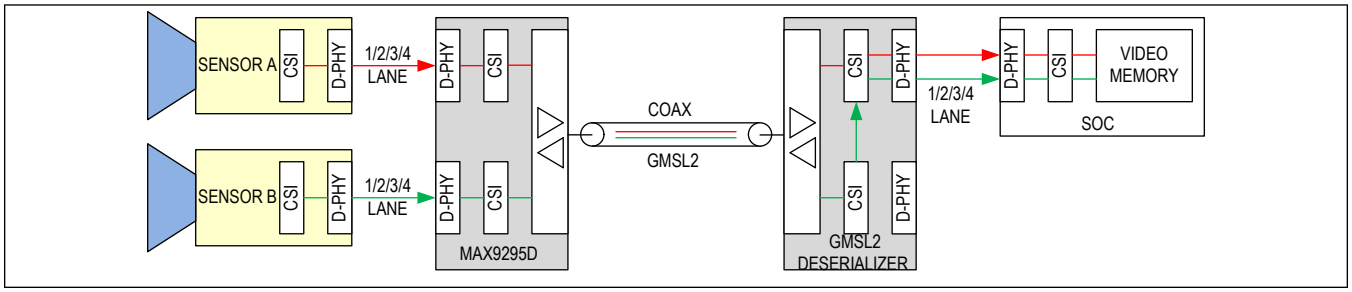


Figure 15. Dual Sensors, Single Port

GMSL2 Overview

GMSL2 is a fixed-rate transmission medium that is designed to carry multiple types of communication channels concurrently. The link bit rate is based on a constant-frequency link clock generated from the 25MHz crystal oscillator or external reference frequency. The link clock is independent of the video pixel clock, aside from the natural constraint that the video bandwidth cannot exceed the available link bandwidth.

GMSL2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels. Bandwidth allocation is dynamic. An inactive channel consumes no link bandwidth, which allows other active channels to share the full link bandwidth. Maximum packet size is limited, preventing a single channel from consuming link bandwidth for an extended time. In most cases, available link bandwidth exceeds the bandwidth requirement. Idle packets are used to fill the unused link bandwidth. The same data protocol is used on forward and reverse channels, and for both video and control-channel data.

GMSL2 provides a flexible broadband data link that can transport high bandwidth bidirectional data between remotely located devices. The MAX9295D is specifically designed to be an interface between remotely located high resolution cameras or similar sensors and a centrally located processor. In addition to the core video/broadband streaming portion of the link, GMSL2 devices provide a variety of peripheral/auxiliary functions to enable flexible, robust system implementations.

A comprehensive suite of common embedded communication protocols are supported. All devices utilize a primary I^2C/UART control-channel interface that an ECU uses to access serializer and deserializer registers, as well as peripheral devices, from either end of the link. Each device also has two pass-through I^2C/UART channels available for peripheral control.

An SPI main/subordinate interface, including two subordinate-select pins, is included in the GMSL2 family. The SPI interface enables a host SPI main on one side of the GMSL2 link to control a peripheral SPI subordinate on the opposite side. The host can be located at either end of the link or can swap ends by reprogramming the GMSL2 devices (a GMSL2 device can be configured as a SPI main or subordinate).

GMSL2 devices include a flexible suite of GPIO pins. These pins are shared with the aforementioned peripheral communication protocols. In general, the GPIOs can be used as user-defined inputs or outputs whose state can be either automatically forwarded across the link or specified by register writing. GPIOs are typically used to tunnel low speed (< 100Kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward or reverse direction.

Useful auxiliary features include a video crossbar switch and watermark generation/detection. The crossbar can be used to arbitrarily reorder the color and sync signals. The watermark generation and detection is used for verifying that the video image is not frozen.

GMSL2 devices incorporate numerous link-margin optimization and monitoring functions to ensure high link margin and robust functionality. Continuous (1Hz) adaptive equalization optimizes link margin to adapt to environmental changes and cable aging. An eye-opening monitor function for continuous link-margin diagnosis with various threshold alarm levels is available for run-time alerts of link degradation. PRBS checking verifies correct link and video channel operation.

Video Pipeline

The video channel is designed for transmitting video data received from the CSI-2 interface to the deserializer side of the link. Several data types are supported, including RAW8/10/12/14/16/20, RGB565/666/888, and YUV8/10-bit. Video input data consists of color, HS, and VS synchronous to the PCLK. Video flows through the design as described in the following sections.

Video Pipes, Aggregation and Replication

In GMSL2 mode, the transmission of video data is based on the concept of video pipes. Carrying data in pipes allows GMSL2 to bridge different digital video interfaces and perform watermark generation and detection. A pipe carries a video stream (or streams) and video-synchronization data. Each pipe can carry multiple concurrent video streams, with different virtual channels and data types for each stream, in one of the following modes:

- Mode 1: Streams with constant bits per pixel (bpp) of up to 24bpp. The bpp of the streams must be the same.
- Mode 2: Streams with 16, 14, 12, 10, or 8bpp. Streams less than 16bpp are padded with zeros.
- Mode 3: Streams with two different bpp. The bpp of one stream must be twice the bpp of the other stream. The higher bpp stream maximum is 24bpp.

Modes 1 and 3 carry data at full bandwidth but put more restrictions on bpp than Mode 2. Mode 2 allows streams with different bpp, but streams of less than 16bpp are carried using more bandwidth than necessary on the GMSL2 link because of zero padding. Mode 1 or Mode 3 are sufficient for most applications. Mode 2 requires less programming and is more convenient if the application does not require maximum link bandwidth. The MAX9295D has dual input ports and four total video pipes shared by the two inputs as shown in Figure 16. In typical camera applications, one pipe can carry a YUV422 video stream from the source device. Cameras that output RAW or multiple-exposure HDR data often require more than one pipe as shown in Figure 17, where transmission of RAW16/8-bit embedded data and RAW12 requires utilization of two pipes. In the examples shown in the figures, each camera is routed to a separate pipe or pair of pipes. Depending on the formatting of the video data, it may also be possible to route both cameras on a common pipe or pair of pipes by appropriately using virtual channels. This depends on whether the previously described constraints for the pipe's operating mode are met by the cameras' outputs.

The following section describes the flow of data through the GMSL2 deserializer side of the GMSL link. Note that this

portion of the data path is not included in the MAX9295D serializer, and it is described here to aid in the understanding of the typical operation of a GMSL link.

Each of the four pipes in the MAX9295D has a dedicated MIPI receiver buffer. Each retiming buffer has the capacity to buffer 96 24-bit pixels. This provides sufficient memory for transmission of a line to start without overflow or underflow. The number of pipes used by a deserializer is equal to the number of pipes used by all connected serializers. For example, a link consisting of a GMSL2 deserializer connected to a MAX9295D serializer can utilize four data pipes. This would enable flexible formatting of the output of two independent sensors, as shown in Figure 17. After data exits the retiming buffer, it goes through a crosspoint switch and a data type (DT) and virtual channel (VC) reassignment stage. If the video source has a CSI-2 output, packet DT and VC can be left as-is or reassigned by register programming as desired. Up to four DT/VC incoming pairs can be mapped to four DT/VC outgoing pairs.

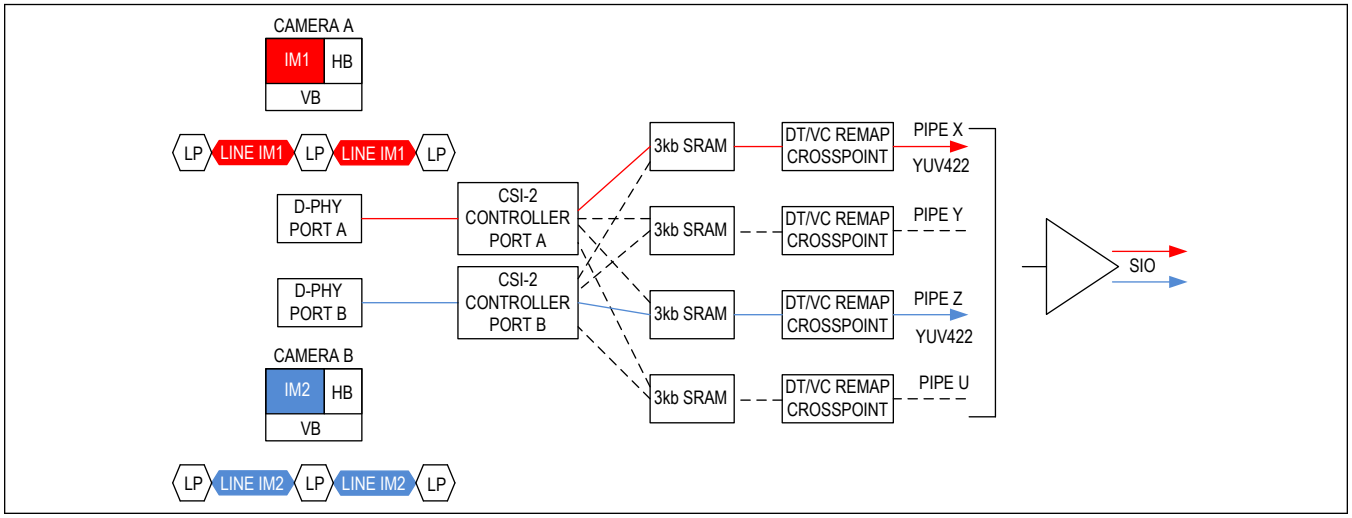


Figure 16. Serializer Video Pipes for Dual Port YUV422

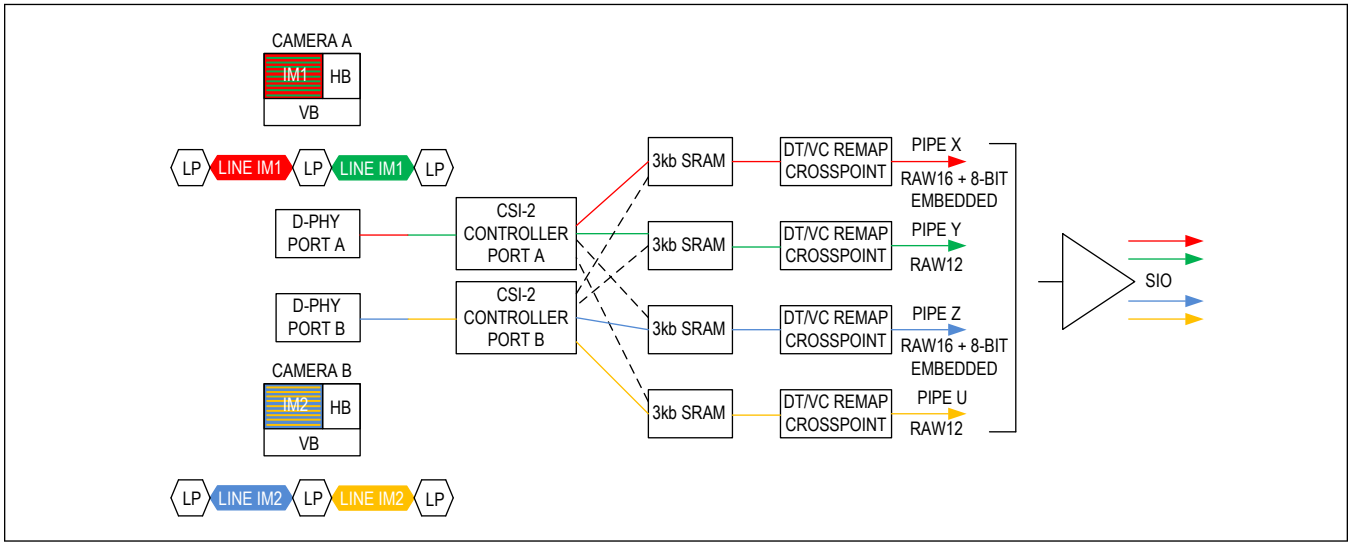


Figure 17. Serializer Video Pipes for Dual Port RAW16 with 8-Bit Embedded Data and RAW12

In GMSL1 mode, only a single video pipe is available. This requires a single data type for all incoming data. In dual CSI-2 port applications, both input ports are required to use identical video formatting in GMSL1 mode.

After transmission over the GMSL link, data is received by the deserializer. The virtual channel ID of CSI streams can

be remapped if desired, and ultimately data from each pipe is stored in the line buffer. A complete line of video data is buffered before the data is available for read-out by the aggregators, which can be used to combine data from multiple video pipes and/or virtual channels within a single CSI-2 stream. Each buffer connects to two aggregators, but only one aggregator (as programmed by the user) can read data out of a given buffer. Once data is read, it cannot be read a second time by the other aggregator. Up to four pipes can be aggregated by one aggregator as shown in Figure 18. Aggregated data is read out from line memory on a first-come, first-served basis. When a complete line of video data has filled line memory, it is routed as specified by the aggregator. The order in which the line memories reach filled status is the order in which they are read out. Video data can be routed to the desired aggregator or CSI controller according to DT or VC based on the source CSI-2 packet's DT/VC, or by a DT/VC assigned or reassigned by the deserializer.

For example, data in Pipe X with VC0 can be programmed to be read-out by Aggregator A while data in Pipe X with VC1 can be programmed to be read-out by Aggregator B. This maximizes data-routing flexibility and enables multiple streams within a single pipe to be routed to separate CSI output ports. The aggregator forwards the line of video from the line buffer and video synchronization data to its associated CSI-2 controller for packet generation. Packets can be driven to the controller's default output port or replicated and routed to the other CSI-2 port. For example, CSI-2 controller A can output packets on D-PHY Port A and/or D-PHY Port B as shown in Figure 19.

A D-PHY port can only accept packets from one controller. It cannot aggregate packets from the two controllers. All aggregation must be realized in the prior aggregation blocks. To prevent buffer overflow, the CSI-2 port data rate must be programmed to a value that is greater than or equal to the incoming data rate. Programming the output rate to be faster than the bandwidth of the incoming video increases packet spacing (LP time between packets).

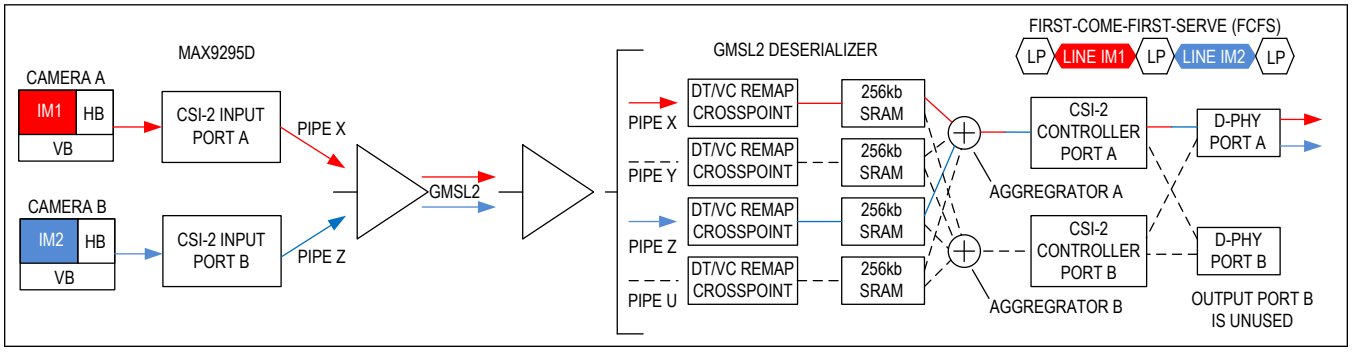


Figure 18. Deserializer Aggregation

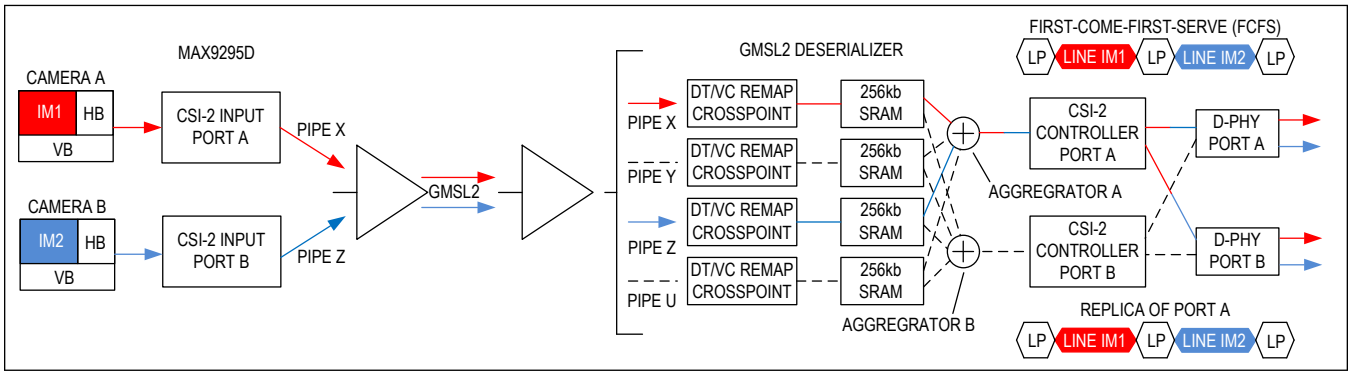


Figure 19. Deserializer Aggregation and Replication

Tx Crossbar

The incoming video stream or VPG output passes through a crossbar switch that enables arbitrary remapping of all bits in the video stream. A single bit can be remapped to multiple locations in the serial stream if desired. The default routing of the crossbar is such that no remapping occurs (crossbar function is completely transparent by default).

Watermarking

The watermarking block allows users to detect a frozen-frame failure in a frame-based processing system between the generator and detector. This feature is designed to detect frozen frames caused by errors in safety-critical applications. It does not detect frozen frames that occur before the watermark generator or after the watermark detector. GMSL2 parts contain both a watermark generator and watermark detector. This allows both serializers and deserializers to insert a watermark or detect a watermark in a safety-relevant video stream. The watermark generator inserts a time-varying watermark that is highly redundant and robust to image processing and display-stream compression. The watermark detector looks for this time-varying watermark, and failure to detect all of the generated watermarks indicates a frozen-frame failure between the generator and detector in a frame-based processing system. In this error condition, the watermark detector can generate an interrupt and/or blank the output video, returning the display to a safe state in less than 500ms.

Video-Line CRC

A CRC32 polynomial is used to generate an optional 32-bit code at the end of each HS pulse in the serializer. This code is transferred to the deserializer side of the link. The CRC checker in the deserializer generates the same code and checks if the generated and received CRC codes are the same. If not, it asserts an error.

Control Channel and Side Channels

A µC or other controller can send and receive control and side-channel data over the GMSL2 serial link simultaneously with high-speed video data. MAX9295D supports the following interfaces:

- Primary I^2C/UART (internal access)
- Dual Pass-Through I^2C/UART
- SPI
- GPIO

Data from all interfaces tunnels through the GMSL2 link, but it is only through the primary I^2C/UART interface that the GMSL2 device registers can be accessed and configured only through the primary I^2C/UART interface.

The side channel, with its various interfaces, is accessed using multifunction GPIO pins (MFP pins). Multifunction pins have a default function and can be programmed to a variety of alternate functions after power-up. Due to a practical limit on the number of pins available on a given device, not all interfaces can be simultaneously supported. See Table 12 and the *Pin Descriptions* section for default and alternate multifunction pin functions, as well as available combinations of interfaces.

Primary I^2C/UART

The primary I^2C/UART is located on the SDA_RX and SCL_TX pins of each GMSL2 device. The I^2C (SDA, SCL) or UART (TX, RX) interface is selected by the CFG0 pin state at power-up (see the *CFG Latch at Power-Up Pins* section). The selected interface provides access to all GMSL2 serializer and deserializer registers, as well as peripheral device registers, to an external main on either side of the link. This the only interface that can be used by an external main to access internal registers within the GMSL2 devices.

The main µC can be located on either end of the link (usually the serializer side for display applications and the deserializer side for camera applications). Dual mains are supported provided software arbitration (such as token passing) is used to prevent packet collisions. The control channel allows only one main µC to communicate at a time.

To configure peripheral devices over the link, the GMSL2 serializer and deserializer must use the same control-channel interface (both I^2C or both UART). Unlike GMSL1 devices, there is no I^2C-to-UART conversion capability. I^2C/UART outputs are open drain and require appropriately sized external pull-up resistors for proper operation.

For details regarding using the I^2C/UART, see the *Control Channel Programming* section.

Pass-Through I^2C/UART

GMSL2 devices have 2 pass-through I^2C/UART ports. These ports do not have access to internal registers in either the GMSL2 serializer or the deserializer; they simply tunnel the I^2C or UART data across the GMSL2 link to the corresponding I/O pin on the opposite side of the link. This can be useful for separating I^2C channels so that multimain or replicated address conflicts do not occur. Pass-through I^2C/UART outputs are open drain and require appropriately sized external pull-up resistors for proper operation.

In the case of the MAX9295D, pass-through Port 2 shares the same pair of I/O pins that is used by the primary I2C/UART. This prevents simultaneous peripheral communication using all three I2C/UART interfaces on the serializer side of the link. Simultaneous peripheral communication is limited to pass-through Port 1, in conjunction with either pass-through Port 2 or the primary I2C/UART. All three ports are still available on the deserializer side of the link, assuming that the MAX9295D is programmed to enable pass-through Port 1 and Port 2 and disable the local control channel (DIS_LOCAL_CC = 1), with the limitation that the primary I2C/UART is only available for internal register programming. In this case, pass-through Port 1 and Port 2 are routed to MFP I/Os for peripheral communication while the primary port is available only for internal register programming that is driven by a main on the deserializer side of the link.

SPI

GMSL2 enables a host SPI main on one side of the GMSL2 link to control a peripheral SPI subordinate on the opposite side. Communication can be in either direction across the GMSL2 link.

The SPI clock range is 600kHz to 50MHz. Take care to meet setup and hold time requirements when using at speeds higher than 20MHz.

Control-Channel Latency

All control channels exhibit finite latency. Typical latency for each function is given in Table 5. For I2C, which requires an immediate acknowledgement from the receiver following each byte, clock stretching is used to temporarily pause communication as the acknowledge propagates through the control channel. All I2C devices that communicate over the link must support clock stretching.

Table 5. Control-Channel Latency

FUNCTION	FORWARD	REVERSE	NOTES
I2C	<10µs	<10µs	
UART	<10µs	<10µs	
SPI	<10µs	<10µs	Round Trip

General-Purpose Inputs and Outputs (GPIO)

GPIOs are typically used to tunnel low-speed (< 100Kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward (serializer to deserializer) or reverse (deserializer to serializer) direction. GPIO transmissions are transition based. A GPIO packet is created and transmitted on the GMSL2 link when a rising- or falling-edge transition is detected at a GPI pin. The transition is regenerated at the corresponding GPO on the other end of the link.

Multifunction pins can be programmed as GPI (input), GPO (push-pull output or open-drain output—some MFPs only support open-drain output), or GPIO (bidirectional input/output). The MFPs that are shared with the CFG power-up function can only be used as GPO outputs following power-up. They do not have any GPI functionality. Most GPIOs can also be programmed for 1MΩ or 40kΩ pull-up or pull-down (or none). Although an internal pull-up is provided, high-speed open-drain outputs require an appropriate-value external pull-up resistor to V_{DDIO}. Inputs cannot be left floating. Always ensure that every pin configured as an input has a pull-up or pull-down programmed or is driven by another IC or external pull-up/pull-down.

A GPI on one side of the serial link can be mapped to a single GPO or multiple GPOs on the other side of the link. Each GPI is assigned a pin ID with the destination GPO(s) on the other side of the link set to the same pin ID. By default, the ID mapping is GPIO0-GPIO0, GPIO1-GPIO1, GPIO2-GPIO2, etc. However, the GPIO mapping can be arbitrarily changed through register settings.

GPI transitions can be transmitted in two modes: delay-compensated and non-delay-compensated. When delay compensation is enabled, the GPI-to-GPO delay across the link is a precise, fixed value. Latency increases but jitter and skew decrease.

The state of each GPIO can be read or written by register, either locally or remotely over the GMSL2 link by a µC using the control-channel I2C/UART interface.

In non-delay-compensated mode, channel latency is not fixed. The GPI transition is sent as soon as possible based on priority and available link bandwidth. This variable delay is a result of multiple communication channels sharing the link. Non-delay-compensated mode should be used with signals tolerant to delay variation (i.e., µC interrupts).

Priority can be set for GPI pins via register control. If no priority is set, GPI transitions are transmitted in the order they occur. However, when priority is set, transitions on GPI with higher priority are transmitted earlier. Typical GMSL2-only device delays for 6Gbps forward and 187Mbps reverse link rates are shown in Table 6.

Table 6. Typical GPIO Delays for Forward and Reverse Link Transmission

	DELAY COMPENSATION	DELAY
GPIO forwarding from serializer to deserializer (6Gbps forward channel)	0	720ns
	1	3.5µs
GPIO forwarding from deserializer to serializer (187Mbps reverse channel)	0	6µs
	1	15µs

GMSL2 Physical Layer

Analog Devices' GMSL2 family of serial links have transmitter and receiver capability enabled simultaneously, enabling full-duplex operation on a single wire. A single cable between the serializer and deserializer delivers data being transmitted from each end of the link. Forward transmission is data being sent from the serializer to the deserializer. Reverse transmission is data being sent from the deserializer to the serializer.

Forward-rate options are fixed at 3Gbps or 6Gbps, with defaults of 6Gbps in coax mode and 3Gbps in STP mode. Reverse data rate is fixed at 187.5Mbps.

Cabling Options

GMSL1/2 supports operation with either 50Ω coaxial or 100Ω shielded twisted pair (STP) cabling. Cables must have sufficient return and insertion loss characteristics for best full-duplex link performance. The available link rates and GMSL dynamic link optimization enable support of a wide range of cabling options. Contact the factory for insertion and return loss guidelines.

Coax or STP operation is determined by the level of CFG1 at power-up. See Table 9 and Table 10.

In coax mode, use only the noninverted SIO pin. In STP configurations, both the noninverted and inverted SIO pins are enabled by default. Any unused SIO pins should be AC terminated with 50Ω to ground.

Following the GMSL2 design guidelines allows use of common automotive industry cables with lengths in excess of 15m for coax and 7.5m for STP. Longer cable lengths may potentially be used with careful system design and appropriate cable and connector specification. The cable lengths specified assume two inline connectors in addition to the endpoint connectors, 25mm of PCB trace at each end, proper layout techniques, and high cable quality. Contact the factory for additional details regarding the GMSL2 channel specification.

A 100nF AC coupling capacitor is normally used for GMSL2 links. A 220nF AC coupling capacitor is normally used for non-HIM GMSL1 links. The coupling capacitor can be reduced to 100nF in GMSL1 links with HIM.

GMSL2 Bandwidth Sharing

The GMSL forward bandwidth is shared between video, the I^2C/UART control channel, pass-through I^2C/UARTs, SPI, and GPIOs, plus various protocol-specific data exchanges (i.e. info frames, sync, and acknowledgements). The reverse-channel bandwidth is also shared with all of the above, with the exception of video packets.

The total link bandwidth used by all communication channels cannot exceed the fixed available link bandwidth.

Link bandwidth is shared flexibly among the various communication channels requesting the link for packet transmissions. This flexibility comes from packet-based transmission format and dynamic bandwidth allocation: if a certain channel is not active, it does not consume any link bandwidth, leaving the full link bandwidth available for all active communication channels to share. The packet-based protocol fulfills this sharing requirement. The maximum packet size is limited to prevent a single channel from monopolizing the link bandwidth and to ensure other channels are served.

The video and control-channel packets can be assigned a priority level. There are four priority levels: low, normal, high, and urgent. The scheduler transmits the packet with the highest priority among the pending requests. Packets with stringent latency requirements can be assigned an increased priority.

GMSL2 Bandwidth Calculations

The GMSL2 forward link has a fixed link rate of 3Gbps or 6Gbps. The reverse link rate is fixed at 187.5Mbps. The GMSL2 protocol overhead is roughly 14%. This leaves approximately 2.6Gbps or 5.2Gbps of data throughput in the forward direction and 162Mbps in the reverse direction.

Worst-case applications must not exceed the available throughput of the forward and reverse links. Maxim's evaluation kit (EV kit) GUI includes a bandwidth (BW) calculator that estimates initial bandwidth requirements. Maxim also offers other tools that are useful for calculating link bandwidth utilization. For high-bandwidth use cases, consult the factory to ensure error-free performance.

Table 7 provides rough estimates of the bandwidth utilization for each of the communication channels. Note that the video channel is available only in the forward link direction, and therefore bandwidth cannot be allocated to video in the reverse link. Bandwidth can be allocated to all other functions in both the forward and reverse directions.

Table 7. Forward and Reverse Link Bandwidth Utilization

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Video	H x V x fps x bpp x(1 + % blanking/100) x 1.14 (forward direction only)
I^2C	18 to 60 x I^2C clock rate, depending on available link bandwidth
UART	6 x UART bit rate, 5.5 x when parity bit enabled
SPI	2.5 x SPI rate
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation enabled

Definitions:

H = Horizontal resolution

V = Vertical resolution

fps = Frames per second

bpp = Bits per pixel

Eye-Opening Monitor (EOM)

The eye-opening monitor (EOM) enables GMSL2 parts to monitor the link margin on an active link and generate an interrupt if it falls below an acceptable level. For example, if a cable is damaged, the link can run error-free but have less link-margin than desired. This allows the user to proactively react to deteriorating cable performance before any link errors occur. GMSL2 parts can measure the horizontal or vertical eye opening of the equalizer's output. The measurement is activated automatically at a rate of approximately 1Hz once a link is active. The EOM block compares the data sampled at the center of the eye with a sample offset in phase for the horizontal EOM or offset in voltage for the vertical EOM. The eye opening is then reported, and the EOM can trigger an interrupt or a reset if the opening falls below user-defined thresholds.

Video PRBS

The video channel has a PRBS generator in the serializer and a PRBS checker in the deserializer for testing the video channel operation. The video PRBS generator can operate from the recovered PCLK received from one of the video input ports.

Note that all link bandwidth is not used by the video channel alone in GMSL2 mode, so it is possible to have a bit error on the link which does not cause a video PRBS error.

RGB888 Video Pattern Generator

The RGB888 video-pattern generator (VPG) is another auxiliary block that can be used for various diagnostic and test purposes. If desired, video from the peripheral source can be replaced by the video pattern generated by the VPG. The VPG can generate various patterns and is configured by appropriate register writes. The VPG only generates RGB888 data. To use the VPG function, the user must apply a clock using one of the CSI-2 input ports.

Adaptive Equalization (AEQ)

GMSL2 devices automatically adapt receiver characteristics to compensate for the insertion and return loss characteristics of the channel, which consists of the cables, connectors, and PCBs. This approach optimizes performance on any channel that meets the GMSL2 channel specification. The equalizer architecture makes GMSL2 links robust against noise, crosstalk, and reflections. Initial adaptation is performed during link lock. After the link is established, the AEQ continues running in the background, updating settings at a rate of approximately 1Hz to track temperature and voltage variations. The adaptation process optimizes the equalizer coefficients to maximize the eye opening by using the built-in eye-opening monitor.

GMSL1 Backwards Compatibility

The MAX9295D is designed to pair with any GMSL1 deserializer. However, all features of a given GMSL1 deserializer may not be supported. GMSL1 backwards compatibility is only supported with forward link rates from 500Mbps to 4.5Gbps and a reverse link rate of 1Mbps. The full 4.5Gbps GMSL1 forward link bandwidth is available only when the MAX9295D is paired with select GMSL2 deserializers that include GMSL1 support. In this case, both devices must be configured to use GMSL1 compatibility mode. When the MAX9295D is paired with a legacy GMSL1-only deserializer, the MAX9295D must be configured for GMSL1 compatibility mode, and the available forward link rate is reduced such that it is within the limitations of the specified GMSL1 deserializer.

Table 8 specifies the availability of common GMSL1/GMSL2 features in GMSL2 devices that are operated in GMSL1 mode. Note that some GMSL2 features, such as SPI, are only available in GMSL2 mode, and as a result they are never available in GMSL1 mode regardless of the devices used. If a feature is not supported by both devices in a link, then it should be disabled. To utilize a feature, it must be enabled and configured consistently such that appropriate settings are applied to both ends of the link.

Most features specified in Table 8 can be enabled/disabled by appropriate register configuration and/or configuration input pin power-up state. Hardware design of both serializer and deserializer subsystems should account for correct connection of configuration pins to achieve the desired settings. Interfacing coax interconnects to non-coax-capable GMSL1 devices requires special hardware considerations to ensure reliable functionality. Please contact the factory for additional information regarding general GMSL1 operation or GMSL1/GMSL2 device interoperability.

Table 8. Feature Availability in GMSL1 Mode

FEATURE NAME	GMSL2 SERIALIZER IN GMSL1 MODE	GMSL2 DESERIALIZER IN GMSL1 MODE
Coax	Yes	Yes
Bus Width Select (BWS)	Yes	Yes
High-Bandwidth Mode (HIBW)	Yes	Yes
Data Rate Select (DRS) (Low speed mode)	Yes	Yes
DBL (Double Mode)	Yes	Yes
HSYNC/VSYNC Encoding	Yes	Yes
Pixel CRC (6 bits per pixel)	Yes	Yes
Video Line CRC (32 bits per line)	Yes	Yes
Hamming Error Correction	No	No
I^2C to I^2C	Yes	Yes
UART to UART	Yes	Yes
UART to I^2C	No	No
Pass-Through I^2C Channels	No	No
I^2C Address Translation	Yes	Yes
SPI Control Channel	No	No
High-Immunity Mode	Yes	Yes
REV_FAST with HIBW Mode	Yes	Yes
Packet Control Channel with CRC	Yes	Yes

Table 8. Feature Availability in GMSL1 Mode (continued)

Packet CC Retransmission	Yes	Yes
Configuration Link	Yes	Yes
GPI to GPO on reverse channel	Yes	Yes
Frame Sync	Yes	Yes
Delay Compensated GPI/GPO	No	No
Line Fault	Yes	Yes
UART Base mode	Yes	Yes
UART Bypass mode	Yes	Yes
Spread Spectrum	Yes	Yes
Serializer Pre/Deemphasis	No	No
Deserializer Legacy Programmable Equalization	No	No
Deserializer Adaptive Equalization	Yes	Yes
Twisted Pair Splitter Mode	No	N/A
Watermark	Yes	Yes
Video Timing Generator	Yes	No
Video Crossbar	Yes	Yes
PRBS	Yes	Yes
CNTL0,1,2,3 on forward channel	Yes	Yes
A/V Status Register Interrupt	No	No
HS/VS/DE Inversion	Yes	Yes
WS/SCK Inversion	Yes	N/A
Jitter-Filtering PLL	No	No
Sleep Mode	Yes	Yes

Dual CSI Video Input Ports

The MAX9295D's dual CSI-2 input ports each utilize D-PHY v1.2. Each D-PHY block is fully compliant with D-PHY v1.2 requirements and includes four data lanes and one clock lane. Each D-PHY lane supports HS data rates from 80Mbps to 2.5Gbps and lane configurations of 1, 2, or 4 lanes. Lanes can be arbitrarily assigned and lane polarity can be inverted to ease signal routing.

The two CSI ports are totally independent, and the user can separately configure each port and specify whether one or two ports are active. In dual-CSI input port use cases, ports can be processed completely independently of each other, enabling unrelated sensors with unsynchronized data streams and different data types to be processed in parallel (GMSL2 mode only).

Low-power data transmission mode (LPDT) functionality is not supported, and the CSI-2 inputs operate only in continuous clock mode. Any data source that drives the CSI-2 inputs must be compatible with these constraints.

The CSI controllers have various error-detection and reporting mechanisms that utilize the CRC and ECC functions. Errors are reported in the interrupt registers.

MIPI Receive Clock Spread Tracking

The MAX9295D can operate with a spread MIPI clock signal (CKAP/N, CKBP/N). Do not exceed 0.5% spread for f_{PCLK} > 50MHz and 1% spread for f_{PCLK} < 50MHz. Maintain spread modulation frequency less than 40kHz in all cases. In addition, turn off spread spectrum in the serializer and deserializer when the CSI source has spreading enabled. Otherwise, the serializer and deserializer track the spread on the received MIPI clock.

CFG Latch at Power-Up Pins

Voltage levels at the CFG0 and CFG1 pins are latched at power-up, or upon a low-to-high transition of PWDNB. These levels set initial register values and functional modes that may not be easily programmed through I^2C or UART after the IC powers up. The CFG pins select device address, I^2C or UART primary control channel, GMSL2 serial rate, and Coax or STP cable (see Table 9 and Table 10).

The voltage level for each pin is set by an external precision resistor divider connected between V_{DDIO} and ground, or for some configurations, by a single resistor connected to V_{DDIO} or ground. Table 9 and Table 10 show the recommended resistor values to select each configuration. The voltage level at the CFG pins is typically latched 1ms after all power supplies reach minimum levels required by the Power-on-Reset (PoR) circuit. CFG pins must not be loaded with more than 10pF at power-up to ensure the proper voltage level.

If the requirements described in the Table 9 and Table 10 notes are met, the CFG pin's secondary functions can be used after the CFG pin voltage levels are latched at power-up (see the *Pin Descriptions* section and Table 12 for secondary functions). CFG pins cannot be used as general-purpose inputs.

Table 9. CFG0 Input Map

CFG0 INPUT VOLTAGE (PERCENTAGE OF V_{DDIO}) (NOTES A, B)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (NOTE C)		MAPPED CONFIGURATION (NOTE D)	
MIN (%)	TYP (%)	MAX (%)	R1 (Ω)	R2 (Ω)	I2CSEL	DEVICE ADDRESS
0.0	0.0	11.7	OPEN	10,000	I^2C	0x80
16.9	20.2	23.6	80,600	20,500		0x84
28.8	32.1	35.5	68,100	32,400		0xC0
40.7	44.0	47.4	56,200	44,200		0xC4
52.6	56.0	59.3	44,200	56,200	UART	0xC4
64.5	67.9	71.2	32,400	68,100		0xC0
76.4	79.8	83.1	20,500	80,600		0x84
88.3	100	100	10,000	OPEN		0x80

Table 10. CFG1 Input Map

CFG1 INPUT VOLTAGE (PERCENTAGE OF V_{DDIO}) (NOTES A, B)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (NOTE C)		MAPPED CONFIGURATION (NOTES D, E)		
MIN (%)	TYP (%)	MAX (%)	R1 (Ω)	R2 (Ω)	CXTP	GMSL1/GMSL2	HIM/GMSL2 RATE
0.0	0.0	11.7	OPEN	10,000	COAX	GMSL2	6Gbps
16.9	20.2	23.6	80,600	20,500		GMSL1	HIM Enabled
28.8	32.1	35.5	68,100	32,400			HIM Enabled
40.7	44.0	47.4	56,200	44,200	STP	GMSL2	6Gbps
52.6	56.0	59.3	44,200	56,200			3Gbps
64.5	67.9	71.2	32,400	68,100		GMSL1	HIM Enabled
76.4	79.8	83.1	20,500	80,600			HIM Enabled
88.3	100	100	10,000	OPEN	COAX	GMSL2	3Gbps

Notes:

A. Voltage-divider resistor tolerance, V_{DDIO} supply ripple, and external loading must not cause the CFG0 or CFG1 input voltage to exceed the maximum or minimum limits.

B. Until the input voltage is latched, any load on CFG0 or CFG1 (other than R1 and R2) must be ≥ 25 x (R1 + R2). Load capacitance (including R1 and R2) must be lumped-load ≤ 10pF.

C. Each resistor in the voltage-divider must be ≤ 100kΩ.

D. I2CSEL: I2C or UART interface for SDA_RX and SCL_TX

DEVICE ADDRESS: device address.

CXTP: shielded twisted-pair (SIO_P, SIO_N) or coax (SIO_P) serial link.GMSL1/GMSL2: GMSL1 or GMSL2 operating mode.

HIM applies when GMSL1 operating mode is selected. High-immunity mode for reverse control channel.

E. GMSL2 Rate applies when GMSL2 operating mode is selected. 3Gbps or 6Gbps serial-link bit rate. Control-channel rate is 187.5Mbps for both cases.GMSL1 default BWS = 0 (24-bit).

Speed Programming for SPI

The SPI interface may be used over a wide range of frequencies. The MAX9295D provides flexible GPIO speed programming to maintain timing margins while minimizing radiated EMI.

Table 11 provides guidance on recommended speed settings for various SPI operating frequencies and V_{DDIO} supply voltages. See Table 13 for generic GPIO pin speed-programming information.

At lower frequencies, SPI data is typically latched on the opposite clock edge from which it is shifted as shown in Figure 12 and Figure 13. At higher frequencies, however, the data must be latched on the same edge as the shift to meet setup and hold-time requirements. Table 11 provides guidance for programming the latching clock edge.

Table 11. Recommended SPI Pin Programming

FREQUENCY (MHZ)	V_{DDIO} (V)	LATCHING EDGE	RECOMMENDED TTS
< 12.5	1.7 to 2.24	Opposite from shift	01
	2.25 to 3.6		10
12.5 to 25	1.7 to 2.24	Opposite from shift	00
	2.25 to 3.6		01
25 to 50	1.7 to 2.24	Same as shift	00
	2.25 to 3.6		01

Multifunction Pin Assignments

The MAX9295D provides a wide range of peripheral I/O functions. These functions are mapped through register control to an array of multifunction pins (MFP). Each MFP has several possible functions, but only one can be used at a time.

In most cases, multifunction pins can be used as a generic I/O pins, although there are some limitations with a limited number of pins supporting only CMOS GPO functionality or open-drain output functions. The various peripheral interfaces and other special functions are distributed among different pins, enabling the user to select a variety of interfaces and special functions simultaneously.

Some functions require only a single MFP, but many are implemented across a group of MFPs. For example, ERRB is a single MFP while SPI requires several pins. A user selects MFP functions to suit their use-case by programming the appropriate registers.

The *Pin Descriptions* table shows default and alternate functions for each MFP, listed in order of priority (highest priority listed first). Table 12 also shows priority, with highest priority on the left. A higher priority function must be disabled when a lower-priority function is enabled, both by register writes.

Each MFP is placed in one of four speed groups, with each speed group having a default output transition-time setting (TTS). Pins are grouped such that the most frequently used functions that consist of multiple pins are grouped together. The transition-time default suits the MFP's most common application requirements. Except for I2C/UART and GPI/ODO functions, whose transition times are fixed and specified as I2C speed group, the transition time of each speed group can be changed from the default value by register programming. When the speed group's transition time is changed, the transition time of all MFPs in the speed group are changed. The drive strength of individual MFPs cannot generally be specified (aside from MFP3, which is uniquely associated with speed group REFCLK). The main-channel and pass-through I2C/UART channel's transition times are not affected by the adjustable speed group transition-time settings.

Transition times depend on the transition-time setting and V_{DDIO} supply voltage. See Table 13 for typical transition times

for each TTS setting. To change drive strength of a group of pins, simply find the desired I/O function in Table 12 and check the speed group with which it is associated. This is specified in the Speed Group column. The relevant register field for each speed group is called xx_SPEED, where xx is A, REFCLK, or D, depending on the speed group. The register field can be programmed with one of the four possible TTS settings given in Table 13 to specify the transition time of a given group of pins. MFPs associated with speed group I^2C have fixed output drive strength, and as a result no register adjustment of TTS is available for these pins.

Table 12. MFP Pin Function Map

PIN	LATCH ON POWER-UP	GMSL1 CNTL	I^2C/UART PRIMARY	SPI	I^2C/UART PASS-THROUGH	OTHER FUNCTIONS	GPIO	SPEED GROUP (DEFAULT TTS)
MFP0		CNTL1		SCLK			GPIO0	A (10)
MFP1		CNTL2		MOSI			GPIO1	A (10)
MFP2				MISO		GPO ALT	GPIO2	A (10)
MFP3		CNTL3				RCLKOUT DPLL_OUT	GPIO3	REFCLK (10)
MFP4	CFG0			BNE/ SSI			GPO4	D (11)
MFP5	CFG1						GPO5	D (11)
MFP6		CNTL0				ERRB	GPO6	D (11)
MFP7						ADC0	GPIO07	D (10)
MFP8						ADC1	GPIO08	D (11)
MFP9						LOCK ADC2 GPO	GPIO09	D (11)
MFP10		CNTL4		RO/ SS2		MS	GPIO10	D (11)
MFP11					SDA1/RX1		ODO11/ GPIO11	I^2C
MFP12					SCL1/TX1		ODO12/ GPIO12	I^2C
MFP13						LMN0	ODO13/ GPIO13	I^2C
MFP14						LMN1	ODO14/ GPIO14	I^2C
MFP15			SDA/RX		SDA1/RX2		ODO15/ GPIO15	I^2C
MFP16			SCL/TX		SCL2/TX2		ODO16/ GPIO16	I^2C

Table 13. Control- and Side-Channel Typical Rise and Fall Times

TRANSITION TIME SETTING (TTS)	RISE TIME (ns) (20% to 80%), C_L = 10pF		FALL TIME (ns) (80% to 20%), C_L = 10pF	
	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V
00	1.0	0.6	0.8	0.5
01	2.1	1.1	2.0	1.1
10	4.0	2.3	4.3	2.9
11	8.8	5.0	10.1	5.1
I^2C	N/A	N/A	40	30

Power-Up and Link Start-Up

GMSL2 ICs are in power-down mode when PWDNB pin is low or when any of the power supplies are disabled. When in power-down mode, device configuration is reset to the default power-up state.

The serializer and deserializer may power up in any order. After PWDNB is released and all power supplies have settled, each device begins its power-up sequence and performs the following operations:

1. CFG pin states are set and internal registers are set accordingly. See Table 9 and Table 10.
2. Main control channel (I^2C or UART) is functional on local side. Device registers are writable and readable.
3. The link is established based on the following:
   a. Single link auto selection mode (AUTO_LINK = 1 and LINK_CFG = 1 or 2): Automatically select which PHY to use to establish a GMSL2 link by periodically trying to handshake using PHY A and PHY B.
   b. Single link manual selection mode (AUTO_LINK = 0 and LINK_CFG = 1 or 2): If LINK_CFG = 1, establish a link using PHY A. If LINK_CFG = 2, establish a link using PHY B.
   c. Dual-link mode (LINK_CFG = 0): Establish a link using both PHYs.
   d. Splitter (serializer)/aggregator (deserializer) mode (LINK_CFG = 3): Establish a link using both PHYs (for specific applications only)
4. Each enabled PHY performs link calibration, equalizer adaptation, and data channel locking. Both devices set their LOCK pins high.
5. The control channel is available from/to the remote side. If using the internal V_{DD} regulator (V_{DD} = 1.2V), enable the regulator function as described in the *Power Supplies* section.

The entire link-initialization process, from the time that the last device's PWDNB input transitions from low to high, takes approximately 20ms nominally and 100ms maximum for any channels that meet the GMSL2 channel specification.

After the link is established, all devices can be configured. This can be done locally or remotely over the control channel by a microcontroller on either side of the link.

Device Reset

The following general reset options are available through register writes:

1. RESET_ALL resets all blocks, including all registers and digital and analog blocks. This is similar to driving the PWDNB pin low and then high.
2. Setting RESET_LINK resets all GMSL PHY related logic as well as the data pipeline. After this bit is set, all control registers are still accessible through the local control channel. The link remains in RESET until RESET_LINK is cleared.
3. RESET_ONESHOT resets all GMSL PHY-related logic and the data pipeline and then automatically clears itself. This is similar to setting and clearing RESET_LINK.

Program registers that affect GMSL2 link operation (i.e., TX_RATE, RX_RATE, CXTP, AUTO_LINK, LINK_CFG, GMSL2) first, followed by RESET_LINK or RESET_ONESHOT.

Link and Video Lock

Link Lock

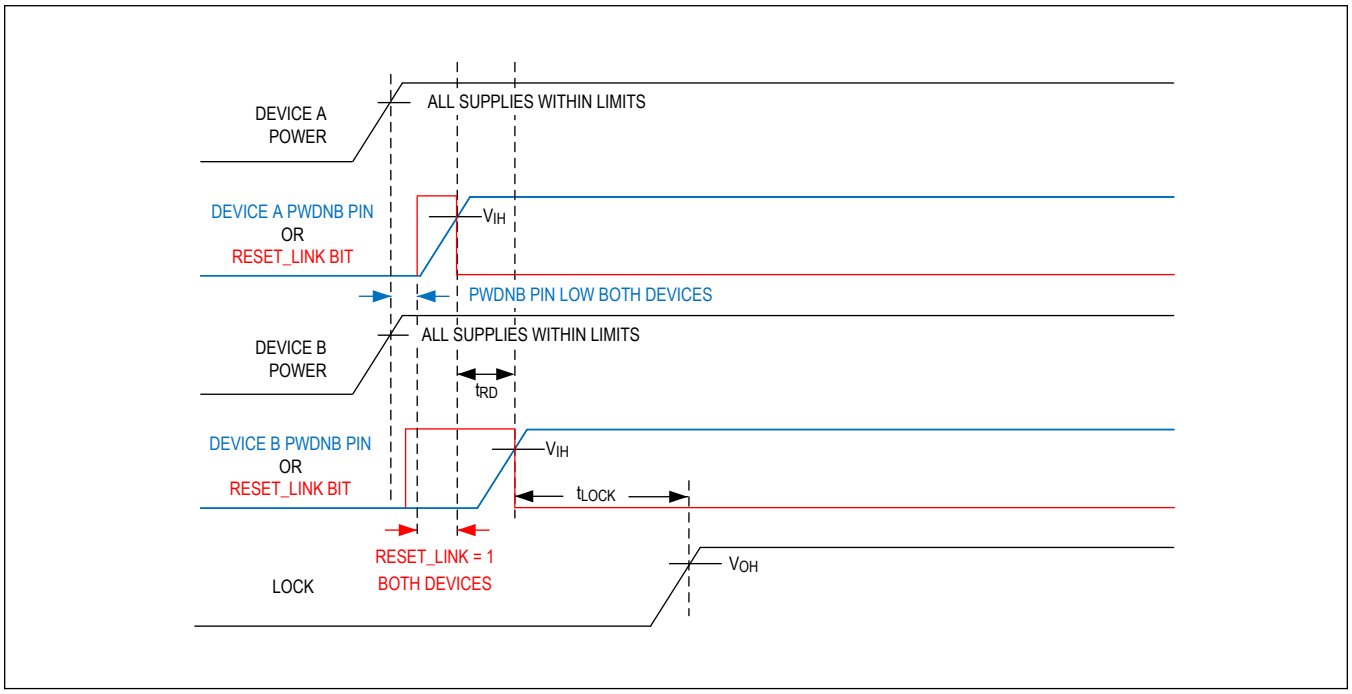


Figure 20. GMSL2 Lock Time

Figure 20 illustrates the sequence that is used to characterize GMSL2 link lock time. Device A is the first device (serializer or deserializer) to power up or resume operation from a RESET_LINK state. Device B is the device (deserializer or serializer) at the other end of the GMSL link.

Link lock indicates that the data receive paths are locked (forward channel in the deserializer, reverse channel in the serializer). Video and control channel functions (I^2C/UART, SPI, GPIO, and audio) can be used immediately after link lock is asserted.

The device establishes single link GMSL2 connectivity and link lock automatically following power-up. This is an indication that the cable is plugged in and the system is up and running. Lock is obtained without interaction between the µC and GMSL devices. Both serializers and deserializers have an open-drain LOCK output pin and a related status register.

The MAX9295D has only one link; therefore, it does not support dual-link and splitter configurations.

The GMSL2 link uses the crystal as the reference clock for GMSL2 links, so a valid video input (PCLK) is not needed for the GMSL2 link to lock.

Notes:

1. The lock sequence is initiated by the release of the PWDNB pin or the RESET_LINK bit in either the serializer or the deserializer.
2. The lock time is measured from the later of the PWDNB or the RESET_LINK release on either the serializer or the deserializer to LOCK being asserted.
3. The PWDNB/RESET_LINK states on the two sides of the link must have overlap when both devices are in PWDNB/RESET_LINK mode prior to the lock process starting.
4. If RESET_LINK is used to initiate the lock, the PWDNB is assumed to be high after power-up (normal operation).
5. If PWDNB is used to initiate the lock, the RESET_LINK is assumed to be low after power-up (normal operation).

6. Device A is the first device (serializer or deserializer) to be powered up. Device B is the device (deserializer or serializer) at the other end of the GMSL link.
7. To achieve the specified lock time, time delay t_{RD} (delay between release of the PWDNB/RESET_LINK on the two devices) must be less than 90ms. If this timing cannot be guaranteed, contact the factory for guidance.
8. Lock time and maximum allowed t_{RD} vary between different families of GMSL devices. They depend on the characteristics of both the serializer and deserializer. The typical lock time of a specific link can be best estimated as the longer of the lock times specified in each device data sheet. Similarly, the maximum permission t_{RD} for a specific link can be estimated as the smaller of the values specified in each device data sheet. For further guidance, contact the factory.
9. If there is an instantaneous interruption to link lock, a period of 100ms following loss of lock should be provided to enable the link to automatically recover prior to any ECU initiated resets being issued. This minimizes any disruptions caused by a transient loss in connectivity.

Video Lock

Video lock indicates that the deserializer is receiving valid video data. After the GMSL2 link has locked, the deserializer video-output PLL begins its locking sequence. The deserializer normally starts outputting video data several milliseconds after it establishes link lock, provided that it is receiving video packets from the serializer. Video-lock status is typically read from a register. However, the deserializer LOCK pin behavior can be changed through a register setting so that the LOCK pin is asserted only when the deserializer is outputting video.

Clocking

GMSL2 Reference Clock

The GMSL2 devices require a reference clock source to generate the 6GHz line-rate clock and associated internal clocks. Both the serializer and deserializer can be clocked with an external 25MHz crystal or an external clock source with a frequency accuracy of ±200ppm.

GMSL1 Reference Clock

In GMSL1 mode, an internal oscillator is used to generate the main clock. The crystal/reference clock input is not used. A valid video stream must be provided to enable generation of the required clock. If the video stream is not available, the link can be placed in configuration link mode, in which case it is clocked using an internally generated clock to enable control-channel operation in the absence of an incoming video stream. When streaming is enabled, the link will synchronize to the PCLK generated from the incoming video stream. GMSL1 operation enables automatic switching between configuration link mode (internally generated clock) and video-link mode (link synchronized to external video-stream clock) to ensure that control-channel communication is always available regardless of the status of the video source.

Spread-Spectrum Clocking

Analog Devices' GMSL2 links provide exceptional EMI performance. Optional spread-spectrum clocking (SSC) is available to mitigate electromagnetic interference emitted from devices and interconnections and provide additional margin.

SSC reduces peaks in the frequency spectrum by spreading the signal over a wider bandwidth. The spread has a 25kHz sawtooth modulation profile, programmable to deviate up to 2500ppm pk-pk from the center frequency.

Reference Clock Generation

The MAX9295D includes a frequency reference output that enables it to provide a frequency reference for sensors or other serializers located in close proximity, eliminating the need for duplicate references and thus saving cost and area.

The output can either drive the 25MHz crystal-based frequency reference with an optional divide by 2 or 4 (RCLKOUT), or it can drive the output of an internal clock generator PLL (DPLL_OUT). DPLL_OUT is generated from the 25MHz crystal for precise absolute frequency, and it can be configured to generate a multitude of output frequencies, such as 19.2MHz, 27MHz, 37.125MHz, or 74.25MHz.

Error and Fault Condition Monitoring

MAX9295D has an open-drain, multipurpose error reporting, and interrupt status output. The active-low ERRB pin is driven by the logical OR of a wide variety of error and event status indicators. The ability of each error condition to drive ERRB is maskable by register settings. Each error and event that can drive ERRB has a status flag within a sub-block of registers, so the reason for assertion of ERRB can be determined by reading the register status.

Line Fault

GMSL2 devices include a novel line-fault detection circuit. It detects and reports open-circuit, short to battery, short to ground, and line-to-line short conditions on the GMSL interconnect. The line-fault monitor requires external resistors REXT and RPD connected to the LMN pins as shown in Figure 21 and Figure 22. Note that these figures illustrate the connection scheme that is employed when the deserializer's line-fault detectors are used, which is typically the case in camera applications. The serializer's line-fault detectors can alternatively be used, and in this case the LMN connections and placement of REXT and RPD are reversed between the serializer and deserializer sides of the link. Whether serializer or deserializer line-fault detectors should be used depends on the architecture of a given system. In general, the device that is used to detect line fault should have a clear communication channel to the primary system controller module that does not depend on the integrity of the GMSL link. In both cases, a 49.9kΩ, 1% tolerance resistor (RPD) is connected from each GMSL signal line to ground at the end of the link opposite the location of the line-fault detectors, while a 42.2kΩ (LMN0 with STP) or 48.7kΩ (LMN0 with coax, LMN1), 1% tolerance resistor (REXT) is connected from each GMSL signal line to the relevant LMN_ pin of the device whose line-fault detectors are utilized. Only the specified resistor values/tolerances should be used to ensure correct functionality. Note that RPD and REXT are located on opposite sides of the link, so the line-fault detection must be considered in the design of both the serializer and deserializer portions of a system. Line-fault detection cannot be used in conjunction with power-over-cable (PoC), and it should not be used in applications in which there is a potential difference between the grounds at opposite ends of the link.

The MAX9295D provides a pair of line-fault detection inputs on pins MFP13 (LMN0) and MFP14 (LMN1). The presence of a fault condition can be flagged using MFP6 configured as ERRB output. The line-fault monitor pins offer flexible connection and programming. Each line-fault input can be assigned to either polarity of the link when in STP mode. In coax mode, a single line fault input is required, and in this case either of the available line fault input functions can be used. The unneeded line fault function can be disabled, and the corresponding MFP can be used for another function in coax mode. In applications that do not require line-fault detection, both line fault inputs can be disabled and the corresponding MFPs can be used for alternate functions as needed.

The presence of a fault can be reported by the ERRB MFP function as mentioned previously. A fault condition generates an interrupt that is forwarded across the link such that the ERRB output of the serializer will flag a line-fault detected by the deserializer and vice-versa. In addition, the LFLT_INT bit flags the presence of a fault condition, enabling convenient register access. In the event of a fault, ERRB will be driven low while the LFLT_INT bit is written to a value of 1. Further details of a fault event are available in register fields LF_0 and LF_1 (depending on which line-fault inputs are being used in a given application).

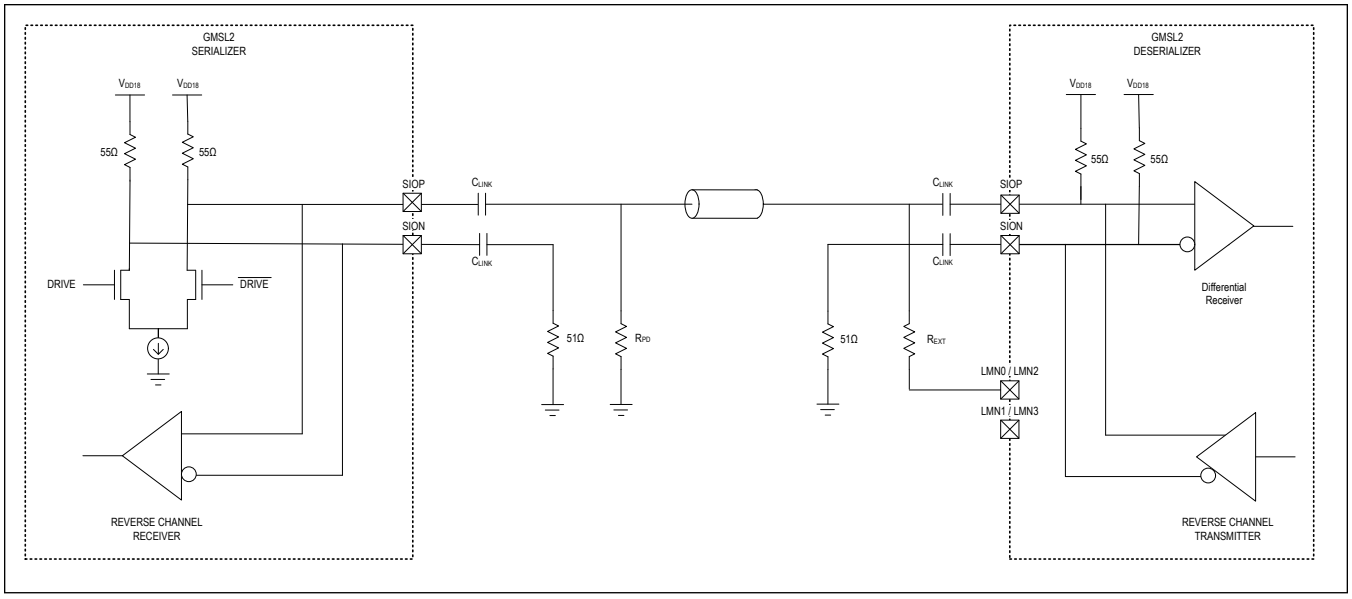


Figure 21. Typical GMSL1/2 Link Application Circuit for Coax Cable

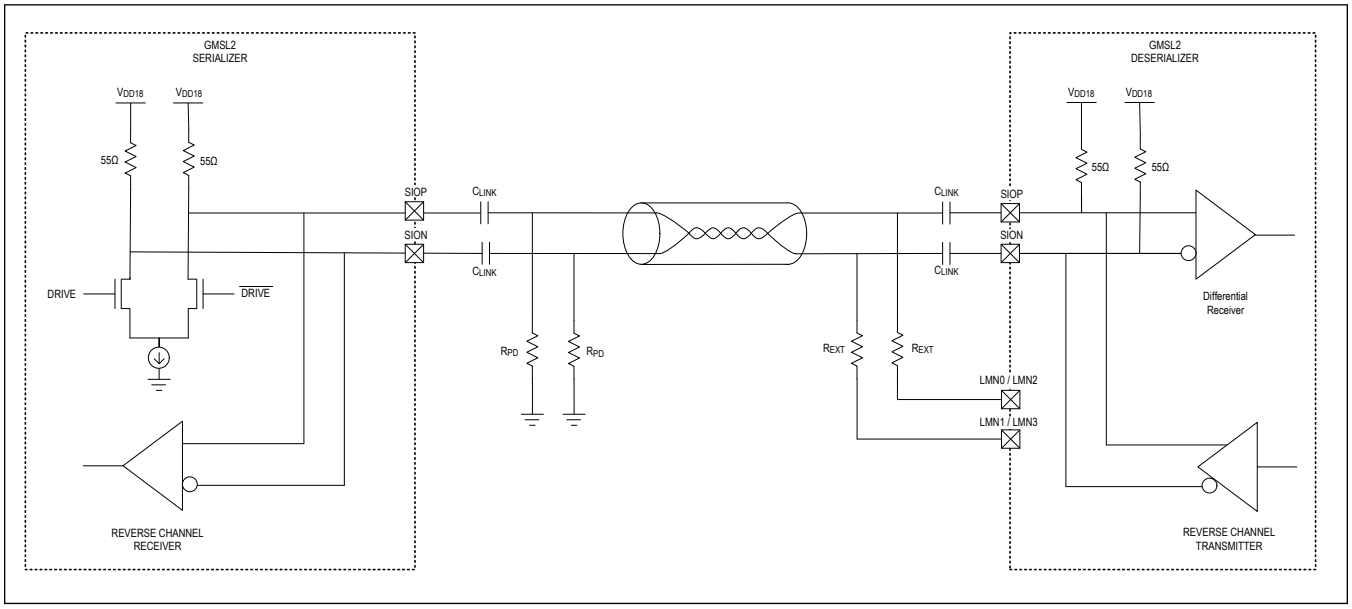


Figure 22. Typical GMSL1/2 Link Application Circuit for Twisted Pair

CSI-2 ECC and Checksum Error Detection

The ERRB pin function also flags CSI-2 ECC and checksum errors and several other configurable D-PHY errors. These errors generate an interrupt that asserts the ERRB output on the deserializer side of the link, alerting the µC on the far side of the link to the presence of the error condition. Each error that drives ERRB has a corresponding status flag in the registers. Information regarding ERRB assertion is accessible by reading these flags either locally or from the remote (deserializer) side.

Analog-to-Digital Converter

The MAX9295D features a 10-bit, integrating analog-to-digital converter (ADC) with an analog input multiplexer. This

multiplexer selects a single-ended input channel from external input lines (ADC0, ADC1, ADC2), and internal power-supply monitors. The ADC has a single-ended input with a full-scale range that extends from ground to the applied reference voltage (VREF). The input range can be extended beyond VREF if the programmable input voltage-divider is enabled. The reference voltage that sets the full-scale range for the ADC can be an internal reference, an external precision reference, or the VDD18 supply voltage divided by 2.

The ADC is controlled through the MAX9295D's registers with feedback through the device's interrupt functionality. Controls include channel selection, overrange/underrange thresholds, input divider/buffer configuration, and conversion start. Feedback includes ADC conversion done, ADC power-up complete (ADC ready), ADC overflow, ADC overrange, and ADC underrange.

The overvoltage/undervoltage threshold can be programmed separately for up to eight ADC input channels. These thresholds can be enabled to assert an interrupt if the converted ADC value is out of range. This feature allows voltage monitoring without the need to read out the converted value at each A/D conversion such that the user can issue a conversion, review the interrupt status for overrange/underrange, and then proceed to the next channel when ready.

The ADC also contains a round-robin state machine that will continuously cycle through up to eight input channels for continuous voltage monitoring. When an overrange/underrange or overflow has occurred, an interrupt is generated. The ADC inputs to be monitored and the corresponding interrupt thresholds are configured through the ADC control registers.

The state machine also contains an ADC shutdown mode that powers off the ADC for up to 64,000 ADC conversion cycles.

The conversion time is approximately 430µs.

A 1.22V internal reference can be used as the ADC's reference. The absolute accuracy of the ADC is ±2% using the internal reference. Using an external reference can provide ±1% absolute accuracy.

The ADC contains a low-offset input buffer that can be used when sampling signals with high source impedance. If the input buffer is used, the ADC will show some non-linearity affecting its accuracy below 100mV, which is the minimum input voltage for the buffered input.

ADC Features

See Figure 23.

- Input buffer, ADC and voltage reference.
- Programmable input multiplexer with 3 channels for monitoring external voltages and 3 channels for monitoring internal supply voltages.
- Integrated voltage-dividers (/1, /2, /3 and /4) for external inputs to enable measurement of voltages as high as V_{DDIO}.
- Input for optional external precision voltage reference.
- Overvoltage and undervoltage interrupt generation.
- ADC conversion-start and conversion-done interrupt generation.
- Power control and interrupt generation when ADC power-up is complete.
- Continuous round-robin monitoring of all channels.
- Programmable input and reference gains for scaling the input and reference.

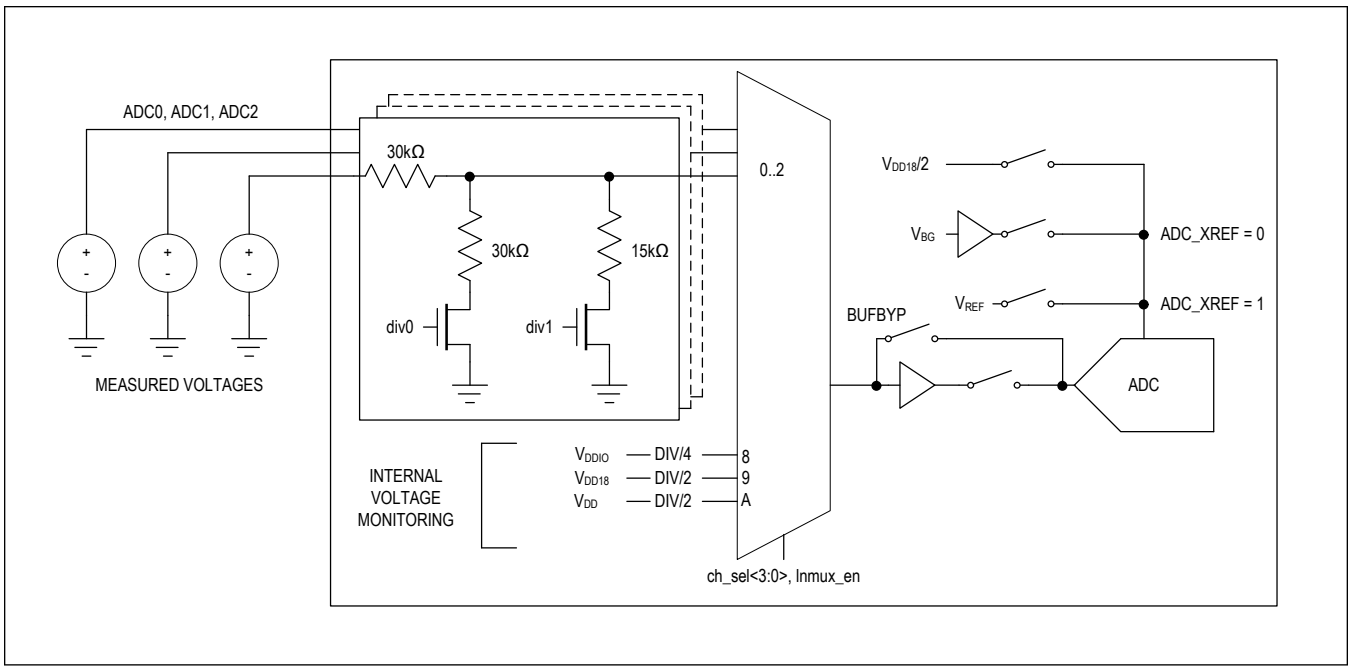


Figure 23. ADC Block Diagram

Power Supplies

The MAX9295D provides flexible power-supply configurations.

The 1V core supply can be provided directly or supplied by an internal regulator. To minimize power dissipation, connect 1.0V ±5% to V_{DD}. If V_{DD} < 1.1V and CAP_VDD < 1.05V, the regulator is automatically disabled at power-up and low-resistance switches connect V_{DD} to the internal supply rails. If using the internal regulator, connect 1.2V ±5% to V_{DD} and write REG_ENABLE = 1 and REG_MNL = 1 in order following power-up as part of the device initialization to enable the internal LDO.

The V_{DDIO} supply for the I/O pins can be 1.8V to 3.3V for flexibility in accommodating devices interfacing to the MAX9295D. The allowable supply voltage range is 1.7V (1.8V -5%) to 3.6V (3.3V +9%).

V_{DD18} is the primary analog supply. Connect 1.8V ±5%.

Proper bypassing of all supplies is essential for optimal performance. In all cases, a decoupling capacitor should be placed as close as possible to each supply pin. See Table 3 for guidance regarding appropriate decoupling for each supply pin. See Table 2 for power supply tolerances and noise requirements. Contact the factory for guidance on sharing supplies and optimizing supply decoupling.

Extensive power supply diagnostics capabilities are provided by the device. Undervoltage detection is included for all power supplies. Moderate undervoltage conditions on the V_{DD18} and V_{DDIO} supply voltages can be indicated using either the ERRB pin or by reading the register field associated with the power supply undervoltage flag. An undervoltage condition on the V_{DD} supply, which could corrupt the register configuration, is detected by the power manager and results in a reset. Similarly, a severe undervoltage condition on V_{DD18} or V_{DDIO} also results in a reset. In the case of a reset, device configuration reverts to the power-up default state when the supplies have recovered, and the host device must initiate the power-on initialization procedure to return the device to full operation.

Overvoltage detection is also provided, although only for the internal V_{DD} supply voltage (CAP_VDD). As in the case of undervoltage events, an overvoltage situation can be reported by the ERRB pin in addition to a dedicated internal interrupt flag. No further action is taken by the power manager during an overvoltage situation, and the device will continue to operate normally, although it may sustain damage depending on the duration and magnitude of the overvoltage event.

In addition to the dedicated power supply monitor functions described here, the ADC can also be used to monitor all

supplies. See the *Analog-to-Digital Converter* section for further details regarding the ADC.

When relying on the ERRB pin to convey the occurrence of an undervoltage event, it is recommended that an external 1MΩ resistor be connected between the ERRB pin and ground. This is suggested because ERRB is not a power-up default MFP function. As a result, following a reset that is triggered by an undervoltage event, the ERRB MFP pin reverts to high impedance as opposed to ERRB. During an error state, the host device expects ERRB to drive logic low, and the presence of the aforementioned resistor enables the appropriate logic level to be maintained following the reset, alerting the host device that attention is required.

Standby and Sleep Mode

The MAX9295D includes a power manager block. Its primary function is to monitor supply voltages and control low-power standby and sleep modes.

There are two ways to enter low-power mode while all power supplies are active. One option is to assert the PWDNB pin (active low). This places the device in standby mode and resets the registers and device configurations to their default power-up state. If any supply drops below its internal threshold, the device automatically enters standby mode, regardless of the state of PWDNB.

The second low-power state is referred to as sleep mode. The sleep mode preserves all critical register settings and configurations. The device can be put into the sleep mode using an I^2C/UART command. The RESUME state restores the device to the pre-sleep condition without the need for additional register writes. RESUME is invoked by an I^2C command or a low-frequency clock beacon transmitted from the main device over the GMSL2 link.

Thermal Management

Power consumption of the MAX9295D varies based on the use case. Care must be taken by the user to provide sufficient heat dissipation with proper board design and cooling techniques. The package's exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below 125°C to meet electrical specifications and avoid impacting device reliability.

Refer to Application Note 4083: *Thermal Characterization of IC Packages* for further guidance.

Applications Information

Software Programming Model

Analog Devices' automotive serializers and deserializers follow a general software programming model. Except for features that require in-operation control channel accesses such as the ASIL safety measures and interrupt handling, the following programming model is used:

1. Set the impacted functional blocks to disabled or reset mode. A general method to place the part in IDLE state is to stop all side channel and video traffic, followed by a register write (RESET_LINK = 1) to stop the GMSL link.
2. Fully configure the settings for each feature before it is enabled.
3. Establish the link by setting RESET_LINK = 0 and wait for the link to lock.
4. Start video and side-channel traffic.

If changing the configuration of a feature during the operation of other features, disable the reconfigured feature, change its settings, and re-enable it.

Control Channel Programming

GMSL device registers can only be accessed and configured through the primary I^2C/UART interface. By default, the primary I^2C/UART channel is also sent to the remote-side device and any peripheral connections. For multimain configurations, with microcontrollers connected to both the serializer and deserializer, disabling the remote control channel through register settings is recommended to prevent bus contention.

Host-to-Peripheral Primary I^2C and Pass-Through I^2C Communication

When communicating between a host and peripheral, primary, and pass-through I^2C operation is the same. An I^2C tunnel across the GMSL2 link connects the host's I^2C primary to the remote I^2C subordinate. This logically connects separated I^2C buses, enabling I^2C transactions across the serial link to occur (with some delay) as if performed on the same physical I^2C bus. The GMSL2 serializer and deserializer are intermediary devices; the host I^2C primary connects to a GMSL2 device I^2C subordinate, and the peripheral I^2C subordinate connects to a GMSL2 device I^2C primary.

For example, when the host I^2C primary transacts on one side of the link (local-side), data is forwarded to the other side (remote-side) by the I^2C subordinate of the local-side GMSL2 device. Data is then received by the I^2C primary of the remote-side GMSL2 device, which in turn generates the same I^2C transaction with the peripheral subordinate I^2C. The remote-side GMSL2 device sends back any I^2C data expected by the local-side.

The I^2C interface uses clock stretching (holding SCL low) to account for timing differences between primary and subordinate and to allow time for data to be forwarded and received across the serial link. The host I^2C primary and peripheral I^2C subordinate must support clock stretching by the GMSL2 device.

SDA and SCL lines operate as both an input and an open-drain output. Pull-up resistors are required on SDA and SCL.

Each transmission consists of a START condition sent by a main, followed by the device's 7-bit subordinate address plus a R/W bit, register address bytes, one or more data bytes, and finally a STOP condition.

Register addresses are 16-bits wide. Single or multiple data bytes can be written or read (by address autoincrements).

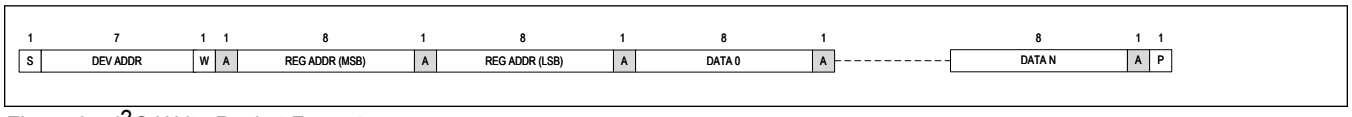


Figure 24. I^2C Write Packet Format

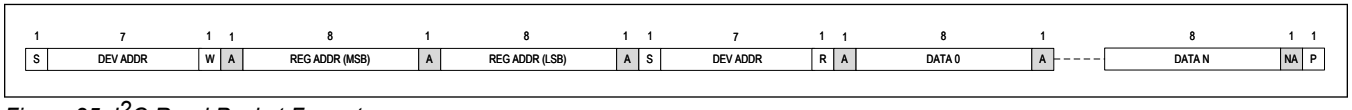


Figure 25. I^2C Read Packet Format

I²C Write-Packet Format

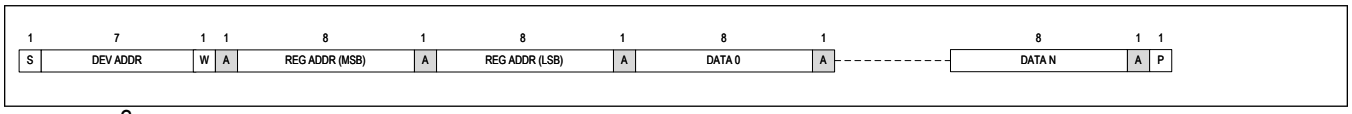


Figure 26. I²C Write-Packet Format

I²C Read-Packet Format

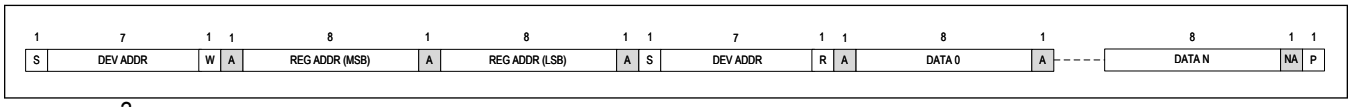


Figure 27. I²C Read-Packet Format

Device Address

Each device on the I²C/UART control channel must have a unique address. The GMSL2 device address is set to one of several 7-bit addresses according to the voltage level of the CFG0 pin at power-up. See the *CFG Latch at Power-Up Pins* section. Note that device address can be changed after power-up by writing to the DEV_ADDR register.

Primary I²C Host-to-GMSL2 Device Communication

The host I²C primary has access to GMSL2 serializer and deserializer registers. The host can program GMSL2 device registers to configure the pass-through I²C/UART interface as either I²C or UART.

Main UART

When the primary I²C/UART interface is configured as UART, there are two operating modes: base and bypass.

UART Base Mode

Base mode is a µC communication methodology that allows the serializer and deserializer to access each other's registers, as well as the registers of peripheral devices. Base mode is enabled by default at power-up. In base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL2 UART packet protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings). The device addresses of the serializer and deserializer in this mode are programmable.

In base mode, serializer, deserializer, and peripheral registers can be written and read using the half-duplex GMSL2 UART protocol.

Figure 28 shows the UART protocol for writing and reading in base mode.

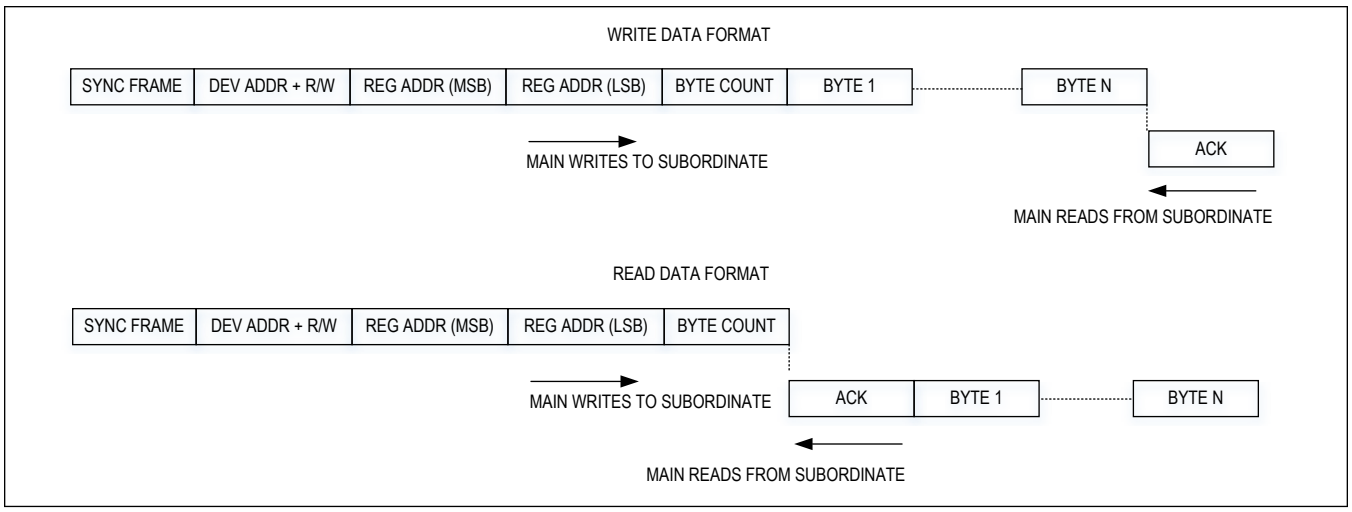


Figure 28. GMSL2 UART Protocol for Base Mode

UART Bypass Mode

In bypass mode, the serializer/deserializer ignore UART commands from the µC, allowing the µC to communicate only with peripheral devices. The µC cannot access the serializer/deserializer's registers in this mode. The UART transitions are simply sent over the GMSL link. Ignoring UART transactions prevents inadvertent misprogramming of serializer and deserializer registers. The device addresses of the serializer and deserializer in this mode are not programmable.

Switching Between UART Base and Bypass Modes

There are two ways to switch between base mode and bypass mode: by programming the register or by using the MS pin.

Two modes can be set by programming: temporary or permanent. In temporary mode, bypass mode is active only as long as there is UART activity. When there is no UART activity for a selected timeout, both devices exit bypass mode and the bit is automatically cleared. In permanent mode, the devices stay in bypass mode until the next power-down.

When set by the MS pin, a high pin level puts the device into bypass mode, and a low level puts the device in base mode. MS is set on-the-fly and is not latched on power-up.

UART Frame Format

Regular UART frames with an even parity bit are used to carry 1 byte of data each. A frame consists of a low start bit followed by 8 data bits, a parity bit, and a high stop bit. The parity bit is high if the number of ones in the 8 bits of data is odd. Otherwise, the parity bit is low. There must be at least 1 high stop bit. If the next frame is in the same packet, there can be at most 4 high bits from the end of the stop bit to the beginning of the next start bit. Note that in the case of a parity bit error, the packet, starting from the frame with the error, is discarded. The start of each frame is always a high-to-low transition (i.e., the stop bit is high and the start bit is low). The phase of the internal UART bit clock is adjusted using the start bit of each frame. The framer calibrates the length of 1 UART bit in terms of the internal oscillator clock using the synchronization frame (i.e., the first frame of a UART packet transmission). In bypass mode, the parity bit is enabled by default, but the frames are not checked for parity errors. Either even or odd parity can be used. The parity bit is passed along with UART data transmissions; the recipient of the data must perform error checking. The parity bit can optionally be disabled in bypass mode before entering bypass mode. Note that the bit rate in bypass mode must be the same bit rate last used in base mode.

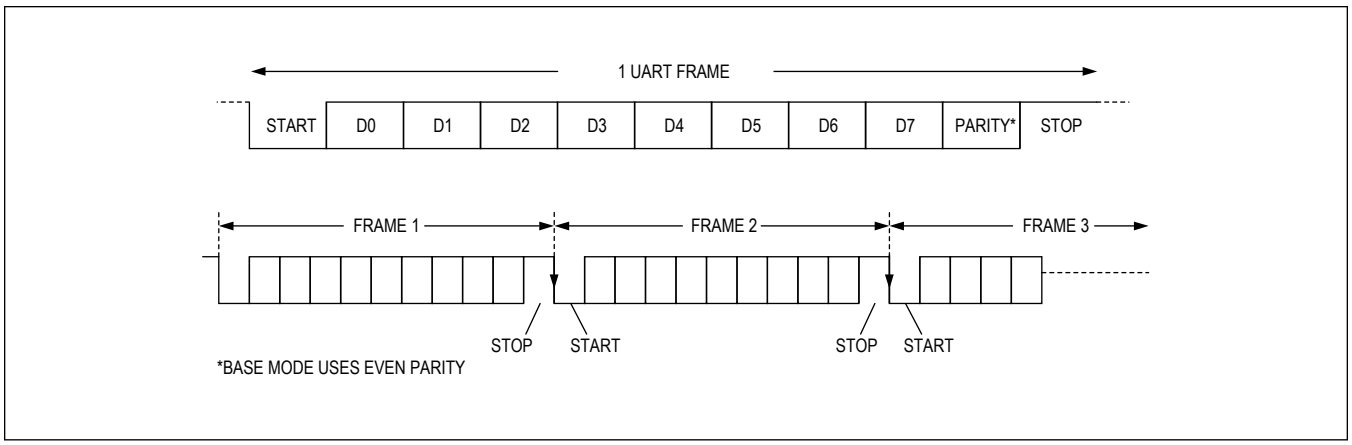


Figure 29. UART Data Format for Base Mode

Synchronization Frame

The serializer/deserializer must calibrate internal bit length counters with the UART bit rate for proper recovery of UART frames. A sync frame (a regular UART frame with the value 0x79) is sent as the first frame of each data packet from the µC and is used to calibrate the bit length in terms of the device's internal clock. Sync frames must be properly detected before the subsequent frames of the packet can be correctly received. When the line stays high for at least 32 bits, the packet boundary is reset and the framer begins waiting for the next sync frame.

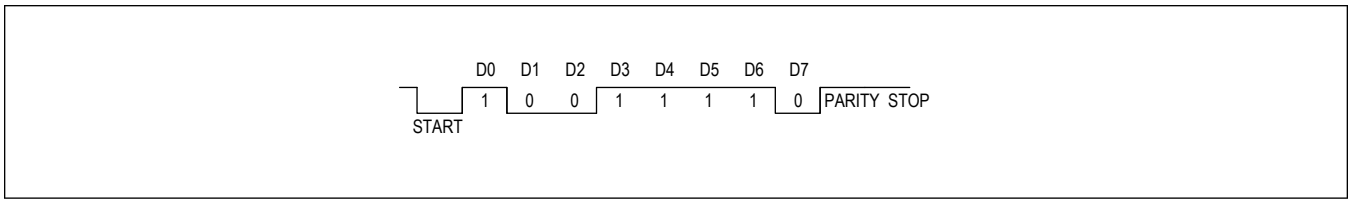


Figure 30. UART Synchronization Frame

Acknowledge Frame

When a packet is successfully received, the addressed device responds with an acknowledge frame to inform the µC that no errors were detected in the transmitted packet, and it was recognized as valid. This is sent after the last bit of a successfully recognized packet has been received. The acknowledge frame is a regular UART frame (value 0xC3). Data written to the serializer/deserializer registers do not take effect until after the acknowledge byte is sent.

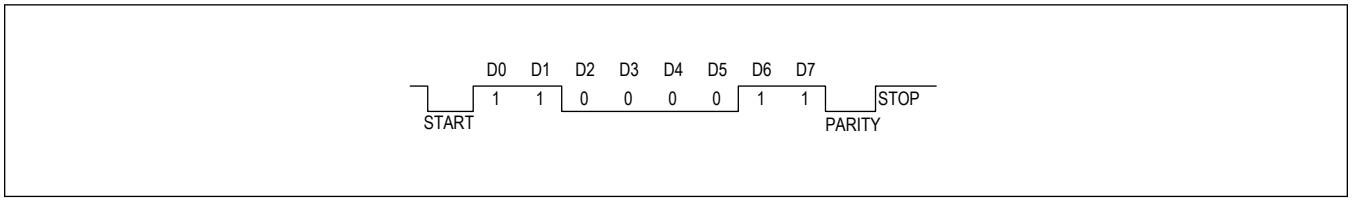


Figure 31. UART Acknowledge Frame

Write Packet

Write packets consist of a 5-byte packet header followed by 1 or more data bytes. A packet is recognized as a write packet when the LSB of the device address frame is 0. The addressed device responds with an acknowledge frame if no errors were detected while receiving the write packet and the write packet is valid. Byte count indicates the number of data bytes to be written and it cannot be 0.

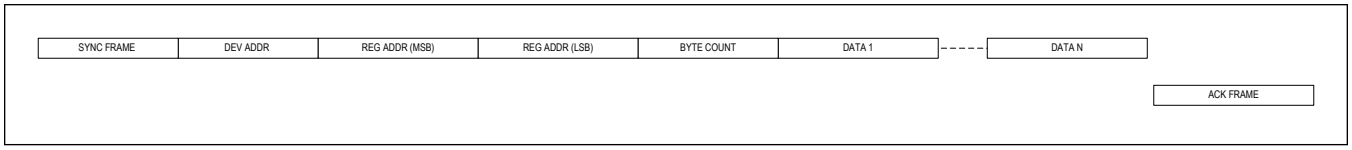


Figure 32. UART Write Packet Format

Read Packet

Read packet consists of 5 bytes. The LSB of the device address frame is 1 for read packets. If no errors were detected while receiving the read packet and the packet is valid, the addressed device responds with an acknowledge frame followed by 1 or more data bytes. Byte count indicates the number of data bytes to be read and it cannot be 0.

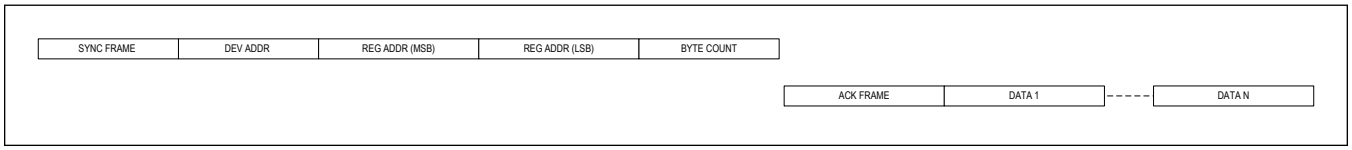


Figure 33. UART Read Packet Format

Ordering Information

PART NUMBER	TEMPERTURE RANGE	PACKAGE
MAX9295DGTM/V+	-40°C TO +105°C	48 TQFN-EP
MAX9295DGTM/V+T	-40°C TO +105°C	48 TQFN-EP (Tape and Reel)
MAX9295DGTM/VY+	-40°C TO +105°C	48 TQFN-SW-EP
MAX9295DGTM/VY+T	-40°C TO +105°C	48 TQFN-SW-EP (Tape and Reel)

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape and reel.

/V Denotes an automotive qualified part.

Y Denotes wettable flank.

EP Denotes exposed pad.

Register Map

MAX9295D

Reserved, Unused, and Read-Only Register Bits

Not all register bits in the register space are shown in the register table. Any bit not explicitly defined in the register table should be treated as reserved and should not be modified. When a write is required to a register with both defined and undefined register bits, first read the register's contents, then create a new register value by only changing the defined bits, and finally, write the new byte to the register (Read/Replace/Write).

In this document, default values are provided for read-only register bits. Read-only bit states are changed at powerup according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

Note: * Indicates that the register is stored when entering sleep mode and is restored upon exit from sleep mode.

ADDRESS	RESET	NAME	MSB							LSB
DEV										
0x00	0x80	REG0[7:0]*	DEV_ADDR[6:0]							CFG_BLOCK
0x01	0x08	REG1[7:0]*	IIC_2_EN	IIC_1_EN	DIS_LOCAL_CC	DIS_REM_CC	TX_RATE[1:0]		RSVD[1:0]	
0x02	0x53	REG2[7:0]*	VID_TX_EN_U	VID_TX_EN_Z	VID_TX_EN_Y	VID_TX_EN_X	RSVD	RSVD	RSVD	RSVD
0x03	0x00	REG3[7:0]*	–	–	UART_2_EN	UART_1_EN	RSVD	RSVD	RCLKSEL[1:0]	
0x05	0xC0	REG5[7:0]*	LOCK_EN	ERRB_EN	–	–	RSVD	RSVD	PU_LF1	PU_LF0
0x06	0x80	REG6[7:0]*	GMSL2	–	RCLKEN	RSVD	RSVD[3:0]			
0x0D	0x9B	REG13[7:0]	DEV_ID[7:0]							
0x0E	0x00	REG14[7:0]	RSVD[3:0]				DEV_REV[3:0]			
0x0F	0x00	REG15[7:0]	RSVD	RSVD	RSVD[1:0]		DV_CPBL_N	DUAL_CPBL_N	SPLTR_CPBL_N	RSVD
0x26	0x22	REG26[7:0]	–	LF_1[2:0]			–	LF_0[2:0]		
OVERLAP										
TCTRL										
0x08	0x00	PWR0[7:0]	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
0x0C	0x1A	PWR4[7:0]*	RSVD	DIS_LOCAL_WAKE	RSVD	WAKE_EN_A	RSVD[3:0]			
0x10	0x11	CTRL0[7:0]*	RESET_ALL	RESET_LINK	RESET_ONESHOT	RSVD	SLEEP	REG_ENABLE	RSVD[1:0]	
0x11	0x0A	CTRL1[7:0]*	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CXTP_A
0x12	0x04	CTRL2[7:0]	RSVD	RSVD	–	REG_MNL	RSVD[1:0]		RSVD[1:0]	
0x13	0x10	CTRL3[7:0]	RSVD	RSVD	RSVD[1:0]		LOCKED	ERROR	CMU_LOCKED	–
0x18	0xA0	INTR0[7:0]*	RSVD	RSVD	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		

ADDRESS	RESET	NAME	MSB							LSB
0x19	0x00	INTR1[7:0]*	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
0x1A	0x0B	INTR2[7:0]*	RSVD	RSVD	REM_ERR_OEN	MEM_INT_ERR_OEN	LFLT_INT_OEN	IDLE_ERR_OEN	RSVD	DEC_ERR_OEN_A
0x1B	0x00	INTR3[7:0]	RSVD	RSVD	REM_ERR_FLAG	MEM_INT_ERR_FLAG	LFLT_INT	IDLE_ERR_FLAG	RSVD	DEC_ERR_FLAG_A
0x1C	0x09	INTR4[7:0]*	RSVD	EOM_ERR_OEN_A	VDD_OV_OEN	RSVD	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	WM_ERR_OEN
0x1D	0x00	INTR5[7:0]	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	VDD_OV_FLAG	RSVD	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	WM_ERR_FLAG
0x1E	0xE3	INTR6[7:0]*	VDDCMP_INT_OEN	RSVD	VDDBAD_INT_OEN	–	–	ADC_INT_OEN	RSVD	MIPI_ERR_OEN
0x1F	0x00	INTR7[7:0]	VDDCMP_INT_FLAG	RSVD	VDDBAD_INT_FLAG	–	–	ADC_INT_FLAG	RSVD	MIPI_ERR_FLAG
0x20	0x9F	INTR8[7:0]*	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
0x21	0xDF	INTR9[7:0]*	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
0x22	0x00	CNT0[7:0]	DEC_ERR_A[7:0]							
0x24	0x00	CNT2[7:0]	IDLE_ERR[7:0]							
0x25	0x00	CNT3[7:0]	PKT_CNT[7:0]							
GMSL										
0x29	0x00	TX1[7:0]*	LINK_PRBS_GEN	–	RSVD	ERRG_EN_A	–	–	RSVD	RSVD
0x2A	0x20	TX2[7:0]*	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x2B	0x44	TX3[7:0]*	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
0x2C	0x00	RX0[7:0]*	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
0x30	0x41	GPIOA[7:0]*	GPIO_RX_FAST_BIDIR_EN	RSVD	GPIO_FWD_CDLY[5:0]					
0x31	0x88	GPIOB[7:0]*	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
CC										
0x40	0x26	I2C_0[7:0]*	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
0x41	0x56	I2C_1[7:0]*	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
0x42	0x00	I2C_2[7:0]*	SRC_A[6:0]							–
0x43	0x00	I2C_3[7:0]*	DST_A[6:0]							–
0x44	0x00	I2C_4[7:0]*	SRC_B[6:0]							–
0x45	0x00	I2C_5[7:0]*	DST_B[6:0]							–

ADDRESS	RESET	NAME	MSB							LSB
0x47	0x00	I2C_7[7:0]	UART_RX_OVERFLOW	RSVD	–	–	–	I2C_TIMED_OUT	REM_ACK_ACKED	REM_ACK_RECVED
0x48	0x42	UART_0[7:0]*	ARB_TO_LEN[1:0]		REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
0x49	0x96	UART_1[7:0]	BITLEN_LSB[7:0]							
0x4A	0x80	UART_2[7:0]	OUT_DELAY[1:0]		BITLEN_MSB[5:0]					
0x4C	0x26	I2C_PT_0[7:0]	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
0x4D	0x56	I2C_PT_1[7:0]	RSVD	MST_BT_PT[2:0]			–	MST_TO_PT[2:0]		
0x4E	0x00	I2C_PT_2[7:0]	XOVER_EN_2	I2C_TIMED_OUT_2	REM_ACK_ACKED_2	REM_ACK_RECVED_2	XOVER_EN_1	I2C_TIMED_OUT_1	REM_ACK_ACKED_1	REM_ACK_RECVED_1
0x4F	0x00	UART_PT_0[7:0]	BITLEN_MAN_CFG_2	DIS_PAR_2	UART_RX_OVERFLOW_2	UART_TX_OVERFLOW_2	BITLEN_MAN_CFG_1	DIS_PAR_1	UART_RX_OVERFLOW_1	UART_TX_OVERFLOW_1
CFGV VIDEO_X										
0x50	0x30	TX0[7:0]*	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x53	0x10	TX3[7:0]*	–	–	RSVD	RSVD	–	–	TX_STR_SEL[1:0]	
CFGV VIDEO_Y										
0x54	0x30	TX0[7:0]*	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x57	0x11	TX3[7:0]*	–	–	RSVD	RSVD	–	–	TX_STR_SEL[1:0]	
CFGV VIDEO_Z										
0x58	0x30	TX0[7:0]*	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x5B	0x12	TX3[7:0]*	–	–	RSVD	RSVD	–	–	TX_STR_SEL[1:0]	
CFGV VIDEO_U										
0x5C	0x30	TX0[7:0]*	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x5F	0x13	TX3[7:0]*	–	–	RSVD	RSVD	–	–	TX_STR_SEL[1:0]	
CFGI INFOFR										
0x78	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x7B	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0x7C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
CFGL SPI										
0x80	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x83	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0x84	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x85	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–

ADDRESS	RESET	NAME	MSB							LSB
0x86	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x87	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC CC										
0x88	0xF0	TR0[7:0]*	RSVD	RSVD	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x8B	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0x8C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x8D	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x8E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x8F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL GPIO										
0x90	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x93	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0x94	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x95	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x96	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x97	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL IIC_X										
0xA0	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xA3	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0xA4	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0xA5	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0xA6	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0xA7	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL IIC_Y										
0xA8	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xAB	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0xAC	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0xAD	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–

ADDRESS	RESET	NAME	MSB							LSB
0xAE	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0xAF	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
VID_TX X										
0x100	0x68	VIDEO_TX0[7:0]*	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		AUTO_BPP	RSVD	RSVD[1:0]	
0x101	0x58	VIDEO_TX1[7:0]*	RSVD[1:0]		BPP[5:0]					
0x102	0x0A	VIDEO_TX2[7:0]*	PCLKDET	DRIFT_ERR	OVERFLOW	FIFO_WARN	RSVD	LIM_HEART	RSVD	RSVD
0x106	0x00	VIDEO_TX6[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
VID_TX Y										
0x108	0x68	VIDEO_TX0[7:0]*	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		AUTO_BPP	RSVD	RSVD[1:0]	
0x109	0x58	VIDEO_TX1[7:0]*	RSVD[1:0]		BPP[5:0]					
0x10A	0x0A	VIDEO_TX2[7:0]*	PCLKDET	DRIFT_ERR	OVERFLOW	FIFO_WARN	RSVD	LIM_HEART	RSVD	RSVD
0x10E	0x00	VIDEO_TX6[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
VID_TX Z										
0x110	0x68	VIDEO_TX0[7:0]*	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		AUTO_BPP	RSVD	RSVD[1:0]	
0x111	0x58	VIDEO_TX1[7:0]*	RSVD[1:0]		BPP[5:0]					
0x112	0x0A	VIDEO_TX2[7:0]*	PCLKDET	DRIFT_ERR	OVERFLOW	FIFO_WARN	RSVD	LIM_HEART	RSVD	RSVD
0x116	0x00	VIDEO_TX6[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
VID_TX U										
0x118	0x68	VIDEO_TX0[7:0]*	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		AUTO_BPP	RSVD	RSVD[1:0]	
0x119	0x58	VIDEO_TX1[7:0]*	RSVD[1:0]		BPP[5:0]					
0x11A	0x0A	VIDEO_TX2[7:0]*	PCLKDET	DRIFT_ERR	OVERFLOW	FIFO_WARN	RSVD	LIM_HEART	RSVD	RSVD
0x11E	0x00	VIDEO_TX6[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
SPI										
0x170	0x08	SPI_0[7:0]*	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
0x171	0x1D	SPI_1[7:0]*	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	

ADDRESS	RESET	NAME	MSB							LSB
0x172	0x03	SPI_2[7:0]*	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
0x173	0x00	SPI_3[7:0]*	SPIM_SS_DLY_CLKS[7:0]							
0x174	0x00	SPI_4[7:0]*	SPIM_SCK_LO_CLKS[7:0]							
0x175	0x00	SPI_5[7:0]*	SPIM_SCK_HI_CLKS[7:0]							
0x176	0x00	SPI_6[7:0]*	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
0x177	0x00	SPI_7[7:0]	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
0x178	0x00	SPI_8[7:0]*	REQ_HOLD_OFF_TO[7:0]							
WM										
0x190	0x00	WM_0[7:0]*	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		–	WM_EN
0x192	0x50	WM_2[7:0]*	–	RSVD[2:0]			HsyncPol	VsyncPol	WM_NPFILT[1:0]	
0x193	0x14	WM_3[7:0]*	–	WM_TH[6:0]						
0x194	0x10	WM_4[7:0]*	–	–	RSVD[1:0]		WM_COLORADJ	–	WM_MASKMODE[1:0]	
0x195	0x00	WM_5[7:0]	–	–	–	–	–	RSVD	RSVD	WM_ERROR
0x196	0x00	WM_6[7:0]	WM_TIMER[7:0]							
0x1AE	0x00	WM_WREN_0[7:0]	WM_WREN_L[7:0]							
0x1AF	0x00	WM_WREN_1[7:0]	WM_WREN_H[7:0]							
GPIO 0										
0x2BE	0x1C	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2BF	0x40	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C0	0x40	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO1 1										
0x2C1	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C2	0x21	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C3	0x41	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO2 2										
0x2C4	0x99	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C5	0x22	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C6	0x42	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
GPIO3 3										
0x2C7	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C8	0x23	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C9	0x43	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO4 4										
0x2CA	0x99	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2CB	0x24	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2CC	0x44	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO5 5										
0x2CD	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2CE	0x25	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2CF	0x45	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO6 6										
0x2D0	0x99	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2D1	0x26	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2D2	0x46	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO7 7										
0x2D3	0x83	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2D4	0xA7	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2D5	0x47	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO8 8										
0x2D6	0x9C	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2D7	0xA8	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2D8	0x48	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO9 9										
0x2D9	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2DA	0x29	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x2DB	0x49	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO10 10										
0x2DC	0x99	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2DD	0x2A	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2DE	0x4A	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO11 11										
0x2DF	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2E0	0x2B	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2E1	0x4B	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO12 12										
0x2E2	0x99	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2E3	0x2C	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2E4	0x4C	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO13 13										
0x2E5	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2E6	0x2D	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2E7	0x4D	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO14 14										
0x2E8	0x99	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2E9	0x2E	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2EA	0x4E	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO15 15										
0x2EB	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2EC	0x2F	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2ED	0x4F	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO16 16										
0x2EE	0x99	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS

ADDRESS	RESET	NAME	MSB							LSB
0x2EF	0x30	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2F0	0x50	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
CMU										
0x304	0xAB	CMU4[7:0]	A_SPEED[1:0]		B_SPEED[1:0]		RSVD[1:0]		D_SPEED[1:0]	
FRONTTOP										
0x308	0x7C	FRONTTOP_0[7:0]*	RSVD	enable_line_info	START_PORTB	START_PORTA	CLK_SELU	CLK_SELZ	CLK_SELY	CLK_SELX
0x309	0xFF	FRONTTOP_1[7:0]*	VC_SELX_L[7:0]							
0x30B	0xFF	FRONTTOP_3[7:0]*	VC_SELY_L[7:0]							
0x30D	0xFF	FRONTTOP_5[7:0]*	VC_SELZ_L[7:0]							
0x30F	0xFF	FRONTTOP_7[7:0]*	VC_SELU_L[7:0]							
0x311	0x55	FRONTTOP_9[7:0]*	START_PORTBU	START_PORTBZ	START_PORTBY	START_PORTBX	START_PORTAU	START_PORTAZ	START_PORTAY	START_PORTAX
0x312	0x00	FRONTTOP_10[7:0]*	RSVD	RSVD	RSVD	RSVD	bpp8dblu	bpp8dblz	bpp8dbly	bpp8dblx
0x313	0x00	FRONTTOP_11[7:0]*	bpp12dblu	bpp12dblz	bpp12dbly	bpp12dblx	bpp10dblu	bpp10dblz	bpp10dbly	bpp10dblx
0x314	0x00	FRONTTOP_12[7:0]	RSVD	mem_dt1_selx[6:0]						
0x315	0x00	FRONTTOP_13[7:0]	RSVD	mem_dt2_selx[6:0]						
0x316	0x00	FRONTTOP_14[7:0]	–	mem_dt1_sely[6:0]						
0x317	0x00	FRONTTOP_15[7:0]	–	mem_dt2_sely[6:0]						
0x318	0x00	FRONTTOP_16[7:0]	–	mem_dt1_selz[6:0]						
0x319	0x00	FRONTTOP_17[7:0]	–	mem_dt2_selz[6:0]						
0x31A	0x00	FRONTTOP_18[7:0]	–	mem_dt1_selu[6:0]						
0x31B	0x00	FRONTTOP_19[7:0]	–	mem_dt2_selu[6:0]						
0x31C	0x18	FRONTTOP_20[7:0]	soft_dtx_en	soft_vcx_en	soft_bppx_en	soft_bppx[4:0]				
0x31D	0x18	FRONTTOP_21[7:0]	soft_dty_en	soft_vcy_en	soft_bppy_en	soft_bppy[4:0]				
0x31E	0x18	FRONTTOP_22[7:0]	soft_dtz_en	soft_vcz_en	soft_bppz_en	soft_bppz[4:0]				
0x31F	0x18	FRONTTOP_23[7:0]	soft_dtu_en	soft_vcu_en	soft_bppu_en	soft_bppu[4:0]				
0x320	0x00	FRONTTOP_24[7:0]	soft_vcu[1:0]		soft_vcz[1:0]		soft_vcy[1:0]		soft_vcx[1:0]	

ADDRESS	RESET	NAME	MSB							LSB
0x321	0x30	FRONTTOP_25[7:0]	–	–	soft_dtx[5:0]					
0x322	0x30	FRONTTOP_26[7:0]	–	–	soft_dty[5:0]					
0x323	0x30	FRONTTOP_27[7:0]	–	–	soft_dtz[5:0]					
0x324	0x30	FRONTTOP_28[7:0]	–	–	soft_dtu[5:0]					
MIPI_RX										
0x330	0x00	MIPI_RX0[7:0]*	RSVD	–	ctrl1_vc_map_en	ctrl0_vc_map_en	mipi_rx_reset	phy_config[2:0]		
0x331	0x33	MIPI_RX1[7:0]*	RSVD	ctrl1_deskewen	ctrl1_num_lanes[1:0]		RSVD	ctrl0_deskewen	ctrl0_num_lanes[1:0]	
0x332	0xEE	MIPI_RX2[7:0]*	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
0x333	0xE4	MIPI_RX3[7:0]*	phy3_lane_map[3:0]				phy2_lane_map[3:0]			
0x334	0x00	MIPI_RX4[7:0]*	–	phy1_pol_map[2:0]			–	phy0_pol_map[2:0]		
0x335	0x00	MIPI_RX5[7:0]*	–	phy3_pol_map[2:0]			–	phy2_pol_map[2:0]		
0x338	0x55	MIPI_RX8[7:0]	RSVD[1:0]		t_hs_settle[1:0]		t_clk_miss[1:0]		t_clk_settle[1:0]	
0x339	0x00	MIPI_RX9[7:0]	–	–	–	phy0_lp_err[4:0]				
0x33A	0x00	MIPI_RX10[7:0]	phy0_hs_err[7:0]							
0x33B	0x00	MIPI_RX11[7:0]	–	–	–	phy1_lp_err[4:0]				
0x33C	0x00	MIPI_RX12[7:0]	phy1_hs_err[7:0]							
0x33D	0x00	MIPI_RX13[7:0]	–	–	–	phy2_lp_err[4:0]				
0x33E	0x00	MIPI_RX14[7:0]	phy2_hs_err[7:0]							
0x33F	0x00	MIPI_RX15[7:0]	–	–	–	phy3_lp_err[4:0]				
0x340	0x00	MIPI_RX16[7:0]	phy3_hs_err[7:0]							
0x341	0x00	MIPI_RX17[7:0]	ctrl0_csi_err_l[7:0]							
0x342	0x00	MIPI_RX18[7:0]	–	–	–	–	–	ctrl0_csi_err_h[2:0]		
0x343	0x00	MIPI_RX19[7:0]	ctrl1_csi_err_l[7:0]							
0x344	0x00	MIPI_RX20[7:0]	–	–	–	–	–	ctrl1_csi_err_h[2:0]		
0x345	0x00	MIPI_RX21[7:0]*	ctrl1_vc_map0[3:0]				ctrl0_vc_map0[3:0]			

ADDRESS	RESET	NAME	MSB							LSB
0x346	0x00	MIPI_RX22[7:0]*	ctrl1_vc_map1[3:0]				ctrl0_vc_map1[3:0]			
0x347	0x00	MIPI_RX23[7:0]	ctrl1_vc_map2[3:0]				ctrl0_vc_map2[3:0]			
0x36C	0x00	MIPI_RX60[7:0]	ctrl1_vc_map3[3:0]				ctrl0_vc_map3[3:0]			
FRONTTOP_EXT										
0x3C0	0x00	FRONTTOP_EXT0[7:0]	mem_dt3_selx[7:0]							
0x3C1	0x00	FRONTTOP_EXT1[7:0]	mem_dt4_selx[7:0]							
0x3C2	0x00	FRONTTOP_EXT2[7:0]	mem_dt5_selx[7:0]							
0x3C3	0x00	FRONTTOP_EXT3[7:0]	mem_dt6_selx[7:0]							
0x3C4	0x00	FRONTTOP_EXT4[7:0]	mem_dt3_sely[7:0]							
0x3C5	0x00	FRONTTOP_EXT5[7:0]	mem_dt4_sely[7:0]							
0x3C6	0x00	FRONTTOP_EXT6[7:0]	mem_dt5_sely[7:0]							
0x3C7	0x00	FRONTTOP_EXT7[7:0]	mem_dt6_sely[7:0]							
0x3C8	0x00	FRONTTOP_EXT8[7:0]	mem_dt3_selz[7:0]							
0x3C9	0x00	FRONTTOP_EXT9[7:0]	mem_dt4_selz[7:0]							
0x3CA	0x00	FRONTTOP_EXT10[7:0]	mem_dt5_selz[7:0]							
0x3CB	0x00	FRONTTOP_EXT11[7:0]	mem_dt6_selz[7:0]							
0x3CC	0x00	FRONTTOP_EXT12[7:0]	mem_dt3_selu[7:0]							
0x3CD	0x00	FRONTTOP_EXT13[7:0]	mem_dt4_selu[7:0]							
0x3CE	0x00	FRONTTOP_EXT14[7:0]	mem_dt5_selu[7:0]							
0x3CF	0x00	FRONTTOP_EXT15[7:0]	mem_dt6_selu[7:0]							
0x3D0	0x00	FRONTTOP_EXT16[7:0]	mem_dt6_sely_en	mem_dt5_sely_en	mem_dt4_sely_en	mem_dt3_sely_en	mem_dt6_selx_en	mem_dt5_selx_en	mem_dt4_selx_en	mem_dt3_selx_en
0x3D1	0x00	FRONTTOP_EXT17[7:0]	mem_dt6_selu_en	mem_dt5_selu_en	mem_dt4_selu_en	mem_dt3_selu_en	mem_dt6_selz_en	mem_dt5_selz_en	mem_dt4_selz_en	mem_dt3_selz_en
MIPI_RX_EXT2										
0x3D8	0x00	EXT6[7:0]	–	mem_dt7_selx[6:0]						
0x3D9	0x00	EXT7[7:0]	–	mem_dt8_selx[6:0]						
0x3DA	0x00	EXT8[7:0]	–	mem_dt7_sely[6:0]						
0x3DB	0x00	EXT9[7:0]	–	mem_dt8_sely[6:0]						

ADDRESS	RESET	NAME	MSB							LSB
0x3DC	0x00	EXTA[7:0]	–	mem_dt7_selz[6:0]						
0x3DD	0x00	EXTB[7:0]	–	mem_dt8_selz[6:0]						
0x3DE	0x00	EXTC[7:0]	–	mem_dt7_selu[6:0]						
0x3DF	0x00	EXTD[7:0]	–	mem_dt8_selu[6:0]						
REF_VTG										
0x3F0	0x58	REF_VTG0[7:0]	REFGEN_LOCKED	REFGEN_PREDEF_EN	REFGEN_PREDEF_FREQ[1:0]		REFGEN_PREDEF_FREQ_ALT	–	REFGEN_RST	REFGEN_EN
0x3F4	0x00	REF_VTG4[7:0]	REFGEN_FB_FRACT_L[7:0]							
0x3F5	0x00	REF_VTG5[7:0]	–	–	–	–	REFGEN_FB_FRACT_H[3:0]			
GMSL1										
0x402	0x00	GMSL1_2[7:0]*	–	–	SSEN	–	–	–	–	–
0x404	0x83	GMSL1_4[7:0]*	SEREN	CLINKEN	PRBSEN	–	–	–	REVCCEN	FWDCCEN
0x405	0x00	GMSL1_5[7:0]*	–	–	PRBS_LEN[1:0]		–	–	–	–
0x407	0x00	GMSL1_7[7:0]*	DBL	HIBW	BWS	–	DRS	HVEN	–	PXL_CRC
0x40D	0x00	GMSL1_D[7:0]*	I2C_LOC_ACK	–	–	–	–	–	–	–
0x40F	0x7C	GMSL1_F[7:0]*	CNTL_IN_EN[4:0]					GPO_RX_EN	GPO_OUT_SEL	SET_GPO
0x411	0x00	GMSL1_11[7:0]*	ERRG_RATE2[1:0]		ERRG_TYPE2[1:0]		ERRG_CNT2[1:0]		ERRG_PER2	ERRG_EN
0x412	0x00	GMSL1_12[7:0]*	–	–	–	–	–	CNTL_IN_ORD[2:0]		
0x413	0x00	GMSL1_13[7:0]*	RSVD	ALLOW_PKTCC	–	RSVD	RSVD	RSVD	–	–
0x414	0x00	GMSL1_14[7:0]	–	–	–	I2C_TIMED_OUT2	CC_WBLOCK_LOST	REV_BIT_LOCK	CC_WBLOCK	REM_CCLOCK
0x415	0x03	GMSL1_15[7:0]*	–	–	–	–	–	–	SEL_VESA	SEL_RGB888
0x416	0x00	GMSL1_16[7:0]	–	MAX_RT_ERR	–	–	–	–	–	–
0x41C	0x00	GMSL1_18[7:0]	CC_I2C_RETR_CNT[7:0]							
0x41D	0x00	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0x438	0x18	GMSL1_39[7:0]	–	CROSS24_I	CROSS24_F	CROSS24[4:0]				
0x439	0x19	GMSL1_3A[7:0]	–	CROSS25_I	CROSS25_F	CROSS25[4:0]				
0x43A	0x1A	GMSL1_3B[7:0]	–	CROSS26_I	CROSS26_F	CROSS26[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x43B	0x1B	GMSL1_3C[7:0]	–	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x43C	0x1C	GMSL1_3D[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x43D	0x1D	GMSL1_3E[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
0x43E	0x1E	GMSL1_3F[7:0]	–	CROSS30_I	CROSS30_F	CROSS30[4:0]				
0x442	0x5B	GMSL1_42[7:0]*	RSVD[1:0]		–	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	GPO_EN
0x44D	0x00	GMSL1_4D[7:0]	HIGHIMM	–	–	–	–	–	–	–
0x466	0x60	GMSL1_66[7:0]*	RSVD[1:0]		PRBS_TYPE	REV_FAST	DIS_DE	–	–	–
0x467	0x07	GMSL1_67[7:0]*	CNTL_TRIG[1:0]		AUTO_CLINK	DE_RGB888_DBL	–	DBL_ALIGN_TO[2:0]		
0x468	0x19	GMSL1_68[7:0]*	–	RSVD[2:0]			RSVD[1:0]		CC_CRC_LENGTH[1:0]	
0x496	0x02	GMSL1_96[7:0]*	RSVD	–	–	–	BYPASS_HVD_ALIGN	–	RSVD[1:0]	
0x499	0x0C	GMSL1_99[7:0]*	RSVD	–	RSVD	REV_FILT_EN	ALIGN_VS_MODE	ALIGN_INFO	–	–
0x49A	0x10	GMSL1_9A[7:0]*	–	–	RSVD[1:0]		PKTCC_EN	RSVD[1:0]		RSVD
0x4C8	0x00	GMSL1_C8[7:0]	–	ALIGNING	I2C_ACK_RECVED	I2C_ACK_ACKED	–	–	–	–
AFE										
0x500	0x00	ADC_CTRL_0[7:0]	buf_bypass	RSVD	RSVD	adc_chgpump_pu	adc_refbuf_pu	buf_pu	adc_pu	cpu_adc_start
0x501	0x00	ADC_CTRL_1[7:0]	adc_chsel[3:0]				adc_clk_en	adc_refsel	adc_scale	adc_refscl
0x502	0x00	ADC_CTRL_2[7:0]	RSVD	–	RSVD	RSVD	adc_div[1:0]		adc_xref	Inmux_en
0x503	0x0A	ADC_CTRL_3[7:0]	AfePwrUpDly[7:0]							
0x504	0x00	ADC_STATUS0[7:0]	–	–	–	–	–	–	–	adc_active
0x508	0x00	ADC_DATA0[7:0]	adc_data_l[7:0]							
0x509	0x00	ADC_DATA1[7:0]	–	–	–	–	–	–	adc_data_h[1:0]	
0x50C	0x00	ADC_INTRIE0[7:0]	–	–	–	adc_overflow_ie	adc_lo_limit_ie	adc_hi_limit_ie	adc_ref_ready_ie	adc_done_ie
0x50D	0x00	ADC_INTRIE1[7:0]	ch7_hi_limit_ie	ch6_hi_limit_ie	ch5_hi_limit_ie	ch4_hi_limit_ie	ch3_hi_limit_ie	ch2_hi_limit_ie	ch1_hi_limit_ie	ch0_hi_limit_ie
0x50E	0x00	ADC_INTRIE2[7:0]	ch7_lo_limit_ie	ch6_lo_limit_ie	ch5_lo_limit_ie	ch4_lo_limit_ie	ch3_lo_limit_ie	ch2_lo_limit_ie	ch1_lo_limit_ie	ch0_lo_limit_ie

ADDRESS	RESET	NAME	MSB							LSB
0x50F	0x00	ADC_INTRIE3[7:0]	–	–	–	–	–	–	–	invalid_ch_sel_ie
0x510	0x00	ADC_INTR0[7:0]	–	–	–	adc_overflow_if	adc_lo_limit_if	adc_hi_limit_if	adc_ref_ready_if	adc_done_if
0x511	0x00	ADC_INTR1[7:0]	ch7_hi_limit_if	ch6_hi_limit_if	ch5_hi_limit_if	ch4_hi_limit_if	ch3_hi_limit_if	ch2_hi_limit_if	ch1_hi_limit_if	ch0_hi_limit_if
0x512	0x00	ADC_INTR2[7:0]	ch7_lo_limit_if	ch6_lo_limit_if	ch5_lo_limit_if	ch4_lo_limit_if	ch3_lo_limit_if	ch2_lo_limit_if	ch1_lo_limit_if	ch0_lo_limit_if
0x513	0x00	ADC_INTR3[7:0]	–	–	–	–	–	–	–	invalid_ch_sel_if
0x514	0x00	ADC_LIMIT0_0[7:0]	chLoLimit_l0[7:0]							
0x515	0xF0	ADC_LIMIT0_1[7:0]	chHiLimit_l0[3:0]				–	–	chLoLimit_h0[1:0]	
0x516	0x3F	ADC_LIMIT0_2[7:0]	–	–	chHiLimit_h0[5:0]					
0x517	0x03	ADC_LIMIT0_3[7:0]	–	–	div_sel0[1:0]		ch_sel0[3:0]			
0x518	0x00	ADC_LIMIT1_0[7:0]	chLoLimit_l1[7:0]							
0x519	0xF0	ADC_LIMIT1_1[7:0]	chHiLimit_l1[3:0]				–	–	chLoLimit_h1[1:0]	
0x51A	0x3F	ADC_LIMIT1_2[7:0]	–	–	chHiLimit_h1[5:0]					
0x51B	0x03	ADC_LIMIT1_3[7:0]	–	–	div_sel1[1:0]		ch_sel1[3:0]			
0x51C	0x00	ADC_LIMIT2_0[7:0]	chLoLimit_l2[7:0]							
0x51D	0xF0	ADC_LIMIT2_1[7:0]	chHiLimit_l2[3:0]				–	–	chLoLimit_h2[1:0]	
0x51E	0x3F	ADC_LIMIT2_2[7:0]	–	–	chHiLimit_h2[5:0]					
0x51F	0x03	ADC_LIMIT2_3[7:0]	–	–	div_sel2[1:0]		ch_sel2[3:0]			
0x520	0x00	ADC_LIMIT3_0[7:0]	chLoLimit_l3[7:0]							
0x521	0xF0	ADC_LIMIT3_1[7:0]	chHiLimit_l3[3:0]				–	–	chLoLimit_h3[1:0]	
0x522	0x3F	ADC_LIMIT3_2[7:0]	–	–	chHiLimit_h3[5:0]					
0x523	0x03	ADC_LIMIT3_3[7:0]	–	–	div_sel3[1:0]		ch_sel3[3:0]			
0x524	0x00	ADC_LIMIT4_0[7:0]	chLoLimit_l4[7:0]							
0x525	0xF0	ADC_LIMIT4_1[7:0]	chHiLimit_l4[3:0]				–	–	chLoLimit_h4[1:0]	
0x526	0x3F	ADC_LIMIT4_2[7:0]	–	–	chHiLimit_h4[5:0]					
0x527	0x03	ADC_LIMIT4_3[7:0]	–	–	div_sel4[1:0]		ch_sel4[3:0]			

ADDRESS	RESET	NAME	MSB							LSB
0x528	0x00	ADC_LIMIT5_0[7:0]	chLoLimit_l5[7:0]							
0x529	0xF0	ADC_LIMIT5_1[7:0]	chHiLimit_l5[3:0]				–	–	chLoLimit_h5[1:0]	
0x52A	0x3F	ADC_LIMIT5_2[7:0]	–	–	chHiLimit_h5[5:0]					
0x52B	0x03	ADC_LIMIT5_3[7:0]	–	–	div_sel5[1:0]		ch_sel5[3:0]			
0x52C	0x00	ADC_LIMIT6_0[7:0]	chLoLimit_l6[7:0]							
0x52D	0xF0	ADC_LIMIT6_1[7:0]	chHiLimit_l6[3:0]				–	–	chLoLimit_h6[1:0]	
0x52E	0x3F	ADC_LIMIT6_2[7:0]	–	–	chHiLimit_h6[5:0]					
0x52F	0x03	ADC_LIMIT6_3[7:0]	–	–	div_sel6[1:0]		ch_sel6[3:0]			
0x530	0x00	ADC_LIMIT7_0[7:0]	chLoLimit_l7[7:0]							
0x531	0xF0	ADC_LIMIT7_1[7:0]	chHiLimit_l7[3:0]				–	–	chLoLimit_h7[1:0]	
0x532	0x3F	ADC_LIMIT7_2[7:0]	–	–	chHiLimit_h7[5:0]					
0x533	0x03	ADC_LIMIT7_3[7:0]	–	–	div_sel7[1:0]		ch_sel7[3:0]			
0x534	0x00	ADC_RR_CTRL0[7:0]	–	–	–	–	–	–	–	adc_rr_run
0x536	0x00	ADC_RR_CTRL2[7:0]	adc_rr_sleep_l[7:0]							
0x537	0x00	ADC_RR_CTRL3[7:0]	adc_rr_sleep_h[7:0]							
0x53E	0x00	ADC_CTRL_4[7:0]	–	–	–	–	–	adc_pin_en[2:0]		
MISC										
0x548	0xDC	UART_PT_0[7:0]*	BITLEN_PT_1_L[7:0]							
0x549	0x05	UART_PT_1[7:0]*	–	–	BITLEN_PT_1_H[5:0]					
0x54A	0xDC	UART_PT_2[7:0]*	BITLEN_PT_2_L[7:0]							
0x54B	0x05	UART_PT_3[7:0]*	–	–	BITLEN_PT_2_H[5:0]					
0x550	0x00	I2C_PT_4[7:0]	SRC_A_1[6:0]							–
0x551	0x00	I2C_PT_5[7:0]	DST_A_1[6:0]							–
0x552	0x00	I2C_PT_6[7:0]	SRC_B_1[6:0]							–
0x553	0x00	I2C_PT_7[7:0]	DST_B_1[6:0]							–

ADDRESS	RESET	NAME	MSB							LSB
0x554	0x00	I2C_PT_8[7:0]	SRC_A_2[6:0]							–
0x555	0x00	I2C_PT_9[7:0]	DST_A_2[6:0]							–
0x556	0x00	I2C_PT_10[7:0]	SRC_B_2[6:0]							–
0x557	0x00	I2C_PT_11[7:0]	DST_B_2[6:0]							–
0x55D	0x00	HS_VS_X[7:0]	–	DE_DET_X	VS_DET_X	HS_DET_X	–	–	VS_POL_X	HS_POL_X
0x55E	0x00	HS_VS_Y[7:0]	–	DE_DET_Y	VS_DET_Y	HS_DET_Y	–	–	VS_POL_Y	HS_POL_Y
0x55F	0x00	HS_VS_Z[7:0]	–	DE_DET_Z	VS_DET_Z	HS_DET_Z	–	–	VS_POL_Z	HS_POL_Z
0x56A	0x00	HS_VS_U[7:0]	–	DE_DET_U	VS_DET_U	HS_DET_U	–	–	VS_POL_U	HS_POL_U
0x56C	0x05	PM_OV_STAT[7:0]	–	–	–	–	RSVD[1:0]		OV_LEVEL[1:0]	
MIPI_RX_EXT3										
0x580	0x00	EXT0[7:0]	ctrl0_fs_cnt_l[7:0]							
0x581	0x00	EXT1[7:0]	ctrl0_fs_cnt_h[7:0]							
0x582	0x00	EXT2[7:0]	ctrl0_fe_cnt_l[7:0]							
0x583	0x00	EXT3[7:0]	ctrl0_fe_cnt_h[7:0]							
0x584	0x00	EXT4[7:0]	ctrl1_fs_cnt_l[7:0]							
0x585	0x00	EXT5[7:0]	ctrl1_fs_cnt_h[7:0]							
0x586	0x00	EXT6[7:0]	ctrl1_fe_cnt_l[7:0]							
0x587	0x00	EXT7[7:0]	ctrl1_fe_cnt_h[7:0]							
0x588	0x00	EXT8[7:0]	ctrl0_fs_vc_sel[3:0]				ctrl1_fs_vc_sel[3:0]			
SPI_CC_WR										
0x1300	0x00	SPI_CC_WR_[7:0]	–	–	–	–	–	–	–	–
SPI_CC_RD										
0x1380	0x00	SPI_CC_RD_[7:0]	–	–	–	–	–	–	–	–
RLMS A										
0x1403	0x0A	RLMS3[7:0]	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
0x1404	0x29	RLMS4[7:0]*	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1405	0x10	RLMS5[7:0]*	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1406	0x80	RLMS6[7:0]*	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x1407	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x1434	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x1435	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x1437	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMon Done	EyeMon CntClr	EyeMon Start	EyeMon Ph	EyeMon DPol
0x1438	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							
0x1439	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x143A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x143B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x143D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							RSVD
0x143E	0xBA	RLMS3E[7:0]	ErrChPh SecTA	ErrChPhSec[6:0]						
0x143F	0x79	RLMS3F[7:0]	ErrChPh PriTA	ErrChPhPri[6:0]						
0x1449	0x71	RLMS49[7:0]	–	RSVD	RSVD	RSVD	RSVD	ErrChPw rUp	–	RSVD
0x1458	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x1459	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x1464	0x00	RLMS64[7:0]*	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
0x1470	0x01	RLMS70[7:0]*	–	TxSSCFrqCtrl[6:0]						
0x1471	0x02	RLMS71[7:0]*	–	TxSSCCenSprSt[5:0]						TxSSCE n
0x1472	0xCF	RLMS72[7:0]*	TxSSCPreSclL[7:0]							
0x1473	0x00	RLMS73[7:0]*	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1474	0x00	RLMS74[7:0]*	TxSSCPhL[7:0]							
0x1475	0x00	RLMS75[7:0]*	–	TxSSCPhH[6:0]						
0x1476	0x00	RLMS76[7:0]*	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x1495	0x69	RLMS95[7:0]	TxAmpl ManEn	RSVD	TxAmplMan[5:0]					
0x14A4	0xC8	RLMSA4[7:0]*	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
0x14AC	0xCD	RLMSAC[7:0]	ErrChPh SecTAF R3G	ErrChPhSecFR3G[6:0]						
0x14AD	0x0D	RLMSAD[7:0]	ErrChPh PriTAFR 3G	ErrChPhPriFR3G[6:0]						
0x14B6	0xBB	RLMSB6[7:0]	ErrChPh SecTAS RG1875	ErrChPhSecSRG1875[6:0]						
0x14B7	0x7A	RLMSB7[7:0]	ErrChPh PriTASR G1875	ErrChPhPriSRG1875[6:0]						
DPLL REF										
0x1A00	0xF5	DPLL_0[7:0]*	config_m ain_state _machin e_enable _fref_cal _ss	config_m ain_state _machin e_enable _coarse_ cal	config_m ain_state _machin e_enable _divide_ cal	config_m ain_state _machin e_enable _fref_cal	config_fo rce_enab le	config_e nable_fu nc_clk	config_e nable_co nfig_clk	config_s oft_rst_n

ADDRESS	RESET	NAME	MSB							LSB
0x1A01	0xEF	DPLL_1[7:0]*	config_enable_fref_cal	config_enable_integ_delta_sigma	config_enable_divider_delta_sigma	config_main_state_machine_force_recal	config_main_state_machine_enable_fref_recal_ss	config_main_state_machine_enable_coarse_recal	config_main_state_machine_enable_divide_recal	config_main_state_machine_enable_fref_recal
0x1A02	0x3F	DPLL_2[7:0]*	config_triangle_wave_freq_multiplier[1:0]		config_enable_triangle_wave	config_enable_integ_controller	config_enable_freq_divider_cal	config_enable_state_machine	config_enable_freq_lock_coarse	config_enable_fb_tune
0x1A03	0x82	DPLL_3[7:0]*	RSVD	RSVD	RSVD	RSVD	config_force_enable_ss	config_spread_bit_ratio[2:0]		
0x1A04	0x37	DPLL_4[7:0]	config_fref_cal_timer_max_ss_L[7:0]							
0x1A05	0x00	DPLL_5[7:0]	config_testout_address[4:0]					config_fref_cal_timer_max_ss_H[2:0]		
0x1A06	0x28	DPLL_6[7:0]	config_fref_cal_timer_max_L[7:0]							
0x1A07	0x04	DPLL_7[7:0]	config_div_fb_L	config_div_in[4:0]					config_fref_cal_timer_max_H[1:0]	
0x1A08	0x14	DPLL_8[7:0]	config_div_fb_H[7:0]							
0x1A09	0x40	DPLL_9[7:0]	config_div_out_L[4:0]					config_div_fb_exp[2:0]		
0x1A0A	0x81	DPLL_10[7:0]	config_allow_coarse_change	config_div_out_exp[2:0]			config_div_out_H[3:0]			
0x1A0C	0x54	DPLL_12[7:0]	config_int_gain2[3:0]				config_int_gain1[3:0]			
0x1A0D	0xA8	DPLL_13[7:0]	config_int_gain4[3:0]				config_int_gain3[3:0]			
0x1A0E	0x8C	DPLL_14[7:0]	config_dac_fine_filter_bw[3:0]				config_int_gain5[3:0]			
0x1A0F	0x21	DPLL_15[7:0]	config_prop_gain1[4:0]					config_dac_prop_filter_bw[2:0]		
0x1A10	0x65	DPLL_16[7:0]	config_prop_gain3_L[2:0]			config_prop_gain2[4:0]				
0x1A11	0x41	DPLL_17[7:0]	config_prop_gain5_L	config_prop_gain4[4:0]					config_prop_gain3_H[1:0]	
0x1A12	0x0B	DPLL_18[7:0]	config_prevent_unlock	config_force_pll_lock	config_prop_subgain[1:0]		config_prop_gain5_H[3:0]			
0x1A13	0x4E	DPLL_19[7:0]	config_div_ds_lowF[2:0]			config_force_div_ds_lowF	config_pll_lock_time[1:0]		config_pll_lock_thresh[1:0]	
0x1A14	0x83	DPLL_20[7:0]	config_pfd_delay_ctrl[1:0]		config_bbpd_mode[1:0]		config_force_disable_dcro	config_div_ds_highF[2:0]		
0x1A15	0x00	DPLL_21[7:0]	config_sel_clock_dsm	config_sel_clock_fb	config_int_divider3[1:0]		config_int_divider2[1:0]		config_int_divider1[1:0]	
0x1A16	0xC0	DPLL_22[7:0]	config_spare_ones_H[1:0]		config_shutdown	config_tdc_offset	config_use_internal_div_dsm	config_cdc_double_register	config_dac_coarse_bw_increase	config_en_clock_out_rf
0x1A17	0x06	DPLL_23[7:0]	config_spare_zeroes[3:0]				–	config_bbpd_gain[2:0]		

Register Details

REG0 (0x0)*

BIT	7	6	5	4	3	2	1	0
Field	DEV_ADDR[6:0]							CFG_BLOCK
Reset	0b1000000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ADDR	7:1	Device I2C address	0b0000000: I2C write/read address is 0x00/0x01 0b0000001: I2C write/read address is 0x02/0x03 ... ... 0b1000000: I2C write/read address is 0x80/0x81 0b1000010: I2C write/read address is 0x84/0x85 0b1000100: I2C write/read address is 0x88/0x89 0b1100000: I2C write/read address is 0xC0/0xC1 0b1100010: I2C write/read address is 0xC4/0xC5 0b1100100: I2C write/read address is 0xC8/0xC9 0b0100000: I2C write/read address is 0x40/0x41 0b0100010: I2C write/read address is 0x44/0x45 ... ... 0b1111111: I2C write/read address is 0xFE/0xFF
CFG_BLOCK	0	Configuration Block When set, all registers become non-writable (read-only). This bit can be used to freeze the chip configuration.	0b0: Not Blocked 0b1: Blocked

REG1 (0x1)*

BIT	7	6	5	4	3	2	1	0
Field	IIC_2_EN	IIC_1_EN	DIS_LOCAL_CC	DIS_REM_CC	TX_RATE[1:0]		RSVD[1:0]	
Reset	0x0	0x0	0b0	0b0	0x2		0b0	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
IIC_2_EN	7	Enables pass-through I2C Channel 2 (SDA2/RX2, SCL2/TX2)	0b0: I2C pass-through Channel 2 disabled 0b1: I2C pass-through Channel 2 enabled
IIC_1_EN	6	Enables pass-through I2C Channel 1 (SDA1/RX1, SCL1/TX1)	0b0: I2C pass-through Channel 1 disabled 0b1: I2C pass-through Channel 1 enabled
DIS_LOCAL_CC	5	Disables control-channel connection to RX/SDA and TX/SCL pins	0b0: RX/SDA and TX/SCL connected to control channel 0b1: RX/SDA and TX/SCL disconnected from control channel
DIS_REM_CC	4	Disables remote control-channel link over GMSL2 connection	0b0: Remote control-channel enabled 0b1: Remote control-channel disabled

BITFIELD	BITS	DESCRIPTION	DECODE
TX_RATE	3:2	Transmitter (Forward Channel) Bit Rate When changed, becomes active after next link reset. Default value is set by the CFG1 pin at power-up.	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved

REG2 (0x2)*

BIT	7	6	5	4	3	2	1	0
Field	VID_TX_EN_U	VID_TX_EN_Z	VID_TX_EN_Y	VID_TX_EN_X	RSVD	RSVD	RSVD	RSVD
Reset	0x0	0x1	0x0	0x1	0x0	0x0	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
VID_TX_EN_U	7	Enables Video Transmit for Port U	0b0: Video transmit Channel U disabled 0b1: Video transmit Channel U enabled
VID_TX_EN_Z	6	Enables Video Transmit for Port Z	0b0: Video transmit Channel Z disabled 0b1: Video transmit Channel Z enabled
VID_TX_EN_Y	5	Enables Video Transmit for Port Y	0b0: Video transmit Channel Y disabled 0b1: Video transmit Channel Y enabled
VID_TX_EN_X	4	Enables Video Transmit for Port X	0b0: Video transmit Channel X disabled 0b1: Video transmit Channel X enabled

REG3 (0x3)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	UART_2_EN	UART_1_EN	RSVD	RSVD	RCLKSEL[1:0]	
Reset	–	–	0x0	0x0	0x0	0x0	0x0	
Access Type	–	–	Write, Read	Write, Read			Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
UART_2_EN	5	Enables pass-through UART Channel 2 (SDA2/RX2, SCL2/TX2)	0b0: Pass-through UART Channel 2 disabled 0b1: Pass-through UART Channel 2 enabled
UART_1_EN	4	Enables pass-through UART Channel 1 (SDA1/RX1, SCL1/TX1)	0b0: Pass-through UART Channel 1 disabled 0b1: Pass-through UART Channel 1 enabled
RCLKSEL	1:0	RCLKOUT Clock Selection	0b00: 25MHz 0b01: 12.5MHz 0b10: 6.25MHz 0b11: Reference PLL output

REG5 (0x5)*

BIT	7	6	5	4	3	2	1	0
Field	LOCK_EN	ERRB_EN	–	–	RSVD	RSVD	PU_LF1	PU_LF0
Reset	0x1	0x1	–	–	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	–	–			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_EN	7	Enables LOCK output Disabled by default (0b0). Ignore reset value listed above.	0b0: LOCK output disabled 0b1: LOCK output enabled
ERRB_EN	6	Enables ERRB output Disabled by default (0b0). Ignore reset value listed above.	0b0: ERRB output disabled 0b1: ERRB output enabled
PU_LF1	1	Powers up line-fault monitor 1	0b0: Line-fault monitor 1 disabled 0b1: Line-fault monitor 1 enabled
PU_LF0	0	Powers up line-fault monitor 0	0b0: Line-fault monitor 0 disabled 0b1: Line-fault monitor 0 enabled

REG6 (0x6)*

BIT	7	6	5	4	3	2	1	0
Field	GMSL2	–	RCLKEN	RSVD	RSVD[3:0]			
Reset	0b1	–	0b0	0x0	0x0			
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL2	7	GMSL1 / GMSL2 Selection Bit is set according to the latched GMSL2 pin value at power-up	0x0: GMSL1 0x1: GMSL2
RCLKEN	5	Enables RCLK output.	0b0: RCLK output disabled 0b1: RCLK output enabled

REG13 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0x9B							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	Device Identifier Ignore reset value listed above and refer instead to reset value listed in decode field, which corresponds to given part number.	0x95: MAX9295D

REG14 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				DEV_REV[3:0]			
Reset	0x0				0x0			
Access Type					Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_REV	3:0	Device Revision	0xX: Device revision number

REG15 (0xF)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD[1:0]		DV_CPBL_N	DUAL_CPBL_N	SPLTR_CPBL_N	RSVD
Reset	0x0	0x0	0x0		0x0	0x0	0x0	0x0
Access Type					Read Only	Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
DV_CPBL_N	3	Dual-View Video Capability	0b0: Dual-view video splitting is available 0b1: Dual-view video splitting is not available
DUAL_CPBL_N	2	Dual-Link Capability	0b0: Dual-link mode is available 0b1: Dual-link mode is not available
SPLTR_CPBL_N	1	Splitter Mode Capability	0b0: Splitter mode is available 0b1: Splitter mode is not available

REG26 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_1[2:0]			–	LF_0[2:0]		
Reset	–	0x2			–	0x2		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_1	6:4	Line-fault status of wire connected to LMN1 pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short
LF_0	2:0	Line-fault status of wire connected to LMN0 pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short

PWR0 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_STATUS	7:5	Power manager switched 1V supply comparator status bits	0bXX1: Latched high when V_{DDA_sw} < 0.82V 0bX1X: Latched high when V_{DD_sw} < 0.82V 0b1XX: Reserved
CMP_STATUS	4:0	Power manager comparator status bits	0bXXXX0: Latched low when V_{DD18} < 1.617V 0bXXX0X: Latched low when switched V_{DDIO} supply < 1.617V 0bXX0XX: Latched low when V_{DD_sw} < 0.82V 0bX0XXX: Reserved 0b0XXXX: Reserved

PWR4 (0xC)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	DIS_LOCAL_WAKE	RSVD	WAKE_EN_A	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b1	0xA			
Access Type		Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCAL_WAKE	6	Disable wake-up by local µC from SDA_RX pin	0b0: Local wake-up enabled 0b1: Local wake-up disabled
WAKE_EN_A	4	Enable wake-up by remote chip connected to Link A	0b0: Link A remote wake-up disabled 0b1: Link A remote wake-up enabled

CTRL0 (0x10)*

BIT	7	6	5	4	3	2	1	0
Field	RESET_ALL	RESET_LINK	RESET_ONESHOT	RSVD	SLEEP	REG_ENABLE	RSVD[1:0]	
Reset	0b0	0b0	0b0	0b1	0b0	0x0	0b01	
Access Type	Write, Read	Write, Read	Write Clears All, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	7	Device Reset Writing 1 to this bit resets the device (including all blocks) and resets registers to defaults. This is equivalent to toggling the PWDNB pin. The bit is cleared when written.	0b0: No action 0b1: Activate chip reset

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_LINK	6	Link Reset Resets entire data path (keep register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_ONESHOT	5	One-Shot Link Reset Resets entire data path (keep register settings) one shot. Write 1 to activate reset, bit self clears and automatically releases reset.	0b0: No action 0b1: Reset data path
SLEEP	3	Activates sleep mode	0b0: Sleep mode disabled 0b1: Sleep mode enabled
REG_ENABLE	2	Enables V_{DD} LDO regulator when used with REG_MNL (0x12)	0b0: V_{DD} LDO regulator disabled (bypassed) when REG_MNL = 1 0b1: V_{DD} LDO regulator enabled when REG_ENABLE = 1 and REG_MNL = 1. When V_{DD} = 1.2V, first set REG_ENABLE = 1, and then write REG_MNL = 1.

CTRL1 (0x11)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CXTP_A
Reset	0x0	0x0	0x0	0x0	0b1	0b0	0b1	0b0
Access Type								Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CXTP_A	0	Coax/Twisted-Pair Cable Select for Link A Bit is set according to the latched CFG1 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive

CTRL2 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	REG_MNL	RSVD[1:0]		RSVD[1:0]	
Reset	0x0	0b0	–	0b0	0x1		0x0	
Access Type			–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
REG_MNL	4	Enables LDO manual control via REG_ENABLE	0b0: V_{DD} LDO regulator range sensing on. 0b1: V_{DD} LDO regulator range sensing off. V_{DD} LDO regulator on/bypass state controlled by REG_ENABLE. When V_{DD} = 1.2V, enable V_{DD} LDO regulator by first setting REG_ENABLE = 1 and then setting REG_MNL = 1.

CTRL3 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD[1:0]		LOCKED	ERROR	CMU_LOCKED	–
Reset	0b0	0b0	0b01		0b0	0b0	0b0	–
Access Type					Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED	3	GMSL2 link lock (bidirectional)	0b0: GMSL2 link not locked 0b1: GMSL2 link locked
ERROR	2	Reflects error status (inverse of ERRB pin value)	0b0: ERRB not asserted (ERRB pin = 1) 0b1: ERRB asserted (ERRB pin = 0)
CMU_LOCKED	1	Clock multiplier unit (CMU) lock	0b0: CMU not locked 0b1: CMU locked

INTR0 (0x18)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
Reset	0b1	0b0	0b1	–	0b0	0x0		
Access Type				–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_ERR_RST_EN	3	Automatically resets DEC_ERR_A (0x22) and IDLE_ERR (0x24) bitfields after ERRB pin is asserted for 1µs	0b0: Autoreset disabled 0b1: Autoreset enabled
DEC_ERR_THR	2:0	Decoding and Idle Error-Reporting Threshold DEC_ERR_FLAG_A (0x1B) is asserted when DEC_ERR_A (0x22) ≥ DEC_ERR_THR. IDLE_ERR_FLAG (0x1B) is asserted when IDLE_ERR (0x24) ≥ DEC_ERR_THR.	0b000: 1 error 0b001: 2 errors 0b010: 4 errors 0b011: 8 errors 0b100: 16 errors 0b101: 32 errors 0b110: 64 errors 0b111: 128 errors

INTR1 (0x19)*

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
Reset	0x0				0b0	0x0		
Access Type	Write, Read				Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_EXP	7:4	Packet-Count Multiplier Exponent See the description of PKT_CNT bitfield (register CNT3).	0bXXX: PKT_CNT exponent

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_CNT_RST_EN	3	Automatically resets PKT_CNT bitfield (register CNT3) after ERRB pin is asserted for 1µs	0b0: Autoreset disabled 0b1: Autoreset enabled
PKT_CNT_THR	2:0	Packet count reporting threshold (see PKT_CNT description). PKT_CNT_FLAG is asserted when PKT_CNT ≥ PKT_CNT_THR.	0b000: 1 packet 0b001: 2 packets 0b010: 4 packets 0b011: 8 packets 0b100: 16 packets 0b101: 32 packets 0b110: 64 packets 0b111: 128 packets

INTR2 (0x1A)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_OEN	MEM_INT_ERR_OEN	LFLT_INT_OEN	IDLE_ERR_OEN	RSVD	DEC_ERR_OEN_A
Reset	0b0	0b0	0b0	0x0	0x1	0b0	0b1	0b1
Access Type			Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_OEN	5	Enables reporting of remote-error status (REM_ERR_FLAG - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
MEM_INT_ERR_OEN	4	Enables reporting of memory-error status (MEM_INT_ERR_FLAG - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LFLT_INT_OEN	3	Enables reporting of line-fault interrupt (LFLT_INT - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
IDLE_ERR_OEN	2	Enables reporting of idle-word errors (IDLE_ERR_FLAG - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_A	0	Enables reporting of decoding errors (DEC_ERR_FLAG_A - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR3 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_FLAG	MEM_INT_ERR_FLAG	LFLT_INT	IDLE_ERR_FLAG	RSVD	DEC_ERR_FLAG_A
Reset	0b0	0b0	0b0	0x0	0x0	0b0	0b0	0b0
Access Type			Read Only	Read Only	Read Only	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_FLAG	5	Received remote-side error status (inverse of remote side ERRB pin level). Clear ERRB pin of remote side to clear.	0b0: No remote-side error 0b1: Remote-side error
MEM_INT_ERR_FLAG	4	Memory-Error Status Read to clear.	0b0: No memory error 0b1: Memory error

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT	3	Line-Fault Interrupt Asserted when either line-fault monitor indicates a fault status. See LF_0 and LF_1 bitfields (0x26) for more information.	0b0: No line fault 0b1: Line fault
IDLE_ERR_FLAG	2	Idle-Word Error Flag Read the IDLE_ERR to clear. Asserted when IDLE_ERR (0x24) ≥ DEC_ERR_THR (0x18)	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_A	0	Decoding Error Flag for Link A Read DEC_ERR_A to clear. Asserted when DEC_ERR_A (0x22) ≥ DEC_ERR_THR (0x18)	0b0: Flag not asserted 0b1: Flag asserted

INTR4 (0x1C)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	EOM_ERR_OEN_A	VDD_OV_OEN	RSVD	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	WM_ERR_OEN
Reset	0b0	0b0	0x0	0b0	0b1	0b0	0b0	0b1
Access Type		Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_OEN_A	6	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_A - 0x1D) for Link A at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VDD_OV_OEN	5	Enables reporting of VDD overvoltage status (VDD_OD_FLAG - 0x1D) on ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
MAX_RT_OEN	3	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG - 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
RT_CNT_OEN	2	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG - 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
PKT_CNT_OEN	1	Enables reporting of packet count flag (PKT_CNT_FLAG - 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
WM_ERR_OEN	0	Enables reporting of watermark errors (WM_ERR_FLAG 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR5 (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	VDD_OV_FLAG	RSVD	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	WM_ERR_FLAG
Reset	0b0	0b0	0x0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Clears All		Read Only	Read Only	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_FLAG_B	7	Eye-opening monitor is below configured threshold for Link B	0b0: No EOM error on Link B 0b1: EOM error on Link B
EOM_ERR_FLAG_A	6	Eye-opening monitor is below configured threshold for Link A	0b0: No EOM error on Link A 0b1: EOM error on Link A
VDD_OV_FLAG	5	V_{DD} Overvoltage Indication This bit is set when V_{DD} exceeds the overvoltage threshold and does not clear until read. Additionally, read CMP_STATUS to clear. See OV_LEVEL (0x56C) bitfield for overvoltage threshold value.	0b0: V_{DD} overvoltage not detected 0b1: V_{DD} overvoltage detected
MAX_RT_FLAG	3	Combined ARQ Maximum Retransmission Limit Error Flag Asserted when any of the selected channels' ARQ retransmission limit is reached. Read MAX_RT_ERR register in CFG register blocks to clear. Selection is done by each channel's MAX_RT_ERR_OEN bitfield.	0b0: Flag not asserted 0b1: Flag asserted
RT_CNT_FLAG	2	Combined ARQ Retransmission Event Flag Asserted when any of the selected channels have done at least one ARQ retransmission. Read RT_CNT in CFG register blocks to clear. Selection is done by each channel's RT_CNT_OEN bitfield.	0b0: Flag not asserted 0b1: Flag asserted
PKT_CNT_FLAG	1	Packet Count Flag Read PKT_CNT to clear. Asserted when PKT_CNT ≥ PKT_CNT_THR.	0b0: Flag not asserted 0b1: Flag asserted
WM_ERR_FLAG	0	Watermark Error Flag Read to clear. Asserted when a watermark error is detected.	0b0: Flag not asserted 0b1: Flag asserted

INTR6 (0x1E)*

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_OEN	RSVD	VDDBAD_INT_OEN	–	–	ADC_INT_OEN	RSVD	MIPI_ERR_OEN
Reset	0x1	0x1	0x1	–	–	0b0	0b1	0x1
Access Type	Write, Read		Write, Read	–	–	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_OEN	7	Enables reporting of combined V_{DD} comparator output (VDDCMP_INT_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VDDBAD_INT_OEN	5	Enables reporting of VDDBAD interrupt (VDDBAD_INT_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
ADC_INT_OEN	2	Enables reporting of ADC interrupts (ADC_INT_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
MIPI_ERR_OEN	0	Enables reporting of MIPI Rx errors (MIPI_ERR_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR7 (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_FLAG	RSVD	VDDBAD_INT_FLAG	–	–	ADC_INT_FLAG	RSVD	MIPI_ERR_FLAG
Reset	0x0	0x0	0x0	–	–	0b0	0b0	0x0
Access Type	Read Clears All		Read Clears All	–	–	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_FLAG	7	Combined V_{DD} Comparator Output. Read to clear. Additionally, read CMP_STATUS to clear.	0b0: Flag not asserted 0b1: Flag asserted
VDDBAD_INT_FLAG	5	Combined V_{DDBAD} Indicator. Read to clear. Additionally, read CMP_STATUS to clear.	0b0: Flag not asserted 0b1: Flag asserted
ADC_INT_FLAG	2	ADC Interrupt	0b0: No ADC interrupt 0b1: ADC interrupt
MIPI_ERR_FLAG	0	MIPI Rx Error Flag Asserted when any of the following is asserted: phy0_hs_err [0],[1],[4],[5] phy1_hs_err [0],[1],[4],[5] phy2_hs_err [0],[1],[4],[5] phy3_hs_err [0],[1],[4],[5] ctrl0_csi_err_l [0],[1],[7] ctrl0_csi_err_h [0] ctrl1_csi_err_l [0],[1],[7] ctrl1_csi_err_h [0]	0b0: Flag not asserted 0b1: Flag asserted

INTR8 (0x20)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
Reset	0b1	–	–	0x1F				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_TX_EN	7	Transmit local-error status (inverse of ERRB pin level) to remote side through GPIO channel	0b0: Transmit error status disabled 0b1: Transmit error status enabled
ERR_TX_ID	4:0	GPIO ID used for transmitting ERR_TX	0bXXXXX: Value of GPIO ID for transmitting ERR_TX

INTR9 (0x21)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
Reset	0b1	0b1	–	0x1F				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN	7	Receive remote-error status (inverse of ERRB pin level) through GPIO channel	0b0: Receive error status disabled 0b1: Receive error status enabled
ERR_RX_ID	4:0	GPIO ID used for receiving ERR_RX	0bXXXXX: Value of GPIO ID for receiving ERR_TX

CNT0 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_A	7:0	Number of Decoding (Disparity) Errors Detected at Link A Resets after reading or with the rising edge of LOCK.	0xXX: Number of Link A decoding errors detected

CNT2 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR	7:0	Number of Idle-Word Errors Detected Resets after reading or with the rising edge of LOCK.	0xXX: Number of idle-word errors detected

CNT3 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT	7:0	Number of Received Packets of a Selected Type Packet type is selected with PKT_CNT_SEL (0x2C) bitfield. Reported packet count is a scaled value, such that actual packet count is ≥ PKT_CNT x ($2^{PKT\_CNT\_EXP}$) and < (PKT_CNT + 1) x ($2^{PKT\_CNT\_EXP}$). (PKT_CNT - 0x25, PXK_CNT_EXP - 0x19) When maximum value is reported, packet count is greater than or equal to the reported value.	0xXX: Scaled number of received packets

TX1 (0x29)*

BIT	7	6	5	4	3	2	1	0
Field	LINK_PRBS_GEN	–	RSVD	ERRG_EN_A	–	–	RSVD	RSVD
Reset	0x0	–	0x0	0x0	–	–	0x0	0x0
Access Type	Write, Read	–		Write, Read	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_PRBS_GEN	7	Enables link PRBS-7 generator	0b0: Link PRBS generator disabled 0b1: Link PRBS generator enabled
ERRG_EN_A	4	Enables error generator for Link A	0b0: Link A error generator disabled 0b1: Link A error generator enabled

TX2 (0x2A)*

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0x0		0x2		0x0			0x0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 0b10: 128 0b11: 1024
ERRG_RATE	5:4	Error generator average bit-error rate	0b00: 1 in 5120 bits 0b01: 1 in 81920 bits 0b10: 1 in 1310720 bits 0b11: 1 in 20971520 bits
ERRG_BURST	3:1	Error generator burst-error length	0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 8 0b101: 12 0b110: 16 0b111: 20
ERRG_PER	0	Error generator error-distribution selection	0b0: Pseudorandom 0b1: Periodic

TX3 (0x2B)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
Reset	0x1		–	–	–	0x4		
Access Type			–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TIMEOUT	2:0	ARQ Timeout Duration Multiplier When 12Gbps link is used, values 6 and 7 are reserved. Timeout Base = 8µs	0b000: 0.5 x Timeout base 0b001: 1.0 x Timeout base 0b010: 1.5 x Timeout base 0b011: 2.0 x Timeout base 0b100: 2.5 x Timeout base 0b101: 3.0 x Timeout base 0b110: 3.5 x Timeout base 0b111: 4.0 x Timeout base

RX0 (0x2C)*

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
Reset	0x0		–	0x0	0x0			
Access Type	Write, Read		–		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Selects the sub-type of low-bandwidth packets to count at PKT_CNT (0x25) bitfield	0b00: Count LBW data packets only 0b01: Count LBW acknowledge packets only 0b10: Count LBW data and acknowledge packets 0b11: Reserved
PKT_CNT_SEL	3:0	Selects the type of received packets to count at PKT_CNT (0x25) bitfield (selected packet type must be supported by device)	0x0: None 0x1: VIDEO 0x2: AUDIO 0x3: INFO Frame 0x4: SPI 0x5: I^2C 0x6: UART 0x7: GPIO 0x8: AHDCP 0x9: Reserved 0xA: Reserved 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: All 0xF: Unknown and packets with error

GPIOA (0x30)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RX_FAST_BIDIR_EN	RSVD	GPIO_FWD_CDLY[5:0]					
Reset	0x0	0x1	0x1					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_FAST_BIDIR_EN	7	GPIO fast direction switch for bidirectional IO	0b0: Fast direction switch disabled 0b1: Fast direction switch enabled
GPIO_FWD_CDLY	5:0	Compensation Delay Multiplier for the Forward Direction This must be the same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.	0bXXXXXX: Forward compensation delay multiplier value

GPIOB (0x31)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0x2		0x8					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait Time after a GPIO Transition to Create a Packet This allows grouping transitions of different GPIO inputs in a single packet and therefore increases GPIO bandwidth usage efficiency.	0b00: Disabled 0b01: 200ns 0b10: 500ns 0b11: 1000ns
GPIO_REV_CDLY	5:0	Compensation Delay Multiplier for the Reverse Direction This must be the same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse compensation delay multiplier value

I2C_0 (0x40)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH	5:4	I^2C-to-I^2C Subordinate-Setup and Hold-Time Setting. Configures the interval between SDA and SCL transitions when driven by the internal I^2C subordinate. Set according to the I^2C speed mode: Fast-mode Plus = 00 Fast mode = 01 Standard mode = 10.	0b00: Set for I^2C Fast-mode Plus speed 0b01: Set for I^2C Fast-mode speed 0b10: Set for I^2C standard-mode speed 0b11: Reserved
SLV_TO	2:0	I^2C-to-I^2C Subordinate Timeout Setting Internal GMSL2 I^2C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x41)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT	6:4	I^2C-to-I^2C Primary Bit-Rate Setting Configures the I^2C bit rate used by the internal I^2C primary (in the device on remote side from the external I^2C primary). Set this according to the I^2C speed mode.	0b000: 9.92Kbps - Set for I^2C standard mode speed 0b001: 33.2Kbps - Set for I^2C standard mode speed 0b010: 99.2Kbps - Set for I^2C standard or Fast-mode speed 0b011: 123Kbps - Set for I^2C Fast-mode speed 0b100: 203Kbps - Set for I^2C Fast-mode speed 0b101: 397Kbps - Set for I^2C Fast-mode or Fast-mode Plus speed 0b110: 625Kbps - Set for I^2C Fast-mode Plus speed 0b111: 980Kbps - Set for I^2C Fast-mode Plus speed
MST_TO	2:0	I^2C-to-I^2C Primary Timeout Setting Internal GMSL2 I^2C primary times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x42)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A	7:1	I^2C Address Translator Source A When I^2C device address matches I^2C SRC_A, internal I^2C primary (on remote side) replaces the device address by I^2C DST_A.	0bXXXXXXX: Value of I^2C SRC_A

I2C_3 (0x43)*

BIT	7	6	5	4	3	2	1	0
Field	DST_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A	7:1	I2C Address Translator Destination A See the description of I2C SRC_A .	0bXXXXXXX: Value of I2C DST_A

I2C_4 (0x44)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B	7:1	I2C Address Translator Source B When I2C device address matches I2C SRC_B, internal I2C primary (on remote side) replaces the device address by I2C DST_B.	0bXXXXXXX: Value of I2C SRC_B

I2C_5 (0x45)*

BIT	7	6	5	4	3	2	1	0
Field	DST_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B	7:1	I2C Address Translator Destination B See the description of I2C SRC_B.	0bXXXXXXX: Value of I2C DST_B

I2C_7 (0x47)

BIT	7	6	5	4	3	2	1	0
Field	UART_RX_OVERFLOW	RSVD	–	–	–	I2C_TIMED_OUT	REM_ACK_ACKED	REM_ACK_RECVED
Reset	0b0	0b0	–	–	–	0x0	0x0	0x0
Access Type	Read Clears All		–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
UART_RX_OVERFLOW	7	UART Rx FIFO Overflow	0x0: No overflow occurred 0x1: Overflow occurred
I2C_TIMED_OUT	2	Internal I2C-to-I2C subordinate or primary has timed out while receiving packet from remote device	0x0: Timeout has not occurred 0x1: Timeout has occurred
REM_ACK_ACKED	1	Inverse of the I2C acknowledge bit received from remote side	0x0: I2C acknowledge bit received as 1 0x1: I2C acknowledge bit received as 0

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ACK_RECVED	0	I2C acknowledge bit for any I2C byte is received from remote side for the previous I2C packet	0b0: I2C acknowledge bit not received 0b1: I2C acknowledge bit received

UART_0 (0x48)*

BIT	7	6	5	4	3	2	1	0
Field	ARB_TO_LEN[1:0]		REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
Reset	0x1		0x0	0x0	0x0	0x1		0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ARB_TO_LEN	7:6	UART Rx Source Arbitration Timeout Duration UART Rx processes packets from a single UART source at any time. When UART Rx does not receive any UART packets for this duration, it will select the next UART source according to the source ID of the next following received packet.	0b00: 1ms 0b01: 2ms 0b10: 8ms 0b11: 32ms
REM_MS_EN	5	Enables UART Bypass Mode Control by Remote GPIO Pin When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, chip is in bypass mode. Otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN	4	Enables UART Bypass Mode Control by Local GPIO Pin When MS is high, chip is in bypass mode. Otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_DIS_PAR	3	Selects whether or not to receive and send parity bit in bypass mode	0b0: Receive and send parity bit in bypass mode 0b1: Do not receive and send parity bit in bypass mode
BYPASS_TO	2:1	UART Soft-Bypass Timeout Duration	0b00: 1ms 0b01: 2ms 0b10: 8ms 0b11: 32ms
BYPASS_EN	0	Enables UART Soft-Bypass Mode Bypass mode remains active as long as there is UART activity. When there is no UART activity for the selected duration (configured by BYPASS_TO register), the device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

UART_1 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_LSB[7:0]							
Reset	0x96							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_LSB	7:0	UART detected bit length, low 8 bits	0xXX: UART detected bit length, low 8 bits

UART_2 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	OUT_DELAY[1:0]		BITLEN_MSB[5:0]					
Reset	0x2		0x0					
Access Type	Write, Read		Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
OUT_DELAY	7:6	UART Initial Output Delay In base mode, the first received UART byte of a packet (sync or acknowledge frame) is delayed by the configured number of bit times in order to output the UART frames of the same packet, back to back, on the remote side.	0b00: 0 bits 0b01: 4 bits 0b10: 8 bits 0b11: 1 bit
BITLEN_MSB	5:0	UART detected bit length, high 6 bits	0bXXXXXX: UART detected bit length, high 6 bits

I2C_PT_0 (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_PT	5:4	Pass-Through I^2C-to-I^2C Subordinate Setup and Hold Time Setting (Setup, Hold) Configures the interval between SDA and SCL transitions when driven by the internal I^2C subordinate. Set according to the I^2C speed mode: Fast-mode Plus = 00 Fast mode = 01 standard mode = 10	0b00: Set for I^2C Fast-mode Plus speed 0b01: Set for I^2C Fast-mode speed 0b10: Set for I^2C standard-mode speed 0b11: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_TO_PT	2:0	Pass-Through I²C-to-I²C Subordinate Timeout Setting Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_PT_1 (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_PT[2:0]			–	MST_TO_PT[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_PT	6:4	Pass-Through I²C-to-I²C Primary Bit Rate Setting Configures the I²C bit rate used by the internal I²C primary (in the device on the remote side from the external I²C primary). Set according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast mode = 010 to 101 standard mode = 000 to 010	0b000: 9.92Kbps - Set for I²C standard-mode speed 0b001: 33.2Kbps - Set for I²C standard-mode speed 0b010: 99.2Kbps - Set for I²C standard or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO_PT	2:0	Pass-Through I²C-to-I²C Primary Timeout Setting Internal GMSL2 I²C primary times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_PT_2 (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	XOVER_EN_2	I2C_TIMED_OUT_2	REM_ACK_ACKED_2	REM_ACK_RECVED_2	XOVER_EN_1	I2C_TIMED_OUT_1	REM_ACK_ACKED_1	REM_ACK_RECVED_1
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Read Only	Read Only	Read Only	Write, Read	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
XOVER_EN_2	7	Connects pass-through I²C/UART Channel 2 to primary control channel on remote side	0b0: Do not connect 0b1: Connect

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_TIMED_OUT_2	6	In pass-through I²C Channel 2, internal I²C-to-I²C subordinate or primary has timed out while receiving packet from remote device	0b0: Timeout has not occurred 0b1: Timeout has occurred
REM_ACK_ACKED_2	5	In pass-through I²C Channel 2, inverse of the I²C acknowledge bit received from remote side	0x0: I²C acknowledge bit received as 1 0x1: I²C acknowledge bit received as 0
REM_ACK_RECVED_2	4	In pass-through I²C Channel 2, I²C acknowledge bit for any I²C byte is received from remote side for the previous I²C packet.	0b0: I²C acknowledge bit not received 0b1: I²C acknowledge bit received
XOVER_EN_1	3	Connects pass-through I²C/UART Channel 1 to main control channel on remote side	0b0: Do not connect 0b1: Connect
I2C_TIMED_OUT_1	2	In pass-through I²C Channel 1, internal I²C-to-I²C subordinate or primary has timed out while receiving packet from remote device	0b0: Timeout has not occurred 0b1: Timeout has occurred
REM_ACK_ACKED_1	1	In pass-through I²C Channel 1, inverse of the I²C acknowledge bit received from remote side	0b0: I²C acknowledge bit received as 1 0b1: I²C acknowledge bit received as 0
REM_ACK_RECVED_1	0	In pass-through I²C Channel 1, I²C acknowledge bit for any I²C byte is received from remote side for the previous I²C packet	0b0: I²C acknowledge bit not received 0b1: I²C acknowledge bit received

UART_PT_0 (0x4F)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_MAN_CFG_2	DIS_PAR_2	UART_RX_OVERFLOW_2	UART_TX_OVERFLOW_2	BITLEN_MAN_CFG_1	DIS_PAR_1	UART_RX_OVERFLOW_1	UART_TX_OVERFLOW_1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Read Clears All	Read Clears All	Write, Read	Write, Read	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MAN_CFG_2	7	Uses the custom UART bit rate (selected by the BITLEN_PT_2_L (0x54A) and BITLEN_PT_2_H (0x54B) bitfields) in pass-through UART Channel 2	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_2	6	Disables parity bit in pass-through UART Channel 2	0b0: Parity bit enabled 0b1: Parity bit disabled
UART_RX_OVERFLOW_2	5	Pass-through UART Rx FIFO overflow flag	0b0: No overflow occurred 0b1: Overflow occurred
UART_TX_OVERFLOW_2	4	Pass-through UART Tx FIFO overflow flag	0b0: No overflow occurred 0b1: Overflow occurred
BITLEN_MAN_CFG_1	3	Uses the custom UART bit rate (selected by the BITLEN_PT_1_L (0x548) and BITLEN_PT_1_H (0x549) bitfields) in pass-through UART Channel 1	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_1	2	Disables parity bit in pass-through UART Channel 1	0b0: Parity bit enabled 0b1: Parity bit disabled
UART_RX_OVERFLOW_1	1	Pass-through UART Rx FIFO overflow flag	0b0: No overflow occurred 0b1: Overflow occurred
UART_TX_OVERFLOW_1	0	Pass-through UART Tx FIFO overflow flag	0b0: No overflow occurred 0b1: Overflow occurred

TX0 (0x50, 0x54, 0x58, 0x5C)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Access Type	Write, Read	–			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	Transmits CRC enable	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TX3 (0x53, 0x57, 0x5B, 0x5F)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	–	TX_STR_SEL[1:0]	
Access Type	–	–			–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_STR_SEL	1:0	Stream ID used in packets transmitted from this channel	0bXX: Stream ID for packets from this channel

TR0 (0x78)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0x1	0x1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC, and that CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

BITFIELD	BITS	DESCRIPTION	DECODE
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR3 (0x7B)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
Reset	–	–	0x1	0x1	–	0x0		
Access Type	–	–			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel Default values of the two MSbs are set by CFG0. Default value of the LSb is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x7C)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

TR0 (0x80, 0x90, 0xA0, 0xA8)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0x1	0x1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC, and that CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR3 (0x83, 0x93, 0xA3, 0xAB)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
Reset	–	–	0x1	0x1	–	0x0		
Access Type	–	–			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default values of the two MSbs are set by CFG0. Default value of the LSb is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x84, 0x94, 0xA4, 0xAC)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x85, 0x95, 0xA5, 0xAD)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0x1	0x0	0x0	0x1	0x1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When set to 1, ARQ settings are automatically selected based on splitter mode	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0: Selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets
MATCH_SRC_ID	5	Acknowledge Packet Source ID Checking Method The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG is set to 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID register
ACK_SRC_ID	4	Selects what to use as SRC_ID in Transmitted Acknowledge Packets The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG is set to 0.	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID register
ARQ_EN	3	Enables ARQ	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x86, 0x96, 0xA6, 0xAE)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0x1	0x0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum Retransmission Limit ARQ stops retransmitting after this many retransmission attempts for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR - ARQ2 register) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT (ARQ2 register) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x87, 0x97, 0xA7, 0xAF)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0x0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Indicates maximum retransmit limit (MAX_RT - ARQ1 register) reached for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0xXX: Count of retransmissions for this channel

TR0 (0x88)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0x1	0x1	0x3		0x0		0x0	
Access Type					Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR3 (0x8B)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
Reset	–	–	0x1	0x1	–	0x0		
Access Type	–	–			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source Identifier used in Packets Transmitted from this Channel Default values of the two MSbs are set by CFG0. Default value of the LSb is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x8C)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 1 received 0x02: Packets from source ID 2 received 0x03: Packets from source ID 1 and 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x8D)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0x1	0x0	0x0	0x1	0x1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When set to 1, ARQ settings are automatically selected based on splitter mode	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0: Selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets
MATCH_SRC_ID	5	Acknowledge packet source ID checking method. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG is set to 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID register
ACK_SRC_ID	4	Selects what to use as SRC_ID in Transmitted Acknowledge Packets The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG is set to 0.	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID register
ARQ_EN	3	Enables ARQ	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x8E)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0x1	0x0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum Retransmit Limit ARQ will stop retransmit after trying retransmit for this many times for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR - ARQ2 register) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x8F)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0x0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Indicates maximum retransmit limit (MAX_RT - ARQ1 register) reached for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0xXX: Count of retransmissions for this channel

VIDEO_TX0 (0x100, 0x108, 0x110, 0x118)*

BIT	7	6	5	4	3	2	1	0
Field	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		AUTO_BPP	RSVD	RSVD[1:0]	
Reset	0x0	0x1	0x2		0b1	0x0	0x0	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_SEL	7	Selects whether Line CRC checksum is generated with DE or HS	0b0: Use DE for Line CRC 0b1: Use HS for Line CRC

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_EN	6	Enables Line CRC Generates a CRC code for the video line and send it to the receiver side for comparison	0b0: Line CRC disabled 0b1: Line CRC enabled
ENC_MODE	5:4	HS, VS, DE Encoding Mode	0b00: HS, VS, DE encoding off 0b01: HS, VS, DE encoding on, color bits always sent 0b10: HS, VS, DE encoding on, color bits sent only when DE is high 0b11: HS, VS, DE encoding on, color bits sent only when HS is high
AUTO_BPP	3	Selects BPP Source	0b0: Use BPP from BPP register 0b1: Use BPP from MIPI receiver

VIDEO_TX1 (0x101, 0x109, 0x111, 0x119)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		BPP[5:0]					
Reset	0x1		0x18					
Access Type			Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BPP	5:0	Color bits per pixel (RGB888 = 24)	0bXXXXXX: Number of bits per pixel

VIDEO_TX2 (0x102, 0x10A, 0x112, 0x11A)*

BIT	7	6	5	4	3	2	1	0
Field	PCLKDET	DRIFT_ERR	OVERFLOW	FIFO_WARN	RSVD	LIM_HEART	RSVD	RSVD
Reset	0x0	0x0	0x0	0x0	0x1	0b0	0x1	0x0
Access Type	Read Only	Read Clears All	Read Clears All	Read Clears All		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PCLKDET	7	PCLK Detection	0b0: Video transmit PCLK not detected 0b1: Video transmit PCLK detected
DRIFT_ERR	6	VID_TX PCLK Drift Error Detection After the video pipeline starts, PCLK cannot drift more than a certain amount without restarting the subsystem.	0b0: Video transmit PCLK drift error not detected 0b1: Video transmit PCLK drift error detected
OVERFLOW	5	VID_TX FIFO Overflow Flag Overflow occurs when video input throughput is too high, or BW allocation on GMSL2 link for video is insufficient	0b0: Video transmit FIFO has not overflowed 0b1: Video transmit FIFO has overflowed
FIFO_WARN	4	VID_TX FIFO is more than half full	0b0: Video transmit FIFO is less than or equal to half full 0b1: Video transmit FIFO is more than half full

BITFIELD	BITS	DESCRIPTION	DECODE
LIM_HEART	2	Disables heartbeat during blanking. Use with SEQ_MISS_EN and DIS_PKT_DET bitfields in deserializer.	0b0: Heartbeat enabled during blanking 0b1: Heartbeat disabled during blanking

VIDEO_TX6 (0x106, 0x10E, 0x116, 0x11E)

BIT	7	6	5	4	3	2	1	0
Field	–	MASK_VIDEO_DE	RSVD[5:0]					
Reset	–	0x0	0x00					
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
MASK_VIDEO_DE	6	Masks video with DE	0x0: Do not mask video with DE 0x1: Mask video with DE

SPI_0 (0x170)*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
Reset	0x0		0x0		0x1	0x0	0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_ID	7:6	Programs to local ID if filtering packets based on header ID.	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3
SPI_CC_TRG_ID	5:4	ID for GMSL2 header in SPI control channel bridge mode	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3
SPI_IGNR_ID	3	Selects if SPI should use or ignore header ID to decide on packet acceptance	0b0: Accept only packets with proper ID 0b1: Ignore ID and accept all packets
SPI_CC_EN	2	Enables control-channel SPI bridge function	0b0: SPI bridge disabled 0b1: SPI bridge enabled
MST_SLVN	1	Selects if SPI is main or subordinate	0b0: SPI subordinate 0b1: SPI main
SPI_EN	0	Enables SPI channel	0b0: SPI channel disabled 0b1: SPI channel enabled

SPI_1 (0x171)*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	
Reset	0x07						0x1	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_N	7:2	Packet Size ((2N + 1) bytes) for GMSL2 SPI Packets If this is programmed to a value more than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes ... ... 0b111111: Packet size is 127 bytes
SPI_BASE_PRIO	1:0	Starting GMSL2 Request Priority Advances by 1 if Tx buffer is over half full (and space is available)	0b00: Priority 0 (low) 0b01: Priority 1 0b10: Priority 2 0b11: Priority 3

SPI_2 (0x172)*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
Reset	0x0			0x0	0x0	0x0	0x1	0x1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF	7:5	Suspends GMSL2 request until this number of extra bytes have been received on SPI port	0b00: No extra bytes 0b01: 1 extra byte 0b10: 2 extra bytes 0b11: 3 extra bytes
FULL_SCK_SETUP	4	Samples MISO after half- or full-SCK period.	0b0: MISO sampled after half-SCK period 0b1: MISO sampled after full-SCK period
SPI_MOD3_F	3	Allows the suppression of an extra SCK prior to SS deassertion when SPI mode 3 is selected	0b0: Extra SCK present prior to SS deassertion when in SPI mode 3 0b1: Extra SCK suppressed prior to SS deassertion when in SPI mode 3
SPI_MOD3	2	Selects SPI mode 0 or 3	0b0: SPI mode 0 0b1: SPI mode 3
SPIM_SS2_ACT_H	1	Sets the polarity for SS2 when the SPI is a main	0b0: Subordinate select 2 is active low 0b1: Subordinate select 2 is active high
SPIM_SS1_ACT_H	0	Sets the polarity for SS1 when the SPI is a main	0b0: Subordinate select 1 is active low 0b1: Subordinate select 1 is active high

SPI_3 (0x173)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SS_DLY_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SS_DLY_CLKS	7:0	Number of 300MHz clocks to delay between the following: 1. Assertion of SS and start of SCK pulses 2. End of SCK pulses and deassertion of SS 3. Deassertion of SS and reassertion of SS (if necessary)	0xXX: Number of clock delays

SPI_4 (0x174)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_LO_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_LO_CLKS	7:0	Number of 300MHz clocks for SCK low time	0xXX: Number of clocks for SCK low time

SPI_5 (0x175)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_HI_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_HI_CLKS	7:0	Number of 300MHz clocks for SCK high time	0xXX: Number of clocks for SCK high time

SPI_6 (0x176)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BNE	5	Alternate GPU status register to use for BNE status if GPIO is not available	0b0: Buffer empty 0b1: Buffer not empty

BITFIELD	BITS	DESCRIPTION	DECODE
SPIS_RWN	4	Alternate GPU control register to use for Rd/ WrN control if GPIO is not available	0b0: Write 0b1: Read
SS_IO_EN_2	3	Enables GPIO for use as subordinate select 2 output	0b0: GPIO not used for SPI SS2 function 0b1: GPIO used for SPI SS2 function
SS_IO_EN_1	2	Enables GPIO for use as subordinate select 1 output	0b0: GPIO not used for SPI SS1 function 0b1: GPIO used for SPI SS1 function
BNE_IO_EN	1	Enables GPIO for use as BNE output for SPI data available status	0b0: GPIO not used for SPI BNE function 0b1: GPIO used for SPI BNE function
RWN_IO_EN	0	Enables GPIO for use as RO input for control of SPI data movement	0b0: GPIO not used for SPI RO function 0b1: GPIO used for SPI RO function

SPI_7 (0x177)

BIT	7	6	5	4	3	2	1	0
Field	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
Reset	0b0	0b0	–	0x0				
Access Type	Read Clears All	Read Clears All	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_RX_OVRFLW	7	SPI Rx buffer overflow flag	0b0: No SPI Rx buffer overflow 0b1: SPI Rx buffer overflow
SPI_TX_OVRFLW	6	SPI Tx buffer overflow flag	0b0: No SPI Tx buffer overflow 0b1: SPI Tx buffer overflow
SPIS_BYTE_CNT	4:0	Number of SPI data bytes available for reading from Rx buffer	0bXXXXX: Number of bytes available

SPI_8 (0x178)*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF_TO[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF_TO	7:0	Timeout delay (in 100ns increments) for GMSL2 request hold off (0 is disable)	0xXX: Number of 100ns delay increments for GMSL2 request hold off

WM_0 (0x190)*

BIT	7	6	5	4	3	2	1	0
Field	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		–	WM_EN
Reset	0x0	0x0			0x0		–	0x0
Access Type	Write, Read	Write, Read			Write, Read		–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM_LEN	7	Watermark Length	0b0: 32-bit 0b1: 64-bit
WM_MODE	6:4	Select Watermark Generation Mode	0b000: Default generator mode - cycle through all four watermarks in video stream 0b001: Error generator mode - cycle through only two watermarks to replicate a stuck frame 0b010–0b111: Reserved
WM_DET	3:2	Watermark Detection/Generation	0b00: Insert watermark in video stream 0b01: Detect watermark and remove from outgoing video stream 0b10: Reserved 0b11: Reserved
WM_EN	0	Enable/Disable of Watermark Generation/ Detection Block	0b0: Watermarking block disabled 0b1: Watermarking block enabled

WM_2 (0x192)*

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			HsyncPol	VsyncPol	WM_NPFILT[1:0]	
Reset	–	0x5			0b0	0b0	0x0	
Access Type	–				Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
HsyncPol	3	HS polarity (only effective for watermark block)	0b0: Noninverting 0x1: Invert
VsyncPol	2	VS polarity (only effective for watermark block)	0b0: Noninverting 0x1: Invert
WM_NPFILT	1:0	Phase accumulator terminal count	0bXX: Phase accumulator terminal count

WM_3 (0x193)*

BIT	7	6	5	4	3	2	1	0
Field	–	WM_TH[6:0]						
Reset	–	0x14						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
WM_TH	6:0	Matched filter threshold	0bXXXXXXX: Matched filter threshold

WM_4 (0x194)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD[1:0]		WM_COLORADJ	–	WM_MASKMODE[1:0]	
Reset	–	–	0x1		0x0	–	0x0	
Access Type	–	–			Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WM_COLOR ADJ	3	Color Adjust	0b0: Masked off LSBs of U. Use if temporal dithering is enabled. 0b1: Set U[Ko:0] = 1/2 WM gain. Use this mode if temporal dithering is disabled
WM_MASKM ODE	1:0	Watermark Mask Mode Sets watermark mask for the device	0b00: Mask if WM is detected 0b01: Mask if WM is detected, blank if error is detected 0b10: Reserved b011: Reserved

WM_5 (0x195)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	RSVD	WM_ERRO R
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–			Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
WM_ERROR	0	Live active-high watermark error	0b0: No watermark error 0b1: Watermark error active, bit automatically clears when error clears

WM_6 (0x196)

BIT	7	6	5	4	3	2	1	0
Field	WM_TIMER[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_TIMER	7:0	Time (in 2ms steps) that the frozen frame condition must be observed before an error is generated. 0 = No filter	0xXX: Number of milliseconds

WM_WREN_0 (0x1AE)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_L	7:0	Works in conjunction with WM_WREN_H to enable writing to watermark registers. Writing is enabled to watermark registers when 0xBA is written to WM_WREN_L and 0xDC is written to WM_WREN_H registers. Otherwise, watermark registers are read-only.	0xBA: Enables writing to WM registers Others: WM registers remain read-only

WM_WREN_1 (0x1AF)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_H	7:0	Works in conjunction with WM_WREN_L to enable writing to watermark registers. Writing is enabled to watermark registers when 0xBA is written to WM_WREN_L and 0xDC is written to WM_WREN_H registers. Otherwise, watermark registers are read-only.	0xDC: Enables writing to WM registers Others: WM registers remain read-only

GPIO_A (0x2BE, 0x2C1)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables Jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2BF, 0x2C2)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Pull-Up/Pull-Down Buffer Configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2C0, 0x2C3)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2C4, 0x2C7, 0x2CA, 0x2CD, 0x2D0, 0x2D3, 0x2D6, 0x2D9, 0x2DC, 0x2DF, 0x2E2, 0x2E5, 0x2E8, 0x2EB, 0x2EE)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pull-Up/Pull-Down Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable MFP4 (0x2CA) and MFP5 (0x2CD) I/O functions are output only. TX_COMP_EN feature is not supported on these pins.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level MFP4 (0x2CA) and MFP5 (0x2CD) I/O functions are output only. GPIO_IN feature is not supported on these pins.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO Out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control MFP4 (0x2CA) and MFP5 (0x2CD) I/O functions are output only. GPIO_TX_EN feature is not supported on these pins.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2C5, 0x2C8, 0x2CB, 0x2CE, 0x2D1, 0x2D4, 0x2D7, 0x2DA, 0x2DD, 0x2E0, 0x2E3, 0x2E6, 0x2E9, 0x2EC, 0x2EF)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Pull-Up/Pull-Down Buffer Configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection I/O pins MFP11 (0x2E0), MFP12 (0x2E3), MFP13 (0x2E6), MFP14 (0x2E9), MFP15 (0x2EC), and MFP16 (0x2EF) are open-drain only. OUT_TYPE selection of push-pull output is not available for these pins.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting MFP4 (0x2CB) and MFP5 (0x2CE) I/O functions are output only. GPIO_TX_ID feature is not supported on these pins.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2C6, 0x2C9, 0x2CC, 0x2CF, 0x2D2, 0x2D5, 0x2D8, 0x2DB, 0x2DE, 0x2E1, 0x2E4, 0x2E7, 0x2EA, 0x2ED, 0x2F0)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

CMU4 (0x304)

BIT	7	6	5	4	3	2	1	0
Field	A_SPEED[1:0]		B_SPEED[1:0]		RSVD[1:0]		D_SPEED[1:0]	
Reset	0x2		0x2		0x2		0x3	
Access Type	Write, Read		Write, Read				Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
A_SPEED	7:6	Controls GPIO Speed Group A transition time. First value is for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V.	0x0: 2ns, 1ns 0x1: 4ns, 2ns 0x2: 8ns, 4ns 0x3: 16ns, 8ns
B_SPEED	5:4	Controls GPIO Speed Group REFCLK transition time. First value is for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V.	0x0: 2ns, 1ns 0x1: 4ns, 2ns 0x2: 8ns, 4ns 0x3: 16ns, 8ns
D_SPEED	1:0	Controls GPIO Speed Group D transition time. First value is for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V.	0x0: 2ns, 1ns 0x1: 4ns, 2ns 0x2: 8ns, 4ns 0x3: 16ns, 8ns

FRONTTOP_0 (0x308)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	enable_line_info	START_PORTB	START_PORTA	CLK_SELU	CLK_SELZ	CLK_SELY	CLK_SELX
Reset	0b0	0b1	0b1	0b1	0b1	0b1	0b0	0b0
Access Type		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
enable_line_info	6	Enable sending line start information frames	0b0: Line start information frames disabled 0x1: Line start information frames enabled
START_PORTB	5	Enable CSI Port B	0b0: CSI on Port B disabled 0x1: CSI on Port B enabled

BITFIELD	BITS	DESCRIPTION	DECODE
START_PORTA	4	Enable CSI Port A	0b0: CSI on Port A disabled 0x1: CSI on Port A enabled
CLK_SELU	3	CSI port selection for Video Pipeline U	0b0: Port A 0b1: Port B
CLK_SELZ	2	CSI port selection for Video Pipeline Z	0b0: Port A 0b1: Port B
CLK_SELY	1	CSI port selection for Video Pipeline Y	0b0: Port A 0b1: Port B
CLK_SELX	0	CSI port selection for Video Pipeline X	0b0: Port A 0b1: Port B

FRONTTOP_1 (0x309)*

BIT	7	6	5	4	3	2	1	0
Field	VC_SELX_L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VC_SELX_L	7:0	Virtual channel filter for VID PIPE X	0bxxxx0000: Do not select any VC 0bxxxxxxx1: Select VC = 0 0bxxxxxx1x: Select VC = 1 0bxxxxx1xx: Select VC = 2 0bxxxx1xxx: Select VC = 3 0bxxxx1111: Select VC = 0, 1, 2, 3

FRONTTOP_3 (0x30B)*

BIT	7	6	5	4	3	2	1	0
Field	VC_SELY_L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VC_SELY_L	7:0	Virtual channel filter for VID PIPE Y	0bxxxx0000: Do not select any VC 0bxxxxxxx1: Select VC = 0 0bxxxxxx1x: Select VC = 1 0bxxxxx1xx: Select VC = 2 0bxxxx1xxx: Select VC = 3 0bxxxx1111: Select VC = 0, 1, 2, 3

FRONTTOP_5 (0x30D)*

BIT	7	6	5	4	3	2	1	0
Field	VC_SELZ_L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VC_SELZ_L	7:0	Virtual channel filter for VID PIPE Z	0bxxxx0000: Do not select any VC 0bxxxxxxx1: Select VC = 0 0bxxxxxx1x: Select VC = 1 0bxxxxx1xx: Select VC = 2 0bxxxx1xxx: Select VC = 3 0bxxxx1111: Select VC = 0, 1, 2, 3

FRONTTOP_7 (0x30F)*

BIT	7	6	5	4	3	2	1	0
Field	VC_SELU_L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VC_SELU_L	7:0	Virtual channel filter for VID PIPE U	0bxxxx0000: Do not select any VC 0bxxxxxxx1: Select VC = 0 0bxxxxxx1x: Select VC = 1 0bxxxxx1xx: Select VC = 2 0bxxxx1xxx: Select VC = 3 0bxxxx1111: Select VC = 0, 1, 2, 3

FRONTTOP_9 (0x311)*

BIT	7	6	5	4	3	2	1	0
Field	START_PORTBU	START_PORTBZ	START_PORTBY	START_PORTBX	START_PORTAU	START_PORTAZ	START_PORTAY	START_PORTAX
Reset	0b0	0b1	0b0	0b1	0b0	0b1	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
START_PORTBU	7	Start Video Pipe U from CSI Port B	0b0: Video not started 0b1: Start video
START_PORTBZ	6	Start Video Pipe Z from CSI Port B	0b0: Video not started 0b1: Start video
START_PORTBY	5	Start Video Pipe Y from CSI Port B	0b0: Video not started 0b1: Start video
START_PORTBX	4	Start Video Pipe X from CSI Port B	0b0: Video not started 0b1: Start video
START_PORTAU	3	Start Video Pipe U from CSI Port A	0b0: Video not started 0b1: Start video
START_PORTAZ	2	Start Video Pipe Z from CSI Port A	0b0: Video not started 0b1: Start video
START_PORTAY	1	Start Video Pipe Y from CSI Port A	0b0: Video not started 0b1: Start video
START_PORTAX	0	Start Video Pipe X from CSI Port A	0b0: Video not started 0b1: Start video

FRONTTOP_10 (0x312)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	bpp8dblu	bpp8dblz	bpp8dbly	bpp8dblx
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type					Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dblu	3	Send 8-bit pixels as 16-bit on Video Pipe U	0b0: Send as 8-bit pixels 0b1: Send 8-bit pixels as 16-bit
bpp8dblz	2	Send 8-bit pixels as 16-bit on Video Pipe Z	0b0: Send as 8-bit pixels 0b1: Send 8-bit pixels as 16-bit
bpp8dbly	1	Send 8-bit pixels as 16-bit on Video Pipe Y	0b0: Send as 8-bit pixels 0b1: Send 8-bit pixels as 16-bit
bpp8dblx	0	Send 8-bit pixels as 16-bit on Video Pipe X	0b0: Send as 8-bit pixels 0b1: Send 8-bit pixels as 16-bit

FRONTTOP_11 (0x313)*

BIT	7	6	5	4	3	2	1	0
Field	bpp12dblu	bpp12dblz	bpp12dbly	bpp12dblx	bpp10dblu	bpp10dblz	bpp10dbly	bpp10dblx
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
bpp12dblu	7	Send 12-bit pixels as 24-bit on Video Pipe U	0b0: Send as 12-bit pixels 0b1: Send 12-bit pixels as 24-bit
bpp12dblz	6	Send 12-bit pixels as 24-bit on Video Pipe Z	0b0: Send as 12-bit pixels 0b1: Send 12-bit pixels as 24-bit
bpp12dbly	5	Send 12-bit pixels as 24-bit on Video Pipe Y	0b0: Send as 12-bit pixels 0b1: Send 12-bit pixels as 24-bit
bpp12dblx	4	Send 12-bit pixels as 24-bit on Video Pipe X	0b0: Send as 12-bit pixels 0b1: Send 12-bit pixels as 24-bit
bpp10dblu	3	Send 10-bit pixels as 20-bit on Video Pipe U	0b0: Send as 10-bit pixels 0b1: Send 10-bit pixels as 20-bit
bpp10dblz	2	Send 10-bit pixels as 20-bit on Video Pipe Z	0b0: Send as 10-bit pixels 0b1: Send 10-bit pixels as 20-bit
bpp10dbly	1	Send 10-bit pixels as 20-bit on Video Pipe Y	0b0: Send as 10-bit pixels 0b1: Send 10-bit pixels as 20-bit
bpp10dblx	0	Send 10-bit pixels as 20-bit on Video Pipe X	0b0: Send as 10-bit pixels 0b1: Send 10-bit pixels as 20-bit

FRONTTOP_12 (0x314)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	mem_dt1_selx[6:0]						
Reset	0b0	0x00						
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt1_selx	6:0	Select designated data type to route to Video Pipeline X (MSb is enable)	0xXXXXXXX: Data type selected to route to video pipeline

FRONTTOP_13 (0x315)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	mem_dt2_selx[6:0]						
Reset	0b0	0x00						
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt2_selx	6:0	Select designated data type to route to Video Pipeline X (MSb is enable)	0xXXXXXXX: Data type selected to route to video pipeline

FRONTTOP_14 (0x316)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt1_sely[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt1_sely	6:0	Select designated data type to route to Video Pipeline Y (MSb is enable)	0xXXXXXXX: Data type selected to route to video pipeline

FRONTTOP_15 (0x317)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt2_sely[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt2_sely	6:0	Select designated data type to route to Video Pipeline Y (MSb is enable)	0xXXXXXXX: Data type selected to route to video pipeline

FRONTTOP_16 (0x318)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt1_selz[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt1_selz	6:0	Select designated data type to route to Video Pipeline Z (MSb is enable)	0xXXXXXXX: Data type selected to route to video pipeline

FRONTTOP_17 (0x319)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt2_selz[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt2_selz	6:0	Select designated data type to route to Video Pipeline Z (MSb is enable)	0xXXXXXXX: Data type selected to route to video pipeline

FRONTTOP_18 (0x31A)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt1_selu[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt1_selu	6:0	Select designated data type to route to Video Pipeline U (MSb is enable)	0xXXXXXXX: Data type selected to route to video pipeline

FRONTTOP_19 (0x31B)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt2_selu[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt2_selu	6:0	Select designated data type to route to Video Pipeline U (MSb is enable)	0xXXXXXXX: Data type selected to route to video pipeline

FRONTTOP_20 (0x31C)

BIT	7	6	5	4	3	2	1	0
Field	soft_dtx_en	soft_vcx_en	soft_bppx_en	soft_bppx[4:0]				
Reset	0b0	0b0	0b0	0x18				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dtx_en	7	Datatype software override enable for Video Pipeline X	0b0: Software override disabled 0b1: Software override enabled
soft_vcx_en	6	Virtual channel software override enable for Video Pipeline X	0b0: Software override disabled 0b1: Software override enabled

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bppx_en	5	BPP software override enable for Video Pipeline X	0b0: Software override disabled 0b1: Software override enabled
soft_bppx	4:0	Software override of BPP on Video Pipeline X	0bXXXXX: Software override value

FRONTTOP_21 (0x31D)

BIT	7	6	5	4	3	2	1	0
Field	soft_dty_en	soft_vcy_en	soft_bppy_en	soft_bppy[4:0]				
Reset	0b0	0b0	0b0	0x18				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dty_en	7	Datatype software override enable for Video Pipeline Y	0b0: Software override disabled 0b1: Software override enabled
soft_vcy_en	6	Virtual channel software override enable for Video Pipeline Y	0b0: Software override disabled 0b1: Software override enabled
soft_bppy_en	5	BPP software override enable for Video Pipeline Y	0b0: Software override disabled 0b1: Software override enabled
soft_bppy	4:0	Software override of BPP on Video Pipeline Y	0bXXXXX: Software override value

FRONTTOP_22 (0x31E)

BIT	7	6	5	4	3	2	1	0
Field	soft_dtz_en	soft_vcz_en	soft_bppz_en	soft_bppz[4:0]				
Reset	0b0	0b0	0b0	0x18				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dtz_en	7	Datatype software override enable for Video Pipeline Z	0b0: Software override disabled 0b1: Software override enabled
soft_vcz_en	6	Virtual channel software override enable for Video Pipeline Z	0b0: Software override disabled 0b1: Software override enabled
soft_bppz_en	5	BPP software override enable for Video Pipeline Z	0b0: Software override disabled 0b1: Software override enabled
soft_bppz	4:0	Software override of BPP on Video Pipeline Z	0bXXXXX: Software override value

FRONTTOP_23 (0x31F)

BIT	7	6	5	4	3	2	1	0
Field	soft_dtu_en	soft_vcu_en	soft_bppu_en	soft_bppu[4:0]				
Reset	0b0	0b0	0b0	0x18				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dtu_en	7	Datatype software override enable for Video Pipeline U	0b0: Software override disabled 0b1: Software override enabled
soft_vcu_en	6	Virtual channel software override enable for Video Pipeline U	0b0: Software override disabled 0b1: Software override enabled
soft_bppu_en	5	BPP software override enable for Video Pipeline U	0b0: Software override disabled 0b1: Software override enabled
soft_bppu	4:0	Software override of BPP on Video Pipeline U	0bXXXXX: Software override value

FRONTTOP_24 (0x320)

BIT	7	6	5	4	3	2	1	0
Field	soft_vcu[1:0]		soft_vcz[1:0]		soft_vcy[1:0]		soft_vcx[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
soft_vcu	7:6	Virtual channel software override for Video Pipeline U	0bXX: Software override value
soft_vcz	5:4	Virtual channel software override for Video Pipeline Z	0bXX: Software override value
soft_vcy	3:2	Virtual channel software override for Video Pipeline Y	0bXX: Software override value
soft_vcx	1:0	Virtual channel software override for Video Pipeline X	0bXX: Software override value

FRONTTOP_25 (0x321)

BIT	7	6	5	4	3	2	1	0
Field	–	–	soft_dtx[5:0]					
Reset	–	–	0x30					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dtx	5:0	Datatype software override for Video Channel X	0bXXXXXX: Software override value

FRONTTOP_26 (0x322)

BIT	7	6	5	4	3	2	1	0
Field	–	–	soft_dty[5:0]					
Reset	–	–	0x30					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dty	5:0	Datatype software override for Video Channel Y	0bXXXXXX: Software override value

FRONTTOP_27 (0x323)

BIT	7	6	5	4	3	2	1	0
Field	–	–	soft_dtz[5:0]					
Reset	–	–	0x30					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dtz	5:0	Datatype software override for Video Channel Z	0bXXXXXX: Software override value

FRONTTOP_28 (0x324)

BIT	7	6	5	4	3	2	1	0
Field	–	–	soft_dtu[5:0]					
Reset	–	–	0x30					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dtu	5:0	Datatype software override for Video Channel U	0bXXXXXX: Software override value

MIPI_RX0 (0x330)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	ctrl1_vc_map_en	ctrl0_vc_map_en	mipi_rx_reset	phy_config[2:0]		
Reset	0x0	–	0x0	0x0	0b0	0x0		
Access Type		–	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_vc_map_en	5	Virtual channel mapping enable	0x0: Disable virtual channel mapping 0x1: Enable virtual channel mapping
ctrl0_vc_map_en	4	Virtual channel mapping enable	0x0: Disable virtual channel mapping 0x1: Enable virtual channel mapping
mipi_rx_reset	3	Reset MIPI Rx receiver	0b0: Do not reset MIPI Rx 0b1: Reset MIPI Rx
phy_config	2:0	MIPI Rx PHY configuration Configure CSI port as 2x4. Ignore reset value listed above; reset value for 2x4 CSI devices is 0x6.	0b100: 2x4, only A (1x4). Two Ports with four data lanes each. Only Port A enabled. 0b101: 2x4, only B (1x4).Two Ports with four data lanes each. Only Port B enabled. 0b110: 2x4, A and B. Two Ports with four data lanes each. Both Port A and Port B enabled. Other values: Reserved

MIPI_RX1 (0x331)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	ctrl1_deskewen	ctrl1_num_lanes[1:0]		RSVD	ctrl0_deskewen	ctrl0_num_lanes[1:0]	
Reset	0x0	0x0	0x3		0x0	0x0	0x3	
Access Type		Write, Read	Write, Read			Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_deskewen	6	Enable the deskew calibration for 1.5Gbps and above for Port B	0x0: Deskew calibration disabled 0x1: Deskew calibration enabled
ctrl1_num_lanes	5:4	Select number of data lanes for Port B (If GMSL1 mode is supported, also configures Port A)	0b00: One data lane 0b01: Two data lanes 0b10: Reserved 0b11: Four data lanes
ctrl0_deskewen	2	Enable the deskew calibration for 1.5Gbps and above for Port A	0b0: Deskew calibration disabled 0b1: Deskew calibration enabled
ctrl0_num_lanes	1:0	Select number of data lanes for Port A (GMSL2 only)	0b00: One data lane 0b01: Two data lanes 0b10: Reserved 0b11: Four data lanes

MIPI_RX2 (0x332)*

BIT	7	6	5	4	3	2	1	0
Field	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
Reset	0xE				0xE			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_lane_map	7:4	PHY1 lane mapping. Ignore reset value listed above; reset value is 0x4. Bits [5:4] specify PHY1 data lane 0 mapping to Port A. Bits [7:6] specify PHY1 data lane 1 mapping to Port A. Works in conjunction with phy0_lane_map for CSI-2 2x4 Port A mapping (Port A consists of PHY0 and PHY1 combined). PHY0 and PHY1 lane maps should be exclusive.	0bXX00: Map PHY1 D0 to Port A D0 0bXX01: Map PHY1 D0 to Port A D1 0bXX10: Map PHY1 D0 to Port A D2 0bXX11: Map PHY1 D0 to Port A D3 0b00XX: Map PHY1 D1 to Port A D0 0b01XX: Map PHY1 D1 to Port A D1 0b10XX: Map PHY1 D1 to Port A D2 0b11XX: Map PHY1 D1 to Port A D3
phy0_lane_map	3:0	PHY0 lane mapping. Bits [1:0] specify PHY0 data lane 0 mapping to Port A. Bits [3:2] specify PHY0 data lane 1 mapping to Port A. Works in conjunction with phy1_lane_map for CSI-2 2x4 Port A mapping (Port A consists of PHY0 and PHY1 combined). PHY0 and PHY1 lane maps should be exclusive.	0bXX00: Map PHY0 D0 to Port A D0 0bXX01: Map PHY0 D0 to Port A D1 0bXX10: Map PHY0 D0 to Port A D2 0bXX11: Map PHY0 D0 to Port A D3 0b00XX: Map PHY0 D1 to Port A D0 0b01XX: Map PHY0 D1 to Port A D1 0b10XX: Map PHY0 D1 to Port A D2 0b11XX: Map PHY0 D1 to Port A D3

MIPI_RX3 (0x333)*

BIT	7	6	5	4	3	2	1	0
Field	phy3_lane_map[3:0]				phy2_lane_map[3:0]			
Reset	0xE				0x4			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_lane_map	7:4	PHY3 lane mapping. Bits [5:4] specify PHY3 data lane 0 mapping to Port B. Bits [7:6] specify PHY3 data lane 1 mapping to Port B. Works in conjunction with phy2_lane_map for CSI-2 2x4 Port B mapping (Port B consists of PHY2 and PHY3 combined). PHY2 and PHY3 lane maps should be exclusive.	0bXX00: Map PHY3 D0 to Port B D0 0bXX01: Map PHY3 D0 to Port B D1 0bXX10: Map PHY3 D0 to Port B D2 0bXX11: Map PHY3 D0 to Port B D3 0b00XX: Map PHY3 D1 to Port B D0 0b01XX: Map PHY3 D1 to Port B D1 0b10XX: Map PHY3 D1 to Port B D2 0b11XX: Map PHY3 D1 to Port B D3
phy2_lane_map	3:0	PHY2 lane mapping. Bits [1:0] specify PHY2 data lane 0 mapping to Port B. Bits [3:2] specify PHY2 data lane 1 mapping to Port B. Works in conjunction with phy3_lane_map for CSI-2 2x4 Port B mapping (Port B consists of PHY2 and PHY3 combined). PHY2 and PHY3 lane maps should be exclusive.	0bXX00: Map PHY2 D0 to Port B D0 0bXX01: Map PHY2 D0 to Port B D1 0bXX10: Map PHY2 D0 to Port B D2 0bXX11: Map PHY2 D0 to Port B D3 0b00XX: Map PHY2 D1 to Port B D0 0b01XX: Map PHY2 D1 to Port B D1 0b10XX: Map PHY2 D1 to Port B D2 0b11XX: Map PHY2 D1 to Port B D3

MIPI_RX4 (0x334)*

BIT	7	6	5	4	3	2	1	0
Field	–	phy1_pol_map[2:0]			–	phy0_pol_map[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_pol_map	6:4	PHY1 lane polarity setting	0bXX0: Normal polarity for data lane 0 0bXX1: Inverse polarity for data lane 0 0bX0X: Normal polarity for data lane 1 0bX1X: Inverse polarity for data lane 1 0b0XX: Normal polarity for clock lane 0b1XX: Inverse polarity for clock lane
phy0_pol_map	2:0	PHY0 lane polarity setting	0bXX0: Normal polarity for data lane 0 0bXX1: Inverse polarity for data lane 0 0bX0X: Normal polarity for data lane 1 0bX1X: Inverse polarity for data lane 1

MIPI_RX5 (0x335)*

BIT	7	6	5	4	3	2	1	0
Field	–	phy3_pol_map[2:0]			–	phy2_pol_map[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_pol_map	6:4	PHY3 lane polarity setting	0bXX0: Normal polarity for data lane 0 0bXX1: Inverse polarity for data lane 0 0bX0X: Normal polarity for data lane 1 0bX1X: Inverse polarity for data lane 1
phy2_pol_map	2:0	PHY2 lane polarity setting	0bXX0: Normal polarity for data lane 0 0bXX1: Inverse polarity for data lane 0 0bX0X: Normal polarity for data lane 1 0bX1X: Inverse polarity for data lane 1 0b0XX: Normal polarity for clock lane 0b1XX: Inverse polarity for clock lane

MIPI_RX8 (0x338)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		t_hs_settle[1:0]		t_clk_miss[1:0]		t_clk_settle[1:0]	
Reset	0x1		0x1		0x1		0x1	
Access Type			Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
t_hs_settle	5:4	Set typical DPHY t_{HS_SETTLE} timing in ns (measured at 2.5Gbps rate)	0b00: 132 0b01: 139 0b10: 153 0b11: 166
t_clk_miss	3:2	Set typical DPHY Tclk_miss timing in ns	0b00: Disabled 0b01: 26 0b10: 40 0b11: 66
t_clk_settle	1:0	Set typical DPHY t_{CLK_SETTLE} timing in ns (measured at 2.5Gbps rate)	0b00: 160 0b01: 220 0b10: 286 0b11: 352

MIPI_RX9 (0x339)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	phy0_lp_err[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Read Clears All				

BITFIELD	BITS	DESCRIPTION	DECODE
phy0_lp_err	4:0	PHY0 LP status	0bXXXX1: Unrecognized escape command received from data lane D0 0bXXX1X: Unrecognized escape command received from CLK lane 0bXX1XX: Invalid line sequence detected from data lane D0 0bX1XXX: Invalid line sequence detected from data lane D1

MIPI_RX10 (0x33A)

BIT	7	6	5	4	3	2	1	0
Field	phy0_hs_err[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
phy0_hs_err	7:0	PHY0 high-speed status	0bXXXXXXX1: HS sync pattern with one bit error detected on data lane D0 0bXXXXXX1X: HS sync pattern with one bit error detected on data lane D1 0bXXXXX1XX: HS sync pattern with two or more bit errors detected on data lane D0 0bXXXX1XXX: HS sync pattern with two or more bit errors detected on data lane D1 0bXXX1XXXX: High speed receiver skew calibration failed on data lane D1 0bXX1XXXXX: High speed receiver skew calibration failed on data lane D0 0bX1XXXXXX: High speed receiver skew calibration run on data lane D1 0b1XXXXXXX: High speed receiver skew calibration run on data lane D0

MIPI_RX11 (0x33B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	phy1_lp_err[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Read Clears All				

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_lp_err	4:0	PHY1 LP status	0bXXXX1: Unrecognized escape command received from data lane D0 0bXXX1X: Unrecognized escape command received from CLK lane 0bXX1XX: Invalid line sequence detected from data lane D0 0bX1XXX: Invalid line sequence detected from data lane D1 0b1XXXX: Invalid line sequence detected from CLK lane

MIPI_RX12 (0x33C)

BIT	7	6	5	4	3	2	1	0
Field	phy1_hs_err[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_hs_err	7:0	PHY1 high-speed status	0bXXXXXXX1: HS sync pattern with one bit error detected on data lane D0 0bXXXXXX1X: HS sync pattern with one bit error detected on data lane D1 0bXXXXX1XX: HS sync pattern with two or more bit errors detected on data lane D0 0bXXXX1XXX: HS sync pattern with two or more bit errors detected on data lane D1 0bXXX1XXXX: High speed receiver skew calibration failed on data lane D1 0bXX1XXXXX: High speed receiver skew calibration failed on data lane D0 0bX1XXXXXX: High speed receiver skew calibration run on data lane D1 0b1XXXXXXX: High speed receiver skew calibration run on data lane D0

MIPI_RX13 (0x33D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	phy2_lp_err[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Read Clears All				

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_lp_err	4:0	PHY2 LP status	0bXXXX1: Unrecognized escape command received from data lane D0 0bXXX1X: Unrecognized escape command received from CLK lane 0bXX1XX: Invalid line sequence detected from data lane D0 0bX1XXX: Invalid line sequence detected from data lane D1 0b1XXXX: Invalid line sequence detected from CLK lane

MIPI_RX14 (0x33E)

BIT	7	6	5	4	3	2	1	0
Field	phy2_hs_err[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_hs_err	7:0	PHY2 high-speed status	0bXXXXXXX1: HS sync pattern with one bit error detected on data lane D0 0bXXXXXX1X: HS sync pattern with one bit error detected on data lane D1 0bXXXXX1XX: HS sync pattern with two or more bit errors detected on data lane D0 0bXXXX1XXX: HS sync pattern with two or more bit errors detected on data lane D1 0bXXX1XXXX: High speed receiver skew calibration failed on data lane D1 0bXX1XXXXX: High speed receiver skew calibration failed on data lane D0 0bX1XXXXXX: High speed receiver skew calibration run on data lane D1 0b1XXXXXXX: High speed receiver skew calibration run on data lane D0

MIPI_RX15 (0x33F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	phy3_lp_err[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Read Clears All				

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_lp_err	4:0	PHY3 LP status	0bXXXX1: Unrecognized escape command received from data lane D0 0bXXX1X: Unrecognized escape command received from CLK lane 0bXX1XX: Invalid line sequence detected from data lane D0 0bX1XXX: Invalid line sequence detected from data lane D1

MIPI_RX16 (0x340)

BIT	7	6	5	4	3	2	1	0
Field	phy3_hs_err[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_hs_err	7:0	PHY3 high-speed status	0bXXXXXXX1: HS sync pattern with one bit error detected on data lane D0 0bXXXXXX1X: HS sync pattern with one bit error detected on data lane D1 0bXXXXX1XX: HS sync pattern with two or more bit errors detected on data lane D0 0bXXXX1XXX: HS sync pattern with two or more bit errors detected on data lane D1 0bXXX1XXXX: High speed receiver skew calibration failed on data lane D1 0bXX1XXXXX: High speed receiver skew calibration failed on data lane D0 0bX1XXXXXX: High speed receiver skew calibration run on data lane D1 0b1XXXXXXX: High speed receiver skew calibration run on data lane D0

MIPI_RX17 (0x341)

BIT	7	6	5	4	3	2	1	0
Field	ctrl0_csi_err_l[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl0_csi_err_l	7:0	CSI-2 Controller 0 status, low byte	0bXXXXXXX1: 1-bit ECC error detected 0bXXXXXX1X: 2-bit ECC error detected 0bXYYYYYXX: YYYYY = bit position of the 1-bit error 0b1XXXXXXX: CRC error detected

MIPI_RX18 (0x342)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	ctrl0_csi_err_h[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Read Clears All		

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl0_csi_err_h	2:0	CSI-2 Controller 0 status, high bits	0bXX1: Packets terminated early 0bX1X: Frame-count error detected 0b1XX: Unsupported data type received

MIPI_RX19 (0x343)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_csi_err_l[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_csi_err_l	7:0	CSI-2 Controller 1 status, low byte	0bXXXXXXX1: 1-bit ECC error detected 0bXXXXXX1X: 2-bit ECC error detected 0bXYYYYYXX: YYYYY = bit position of the 1-bit error 0b1XXXXXXX: CRC error detected

MIPI_RX20 (0x344)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	ctrl1_csi_err_h[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Read Clears All		

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_csi_err_h	2:0	CSI-2 Controller 1 status, high bits	0bX1: Packets terminated early 0b1X: Frame-count error detected

MIPI_RX21 (0x345)*

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_vc_map0[3:0]				ctrl0_vc_map0[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_vc_map0	7:4	Controller 1, new virtual channel for VC = 0	0b00xx: Address of new virtual channel 0b0000: New VC address = 0 0b0001: New VC address = 1 0b0010: New VC address = 2 0b0011: New VC address = 3 0b01xx to 0b11xx: Reserved
ctrl0_vc_map0	3:0	Controller 0, new virtual channel for VC = 0	0b00xx: Address of new virtual channel 0b0000: New VC address = 0 0b0001: New VC address = 1 0b0010: New VC address = 2 0b0011: New VC address = 3 0b01xx to 0b11xx: Reserved

MIPI_RX22 (0x346)*

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_vc_map1[3:0]				ctrl0_vc_map1[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_vc_map 1	7:4	Controller 1, new virtual channel for VC = 1	0b00xx: Address of new virtual channel 0b0000: New VC address = 0 0b0001: New VC address = 1 0b0010: New VC address = 2 0b0011: New VC address = 3 0b01xx to 0b11xx: Reserved
ctrl0_vc_map 1	3:0	Controller 0, new virtual channel for VC = 1	0b00xx: Address of new virtual channel 0b0000: New VC address = 0 0b0001: New VC address = 1 0b0010: New VC address = 2 0b0011: New VC address = 3 0b01xx to 0b11xx: Reserved

MIPI_RX23 (0x347)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_vc_map2[3:0]				ctrl0_vc_map2[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_vc_map 2	7:4	Controller 1, new virtual channel for VC = 2	0b00xx: Address of new virtual channel 0b0000: New VC address = 0 0b0001: New VC address = 1 0b0010: New VC address = 2 0b0011: New VC address = 3 0b01xx to 0b11xx: Reserved
ctrl0_vc_map 2	3:0	Controller 0, new virtual channel for VC = 2	0b00xx: Address of new virtual channel 0b0000: New VC address = 0 0b0001: New VC address = 1 0b0010: New VC address = 2 0b0011: New VC address = 3 0b01xx to 0b11xx: Reserved

MIPI_RX60 (0x36C)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_vc_map3[3:0]				ctrl0_vc_map3[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_vc_map 3	7:4	New virtual channel for VC = 3	0b00xx: Address of new virtual channel 0b0000: New VC address = 0 0b0001: New VC address = 1 0b0010: New VC address = 2 0b0011: New VC address = 3 0b01xx to 0b11xx: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl0_vc_map3	3:0	New virtual channel for VC = 3	0b00xx: Address of new virtual channel 0b0000: New VC address = 0 0b0001: New VC address = 1 0b0010: New VC address = 2 0b0011: New VC address = 3 0b01xx to 0b11xx: Reserved

FRONTTOP_EXT0 (0x3C0)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt3_selx[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt3_selx	7:0	Select a designated data type to route to Video Pipeline X for VS	0xXX: Designated data type

FRONTTOP_EXT1 (0x3C1)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt4_selx[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt4_selx	7:0	Select a designated data type to route to Video Pipeline X for VS	0xXX: Designated data type

FRONTTOP_EXT2 (0x3C2)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt5_selx[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt5_selx	7:0	Select a designated data type to route to Video Pipeline X for HS	0xXX: Designated data type

FRONTTOP_EXT3 (0x3C3)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt6_selx[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt6_selx	7:0	Select a designated data type to route to Video Pipeline X for HS	0xXX: Designated data type

FRONTTOP_EXT4 (0x3C4)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt3_sely[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt3_sely	7:0	Select a designated data type to route to Video Pipeline Y for VS	0xXX: Designated data type

FRONTTOP_EXT5 (0x3C5)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt4_sely[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt4_sely	7:0	Select a designated data type to route to Video Pipeline Y for VS	0xXX: Designated data type

FRONTTOP_EXT6 (0x3C6)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt5_sely[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt5_sely	7:0	Select a designated data type to route to Video Pipeline Y for HS	0xXX: Designated data type

FRONTTOP_EXT7 (0x3C7)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt6_sely[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt6_sely	7:0	Select a designated data type to route to Video Pipeline Y for HS	0xXX: Designated data type

FRONTTOP_EXT8 (0x3C8)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt3_selz[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt3_selz	7:0	Select a designated data type to route to Video Pipeline Z for VS	0xXX: Designated data type

FRONTTOP_EXT9 (0x3C9)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt4_selz[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt4_selz	7:0	Select a designated data type to route to Video Pipeline Z for VS	0xXX: Designated data type

FRONTTOP_EXT10 (0x3CA)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt5_selz[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt5_selz	7:0	Select a designated data type to route to Video Pipeline Z for HS	0xXX: Designated data type

FRONTTOP_EXT11 (0x3CB)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt6_selz[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt6_selz	7:0	Select a designated data type to route to Video Pipeline Z for HS	0xXX: Designated data type

FRONTTOP_EXT12 (0x3CC)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt3_selu[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt3_selu	7:0	Select a designated data type to route to Video Pipeline U for VS	0xXX: Designated data type

FRONTTOP_EXT13 (0x3CD)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt4_selu[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt4_selu	7:0	Select a designated data type to route to Video Pipeline U for VS	0xXX: Designated data type

FRONTTOP_EXT14 (0x3CE)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt5_selu[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt5_selu	7:0	Select a designated data type to route to Video Pipeline U for HS	0xXX: Designated data type

FRONTTOP_EXT15 (0x3CF)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt6_selu[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt6_selu	7:0	Select a designated data type to route to Video Pipeline U for HS	0xXX: Designated data type

FRONTTOP_EXT16 (0x3D0)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt6_sely_en	mem_dt5_sely_en	mem_dt4_sely_en	mem_dt3_sely_en	mem_dt6_selx_en	mem_dt5_selx_en	mem_dt4_selx_en	mem_dt3_selx_en
Reset	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt6_sely_en	7	Enable data type designated in mem_dt6_sely to route to video pipeline Y	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt5_sely_en	6	Enable data type designated in mem_dt5_sely to route to Video Pipeline Y	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt4_sely_en	5	Enable data type designated in mem_dt4_sely to route to Video Pipeline Y	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt3_sely_en	4	Enable data type designated in mem_dt3_sely to route to Video Pipeline Y	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt6_selx_en	3	Enable data type designated in mem_dt6_selx to route to Video Pipeline X	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt5_selx_en	2	Enable data type designated in mem_dt5_selx to route to Video Pipeline X	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt4_selx_en	1	Enable data type designated in mem_dt4_selx to route to Video Pipeline X	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt3_selx_en	0	Enable data type designated in mem_dt3_selx to route to Video Pipeline X	0b0: Disable data type routing 0b1: Enable data type routing

FRONTTOP_EXT17 (0x3D1)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt6_selu_en	mem_dt5_selu_en	mem_dt4_selu_en	mem_dt3_selu_en	mem_dt6_selz_en	mem_dt5_selz_en	mem_dt4_selz_en	mem_dt3_selz_en
Reset	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt6_selu_en	7	Enable data type designated in mem_dt6_selu to route to Video Pipeline U	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt5_selu_en	6	Enable data type designated in mem_dt5_selu to route to Video Pipeline U	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt4_selu_en	5	Enable data type designated in mem_dt4_selu to route to Video Pipeline U	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt3_selu_en	4	Enable data type designated in mem_dt3_selu to route to Video Pipeline U	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt6_selz_en	3	Enable data type designated in mem_dt6_selz to route to Video Pipeline Z	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt5_selz_en	2	Enable data type designated in mem_dt5_selz to route to Video Pipeline Z	0b0: Disable data type routing 0b1: Enable data type routing
mem_dt4_selz_en	1	Enable data type designated in mem_dt4_selz to route to Video Pipeline Z	0b0: Disable data type routing 0b1: Enable data type routing

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt3_selz_en	0	Enable data type designated in mem_dt3_selz to route to Video Pipeline Z	0b0: Disable data type routing 0b1: Enable data type routing

EXT6 (0x3D8)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt7_selx[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt7_selx	6:0	Select designated datatype to route to Video Pipeline X (MSB is enable)	0xXXXXXXX: Datatype selected to route to video pipeline

EXT7 (0x3D9)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt8_selx[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt8_selx	6:0	Select designated datatype to route to Video Pipeline X (MSB is enable)	0xXXXXXXX: Datatype selected to route to video pipeline

EXT8 (0x3DA)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt7_sely[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt7_sely	6:0	Select designated datatype to route to Video Pipeline Y (MSB is enable)	0xXXXXXXX: Datatype selected to route to video pipeline

EXT9 (0x3DB)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt8_sely[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt8_sely	6:0	Select designated datatype to route to Video Pipeline Y (MSB is enable)	0xXXXXXXX: Datatype selected to route to video pipeline

EXTA (0x3DC)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt7_selz[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt7_selz	6:0	Select designated datatype to route to Video Pipeline Z (MSB is enable)	0xXXXXXXX: Datatype selected to route to video pipeline

EXTB (0x3DD)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt8_selz[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt8_selz	6:0	Select designated datatype to route to Video Pipeline Z (MSB is enable)	0xXXXXXXX: Datatype selected to route to video pipeline

EXTC (0x3DE)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt7_selu[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt7_selu	6:0	Select designated datatype to route to Video Pipeline U (MSB is enable)	0xXXXXXXX: Datatype selected to route to video pipeline

EXTD (0x3DF)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt8_selu[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt8_selu	6:0	Select designated datatype to route to Video Pipeline U (MSB is enable)	0xXXXXXXX: Datatype selected to route to video pipeline

REF_VTG0 (0x3F0)

BIT	7	6	5	4	3	2	1	0
Field	REFGEN_LOCKED	REFGEN_PREDEF_EN	REFGEN_PREDEF_FREQ[1:0]		REFGEN_PREDEF_FREQ_ALT	–	REFGEN_RST	REFGEN_EN
Reset	0b0	0b1	0x1		0x1	–	0b0	0b0
Access Type	Read Only	Write, Read	Write, Read		Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REFGEN_LOCKED	7	Reference generation PLL is locked	0b0: Reference generation PLL not locked 0b1: Reference generation PLL locked
REFGEN_PREDEF_EN	6	Enable pre-defined clock settings for reference generation PLL	0b0: Disable pre-defined clock settings for reference generation PLL 0b1: Enable pre-defined clock settings for reference generation PLL
REFGEN_PREDEF_FREQ	5:4	Pre-defined reference generation PLL frequency setting Set REFGEN_PREDEF_FREQ_ALT = 1 to select alternative frequency selections	0b00: 19.2MHz 0b01: 27MHz 0b10: 37.125MHz 0b11: 74.25MHz
REFGEN_PREDEF_FREQ_ALT	3	Enable alternative pre-defined reference generation PLL frequency setting	0b00: Alternative frequency selection disabled 0b01: Alternative frequency selection enabled
REFGEN_RST	1	Reset reference generation PLL	0b0: Do not reset reference generation PLL 0b1: Reset reference generation PLL
REFGEN_EN	0	Enable reference generation PLL	0b0: Disable reference generation PLL 0b1: Enable reference generation PLL

REF_VTG4 (0x3F4)

BIT	7	6	5	4	3	2	1	0
Field	REFGEN_FB_FRACT_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
REFGEN_FB_FRACT_L	7:0	Reference generator PLL feedback divider fraction value when pre-defined mode is disabled (REFGEN_PREDEF_EN = 0)	0xXX: Low byte of reference generator PLL feedback divider fraction value

REF_VTG5 (0x3F5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	REFGEN_FB_FRACT_H[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
REFGEN_FB_FRACT_H	3:0	Reference generator PLL feedback divider fraction value when pre-defined mode is disabled (REFGEN_PREDEF_EN = 0)	0xX: High nibble of reference generator PLL feedback divider fraction value

GMSL1_2 (0x402)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	SSEN	–	–	–	–	–
Reset	–	–	0b0	–	–	–	–	–
Access Type	–	–	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
SSEN	5	Spread-spectrum enable	0b0: Spread-spectrum disabled 0b1: Spread-spectrum enabled

GMSL1_4 (0x404)*

BIT	7	6	5	4	3	2	1	0
Field	SEREN	CLINKEN	PRBSEN	–	–	–	REVCCEN	FWDCCEN
Reset	0b1	0b0	0b0	–	–	–	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SEREN	7	Serialization enable	0b0: Disable serialization 0b1: Enable serialization
CLINKEN	6	Configuration link enable	0b0: Disable configuration link 0b1: Enable configuration link
PRBSEN	5	PRBS test enable (In HIBW mode set PRBS_TYPE = 0)	0b0: Set device normal operation 0b1: Enable PRBS test
REVCCEN	1	Enable reverse control channel from deserializer	0b0: Disable reverse control channel receiver 0b1: Enable reverse control channel receiver
FWDCCEN	0	Enable forward control channel to deserializer	0b0: Disable forward control channel transmitter 0b1: Enable forward control channel transmitter

GMSL1_5 (0x405)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	PRBS_LEN[1:0]		–	–	–	–
Reset	–	–	0x0		–	–	–	–
Access Type	–	–	Write, Read		–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_LEN	5:4	PRBS test length	0b00: Continuous 0b01: 167.1 Mbits 0b10: 9.83 Mbits 0b11: 1341.5 Mbits

GMSL1_7 (0x407)*

BIT	7	6	5	4	3	2	1	0
Field	DBL	HIBW	BWS	–	DRS	HVEN	–	PXL_CRC
Reset	0b0	0b0	0b0	–	0b0	0b0	–	0b0
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DBL	7	Double-output mode	0b0: Use single-rate output 0b1: Use double-rate output (2x word rate at 1/2x width)
HIBW	6	High-bandwidth mode enable	0b0: Disable high-bandwidth mode 0b1: Enable high-bandwidth mode (when BWS = 0)
BWS	5	Bus width select	
DRS	3	Data rate select	0b0: Use normal data rate output 0b1: Use 1/2 rate data output (for use with low data rates)
HVEN	2	HS/VS encoding enable	0b0: Disable HS/VS encoding 0b1: Enable HS/VS encoding
PXL_CRC	0	Pixel CRC type	0b0: Use 1-bit parity (compatible with all devices) 0b1: Use 6-bit CRC

GMSL1_D (0x40D)*

BIT	7	6	5	4	3	2	1	0
Field	I2C_LOC_ACK	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_LOC_ACK	7	I^2C-to-I^2C subordinate generates local acknowledge when forward channel is not available	0b0: Disable local acknowledge when forward channel is not available 0b1: Enable local acknowledge when forward channel is not available

GMSL1_F (0x40F)*

BIT	7	6	5	4	3	2	1	0
Field	CNTL_IN_EN[4:0]					GPO_RX_EN	GPO_OUT_SEL	SET_GPO
Reset	0x0F					0x1	0b0	0b0
Access Type	Write, Read					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_IN_EN	7:3	CNTL input enable for CNTL 0, 1, 2, 3, 4	0xXXXX0: CNTL 0 input disabled 0xXXXX1: CNTL 0 input enabled 0xXXX0X: CNTL 1 input disabled 0xXXX1X: CNTL 1 input enabled 0xXX0XX: CNTL 2 input disabled 0xXX1XX: CNTL 2 input enabled 0xX0XXX: CNTL 3 input disabled 0xX1XXX: CNTL 3 input enabled 0x0XXXX: CNTL 4 input disabled 0x1XXXX: CNTL 4 input enabled
GPO_RX_EN	2	Enable receiving GPO signal from reverse channel	0x0: Disable receiving of GPO signal 0x1: Enable receiving of GPO signal
GPO_OUT_SEL	1	Enable alternative GPO output	0b0: Disable alternative GPO output 0b1: Enable alternative GPO output
SET_GPO	0	Set GPO output high or low	0b0: Set GPO output low 0b1: Set GPO output high

GMSL1_11 (0x411)*

BIT	7	6	5	4	3	2	1	0
Field	ERRG_RATE2[1:0]		ERRG_TYPE2[1:0]		ERRG_CNT2[1:0]		ERRG_PER2	ERRG_EN
Reset	0x0		0x0		0x0		0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_RATE2	7:6	Average error-generation rate	0b00: Every 2560 bits 0b01: Every 40960 bits 0b10: Every 655360 bits 0b11: Every 10485760 bits
ERRG_TYPE2	5:4	Type of generated errors	0b00: Single bit 0b01: Two 8b/10b symbols 0b10: Three 8b/10b symbols 0b11: Four 8b/10b symbols
ERRG_CNT2	3:2	Number of generated errors	0b00: Continuous 0b01: 16 0b10: 128 0b11: 1024
ERRG_PER2	1	Periodic error generation enable	0b0: Periodic error generator disabled 0b1: Periodic error generator enabled
ERRG_EN	0	Enable error generator, auto clears when done	0b0: Disable error generator 0b1: Enable error generator

GMSL1_12 (0x412)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	CNTL_IN_ORD[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_IN_ORD	2:0	Internal CNTL_IN order from CNTL4 to CNTL0	0x0: 4,3,2,1,0 0x1: 3,2,1,0,4 0x2: 2,1,0,4,3 0x3: 1,0,4,3,2 0x4: 0,1,2,3,4 0x5: 1,2,3,4,0 0x6: 2,3,4,0,1 0x7: 3,4,0,1,2

GMSL1_13 (0x413)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	ALLOW_PKTCC	–	RSVD	RSVD	RSVD	–	–
Reset	0x0	0x0	–	0b0	0b0	0b0	–	–
Access Type		Write, Read	–				–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ALLOW_PKTCC	6	Allow packet control channel. Set this bit to 1 before turning on the packet-based control channel.	0x0: Not allowed 0x1: Allowed

GMSL1_14 (0x414)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	I2C_TIMED_OUT2	CC_WBLOCK_LOST	REV_BIT_LOCK	CC_WBLOCK	REM_CCLOCK
Reset	–	–	–	0b0	0x0	0b0	0x0	0x0
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_TIMED_OUT2	4	I^2C channel timed out	0b0: I^2C channel not timed out 0b1: I^2C channel timed out
CC_WBLOCK_LOST	3	Word-boundary lock lost	0b0: Word-boundary lock not lost 0b1: Word-boundary lock lost
REV_BIT_LOCK	2	Reverse-channel bit locked	0b0: Reverse-channel bit not locked 0b1: Reverse-channel bit locked
CC_WBLOCK	1	Control-channel word boundary lock	0b0: Control-channel word boundary not locked 0b1: Control-channel word boundary locked
REM_CCLOCK	0	Remote control channel locked	0b0: Remote control channel not locked 0b1: Remote control channel locked

GMSL1_15 (0x415)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	SEL_VESA	SEL_RGB888
Reset	–	–	–	–	–	–	0b1	0b1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SEL_VESA	1	VESA or OLDI mapping selection	0b0: OLDI mapping 0b1: VESA mapping
SEL_RGB888	0	Select RGB888 bit mapping Disabled by default (0b0). Ignore reset value listed above.	0b0: Non-RGB888 0b1: RGB888

GMSL1_16 (0x416)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_ERR	–	–	–	–	–	–
Reset	–	0b0	–	–	–	–	–	–
Access Type	–	Read Only	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	6	Maximum retransmission error flag. Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached

GMSL1_18 (0x41C)

BIT	7	6	5	4	3	2	1	0
Field	CC_I2C_RETR_CNT[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_I2C_RETR_CNT	7:0	I^2C packet retransmit count	0xXX: Number of I^2C packets retransmitted

GMSL1_19 (0x41D)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_ERRCNT[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERRCNT	7:0	Packet-based control-channel CRC error counter	0xXX: Number of control-channel CRC errors

GMSL1_39 (0x438)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS24_I	CROSS24_F	CROSS24[4:0]				
Reset	–	0x0	0x0	0x18				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS24_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS24_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS24	4:0	Maps incoming bit position set by this field to the outgoing bit position 24	0bXXXXX: Incoming bit position

GMSL1_3A (0x439)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS25_I	CROSS25_F	CROSS25[4:0]				
Reset	–	0x0	0x0	0x19				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS25_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS25_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS25	4:0	Maps incoming bit position set by this field to the outgoing bit position 25	0bXXXXX: Incoming bit position

GMSL1_3B (0x43A)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS26_I	CROSS26_F	CROSS26[4:0]				
Reset	–	0x0	0x0	0x1A				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS26_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS26_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS26	4:0	Maps incoming bit position set by this field to the outgoing bit position 26	0bXXXXX: Incoming bit position

GMSL1_3C (0x43B)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS27_I	CROSS27_F	CROSS27[4:0]				
Reset	–	0x0	0x0	0x1B				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS27_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS27_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS27	4:0	Maps incoming bit position set by this field to the outgoing bit position 27	0bXXXXX: Incoming bit position

GMSL1_3D (0x43C)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
Reset	–	0x0	0x0	0x1C				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS28_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS28_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS28	4:0	Maps incoming bit position set by this field to the outgoing bit position 28	0bXXXXX: Incoming bit position

GMSL1_3E (0x43D)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
Reset	–	0x0	0x0	0x1D				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS29_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS29_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS29	4:0	Maps incoming bit position set by this field to the outgoing bit position 29	0bXXXXX: Incoming bit position

GMSL1_3F (0x43E)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS30_I	CROSS30_F	CROSS30[4:0]				
Reset	–	0x0	0x0	0x1E				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS30_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS30_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS30	4:0	Maps incoming bit position set by this field to the outgoing bit position 30	0bXXXXX: Incoming bit position

GMSL1_42 (0x442)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		–	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	GPO_EN
Reset	0x1		–	0b1	0b1	0b0	0b1	0b1
Access Type			–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_EN	4	Maximum retransmission limit enable	0b0: Max retransmission limit disabled 0b1: Max retransmission limit enabled
I2C_RT_EN	3	I^2C retransmission enable	0b0: I^2C retransmission disabled 0b1: I^2C retransmission enabled
GPI_COMP_EN	2	General-purpose input compensation enable	0b0: GPI compensation disabled 0b1: GPI compensation enabled
GPI_RT_EN	1	Enable general-purpose input pin	0b0: GPI pin disabled 0b1: GPI pin enabled
GPO_EN	0	Enable general-purpose output pin	0b0: GPO pin disabled 0b1: GPO pin enabled

GMSL1_4D (0x44D)

BIT	7	6	5	4	3	2	1	0
Field	HIGHIMM	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
HIGHIMM	7	Reverse-channel high-immunity mode	0b0: Reverse-channel high-immunity mode disabled 0b1: Reverse-channel high-immunity mode enabled

GMSL1_66 (0x466)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		PRBS_TYPE	REV_FAST	DIS_DE	–	–	–
Reset	0x1		0b1	0b0	0b0	–	–	–
Access Type			Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_TYPE	5	PRBS type select (in HIBW mode set PRBS_TYPE = 0) PRBS_TYPE setting must match in serializer and deserializer	0b0: GMSL1 legacy style PRBS test 0b1: Non-GMSL1 legacy style PRBS test
REV_FAST	4	Reverse-channel fast mode	0b0: Disable reverse-channel fast mode 0b1: Enable reverse-channel fast mode
DIS_DE	3	Disable processing separate HS and DE signals	0b0: Enable processing separate HS and DE signals 0b1: Disable processing separate HS and DE signals

GMSL1_67 (0x467)*

BIT	7	6	5	4	3	2	1	0
Field	CNTL_TRIG[1:0]		AUTO_CLINK	DE_RGB888_DBL	–	DBL_ALIGN_TO[2:0]		
Reset	0x0		0b0	0b0	–	0x7		
Access Type	Write, Read		Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_TRIG	7:6	Select CNTL trigger of encoded packets in high-bandwidth mode	0b00: No trigger 0b01: Always trigger 0b10: Trigger when DE is low 0b11: Trigger when HS is low
AUTO_CLINK	5	Automatic control of configuration link	0b0: Enable configuration link only when CLINKEN = 1 and SEREN = 0 0b1: Automatically enable configuration link when SEREN = 1 and PCLKDET = 0
DE_RGB888_DBL	4	DBL DE RGB888 processing mode select	0b0: Regular DBL DE processing while mapping input 0b1: Process DBL DE for RGB888 mode while mapping input

BITFIELD	BITS	DESCRIPTION	DECODE
DBL_ALIGN_TO	2:0	Double alignment mode	0b000: Align at each rising edge of HS and turn off the alignment after HS is low 0b001: Reserved 0b010: Force align 0b011: Force align 0b100: Align at each rising edge of HS 0b101: Align at each rising edge of DE 0b110: Reserved 0b111: DBL-DBL mode with no alignment

GMSL1_68 (0x468)*

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			RSVD[1:0]		CC_CRC_LENGTH[1:0]	
Reset	–	0x1			0x2		0x1	
Access Type	–						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_LENGTH	1:0	Control-channel CRC length	0x0: 1-bit 0x1: 5-bit 0x2: 8-bit 0x3: Reserved

GMSL1_96 (0x496)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	–	–	BYPASS_HVD_ALIGN	–	RSVD[1:0]	
Reset	0b0	–	–	–	0b0	–	0x2	
Access Type		–	–	–	Write, Read	–		

BITFIELD	BITS	DESCRIPTION	DECODE
BYPASS_HVD_ALIGN	3	Bypass HS, VS, DE alignment	0b0: Align HS, VS and DE 0b1: Bypass HS, VS and DE through alignment block

GMSL1_99 (0x499)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	RSVD	REV_FILT_EN	ALIGN_VS_MODE	ALIGN_INFO	–	–
Reset	0b0	–	0b0	0b0	0b1	0b1	–	–
Access Type		–		Write, Read	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
REV_FILT_EN	4	Reverse-channel digital filter enable	0b0: Disable filter 0b1: Enable filter
ALIGN_VS_MODE	3	Processing mode while aligning VS in HIBW DBL mode	0b0: Send VSL 0b1: Send VSL or VSH

BITFIELD	BITS	DESCRIPTION	DECODE
ALIGN_INFO	2	Send alignment information through CNTL signals in HBIW mode	0b0: Do not send alignment information 0b1: Send alignment information

GMSL1_9A (0x49A)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD[1:0]		PKTCC_EN	RSVD[1:0]		RSVD
Reset	–	–	0x1		0b0	0x0		0b0
Access Type	–	–			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKTCC_EN	3	Packet-based control-channel mode enable, when enabled and the user enters sleep mode. Required to reduce MST_TO.	0b0: Disable packet-based control-channel mode 0b1: Enable packet-based control-channel mode

GMSL1_C8 (0x4C8)

BIT	7	6	5	4	3	2	1	0
Field	–	ALIGNING	I2C_ACK_RECVED	I2C_ACK_ACKED	–	–	–	–
Reset	–	0b0	0b0	0b0	–	–	–	–
Access Type	–	Read Only	Read Only	Read Only	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ALIGNING	6	Status of DBL alignment	0b0: Not aligning 0b1: Aligning
I2C_ACK_RECVED	5	Remote acknowledge received	0b0: Remote Ack not received 0b1: Remote Ack received
I2C_ACK_ACKED	4	Remote acknowledge acknowledged	0b0: Remote Ack not acknowledged 0b1: Remote Ack acknowledged

ADC_CTRL_0 (0x500)

BIT	7	6	5	4	3	2	1	0
Field	buf_bypass	RSVD	RSVD	adc_chgpump_pu	adc_refbuf_pu	buf_pu	adc_pu	cpu_adc_start
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
buf_bypass	7	Bypass input buffer	0b0: Use input buffer 0b1: Bypass input buffer stage
adc_chgpump_pu	4	ADC charge pump power up	0b0: ADC charge pump powered off 0b1: ADC charge pump powered on
adc_refbuf_pu	3	ADC reference buffer power up	0b0: ADC reference buffer powered off 0b1: ADC reference buffer powered on

BITFIELD	BITS	DESCRIPTION	DECODE
buf_pu	2	ADC input buffer power up	0b0: ADC input buffer powered off 0b1: ADC input buffer powered on
adc_pu	1	ADC power up	0b0: ADC powered off 0b1: ADC powered on
cpu_adc_start	0	Start ADC conversion. Bit is automatically cleared to zero after completion of the conversion	0b0: Conversion complete 0b1: Start ADC conversion

ADC_CTRL_1 (0x501)

BIT	7	6	5	4	3	2	1	0
Field	adc_chsel[3:0]				adc_clk_en	adc_refsel	adc_scale	adc_refscl
Reset	0x0				0b0	0b0	0b0	0b0
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
adc_chsel	7:4	ADC channel select	0x0: ADC0 (see adc_pin_en[0] bit) 0x1: ADC1 (see adc_pin_en[1] bit) 0x2: ADC2 (see adc_pin_en[2] bit) 0x3: Reserved 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved 0x8: $V_{DDIO}/4$ 0x9: $V_{DD18}/2$ 0xA: CAP_VDD/2 0xB: TEMP MON 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved
adc_clk_en	3	ADC clock enable	0b0: ADC clock disable 0b1: ADC clock enable
adc_refsel	2	ADC reference select	0b0: Select internal bandgap voltage as ADC reference 0b1: Select VDD18 as ADC reference
adc_scale	1	ADC scale	0b0: Normal operation 0b1: Scale ADC input down by 1/2
adc_refscl	0	ADC reference scale	0b0: Normal operation 0b1: Scale ADC reference down by 1/2

ADC_CTRL_2 (0x502)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	RSVD	RSVD	adc_div[1:0]		adc_xref	Inmux_en
Reset	0b0	–	0b0	0b0	0x0		0b0	0b0
Access Type		–			Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
adc_div	3:2	ADC[2:0] internal divider	0b00: Divide by 1 0b01: Divide by 2 0b10: Divide by 3 0b11: Divide by 4
adc_xref	1	Enable use of ADC external reference	0b0: Use internal reference for ADC 0b1: Use external reference for ADC
Inmux_en	0	Enable the input mux to the ADC to allow for a break before make connection sequence	0b0: Mux is opened 0b1: Mux selected by adc_chsel field is closed

ADC_CTRL_3 (0x503)

BIT	7	6	5	4	3	2	1	0
Field	AfePwrUpDly[7:0]							
Reset	0x0A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AfePwrUpDly	7:0	AFE power-up delay select (in 2.8 µs increments when using a 2.5MHz ADC clock.)	0xXX: Number of 2.8 µs delays

ADC_STATUS0 (0x504)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	adc_active
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
adc_active	0	ADC conversion in progress	0b0: ADC is idle 0b1: ADC conversion currently in progress

ADC_DATA0 (0x508)

BIT	7	6	5	4	3	2	1	0
Field	adc_data_l[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
adc_data_l	7:0	Lower byte of 10-bit ADC converted sample data output	0xX: Lower byte of 10-bit ADC converted value

ADC_DATA1 (0x509)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	adc_data_h[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
adc_data_h	1:0	Upper 2 bits of 10-bit ADC converted sample data output	0xX: Upper 2-bits of 10-bit ADC converted value

ADC_INTRIE0 (0x50C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	adc_overflow_ie	adc_lo_limit_ie	adc_hi_limit_ie	adc_ref_ready_ie	adc_done_ie
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
adc_overflow_ie	4	ADC overflow interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when ADC overflow interrupt flag is set
adc_lo_limit_ie	3	ADC low limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when ADC low limit monitor interrupt flag is set
adc_hi_limit_ie	2	ADC high limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when ADC high limit monitor interrupt flag is set
adc_ref_ready_ie	1	ADC reference ready interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when ADC reference ready interrupt flag is set
adc_done_ie	0	ADC done interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when ADC done interrupt flag is set

ADC_INTRIE1 (0x50D)

BIT	7	6	5	4	3	2	1	0
Field	ch7_hi_limit_ie	ch6_hi_limit_ie	ch5_hi_limit_ie	ch4_hi_limit_ie	ch3_hi_limit_ie	ch2_hi_limit_ie	ch1_hi_limit_ie	ch0_hi_limit_ie
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ch7_hi_limit_ie	7	Channel 7 high limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 7 high limit monitor interrupt flag is set

BITFIELD	BITS	DESCRIPTION	DECODE
ch6_hi_limit_ie	6	Channel 6 high limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 6 high limit monitor interrupt flag is set
ch5_hi_limit_ie	5	Channel 5 high limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 5 high limit monitor interrupt flag is set
ch4_hi_limit_ie	4	Channel 4 high limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 4 high limit monitor interrupt flag is set
ch3_hi_limit_ie	3	Channel 3 high limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 3 high limit monitor interrupt flag is set
ch2_hi_limit_ie	2	Channel 2 high limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 2 high limit monitor interrupt flag is set
ch1_hi_limit_ie	1	Channel 1 high limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 1 high limit monitor interrupt flag is set
ch0_hi_limit_ie	0	Channel 0 high limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 0 high limit monitor interrupt flag is set

ADC_INTRIE2 (0x50E)

BIT	7	6	5	4	3	2	1	0
Field	ch7_lo_limit_ie	ch6_lo_limit_ie	ch5_lo_limit_ie	ch4_lo_limit_ie	ch3_lo_limit_ie	ch2_lo_limit_ie	ch1_lo_limit_ie	ch0_lo_limit_ie
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ch7_lo_limit_ie	7	Channel 7 low limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 7 low limit monitor interrupt flag is set
ch6_lo_limit_ie	6	Channel 6 low limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 6 low limit monitor interrupt flag is set
ch5_lo_limit_ie	5	Channel 5 low limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 5 low limit monitor interrupt flag is set
ch4_lo_limit_ie	4	Channel 4 low limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 4 low limit monitor interrupt flag is set
ch3_lo_limit_ie	3	Channel 3 low limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 3 low limit monitor interrupt flag is set
ch2_lo_limit_ie	2	Channel 2 low limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 2 low limit monitor interrupt flag is set

BITFIELD	BITS	DESCRIPTION	DECODE
ch1_lo_limit_ie	1	Channel 1 low limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 1 low limit monitor interrupt flag is set
ch0_lo_limit_ie	0	Channel 0 low limit monitor interrupt enable	0b0: ADC interrupt source disabled 0b1: Enable assertion of ADC interrupt when Channel 0 low limit monitor interrupt flag is set

ADC_INTRIE3 (0x50F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	invalid_ch_sel_ie
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
invalid_ch_sel_ie	0	Enable the ADC channel selection invalid function	0b0: Disable ADC channel selection invalid function 0b1: Enable ADC channel selection invalid function

ADC_INTR0 (0x510)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	adc_overflow_if	adc_lo_limit_if	adc_hi_limit_if	adc_ref_ready_if	adc_done_if
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
adc_overflow_if	4	ADC overflow interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
adc_lo_limit_if	3	ADC low limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
adc_hi_limit_if	2	ADC high limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
adc_ref_ready_if	1	ADC reference ready interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
adc_done_if	0	ADC done interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set

ADC_INTR1 (0x511)

BIT	7	6	5	4	3	2	1	0
Field	ch7_hi_limit_if	ch6_hi_limit_if	ch5_hi_limit_if	ch4_hi_limit_if	ch3_hi_limit_if	ch2_hi_limit_if	ch1_hi_limit_if	ch0_hi_limit_if
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
ch7_hi_limit_if	7	Channel 7 high limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch6_hi_limit_if	6	Channel 6 high limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch5_hi_limit_if	5	Channel 5 high limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch4_hi_limit_if	4	Channel 4 high limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch3_hi_limit_if	3	Channel 3 high limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch2_hi_limit_if	2	Channel 2 high limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch1_hi_limit_if	1	Channel 1 high limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch0_hi_limit_if	0	Channel 0 high limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set

ADC_INTR2 (0x512)

BIT	7	6	5	4	3	2	1	0
Field	ch7_lo_limit_if	ch6_lo_limit_if	ch5_lo_limit_if	ch4_lo_limit_if	ch3_lo_limit_if	ch2_lo_limit_if	ch1_lo_limit_if	ch0_lo_limit_if
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
ch7_lo_limit_if	7	Channel 7 low limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch6_lo_limit_if	6	Channel 6 low limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch5_lo_limit_if	5	Channel 5 low limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch4_lo_limit_if	4	Channel 4 low limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch3_lo_limit_if	3	Channel 3 low limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch2_lo_limit_if	2	Channel 2 low limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch1_lo_limit_if	1	Channel 1 low limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set
ch0_lo_limit_if	0	Channel 0 low limit monitor interrupt flag. Cleared when read.	0b0: Flag cleared 0b1: Flag set

ADC_INTR3 (0x513)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	invalid_ch_sel_if
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
invalid_ch_sel_if	0	Invalid channel flag. Indicates that an invalid GPIO channel was attempted to be connected to the ADC input. This can be a result of the package selection or GPIO port configuration. Cleared when read.	0b0: Flag cleared 0b1: Flag set

ADC_LIMIT0_0 (0x514)

BIT	7	6	5	4	3	2	1	0
Field	chLoLimit_l0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
chLoLimit_l0	7:0	Register set 0 - lo limit threshold value, low bits	0xXX: Low limit low byte

ADC_LIMIT0_1 (0x515)

BIT	7	6	5	4	3	2	1	0
Field	chHiLimit_l0[3:0]				–	–	chLoLimit_h0[1:0]	
Reset	0xF				–	–	0x0	
Access Type	Write, Read				–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_l0	7:4	Register set 0 - high limit threshold value, low bits	0bX: High limit low nibble
chLoLimit_h0	1:0	Register set 0 - low limit threshold value, high bits	0bXX: Low limit high bits

ADC_LIMIT0_2 (0x516)

BIT	7	6	5	4	3	2	1	0
Field	–	–	chHiLimit_h0[5:0]					
Reset	–	–	0x3F					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_h0	5:0	Register set 0 - high limit threshold value, high bits	0bXXXXXX: High limit high bits

ADC_LIMIT0_3 (0x517)

BIT	7	6	5	4	3	2	1	0
Field	–	–	div_sel0[1:0]		ch_sel0[3:0]			
Reset	–	–	0x0		0x3			
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
div_sel0	5:4	ADC Channel 0 divider setting	0b00: Divide by 1 0b01: Divide by 2 0b10: Divide by 3 0b11: Divide by 4
ch_sel0	3:0	ADC channel select for register set 0	0x0: ADC0 (see adc_pin_en[0] bit) 0x1: ADC1 (see adc_pin_en[1] bit) 0x2: ADC2 (see adc_pin_en[2] bit) 0x3: Reserved 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved 0x8: $V_{DDIO}/4$ 0x9: $V_{DD18}/2$ 0xA: CAP_VDD/2 0xB: TEMP MON 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

ADC_LIMIT1_0 (0x518)

BIT	7	6	5	4	3	2	1	0
Field	chLoLimit_l1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
chLoLimit_l1	7:0	Register set 1 - low limit threshold value, low bits	0xXX: Low limit low byte

ADC_LIMIT1_1 (0x519)

BIT	7	6	5	4	3	2	1	0
Field	chHiLimit_l1[3:0]				–	–	chLoLimit_h1[1:0]	
Reset	0xF				–	–	0x0	
Access Type	Write, Read				–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_l1	7:4	Register set 1 - high limit threshold value, low bits	0bX: High limit low nibble
chLoLimit_h1	1:0	Register set 1 - low limit threshold value, high bits	0bXX: Low limit high bits

ADC_LIMIT1_2 (0x51A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	chHiLimit_h1[5:0]					
Reset	–	–	0x3F					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_h1	5:0	Register set 1 - high limit threshold value, high bits	0bXXXXXX: High limit high bits

ADC_LIMIT1_3 (0x51B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	div_sel1[1:0]		ch_sel1[3:0]			
Reset	–	–	0x0		0x3			
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
div_sel1	5:4	ADC Channel 1 divider setting	0b00: Divide by 1 0b01: Divide by 2 0b10: Divide by 3 0b11: Divide by 4
ch_sel1	3:0	ADC channel select for register set 1	0x0: ADC0 (see adc_pin_en[0] bit) 0x1: ADC1 (see adc_pin_en[1] bit) 0x2: ADC2 (see adc_pin_en[2] bit) 0x3: Reserved 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved 0x8: $V_{DDIO}/4$ 0x9: $V_{DD18}/2$ 0xA: CAP_VDD/2 0xB: TEMP MON 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

ADC_LIMIT2_0 (0x51C)

BIT	7	6	5	4	3	2	1	0
Field	chLoLimit_l2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
chLoLimit_l2	7:0	Register set 2 - low limit threshold value, low bits	0xXX: Low limit low byte

ADC_LIMIT2_1 (0x51D)

BIT	7	6	5	4	3	2	1	0
Field	chHiLimit_l2[3:0]				–	–	chLoLimit_h2[1:0]	
Reset	0xF				–	–	0x0	
Access Type	Write, Read				–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_l2	7:4	Register set 2 - high limit threshold value, low bits	0bX: High limit low nibble
chLoLimit_h2	1:0	Register set 2 - low limit threshold value, high bits	0bXX: Low limit high bits

ADC_LIMIT2_2 (0x51E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	chHiLimit_h2[5:0]					
Reset	–	–	0x3F					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_h2	5:0	Register set 2 - high limit threshold value, high bits	0bXXXXXX: High limit high bits

ADC_LIMIT2_3 (0x51F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	div_sel2[1:0]		ch_sel2[3:0]			
Reset	–	–	0x0		0x3			
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
div_sel2	5:4	ADC Channel 2 divider setting	0b00: Divide by 1 0b01: Divide by 2 0b10: Divide by 3 0b11: Divide by 4

BITFIELD	BITS	DESCRIPTION	DECODE
ch_sel2	3:0	ADC channel select for register set 2	0x0: ADC0 (see adc_pin_en[0] bit) 0x1: ADC1 (see adc_pin_en[1] bit) 0x2: ADC2 (see adc_pin_en[2] bit) 0x3: Reserved 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved 0x8: $V_{DDIO}/4$ 0x9: $V_{DD18}/2$ 0xA: CAP_VDD/2 0xB: TEMP MON 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

ADC_LIMIT3_0 (0x520)

BIT	7	6	5	4	3	2	1	0
Field	chLoLimit_l3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
chLoLimit_l3	7:0	Register set 3 - low limit threshold value, low bits	0xXX: Low limit low byte

ADC_LIMIT3_1 (0x521)

BIT	7	6	5	4	3	2	1	0
Field	chHiLimit_l3[3:0]				–	–	chLoLimit_h3[1:0]	
Reset	0xF				–	–	0x0	
Access Type	Write, Read				–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_l3	7:4	Register set 3 - hghi limit threshold value, low bits	0bX: High limit low nibble
chLoLimit_h3	1:0	Register set 3 - lo limit threshold value, high bits	0bXX: Lo limit high bits

ADC_LIMIT3_2 (0x522)

BIT	7	6	5	4	3	2	1	0
Field	–	–	chHiLimit_h3[5:0]					
Reset	–	–	0x3F					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_h3	5:0	Register set 3 - hih limit threshold value, high bits	0bXXXXXX: High limit high bits

ADC_LIMIT3_3 (0x523)

BIT	7	6	5	4	3	2	1	0
Field	–	–	div_sel3[1:0]		ch_sel3[3:0]			
Reset	–	–	0x0		0x3			
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
div_sel3	5:4	ADC Channel 3 divider setting	0b00: Divide by 1 0b01: Divide by 2 0b10: Divide by 3 0b11: Divide by 4
ch_sel3	3:0	ADC channel select for register set 3	0x0: ADC0 (see adc_pin_en[0] bit) 0x1: ADC1 (see adc_pin_en[1] bit) 0x2: ADC2 (see adc_pin_en[2] bit) 0x3: Reserved 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved 0x8: $V_{DDIO}/4$ 0x9: $V_{DD18}/2$ 0xA: CAP_VDD/2 0xB: TEMP MON 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

ADC_LIMIT4_0 (0x524)

BIT	7	6	5	4	3	2	1	0
Field	chLoLimit_l4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
chLoLimit_l4	7:0	Register set 4 - low limit threshold value, low bits	0xXX: Low limit low byte

ADC_LIMIT4_1 (0x525)

BIT	7	6	5	4	3	2	1	0
Field	chHiLimit_l4[3:0]				–	–	chLoLimit_h4[1:0]	
Reset	0xF				–	–	0x0	
Access Type	Write, Read				–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_l4	7:4	Register set 4 - high limit threshold value, low bits	0bX: High limit low nibble
chLoLimit_h4	1:0	Register set 4 - low limit threshold value, high bits	0bXX: Low limit high bits

ADC_LIMIT4_2 (0x526)

BIT	7	6	5	4	3	2	1	0
Field	–	–	chHiLimit_h4[5:0]					
Reset	–	–	0x3F					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_h4	5:0	Register set 4 - high limit threshold value, high bits	0bXXXXXX: High limit high bits

ADC_LIMIT4_3 (0x527)

BIT	7	6	5	4	3	2	1	0
Field	–	–	div_sel4[1:0]		ch_sel4[3:0]			
Reset	–	–	0x0		0x3			
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
div_sel4	5:4	ADC Channel 4 divider setting	0b00: Divide by 1 0b01: Divide by 2 0b10: Divide by 3 0b11: Divide by 4
ch_sel4	3:0	ADC channel select for register set 4	0x0: ADC0 (see adc_pin_en[0] bit) 0x1: ADC1 (see adc_pin_en[1] bit) 0x2: ADC2 (see adc_pin_en[2] bit) 0x3: Reserved 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved 0x8: $V_{DDIO}/4$ 0x9: $V_{DD18}/2$ 0xA: CAP_VDD/2 0xB: TEMP MON 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

ADC_LIMIT5_0 (0x528)

BIT	7	6	5	4	3	2	1	0
Field	chLoLimit_l5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
chLoLimit_l5	7:0	Register set 5 - low limit threshold value, low bits	0xXX: Low limit low byte

ADC_LIMIT5_1 (0x529)

BIT	7	6	5	4	3	2	1	0
Field	chHiLimit_l5[3:0]				–	–	chLoLimit_h5[1:0]	
Reset	0xF				–	–	0x0	
Access Type	Write, Read				–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_l5	7:4	Register set 5 - high limit threshold value, low bits	0bX: High limit low nibble
chLoLimit_h5	1:0	Register set 5 - low limit threshold value, high bits	0bXX: Low limit high bits

ADC_LIMIT5_2 (0x52A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	chHiLimit_h5[5:0]					
Reset	–	–	0x3F					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_h5	5:0	Register set 5 - high limit threshold value, high bits	0bXXXXXX: High limit high bits

ADC_LIMIT5_3 (0x52B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	div_sel5[1:0]		ch_sel5[3:0]			
Reset	–	–	0x0		0x3			
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
div_sel5	5:4	ADC Channel 5 divider setting	0b00: Divide by 1 0b01: Divide by 2 0b10: Divide by 3 0b11: Divide by 4

BITFIELD	BITS	DESCRIPTION	DECODE
ch_sel5	3:0	ADC channel select for register set 5	0x0: ADC0 (see adc_pin_en[0] bit) 0x1: ADC1 (see adc_pin_en[1] bit) 0x2: ADC2 (see adc_pin_en[2] bit) 0x3: Reserved 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved 0x8: $V_{DDIO}/4$ 0x9: $V_{DD18}/2$ 0xA: CAP_VDD/2 0xB: TEMP MON 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

ADC_LIMIT6_0 (0x52C)

BIT	7	6	5	4	3	2	1	0
Field	chLoLimit_l6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
chLoLimit_l6	7:0	Register set 6 - low limit threshold value, low bits	0xXX: Low limit low byte

ADC_LIMIT6_1 (0x52D)

BIT	7	6	5	4	3	2	1	0
Field	chHiLimit_l6[3:0]				–	–	chLoLimit_h6[1:0]	
Reset	0xF				–	–	0x0	
Access Type	Write, Read				–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_l6	7:4	Register set 6 - high limit threshold value, low bits	0bX: High limit low nibble
chLoLimit_h6	1:0	Register set 6 - low limit threshold value, high bits	0bXX: Low limit high bits

ADC_LIMIT6_2 (0x52E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	chHiLimit_h6[5:0]					
Reset	–	–	0x3F					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_h6	5:0	Register set 5 - high limit threshold value, high bits	0bXXXXXX: High limit high bits

ADC_LIMIT6_3 (0x52F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	div_sel6[1:0]		ch_sel6[3:0]			
Reset	–	–	0x0		0x3			
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
div_sel6	5:4	ADC Channel 6 divider setting	0b00: Divide by 1 0b01: Divide by 2 0b10: Divide by 3 0b11: Divide by 4
ch_sel6	3:0	ADC channel select for register set 6	0x0: ADC0 (see adc_pin_en[0] bit) 0x1: ADC1 (see adc_pin_en[1] bit) 0x2: ADC2 (see adc_pin_en[2] bit) 0x3: Reserved 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved 0x8: $V_{DDIO}/4$ 0x9: $V_{DD18}/2$ 0xA: CAP_VDD/2 0xB: TEMP MON 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

ADC_LIMIT7_0 (0x530)

BIT	7	6	5	4	3	2	1	0
Field	chLoLimit_l7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
chLoLimit_l7	7:0	Register set 7 - low limit threshold value, low bits	0xXX: Low limit low byte

ADC_LIMIT7_1 (0x531)

BIT	7	6	5	4	3	2	1	0
Field	chHiLimit_l7[3:0]				–	–	chLoLimit_h7[1:0]	
Reset	0xF				–	–	0x0	
Access Type	Write, Read				–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_l7	7:4	Register set 7 - high limit threshold value, low bits	0bX: High limit low nibble
chLoLimit_h7	1:0	Register set 7- lo limit threshold value, high bits	0bXX: Lo limit high bits

ADC_LIMIT7_2 (0x532)

BIT	7	6	5	4	3	2	1	0
Field	–	–	chHiLimit_h7[5:0]					
Reset	–	–	0x3F					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
chHiLimit_h7	5:0	Register set 7 - high limit threshold value, high bits	0bXXXXXX: Hi limit high bits

ADC_LIMIT7_3 (0x533)

BIT	7	6	5	4	3	2	1	0
Field	–	–	div_sel7[1:0]		ch_sel7[3:0]			
Reset	–	–	0x0		0x3			
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
div_sel7	5:4	ADC Channel 7 divider setting	0b00: Divide by 1 0b01: Divide by 2 0b10: Divide by 3 0b11: Divide by 4
ch_sel7	3:0	ADC channel select for register set 7	0x0: ADC0 (see adc_pin_en[0] bit) 0x1: ADC1 (see adc_pin_en[1] bit) 0x2: ADC2 (see adc_pin_en[2] bit) 0x3: Reserved 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved 0x8: $V_{DDIO}/4$ 0x9: $V_{DD18}/2$ 0xA: CAP_VDD/2 0xB: TEMP MON 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

ADC_RR_CTRL0 (0x534)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	adc_rr_run
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
adc_rr_run	0	Enable round robin state machine	0b0: Hold round robin state machine in idle mode, manual ADC control 0b1: Run round robin state machine

ADC_RR_CTRL2 (0x536)

BIT	7	6	5	4	3	2	1	0
Field	adc_rr_sleep_l[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
adc_rr_sleep_l	7:0	Low byte of number of ADC conversion cycles the state machine sleeps between cycles.	0xXX: Low byte of number of ADC conversion cycles

ADC_RR_CTRL3 (0x537)

BIT	7	6	5	4	3	2	1	0
Field	adc_rr_sleep_h[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
adc_rr_sleep_h	7:0	High byte of number of ADC conversion cycles the state machine sleeps between cycles.	0xXX: High byte of number of ADC conversion cycles

ADC_CTRL_4 (0x53E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	adc_pin_en[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
adc_pin_en	2:0	Enable monitoring of selected MFP pins with ADC	0bXX0: Disable monitoring of ADC0 0bXX1: Enable monitoring of ADC0 0bX0X: Disable monitoring of ADC1 0bX1X: Enable monitoring of ADC1 0b0XX: Disable monitoring of ADC2 0b1XX: Enable monitoring of ADC2

UART_PT_0 (0x548)*

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_1_L[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_L	7:0	Custom UART bit length for pass-through UART Channel 1. Set BITLEN_MAN_CFG_1 to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (LSB)	0xXX: Low byte of custom UART bit length for pass-through UART Channel 1

UART_PT_1 (0x549)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_1_H[5:0]					
Reset	–	–	0x05					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_H	5:0	Custom UART bit length for pass-through UART Channel 1. Set BITLEN_MAN_CFG_1 to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (6 MSb)	0xXX: High byte of custom UART bit length for pass-through UART Channel 1

UART_PT_2 (0x54A)*

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_2_L[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_L	7:0	Custom UART bit length for pass-through UART Channel 2. Set BITLEN_MAN_CFG_2 to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (LSB)	0xXX: Low byte of custom UART bit length for pass-through UART Channel 2

UART_PT_3 (0x54B)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_2_H[5:0]					
Reset	–	–	0x05					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_H	5:0	Custom UART bit length for pass-through UART Channel 2. Set BITLEN_MAN_CFG_2 to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (6 MSb)	0xXX: High byte of custom UART bit length for pass-through UART Channel 2

I2C_PT_4 (0x550)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_1[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_1	7:1	I^2C address translator source A When I^2C device address matches SRC_A_1, internal I^2C primary replaces the device address by DST_A_1	0bXXXXXXX: Value of I^2C address translation register

I2C_PT_5 (0x551)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_1[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_1	7:1	I^2C address translator destination A See the description of SRC_A_1.	0bXXXXXXX: Value of I^2C address translation register

I2C_PT_6 (0x552)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_1[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_1	7:1	I^2C address translator source B When I^2C device address matches SRC_B_1, internal I^2C primary replaces the device address by DST_B_1	0bXXXXXXX: Value of I^2C address translation register

I2C_PT_7 (0x553)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_1[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_1	7:1	I^2C address translator destination B See the description of SRC_B_1.	0bXXXXXXX: Value of I^2C address translation register

I2C_PT_8 (0x554)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_2[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_2	7:1	I^2C address translator source A When I^2C device address matches SRC_A_2, internal I^2C primary replaces the device address by DST_A_2	0bXXXXXXX: Value of I^2C address translation register

I2C_PT_9 (0x555)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_2[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_2	7:1	I^2C address translator destination A See the description of SRC_A_2.	0bXXXXXXX: Value of I^2C address translation register

I2C_PT_10 (0x556)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_2[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_2	7:1	I^2C address translator source B When I^2C device address matches SRC_B_2, internal I^2C primary replaces the device address by DST_B_2	0bXXXXXXX: Value of I^2C address translation register

I2C_PT_11 (0x557)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_2[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_2	7:1	I^2C address translator destination B See the description of SRC_B_2.	0bXXXXXXX: Value of I^2C address translation register

HS_VS_X (0x55D)

BIT	7	6	5	4	3	2	1	0
Field	–	DE_DET_X	VS_DET_X	HS_DET_X	–	–	VS_POL_X	HS_POL_X
Reset	–	0x0	0x0	0x0	–	–	0x0	0x0
Access Type	–	Read Only	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DET_X	6	DE activity is detected on Channel X	0x0: DE is not detected 0x1: DE is detected
VS_DET_X	5	VS activity is detected on Channel X	0x0: VS is not detected 0x1: VS is detected
HS_DET_X	4	HS activity is detected on Channel X	0x0: HS is not detected 0x1: HS is detected
VS_POL_X	1	Detected VS polarity on Channel X	0x0: Active low 0x1: Active high
HS_POL_X	0	Detected HS polarity on Channel X	0x0: Active low 0x1: Active high

HS_VS_Y (0x55E)

BIT	7	6	5	4	3	2	1	0
Field	–	DE_DET_Y	VS_DET_Y	HS_DET_Y	–	–	VS_POL_Y	HS_POL_Y
Reset	–	0x0	0x0	0x0	–	–	0x0	0x0
Access Type	–	Read Only	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DET_Y	6	DE activity is detected on Channel Y	0x0: DE is not detected 0x1: DE is detected
VS_DET_Y	5	VS activity is detected on Channel Y	0x0: VS is not detected 0x1: VS is detected
HS_DET_Y	4	HS activity is detected on Channel Y	0x0: HS is not detected 0x1: HS is detected
VS_POL_Y	1	Detected VS polarity on Channel Y	0x0: Active low 0x1: Active high
HS_POL_Y	0	Detected HS polarity on Channel Y	0x0: Active low 0x1: Active high

HS_VS_Z (0x55F)

BIT	7	6	5	4	3	2	1	0
Field	–	DE_DET_Z	VS_DET_Z	HS_DET_Z	–	–	VS_POL_Z	HS_POL_Z
Reset	–	0x0	0x0	0x0	–	–	0x0	0x0
Access Type	–	Read Only	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DET_Z	6	DE activity is detected on Channel Z	0x0: DE is not detected 0x1: DE is detected
VS_DET_Z	5	VS activity is detected on Channel Z	0x0: VS is not detected 0x1: VS is detected
HS_DET_Z	4	HS activity is detected on Channel Z	0x0: HS is not detected 0x1: HS is detected
VS_POL_Z	1	Detected VS polarity on Channel Z	0x0: Active low 0x1: Active high
HS_POL_Z	0	Detected HS polarity on Channel Z	0x0: Active low 0x1: Active high

HS_VS_U (0x56A)

BIT	7	6	5	4	3	2	1	0
Field	–	DE_DET_U	VS_DET_U	HS_DET_U	–	–	VS_POL_U	HS_POL_U
Reset	–	0x0	0x0	0x0	–	–	0x0	0x0
Access Type	–	Read Only	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DET_U	6	DE activity is detected on Channel U	0x0: DE is not detected 0x1: DE is detected

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DET_U	5	VS activity is detected on Channel U	0x0: VS is not detected 0x1: VS is detected
HS_DET_U	4	HS activity is detected on Channel U	0x0: HS is not detected 0x1: HS is detected
VS_POL_U	1	Detected VS polarity on Channel U	0x0: Active low 0x1: Active high
HS_POL_U	0	Detected HS polarity on Channel U	0x0: Active low 0x1: Active high

PM_OV_STAT (0x56C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD[1:0]		OV_LEVEL[1:0]	
Reset	–	–	–	–	0x1		0x1	
Access Type	–	–	–	–			Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
OV_LEVEL	1:0	V_{DDSW} overvoltage comparator trip level Vtrip_ov	0x0: 1.105V + V_{HYST_OV} 0x1: 1.124V + V_{HYST_OV} 0x2: 1.157V + V_{HYST_OV} 0x3: 1.184V + V_{HYST_OV}

EXT0 (0x580)

BIT	7	6	5	4	3	2	1	0
Field	ctrl0_fs_cnt_l[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl0_fs_cnt_l	7:0	FS counter value (low byte) of the VC specified by ctrl0_fs_vc_sel. Only updated when frame count error is detected.	0xXX: The frame count (low byte) of the Frame Start Packet

EXT1 (0x581)

BIT	7	6	5	4	3	2	1	0
Field	ctrl0_fs_cnt_h[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl0_fs_cnt_h	7:0	FS counter value (high byte) of the VC specified by ctrl0_fs_vc_sel. Only updated when frame count error is detected.	0xXX: The frame count (high byte) of the Frame Start Packet

EXT2 (0x582)

BIT	7	6	5	4	3	2	1	0
Field	ctrl0_fe_cnt_l[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl0_fe_cnt_l	7:0	FE counter value (low byte) of the VC specified by ctrl0_fs_vc_sel. Only updated when frame count error is detected.	0xXX: The frame count (low byte) of the Frame End Packet

EXT3 (0x583)

BIT	7	6	5	4	3	2	1	0
Field	ctrl0_fe_cnt_h[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ctrl0_fe_cnt_h	7:0	FE counter value (high byte) of the VC specified by ctrl0_fs_vc_sel. Only updated when frame count error is detected.

EXT4 (0x584)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_fs_cnt_l[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ctrl1_fs_cnt_l	7:0	FS counter value (low byte) of the VC specified by ctrl1_fs_vc_sel. Only updated when frame count error is detected.

EXT5 (0x585)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_fs_cnt_h[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ctrl1_fs_cnt_h	7:0	FS counter value(high byte) of the VC specified by ctrl1_fs_vc_sel. Only updated when frame count error is detected.

EXT6 (0x586)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_fe_cnt_l[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ctrl1_fe_cnt_l	7:0	FE counter value (low byte) of the VC specified by ctrl1_fs_vc_sel. Only updated when frame count error is detected.

EXT7 (0x587)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_fe_cnt_h[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ctrl1_fe_cnt_h	7:0	FE counter value (high byte) of the VC specified by ctrl1_fs_vc_sel. Only updated when frame count error is detected.

EXT8 (0x588)

BIT	7	6	5	4	3	2	1	0
Field	ctrl0_fs_vc_sel[3:0]				ctrl1_fs_vc_sel[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl0_fs_vc_sel	7:4	Selected VC for FS/FE count monitoring on Controller 0	0b0000: Select VC = 0 0b0001: Select VC = 1 0b0010: Select VC = 2 0b0011: Select VC = 3 0b01xx to 0b11xx: Reserved
ctrl1_fs_vc_sel	3:0	Selected VC for FS/FE count monitoring on Controller 1	0b0000: Select VC = 0 0b0001: Select VC = 1 0b0010: Select VC = 2 0b0011: Select VC = 3 0b01xx to 0b11xx: Reserved

SPI_CC_WR_ (0x1300)

SPI/CC bridge write data: When SPI/CC bridge mode is enabled, data written to the address is processed by the SPI bridge function as that which would normally be received by the internal SPI subordinate interface.

This behavior is also true for addresses 0x1301 – 0x137F. This is done to support burst writes on the CC interface.

SPI_CC_RD_ (0x1380)

SPI/CC bridge read data: When SPI/CC bridge mode is enabled, reads from this address return the output of the SPI

Rx FIFO. If the FIFO is not empty (as indicated by BNE), the FIFO advances its read pointer in preparation for the next read from this space. Normally, the SPI subordinate would transmit this data over the SPI interface.

This behavior is also true for addresses 0x1380 – 13FF. This is done to support burst reads on the CC interface. SPIS_BYTE_CNTcan be read to determine the proper burst length to read valid data from the FIFO.

RLMS3 (0x1403)

BIT	7	6	5	4	3	2	1	0
Field	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
Reset	0x0	0x0	0x0	0x0	0x1	–	0x2	
Access Type	Write, Read					–		

BITFIELD	BITS	DESCRIPTION	DECODE
AdaptEn	7	Adapt process enable	0b0: Manual adaptation process disabled 0b1: Manual adaptation process enabled

RLMS4 (0x1404)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
Reset	0x2				0x2		0x0	0x1
Access Type	Write, Read				Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_CHK_AMOUNT	7:4	A factor (N) used to select the order of number of observations in each eye monitor window. N is used in the equation: Observations = 6.29 x $10^{(N + 2)}$	0xX: N factor
EOM_CHK_THR	3:2	Eye-opening monitor number of error bits to allow in a measurement window	0b00: Allow no errors 0b01: Allow 1 error 0b10: Allow 2 errors 0b11: Allow 3 errors
EOM_PER_MODE	1	Eye-opening monitor periodic mode enable	0b0: Eye-opening monitor periodic mode disabled 0b1: Eye-opening monitor periodic mode enabled
EOM_EN	0	Eye-opening monitor enable	0b0: Eye-opening monitor disabled 0b1: Eye-opening monitor enabled

RLMS5 (0x1405)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
Reset	0x0	0x10						
Access Type	Write Only	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_MAN_TRG_REQ	7	Eye-opening monitor manual trigger. For use when periodic mode is disabled.	0b0: No action 0b1: EOM manual trigger request

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_MIN_THR	6:0	The EOM minimum threshold as defined by the following equation: % eye opening = EOM_MIN_THR/64. If the value is zero the EOM is disabled.	0bXXXXXXX: EOM minimum threshold factor

RLMS6 (0x1406)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_PV_MODE	EOM_RST_THR[6:0]						
Reset	0x1	0x00						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_PV_MODE	7	Eye opening is measured vertically or horizontally	0b0: Vertical-opening mode 0b1: Horizonal-opening mode
EOM_RST_THR	6:0	The EOM refresh threshold as defined by the following equation: % eye opening = EOM_MIN_THR/64. If the value is zero the EOM is disabled.	0bXXXXXXX: EOM refresh threshold factor

RLMS7 (0x1407)

BIT	7	6	5	4	3	2	1	0
Field	EOM_DONE	EOM[6:0]						
Reset	0x0	0x00						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_DONE	7	Eye-opening monitor measurement done	0b0: EOM not complete 0b1: EOM complete
EOM	6:0	Last completed EOM observation	0bXXXXXXX: EOM measurement result

RLMS34 (0x1434)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntL	7:0	Eye-monitor period count (RxClk20) LSB	0xXX: Eye-monitor period count (least significant byte)

RLMS35 (0x1435)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntH[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntH	7:0	Eye-monitor period count (RxClk20) MSB	0xXX: Eye-monitor period count (Most Significant Byte)

RLMS37 (0x1437)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
Reset	–	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–			Read Only	Write Only	Write Only	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonDone	4	Eye-monitor period complete (read-only, reset on start)	0b0: Eye-monitor data collection not complete 0b1: Eye-monitor data collection complete
EyeMonCntClr	3	Eye-monitor error/valid count clear (one-shot). Read-back is EyeMonClrPL from long pulse generation.	0b0: NA 0b1: Clear eye-monitor data collection counters
EyeMonStart	2	Eye-monitor start (one-shot). Read-back is EyeMonStClrPL from long pulse generation for both start and clear.	0b0: NA 0b1: Start eye-monitor data collection
EyeMonPh	1	Eye-monitor phase	0b0: Eye-monitor search early phase 0b1: Eye-monitor search late phase
EyeMonDPol	0	Eye-monitor data polarity	0b0: Eye-monitor search for ones 0b1: Eye-monitor search for zeros

RLMS38 (0x1438)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntL	7:0	Eye-monitor error count (read-only)	0xXX: Eye-monitor error count (least significant byte)

RLMS39 (0x1439)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntH	7:0	Eye-monitor error count (read-only)	0xXX: Eye-monitor error count (most significant byte)

RLMS3A (0x143A)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntL	7:0	Eye-monitor valid (hit) count (read-only)	0xXX: Eye-monitor valid count (least significant byte)

RLMS3B (0x143B)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntH	7:0	Eye-monitor valid (hit) count (read-only)	0xXX: Eye-monitor valid count (most significant byte)

RLMS3D (0x143D)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPh[6:0]							RSVD
Reset	0x00							0x1
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPh	7:1	Error-channel phase (read-only)	0bXXXXXXX: 5.6 degrees per step

RLMS3E (0x143E)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTA	ErrChPhSec[6:0]						
Reset	0x1	0x3A						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTA	7	Error-channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSec	6:0	7-bit phase command used for eye monitoring and used during adaptation by the error channel. Value: 7'h3A	0bxxxxxxx: Error-channel phase secondary (odd)

RLMS3F (0x143F)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTA	ErrChPhPri[6:0]						
Reset	0x0	0x79						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTA	7	Error-channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPri	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. Value 7'h79	0bxxxxxxx: Error-channel phase primary (even)

RLMS49 (0x1449)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
Reset	–	0x1	0x1	0x1	0b0	0x0	–	0x1
Access Type	–					Write, Read	–	

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPwrUp	2	Error-channel power-up	0b0: Error-channel power disabled 0b1: Error-channel power enabled

RLMS58 (0x1458)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh1[6:0]						
Reset	–	0x28						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh1	6:0	Error-channel threshold voltage for ones FTSR = 0x30 STFR = 0x20	0bxxxxxxx: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude:: binary amplitude 4.7mV per count

RLMS59 (0x1459)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh0[6:0]						
Reset	–	0x68						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh0	6:0	Error-channel threshold voltage for zeros FTSR = 0x70 STFR = 0x60	0bxxxxxxx: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude:: binary amplitude 4.7mV per count

RLMS64 (0x1464)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
Reset	–	–	–	–	–	0x0	0x0	
Access Type	–	–	–	–	–		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCMode	1:0	Tx spread-spectrum mode	0b00: Spread spectrum disabled 0b01: Reserved 0b10: Reserved 0b11: Spread spectrum enabled (center spread)

RLMS70 (0x1470)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCFrqCtrl[6:0]						
Reset	–	0x01						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCFrqCtrl	6:0	Tx spread-spectrum frequency control	0bXXXXXXX: Tx spread-spectrum center frequency control

RLMS71 (0x1471)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCCenSprSt[5:0]						TxSSCEn
Reset	–	0x01						0x0
Access Type	–	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCCenSprSt	6:1	Tx spread-spectrum center spread startup control	0bXXXXXX: Tx spread-spectrum center spread startup control
TxSSCEn	0	Tx spread spectrum enable	0b0: Tx spread spectrum disabled 0b1: Tx spread spectrum enabled

RLMS72 (0x1472)*

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPreSclL[7:0]							
Reset	0xCF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclL	7:0	Tx spread-spectrum frequency pre-scaler low byte	0xXX: Tx spread-spectrum frequency pre-scaler low byte

RLMS73 (0x1473)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TxSSCPreSclH[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclH	2:0	Tx spread-spectrum frequency pre-scaler high bits	0bXXX: Tx spread-spectrum frequency pre-scaler high bits

RLMS74 (0x1474)*

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPhL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhL	7:0	Tx spread-spectrum interpolator phase low byte	0xXX: Tx spread-spectrum frequency interpolator phase low byte

RLMS75 (0x1475)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCPhH[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhH	6:0	Tx spread-spectrum interpolator phase	0bXXXXXXX: Tx spread-spectrum frequency interpolator phase high bits

RLMS76 (0x1476)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhQuad	1:0	Tx spread-spectrum interpolator phase quadrant	0bXX: Tx spread-spectrum interpolator phase quadrant

RLMS95 (0x1495)

BIT	7	6	5	4	3	2	1	0
Field	TxAmplManEn	RSVD	TxAmplMan[5:0]					
Reset	0x0	0x1	0x29					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
TxAmplManEn	7	Tx amplitude manual override	0b0: Do not manually override Tx amplitude 0b1: Manually override Tx amplitude
TxAmplMan	5:0	Tx amplitude	0bXXXXXX: Binary amplitude 10mV per count

RLMSA4 (0x14A4)*

BIT	7	6	5	4	3	2	1	0
Field	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
Reset	0x3		0x8					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_PER_MULT	7:6	Adaptive EQ period multiplier	0b00: 1ms 0b01: 4ms 0b10: 16ms 0b11: 64ms
AEQ_PER	5:0	Adaptive EQ period Periodic adaptation is disabled when value is 0. Adaptive EQ period is (AEQ_PER value times AEQ_PER_MULT)	0bXXXXXX: Only zeros have a special meaning. See description.

RLMSAC (0x14AC)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						
Reset	0x1	0x4D						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTAFR3G	7	Error-channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecFR3G	6:0	7-bit phase command used for eye monitoring and used during adaptation by the error channel. (fast receive, secondary phase, 3Gbps)	0bXXXXXXX: 7'h4D

RLMSAD (0x14AD)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
Reset	0x0	0x0D						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTAFR3G	7	Error-channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriFR3G	6:0	7-bit phase command used for eye monitoring and used during adaptation by the error channel. (fast receive, primary phase, 3Gbps)	0bXXXXXXX: 7'h0D

RLMSB6 (0x14B6)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTASRG1875	ErrChPhSecSRG1875[6:0]						
Reset	0x1	0x3B						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTASRG1875	7	Error-channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecSRG1875	6:0	7-bit phase command used for eye monitoring and used during adaptation by the error channel. (slow receive, secondary phase, 187.5Mbps)	0bXXXXXXX: 7'h3B

RLMSB7 (0x14B7)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
Reset	0x0	0x7A						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTASRG1875	7	Error-channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriSRG1875	6:0	7-bit phase command used for eye monitoring and used during adaptation by the error channel. (slow receive, primary phase, 187.5Mbps)	0bXXXXXXX: 7'h7A

DPLL_0 (0x1A00)*

BIT	7	6	5	4	3	2	1	0
Field	config_main_state_machine_enable_fref_cal_ss	config_main_state_machine_enable_coarse_cal	config_main_state_machine_enable_divide_cal	config_main_state_machine_enable_fref_cal	config_force_enable	config_enable_func_clk	config_enable_config_clk	config_soft_rst_n
Reset	0x1	0x1	0x1	0x1	0x0	0x1	0x0	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
config_main_state_machine_enable_fref_cal_ss	7	Enables fref CAL SS step of initial PLL enabling
config_main_state_machine_enable_coarse_cal	6	Enables COARSE CAL step of initial PLL enabling
config_main_state_machine_enable_divide_cal	5	Enables DIVIDE CAL step of initial PLL enabling
config_main_state_machine_enable_fref_cal	4	Enables fref CAL step of initial PLL enabling
config_force_enable	3	Bypasses i_en_pll and forces main enable high
config_enable_func_clk	2	Setting this to 1 enables the PLL in functional mode
config_enable_config_clk	1	Setting this to 1 allows writing to functional registers and disables the functional clock, config_regs can always be written.
config_soft_rst_n	0	Setting this to 1 will reset the PLL functional registers, config_regs are not reset.

DPLL_1 (0x1A01)*

BIT	7	6	5	4	3	2	1	0
Field	config_enable_fref_cal	config_enable_integ_delta_sigma	config_enable_divider_delta_sigma	config_main_state_machine_force_recal	config_main_state_machine_enable_fref_recal_ss	config_main_state_machine_enable_coarse_recal	config_main_state_machine_enable_divide_recal	config_main_state_machine_enable_fref_recal
Reset	0x1	0x1	0x1	0x0	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
config_enable_fref_cal	7	Enables the fref_cal module
config_enable_integ_delta_sigma	6	Enables the delta-sigma for the integral path DAC
config_enable_divider_delta_sigma	5	Enables the delta-sigma modulator for the feedback divider
config_main_state_machine_force_recal	4	Write this bit high to force a recalibration (the PLL will loose lock)
config_main_state_machine_enable_fref_recal_ss	3	Enables fref CAL SS step of recalibration (after PLL has been enabled and disabled at least once)
config_main_state_machine_enable_coarse_recal	2	Enables COARSE CAL step of recalibration (after PLL has been enabled and disabled at least once)
config_main_state_machine_enable_divide_recal	1	Enables DIVIDE CAL step of recalibration (after PLL has been enabled and disabled at least once)
config_main_state_machine_enable_fref_recal	0	Enables fref CAL step of recalibration (after PLL has been enabled and disabled at least once)

DPLL_2 (0x1A02)*

BIT	7	6	5	4	3	2	1	0
Field	config_triangle_wave_freq_multiplier[1:0]		config_enable_triangle_wave	config_enable_integ_controller	config_enable_freq_divider_cal	config_enable_state_machine	config_enable_freq_lock_coarse	config_enable_fb_tune
Reset	0x0		0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
config_triangle_wave_freq_multiplier	7:6	The triangle wave frequency can be multiplied by essentially doubling the step size
config_enable_triangle_wave	5	Enables triangle_wave module
config_enable_integ_controller	4	Enables integ_controller module
config_enable_freq_divider_cal	3	Enables freq_divider_cal module

BITFIELD	BITS	DESCRIPTION
config_enable_state_machine	2	Enables the main state machine
config_enable_freq_lock_coarse	1	Enables the coarse frequency locking module
config_enable_fb_tune	0	Enables the fb_tune module

DPLL_3 (0x1A03)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	config_force_enable_ss	config_spread_bit_ratio[2:0]		
Reset	0x1	0x0	0x0	0x0	0x0	0x2		
Access Type					Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
config_force_enable_ss	3	Enables the output of the triangle wave generator (overrides en_ss to force triangle_wave on)	
config_spread_bit_ratio	2:0	Controls the magnitude of the triangle wave input to the divider DSM as a percentage of the nominal divider value. If the configuration registers are reset, the spread_bit_ratio value will not propagate to the triangle wave without rewriting to it. Likewise, if the triangle wave module is reset, the user will need to rewrite to spread_bit_ratio to set it back to the desired value.	000: Off 001: 0.25% 010: 0.5% 011: 1% 100: 2% 101: 4% 110: 4% 111: 4%

DPLL_4 (0x1A04)

BIT	7	6	5	4	3	2	1	0
Field	config_fref_cal_timer_max_ss_L[7:0]							
Reset	0x37							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
config_fref_cal_timer_max_ss_L	7:0	Sets the number of clk_osc cycles to run SS calibration. Value is calculated by: config_fref_cal_timer_max_ss = (150MHz/fosc)*55*(fm/25kHz)

DPLL_5 (0x1A05)

BIT	7	6	5	4	3	2	1	0
Field	config_testout_address[4:0]					config_fref_cal_timer_max_ss_H[2:0]		
Reset	0x0					0x0		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION
config_testout_address	7:3	Address for testout bus
config_fref_cal_timer_max_ss_H	2:0	Sets the number of clk_osc cycles to run SS calibration. Value is calculated by: config_fref_cal_timer_max_ss = (150MHz/fosc)*55*(fm/25kHz)

DPLL_6 (0x1A06)

BIT	7	6	5	4	3	2	1	0
Field	config_fref_cal_timer_max_L[7:0]							
Reset	0x28							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
config_fref_cal_timer_max_L	7:0	Sets the number of clk_osc cycles to run fref calibration. Value is calculated by: config_fref_cal_timer_max = 6GHz/fosc

DPLL_7 (0x1A07)

BIT	7	6	5	4	3	2	1	0
Field	config_div_fb_L	config_div_in[4:0]					config_fref_cal_timer_max_H[1:0]	
Reset	0x0	0x1					0x0	
Access Type	Write, Read	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION
config_div_fb_L	7	Sets the feedback divider value when i_div_use_external = 0
config_div_in	6:2	Sets the divide value of the input divider connected to i_clk_in, the main PLL clock input
config_fref_cal_timer_max_H	1:0	Sets the number of clk_osc cycles to run fref calibration. Value is calculated by: config_fref_cal_timer_max = 6GHz/fosc

DPLL_8 (0x1A08)

BIT	7	6	5	4	3	2	1	0
Field	config_div_fb_H[7:0]							
Reset	0x14							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
config_div_fb_H	7:0	Sets the feedback divider value when i_div_use_external = 0

DPLL_9 (0x1A09)

BIT	7	6	5	4	3	2	1	0
Field	config_div_out_L[4:0]					config_div_fb_exp[2:0]		
Reset	0x8					0x0		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION
config_div_out_L	7:3	Sets the output divider value when i_div_use_external = 0
config_div_fb_exp	2:0	Sets the feedback exponential divider value when i_div_use_external = 0

DPLL_10 (0x1A0A)

BIT	7	6	5	4	3	2	1	0
Field	config_allow_coarse_change	config_div_out_exp[2:0]			config_div_out_H[3:0]			
Reset	0x1	0x0			0x1			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
config_allow_coarse_change	7	When high, the coarse tuning DAC will be allowed to move to correct large changes in the integral path
config_div_out_exp	6:4	Sets the output exponential divider value when i_div_use_external = 0
config_div_out_H	3:0	Sets the output divider value when i_div_use_external = 0

DPLL_12 (0x1A0C)

BIT	7	6	5	4	3	2	1	0
Field	config_int_gain2[3:0]				config_int_gain1[3:0]			
Reset	0x5				0x4			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
config_int_gain2	7:4	Integral gain to use when reference frequency = 13.4 MHz to 23.53 MHz
config_int_gain1	3:0	Integral gain to use when reference frequency < 13.4 MHz

DPLL_13 (0x1A0D)

BIT	7	6	5	4	3	2	1	0
Field	config_int_gain4[3:0]				config_int_gain3[3:0]			
Reset	0xA				0x8			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
config_int_gain4	7:4	Integral gain to use when reference frequency = 47.2 MHz to 95.2 MHz

BITFIELD	BITS	DESCRIPTION
config_int_gain3	3:0	Integral gain to use when reference frequency = 23.53 MHz to 47.2 MHz

DPLL_14 (0x1A0E)

BIT	7	6	5	4	3	2	1	0
Field	config_dac_fine_filter_bw[3:0]				config_int_gain5[3:0]			
Reset	0x8				0xC			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
config_dac_fine_filter_bw	7:4	Changes integral path bandwidth using the following equation: f3dB_i = 0.35/(238ns + 93.71ns*(15-config_dac_fine_filter_bw))
config_int_gain5	3:0	Integral gain to use when reference frequency > 95.2 MHz

DPLL_15 (0x1A0F)

BIT	7	6	5	4	3	2	1	0
Field	config_prop_gain1[4:0]					config_dac_prop_filter_bw[2:0]		
Reset	0x4					0x1		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION
config_prop_gain1	7:3	Proportional gain to use when feedback divider value > 319
config_dac_prop_filter_bw	2:0	Changes proportional path bandwidth using the following equation: f3dB_p = 0.35/(15.0ns + 24.6ns*(7-config_dac_prop_filter_bw))

DPLL_16 (0x1A10)

BIT	7	6	5	4	3	2	1	0
Field	config_prop_gain3_L[2:0]			config_prop_gain2[4:0]				
Reset	0x3			0x5				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION
config_prop_gain3_L	7:5	Proportional gain to use when feedback divider value > 127 and < 192
config_prop_gain2	4:0	Proportional gain to use when feedback divider value > 191 and < 320

DPLL_17 (0x1A11)

BIT	7	6	5	4	3	2	1	0
Field	config_prop_gain5_L	config_prop_gain4[4:0]					config_prop_gain3_H[1:0]	
Reset	0x0	0x10					0x1	
Access Type	Write, Read	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION
config_prop_gain5_L	7	Proportional gain to use when feedback divider value < 64
config_prop_gain4	6:2	Proportional gain to use when feedback divider value > 63 and < 128
config_prop_gain3_H	1:0	Proportional gain to use when feedback divider value > 127 and < 192

DPLL_18 (0x1A12)

BIT	7	6	5	4	3	2	1	0
Field	config_prevent_unlock	config_force_pll_lock	config_prop_subgain[1:0]		config_prop_gain5_H[3:0]			
Reset	0x0	0x0	0x0		0xB			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION
config_prevent_unlock	7	Prevents PLL from becoming unlocked
config_force_pll_lock	6	Forces pll_lock high when PLL enabled
config_prop_subgain	5:4	Proportional subgain
config_prop_gain5_H	3:0	Proportional gain to use when feedback divider value < 64

DPLL_19 (0x1A13)

BIT	7	6	5	4	3	2	1	0
Field	config_div_ds_lowF[2:0]			config_force_div_ds_lowF	config_pll_lock_time[1:0]		config_pll_lock_thresh[1:0]	
Reset	0x2			0x0	0x3		0x2	
Access Type	Write, Read			Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
config_div_ds_lowF	7:5	Delta-sigma divide value when vco_control_coarse < 8
config_force_div_ds_lowF	4	Forces div_delta_sigma to be config_div_ds_lowF
config_pll_lock_time	3:2	Configures PLL lock time
config_pll_lock_thresh	1:0	Configures PLL lock threshold

DPLL_20 (0x1A14)

BIT	7	6	5	4	3	2	1	0
Field	config_pfd_delay_ctrl[1:0]		config_bbpd_mode[1:0]		config_force_disable_dcro	config_div_ds_highF[2:0]		
Reset	0x2		0x0		0x0	0x3		
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION
config_pfd_delay_ctrl	7:6	Increases the delay in the tri-state pfd delay path
config_bbpd_mode	5:4	Selects bbpd mode

BITFIELD	BITS	DESCRIPTION
config_force_disable_dcro	3	When high, forces o_enable_dcro low, otherwise (i_en_PLL | config_force_enable) is used
config_div_ds_highF	2:0	Delta-sigma divide value when vco_control_coarse ≥ 8

DPLL_21 (0x1A15)

BIT	7	6	5	4	3	2	1	0
Field	config_sel_clock_dsm	config_sel_clock_fb	config_int_divider3[1:0]		config_int_divider2[1:0]		config_int_divider1[1:0]	
Reset	0x0	0x0	0x0		0x0		0x0	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
config_sel_clock_dsm	7	When high, clk_dsm going to digital is bypassed and clk_osc is used instead
config_sel_clock_fb	6	When high, the MODout signal of the feedback divider is used (which is needed for divide values of 4-7). Logic already exists to automatically switch this signal based on the divider value, but it can be forced here.
config_int_divider3	5:4	Sets integral path clock divider gain when reference frequency > 47.2 MHz
config_int_divider2	3:2	Sets integral path clock divider gain when reference frequency < 47.2 MHz and > 23.53 MHz
config_int_divider1	1:0	Sets integral path clock divider gain when reference frequency < 23.53 MHz

DPLL_22 (0x1A16)

BIT	7	6	5	4	3	2	1	0
Field	config_spare_ones_H[1:0]		config_shutdown	config_tdc_offset	config_use_internal_div_dsm	config_cdc_double_register	config_dac_coarse_bw_increase	config_en_clock_out_rf
Reset	0x3		0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
config_spare_ones_H	7:6	Spare registers defaulting to 1
config_shutdown	5	When 1, PLL_analog shuts down completely
config_tdc_offset	4	When 1, the tdc_count gets an offset proportional to the gain, 0 offset otherwise
config_use_internal_div_dsm	3	When 1, the internally generated div_dsm will be used for o_dov_dsm, reguardless of div_use_external pin state
config_cdc_double_register	2	When 1, the gray coded select signal coming into integ_delta_sigma is double registered before comparison, otherwise it is single registered for better latency
config_dac_coarse_bw_increase	1	Forces the coarse DRCO DAC bandwidth to increase
config_en_clock_out_rf	0	When high, the DRCO RF clock will output through the clk_rf output pin, otherwise it is gated off

DPLL_23 (0x1A17)

BIT	7	6	5	4	3	2	1	0
Field	config_spare_zeroes[3:0]				–	config_bbpd_gain[2:0]		
Reset	0x0				–	0x6		
Access Type	Write, Read				–	Write, Read		

BITFIELD	BITS	DESCRIPTION
config_spare_zeroes	7:4	Spare registers defaulting to 0
config_bbpd_gain	2:0	Sets the bbpd_scaling_factor

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/19	Initial Release	—
1	4/19	Added future-product designation to MAX9295DGTM/VY+* and MAX9295DGTM/VY+T* in Ordering Information.	60
2	5/19	Removed future-product designation from MAX9295DGTM/VY+* and MAX9295DGTM/VY+T* in Ordering Information	60
3	7/20	Revised Benefits and Features. Updated Absolute Maximum Ratings, Package Information, DC Electrical Characteristics, AC Electrical Characteristics, and Pin Description tables. Updated Product Overview, Video Pipes, Aggregation and Replication, and Dual CSI Video Input Ports sections. Replaced Figure 13 and Figure 14, and updated Figure 15 and Figure 16.	—
4	5/21	Updated GMSL2 MAX values for Power Supply Currents: 3Gbps serial link, two four-lane inputs: • V_{DD} = 1V Range; V_{DD} = 1.2V Range from 240mA to 330mA 3Gbps serial link, one four-lane input: • V_{DD} = 1V Range; V_{DD}= 1.2V Range from 220mA to 330mA 6Gbps serial link, two four-lane inputs: • V_{DD} = 1V Range; V_{DD} =1.2V Range from 300mA to 360mA 6Gbps serial link, one four-lane inputs: • V_{DD} = 1V Range; V_{DD} = 1.2V Range from 275mA to 350mA Updated GMSL1 MAX values for Power Supply Currents: 4.5Gbps serial link, one four-lane inputs: • V_{DD} = 1V Range; V_{DD} = 1.2V Range from 220mA to 295mA	11-12
5	9/23	Global: Updated to Analog Devices' format. Renamed Master and Slave to Main and Subordinate, respectively. EC Table: Updated Note 3 to "Color bar pattern". Rearranged the note numbering. Detailed Description: Paragraphs added and arranged for clarity, understanding and missing information. ESD Protection, Link Lock, Power Up, Device Reset, Stand-by mode.	—
		Register Map: Updated the decodes. Updated descriptions.	
6	11/23	Global: Removed all deserializer part number references. Register Map: Remove all BW_MULTI, BW_VAL, config_sel_clock_out, config_spare_ones_L, and config_pll_mode bitfields.	—

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