

# MOSFET - Power, Single N-Channel, STD Gate, SO8FL

**80 V, 2.55 mΩ, 156 A**  
**NVMFWS2D5N08X**

## Features

- Low  $Q_{RR}$ , Soft Recovery Body Diode
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

## Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives
- Automotive 48 V System

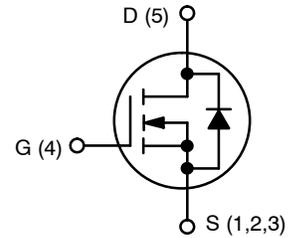
## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	80	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	156
		$T_C = 100^\circ\text{C}$	110
Power Dissipation (Note 1)	$P_D$	133	W
Pulsed Drain Current	$I_{DM}$	$T_C = 25^\circ\text{C}, t_p = 100 \mu\text{s}$	640
Pulsed Source Current (Body Diode)			
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	201	A
Single Pulse Avalanche Energy ( $I_{PK} = 53 \text{ A}$ ) (Note 3)	$E_{AS}$	140	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

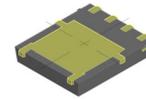
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in<sup>2</sup>, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3.  $E_{AS}$  of 140 mJ is based on started  $T_J = 25^\circ\text{C}$ ,  $I_{AS} = 53 \text{ A}$ ,  $V_{DD} = 64 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ , 100% avalanche tested.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
80 V	2.55 mΩ @ 10 V	156 A



N-CHANNEL MOSFET



DFNW5 (SO-8FL)  
CASE 507BA



2D5N8W = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Assembly Lot Code

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NVMFWS2D5N08XT1G	DFNW5	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.12	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	39	

- Surface-mounted on FR4 board using 1 in<sup>2</sup>, 1 oz. Cu pad.
- $R_{\theta JA}$  is determined by the user's board design.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$ , Referenced to $25^\circ\text{C}$		31.6		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80\text{ V}, T_J = 25^\circ\text{C}$			1	μA
		$V_{DS} = 80\text{ V}, T_J = 125^\circ\text{C}$			250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			100	nA

### ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 37\text{ A}, T_J = 25^\circ\text{C}$		2.2	2.55	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 184\text{ }\mu\text{A}, T_J = 25^\circ\text{C}$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 184\text{ }\mu\text{A}$		-7.5		mV/°C
Forward Transconductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 37\text{ A}$		115		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$		3200		pF
Output Capacitance	$C_{OSS}$			930		
Reverse Transfer Capacitance	$C_{RSS}$			14		
Output Charge	$Q_{OSS}$	$V_{GS} = 6\text{ V}, V_{DD} = 40\text{ V}, I_D = 37\text{ A}$		66		nC
Total Gate Charge	$Q_{G(TOT)}$			28		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DD} = 40\text{ V}, I_D = 37\text{ A}$		45		
Gate-to-Source Charge	$Q_{GS}$			10		
Gate-to-Drain Charge	$Q_{GD}$			15		
Gate Plateau Voltage	$V_{GP}$			7		
Gate Resistance	$R_G$	$f = 1\text{ MHz}$		0.8		Ω

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 64\text{ V},$ $I_D = 37\text{ A}, R_G = 2.5\text{ }\Omega$		24		ns
Rise Time	$t_r$			9		
Turn-Off Delay Time	$t_{d(OFF)}$			36		
Fall Time	$t_f$			6		

### SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 37\text{ A}, T_J = 25^\circ\text{C}$		0.82	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 37\text{ A}, T_J = 125^\circ\text{C}$		0.66		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di/dt = 1000\text{ A}/\mu\text{s},$ $I_S = 37\text{ A}, V_{DD} = 64\text{ V}$		24		ns
Charge Time	$t_a$			13		
Discharge Time	$t_b$			10		
Reverse Recovery Charge	$Q_{RR}$				167	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## TYPICAL CHARACTERISTICS

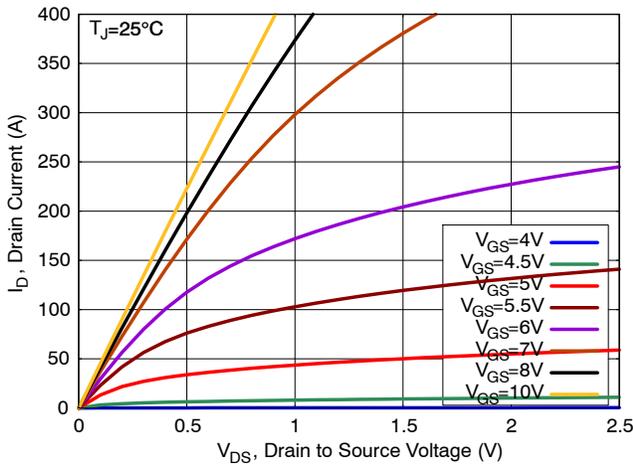


Figure 1. On-Region Characteristics

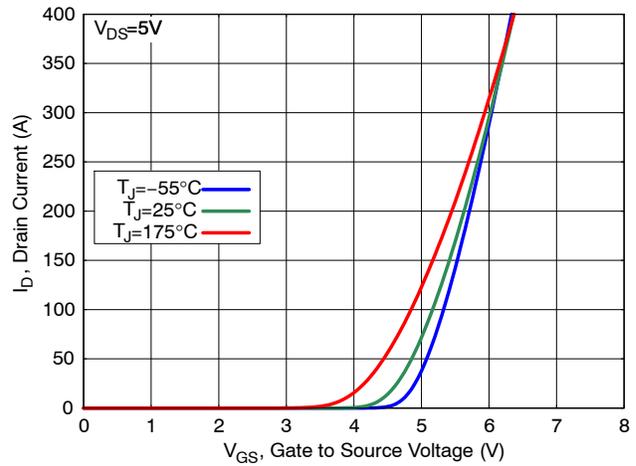


Figure 2. Transfer Characteristics

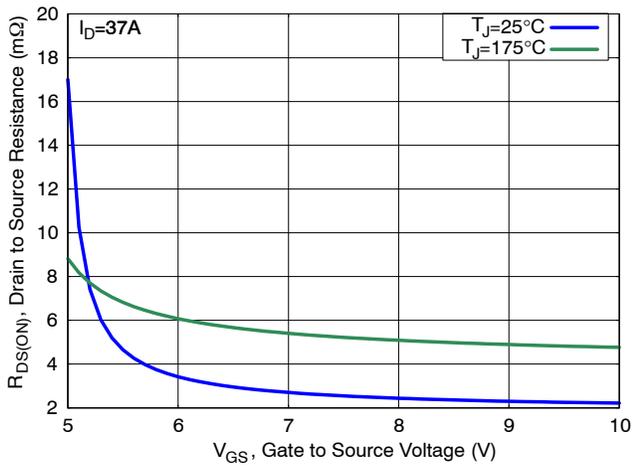


Figure 3. On-Resistance vs. Gate Voltage

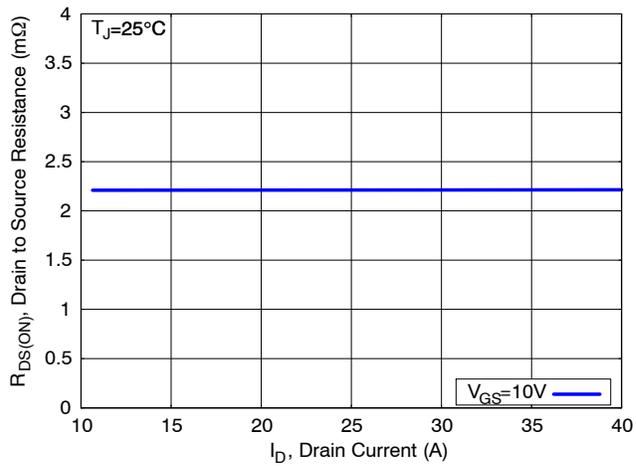


Figure 4. On-Resistance vs. Drain Current

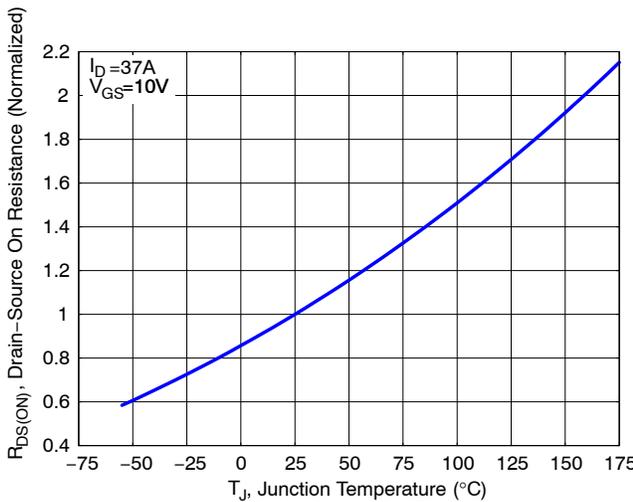


Figure 5. Normalized ON Resistance vs. Junction Temperature

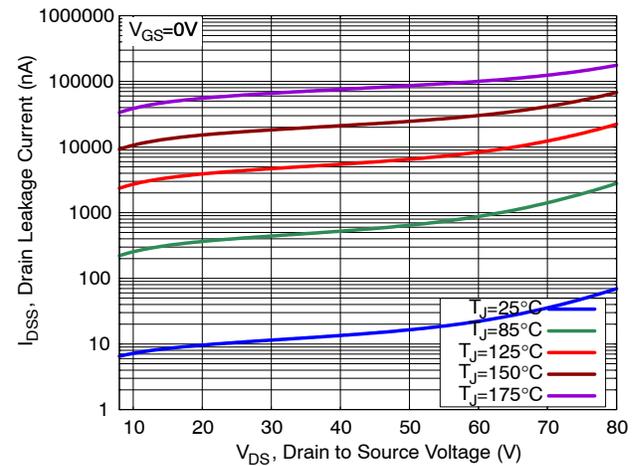


Figure 6. Drain Leakage Current vs. Drain Voltage

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## TYPICAL CHARACTERISTICS

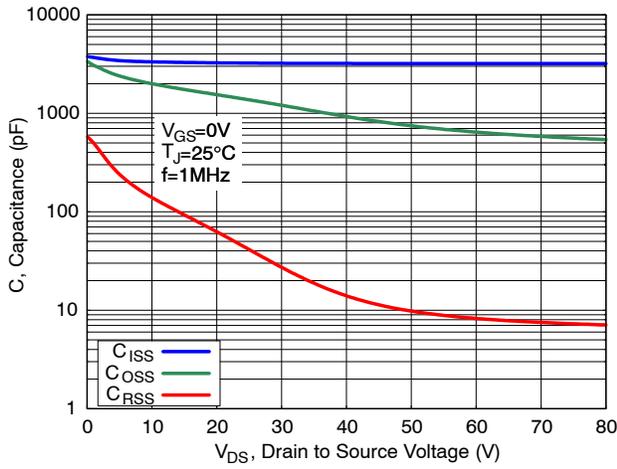


Figure 7. Capacitance Characteristics

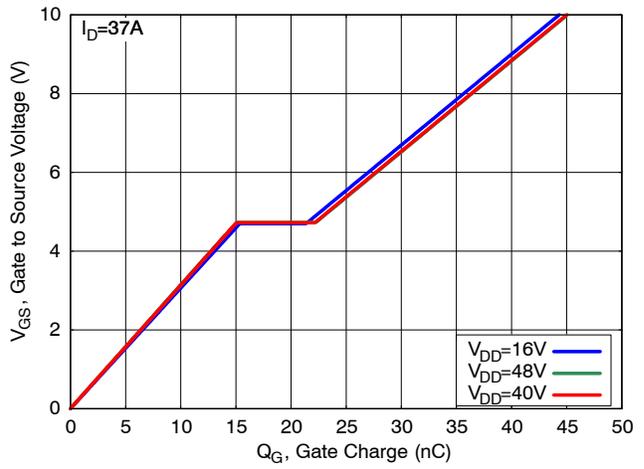


Figure 8. Gate Charge Characteristics

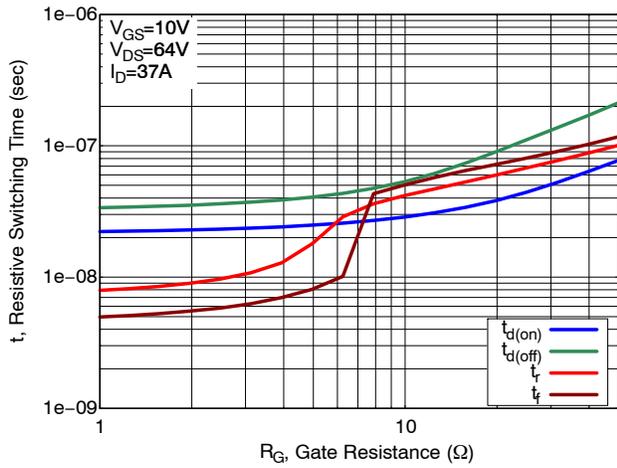


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

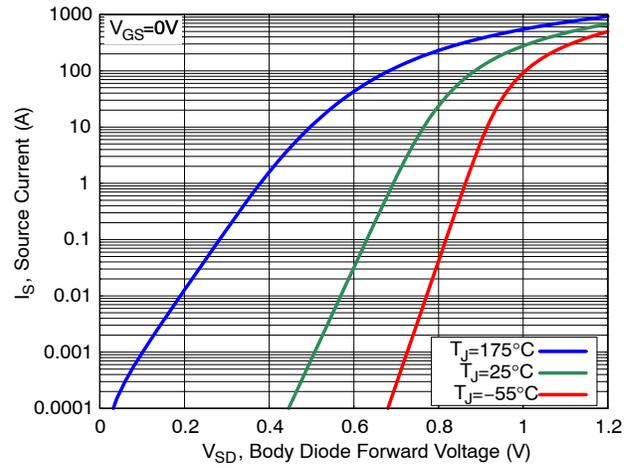


Figure 10. Diode Forward Characteristics

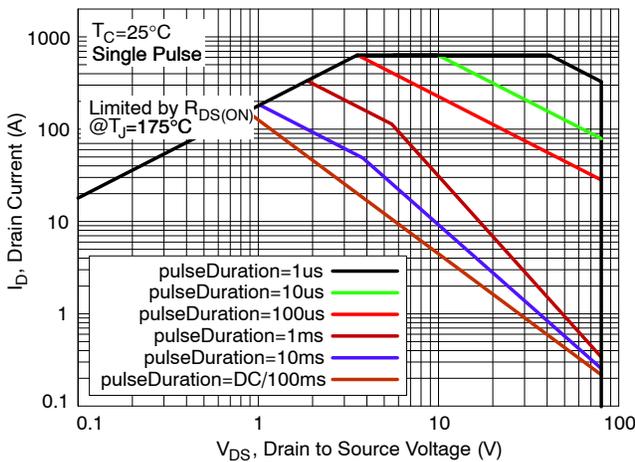


Figure 11. Safe Operating Area (SOA)

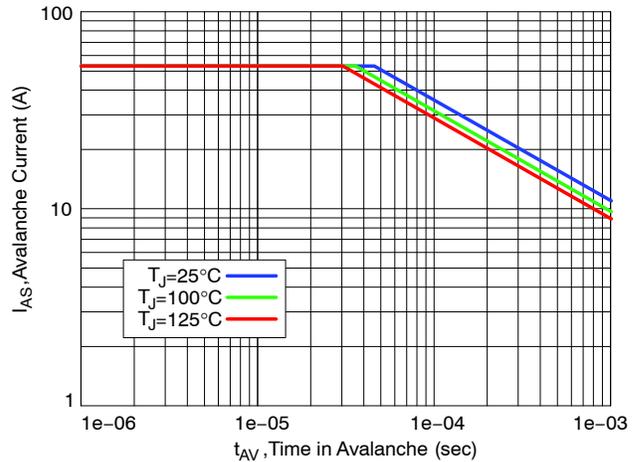
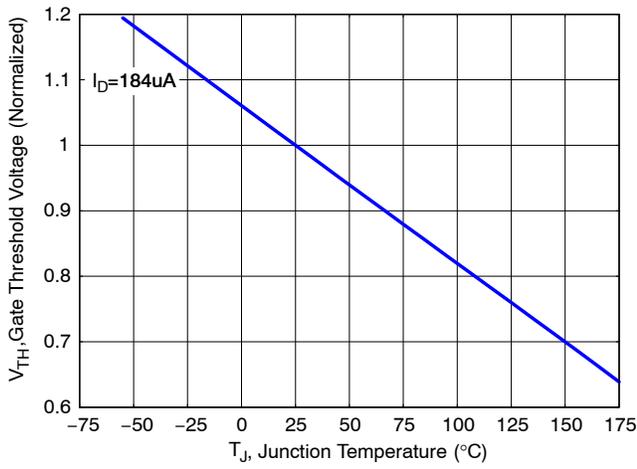


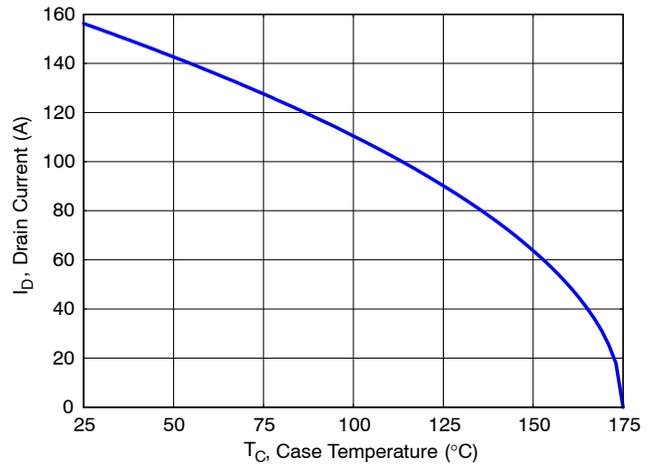
Figure 12. Avalanche Current vs. Pulse Time (UIS)

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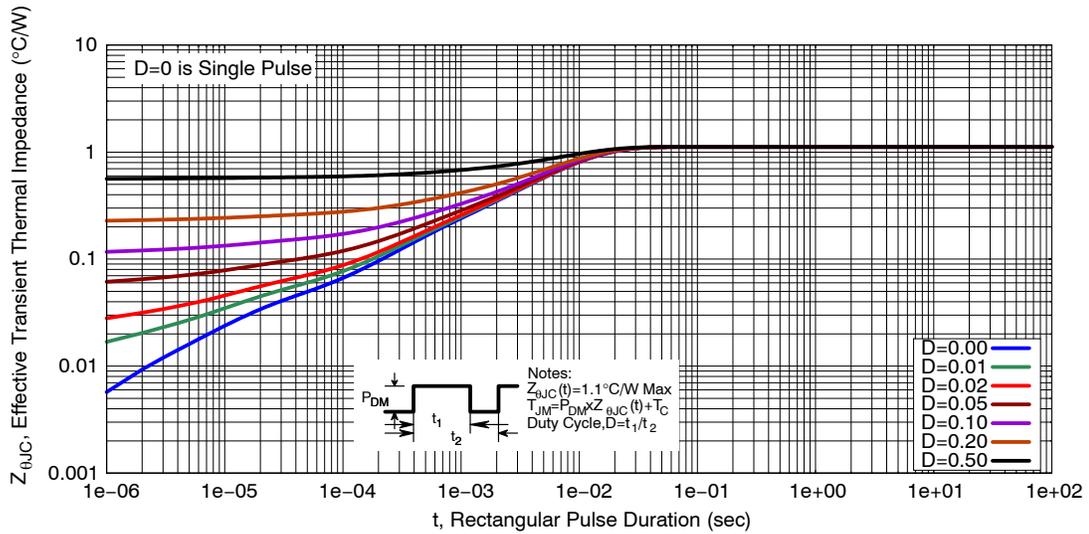
## TYPICAL CHARACTERISTICS



**Figure 13. Gate Threshold Voltage vs. Junction Temperature**



**Figure 14. Maximum Current vs. Case Temperature**

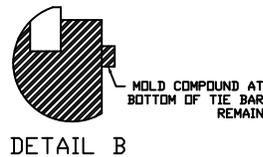
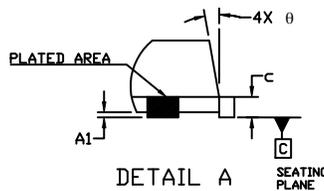
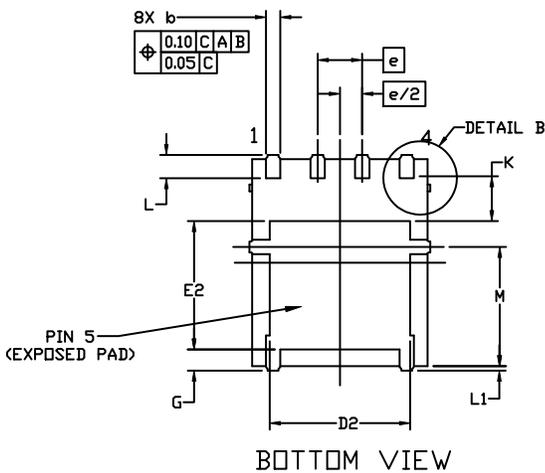
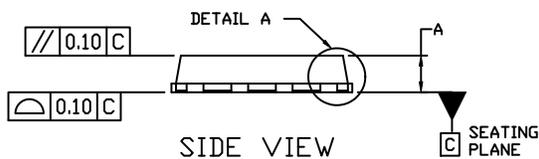
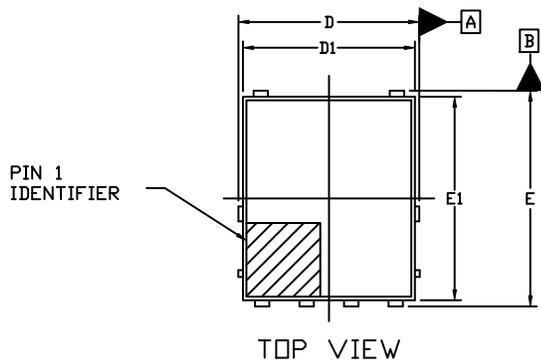


**Figure 15. Transient Thermal Response**

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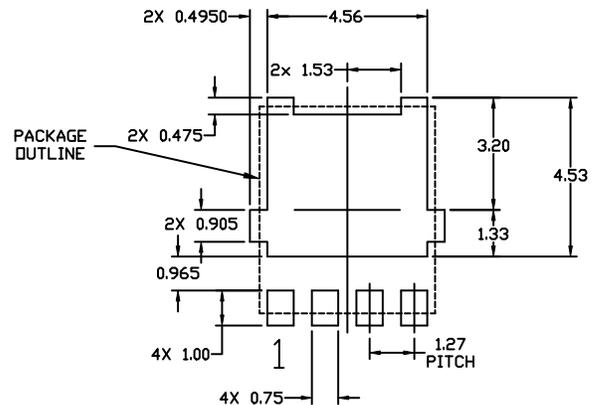
## PACKAGE DIMENSIONS

### DFNW5 5x6 (FULL-CUT SO8FL WF) CASE 507BA ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  2. CONTROLLING DIMENSION: MILLIMETERS
  3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
  4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
$\theta$	0°	---	12°



### RECOMMENDED MOUNTING FOOTPRINT

- \* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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