FEATURES

- Drives up to 32 LCD segments of arbitrary configuration
- CMOS process for: wide supply voltage range, low-power operation, high-noise immunity, wide temperature range
- CMOS and TTL-compatible inputs
- Electrostatic discharge protection on all pins
- Cascadable
- On-chip oscillator
- Requires only three control lines

APPLICATIONS

- Industrial displays
- Consumer product displays
- Telecom product displays
- Automotive dashboard displays

DESCRIPTION

The AY0438 is a CMOS integrated device that drives a liquid crystal display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.

The AY0438 can drive any standard or custom parallel drive LCD display, whether it be field effect or dynamic scattering; 7-, 9-, 14- or 16-segment characters; decimals; leading + or -; or special symbols. Several AY0438 devices can be cascaded. The AC frequency of the LCD waveforms can either be supplied by the user or generated by attaching a capacitor to the LCD input, which controls the frequency of an internal oscillator.

The AY0438 is available in 40-lead dual in-line plastic and 44-lead PLCC packages. Unpackaged dice are also available.
FIGURE 1: PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin # (PDIP Only)</th>
<th>Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>-</td>
<td>Supply voltage</td>
</tr>
<tr>
<td>2</td>
<td>Load</td>
<td>Input</td>
<td>Latch data from registers</td>
</tr>
<tr>
<td>3-29, 32, 33, 37-39</td>
<td>Seg 1-32</td>
<td>Output</td>
<td>Direct drive outputs</td>
</tr>
<tr>
<td>30</td>
<td>BP</td>
<td>Output</td>
<td>Backplane drive output</td>
</tr>
<tr>
<td>31</td>
<td>LCDΦ</td>
<td>Input</td>
<td>Backplane drive input</td>
</tr>
<tr>
<td>34</td>
<td>Data In</td>
<td>Input</td>
<td>Data input to shift register</td>
</tr>
<tr>
<td>35</td>
<td>Data Out</td>
<td>Output</td>
<td>Data output from shift register</td>
</tr>
<tr>
<td>36</td>
<td>VSS</td>
<td>Ground</td>
<td>Ground</td>
</tr>
<tr>
<td>40</td>
<td>Clock</td>
<td>Input</td>
<td>System clock input</td>
</tr>
</tbody>
</table>

FIGURE 2: BLOCK DIAGRAM

FIGURE 3: BACKPLANE AND SEGMENT OUTPUT

FIGURE 4: TIMING DIAGRAM

1.0 OPERATION:

1.1 Data In and Clock

The shift register shifts and outputs on the falling edge of the clock. Every clock falling edge does a logical left shift. As an example, if 32 clock pulses are supplied as in Figure 4, then the data input at the first clock will output at SEG 32, and the last data input (# 32) will output at SEG 1 when a LOAD signal is enabled (Figure 2). It is recommended that a complete 32 bit transfer be done every time the outputs are updated. A logic 1 at the Data In causes the corresponding segment to be enabled or visible, i.e. the output at Segment Output is 180° out-of-phase with the Backplane output (Figure 3).

1.2 Load

A logic 1 at the Load input (Figure 2) causes the parallel load of the data in the shift register into the latches that control the segment drivers. If the Load signal is tied high, then the latches become transparent and the segment drivers are always connected to the shift registers.
1.3 LCD

LCDs can be driven by an external signal or by connecting a capacitor between LCDs and ground (GND), which will enable the on-chip oscillator required to generate the backplane output voltage. Figure 5 shows the relationship between capacitance value and output frequency. Leaving the LCD input unconnected is not recommended. When driven by an external clock, the backplane output is in phase with the input clock. When cascading two AY0438 devices (Figure 6 and Figure 7), the backplane output can be generated using a capacitor to GND on the first AY0438. This backplane output can then be connected to the LCD input of the second AY0438. The backplane output of the second device is then used to drive the backplane of the LCD module.

**FIGURE 5: OSCILLATOR FREQUENCY GRAPH (TYPICAL @ 25°C)**

**FIGURE 6: CASCADING TWO AY0438 DEVICES**

**FIGURE 7: CASCADE TIMING DIAGRAM**
1.4 General

In order to avoid any race conditions, the Data In and Load signals should not be changed during a falling edge of the Clock. Figure 4 and Figure 7 show a typical timing diagram for a 32 segment and 64 segment LCD module.

1.5 Interfacing to a LCD Module and PIC16CXX Device

Figure 8 shows a typical layout of an AY0438 connected to a LCD module and interfaced to a PIC16CXX family device. Example 1 lists code used to program the PIC16CXX device. This code was compiled using MPASM.

EXAMPLE 1: EXAMPLE CODE

;***********************************************************************
;This program shows an interface between a PIC16CXX device
;and the AY0438 LCD controller to control a 7 Segment
;4 digit LCD module.
;The PIC16CXX interface to the AY0438 Hardware:
;
; PORTB bit 0 --> CLK
; PORTB bit 1 --> DATA IN
; PORTB bit 2 --> LOAD
;
;The LCD module is connected to the AY0438 as follows:
;
; Most Significant digit --> seg1 to seg7
; 3rd Significant digit --> seg9 to seg15
; 2nd Significant digit --> seg17 to seg23
; Least Significant digit --> seg25 to seg31
;
;The DP are not connected, but can be connected to seg8, 16, 24 & 32.
;For each digit, the segments are connected as:
; Seg A --> seg(8*n + 1)
; Seg B --> seg(8*n + 2)
; Seg C --> seg(8*n + 3)
; Seg D --> seg(8*n + 4)
; Seg E --> seg(8*n + 5)
; Seg F --> seg(8*n + 6)
; Seg G --> seg(8*n + 7)
;where n = 0, 1, 2 and 3 for MSD, 3rdSD, 2ndSD and LSD respectively.
;The firmware uses the values in registers:
; MSD, THRDSD, SCNDSD and LSD to determine the values to be
;pulsed to the AY0438.
;In this example, a pushbutton connected to PORTB bit 7
;is checked periodically to see if it has been pressed. If so,
;the LCD values in locations MSD to LSD are updated.

;*************************************************************************
list p=16c71,f=inhx8m

;
;
MSD equ 0x20
THRDSD equ 0x21
SCNDSD equ 0x22
LSD equ 0x23
count equ 0x24
temp equ 0x25
PORTB equ 0x06
#define CLK PORTB,0
#define DATAIN PORTB,1
#define LOAD PORTB,2
#define UPDATELCD PORTB,7
w equ 0
STATUS equ 0x03
C equ 0
RP0 equ 5
OPTION equ 0x81
RBPU equ 7
PCL equ 0x02
PCLATH equ 0x0A
;
;
org 0
goto start
org 0x10
;
;This DecodeValue table must reside in page 0 for this program to work
;
DecodeValue
addwf PCL
retlw B'00111111' ;decode for 0
retlw B'00000110' ;decode for 1
retlw B'01011011' ;decode for 2
retlw B'01001111' ;decode for 3
retlw B'01100110' ;decode for 4
retlw B'01101101' ;decode for 5
retlw B'01111101' ;decode for 6
retlw B'00000111' ;decode for 7
retlw B'01111111' ;decode for 8
retlw B'01101111' ;decode for 9

start
clrf PORTB ;set portb 0,1&2 as outputs
bsf STATUS,RP0
movlw B'11111000' ;
movwf PORTB ;
bcf OPTION,RBPU ;enable pull-up for switch
bcf STATUS,RP0

wait
btfsc UPDATELCD ;see if update switch is low
goto wait ;no then wait
bcf LOAD ;make sure load is disabled
movf LSD,w ;get least significant value
clrf PCLATH ;PCH = 0
call DecodeValue ;decode the value
call Send8 ;serially output the seg values
movf SCNDSD,w ;get 2nd significant digit
call DecodeValue ;decode it
call Send8 ;serially output it
movf THRDSD,w ;get 3rd significant digit
call DecodeValue ;decode it
call Send8
movf MSD,w ;get Most significant value
call DecodeValue ;decode it
call Send8 ;serially send it
bsf LOAD ;toggle the LOAD line
bcf LOAD ;to enable the latches

KeyReleased
btfss UPDATELCD ;wait for key to be released
goto KeyReleased ;repeat loop.
goto wait ;repeat loop.

;Send8, sends the 8 bits in the W register
Send8
movwf temp ;save in temp
movlw .8 ;init count
movwf count ;to 8

sendloop
bcf DATAIN ;make sure DATAIN is low
rrf temp ;rotate value through carry
btfsc STATUS,C ;if bit clear then skip
bsf DATAIN ;else set data bit
bsf CLK ;toggle clock
bcf CLK ;
decfsz count ;see if 8 done
goto sendloop ;no then do all
return ;else return

end
2.0 ELECTRICAL CHARACTERISTICS

**Maximum Ratings**

- **VDD**:...-0.3V to +12V
- **Inputs (CLK, Data In, Load)**:...Vcc to Vdd +0.3V
- **LCDΦ Input**:...-0.3V to Vdd +0.3V
- **Power Dissipation**:250 mW
- **Storage Temperature**:...-65˚C to +125˚C
- **Operating Temperature Industrial**:...-40˚C to +85˚C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**TABLE 2: DC CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>VDD</td>
<td>+3.0</td>
<td></td>
<td>+8.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Supply Current</td>
<td>IDD</td>
<td></td>
<td>25</td>
<td>60</td>
<td>µA</td>
<td>LCDΦ OSC &lt; 15 kHz</td>
</tr>
<tr>
<td>Input High Level</td>
<td>VIH</td>
<td>0.5</td>
<td>Vdd</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Low Level Clock</td>
<td>VIL1</td>
<td>0</td>
<td></td>
<td>0.1</td>
<td>Vdd</td>
<td>3.0V ≤ Vdd ≤ 8.5V</td>
</tr>
<tr>
<td>Input Low Level Data, LCDΦ Input</td>
<td>VIL2</td>
<td>0</td>
<td></td>
<td>0.1</td>
<td>Vdd</td>
<td>3.0V ≤ Vdd ≤ 8.5V</td>
</tr>
<tr>
<td>Input Leakage Current Load</td>
<td>IL</td>
<td></td>
<td>0.01</td>
<td>±10</td>
<td>µA</td>
<td>Vin = 0V and +5.0V</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>CI</td>
<td></td>
<td></td>
<td>5.0</td>
<td>pF</td>
<td>VDD = +5.0V</td>
</tr>
<tr>
<td>Segment Output Voltage</td>
<td>VOH</td>
<td>0.8</td>
<td>Vdd</td>
<td></td>
<td>V</td>
<td>IOH = -100 µA</td>
</tr>
<tr>
<td></td>
<td>VOL</td>
<td>0</td>
<td></td>
<td>0.1</td>
<td>Vdd</td>
<td>IOL = 100 µA</td>
</tr>
<tr>
<td>LCDΦ Input High Level</td>
<td>VIN</td>
<td>0.9</td>
<td>Vdd</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>LCDΦ Input Low Level</td>
<td>VIL</td>
<td>0</td>
<td></td>
<td>0.1</td>
<td>Vdd</td>
<td></td>
</tr>
<tr>
<td>LCDΦ Input Leakage</td>
<td>IL</td>
<td></td>
<td></td>
<td>10</td>
<td>µA</td>
<td>Vin = 0V and +5.0V</td>
</tr>
</tbody>
</table>

**TABLE 3: AC CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Rate</td>
<td>f</td>
<td>DC</td>
<td></td>
<td>1.5</td>
<td>MHz</td>
<td>50% duty cycle</td>
</tr>
<tr>
<td>Data Set-up Time</td>
<td>tDS</td>
<td>150</td>
<td></td>
<td></td>
<td>nsec</td>
<td>Data change to Clk falling edge</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>tDH</td>
<td>50</td>
<td></td>
<td></td>
<td>nsec</td>
<td></td>
</tr>
<tr>
<td>Load Pulse Width</td>
<td>tPW</td>
<td>175</td>
<td></td>
<td></td>
<td>nsec</td>
<td></td>
</tr>
<tr>
<td>Data Out Prop. Delay</td>
<td>tPD</td>
<td></td>
<td>500</td>
<td></td>
<td>nsec</td>
<td>CL = 55 pF</td>
</tr>
</tbody>
</table>
AY0438 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

<table>
<thead>
<tr>
<th>PACK NO.</th>
<th>X</th>
<th>/XX</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Package:  
P = Plastic DIP  
L = PLCC  
S = Die in Waffle Pack

Temperature Range:  
- = 0°C to +70°C  
I = 40°C to +85°C

Device: 32 Segment LCD Driver

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