



## Product Change Notification / SYST-03CEKA564

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### Date:

04-Jun-2024

### Product Category:

Complementary MOSFET Arrays

### PCN Type:

Document Change

### Notification Subject:

Data Sheet - TC6320 N-Channel and P-Channel Enhancement-Mode MOSFET Pair Data Sheet

### Affected CPNs:

[SYST-03CEKA564\\_Affected\\_CPN\\_06042024.pdf](#)

[SYST-03CEKA564\\_Affected\\_CPN\\_06042024.csv](#)

### Notification Text:

SYST-03CEKA564

Microchip has released a new Datasheet for the TC6320 N-Channel and P-Channel Enhancement-Mode MOSFET Pair Data Sheet of devices. If you are using one of these devices please read the document located at [TC6320 N-Channel and P-Channel Enhancement-Mode MOSFET Pair Data Sheet](#).

**Notification Status:** Final

**Description of Change:**

- Modified Section "Package Types" from 5-lead DFN to 8-lead VDFN.
- Updated Section 4.1 "Package Marking Information" with the latest Package Drawings.

**Impacts to Data Sheet:** See above details

**Reason for Change:** To improve productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 04 Jun 2024

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

[TC6320 N-Channel and P-Channel Enhancement-Mode MOSFET Pair Data Sheet](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

## Terms and Conditions:

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Affected Catalog Part Numbers (CPN)

TC6320TG-G

TC6320TG-G-D607

TC6320TG-G-D626

TC6320K6-G

TC6320K6-G-D626

## N-Channel and P-Channel Enhancement-Mode MOSFET Pair

### Features

- Integrated Gate-to-source Resistor
- Integrated Gate-to-source Zener Diode
- Low Threshold
- Low On-resistance
- Low Input Capacitance
- Fast Switching Speeds
- Free from Secondary Breakdown
- Low Input and Output Leakage
- Independent Electrically Isolated N-channel and P-channel

### Applications

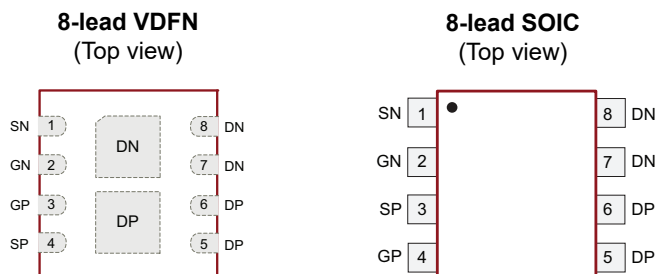
- High-voltage Pulsers
- Amplifiers
- Buffers
- Piezoelectric Transducer Drivers
- General Purpose Line Drivers
- Logic-level Interfaces

### General Description

The TC6320 consists of high-voltage, low-threshold N-channel and P-channel MOSFETs in 8-lead VDFN and SOIC packages. Both MOSFETs have integrated gate-to-source resistors and gate-to-source Zener diode clamps which are desired for high-voltage pulser applications. It is a complimentary, high-speed, high-voltage, gate-clamped N-channel and P-channel MOSFET pair, which utilizes an advanced vertical DMOS structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast-switching speeds are desired.

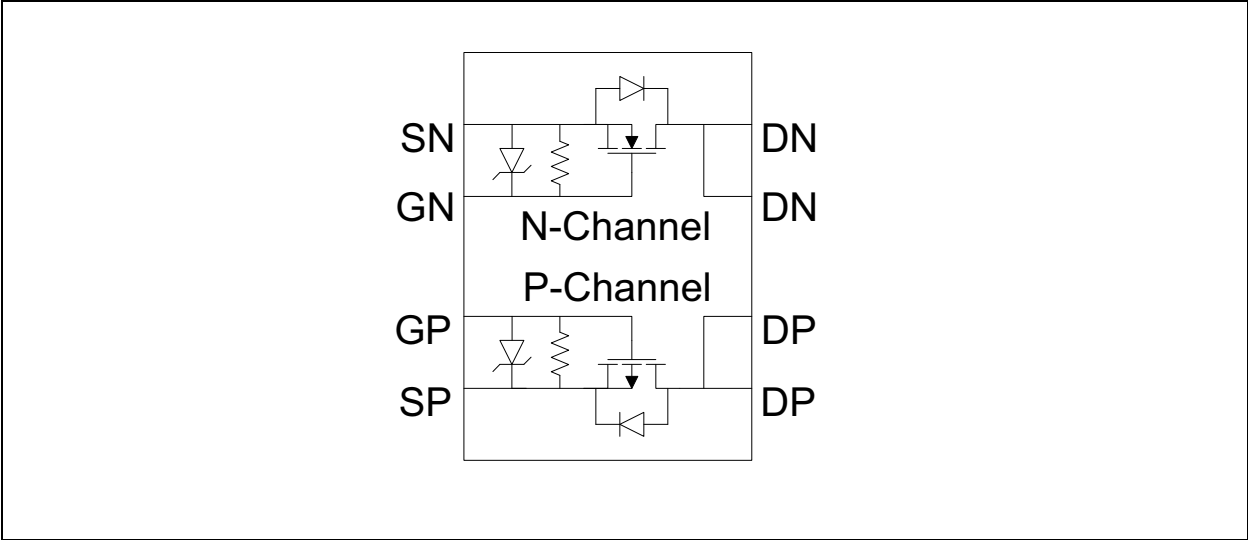
### Package Types



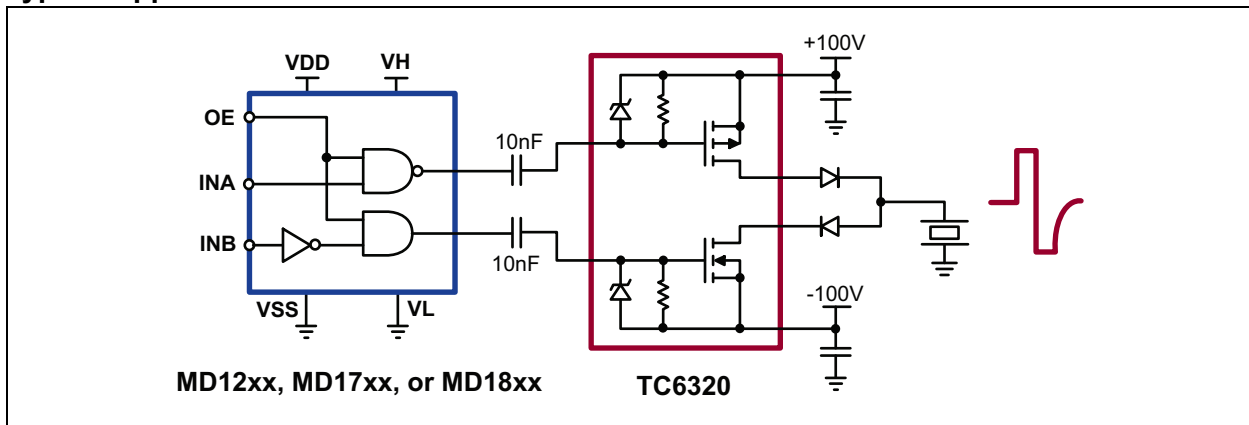
See [Table 2-1](#) and [Table 2-2](#) for pin information.

# TC6320

Functional Block Diagram



## Typical Application Circuit



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Drain-to-source Voltage .....	$BV_{DSS}$
Drain-to-gate Voltage .....	$BV_{DGS}$
Operating Ambient Temperature, $T_A$ .....	-55°C to +150°C
Storage Temperature, $T_S$ .....	-55°C to +150°C

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

### N-CHANNEL ELECTRICAL CHARACTERISTICS

**Electrical Specifications:**  $T_A = T_J = 25^\circ\text{C}$  unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
DC PARAMETER (Note 1 unless otherwise specified)						
Drain-to-source Breakdown Voltage	$BV_{DSS}$	200	—	—	V	$V_{GS} = 0V, I_D = 2\text{ mA}$
Gate Threshold Voltage	$V_{GS(th)}$	1	—	2	V	$V_{GS} = V_{DS}, I_D = 1\text{ mA}$
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	-4.5	mV/°C	$V_{GS} = V_{DS}, I_D = 1\text{ mA}$ (Note 2)
Gate-to-source Shunt Resistor	$R_{GS}$	10	—	50	kΩ	$I_{GS} = 100\text{ }\mu\text{A}$
Gate-to-Source Zener Voltage	$V_{ZGS}$	13.2	—	25	V	$I_{GS} = 2\text{ mA}$
Zero-gate Voltage Drain Current	$I_{DSS}$	—	—	10	μA	$V_{DS} = \text{Maximum rating}, V_{GS} = 0V$
		—	—	1	mA	$V_{DS} = 0.8\text{ Maximum rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$ (Note 2)
On-state Drain Current	$I_{D(ON)}$	1	—	—	A	$V_{GS} = 4.5V, V_{DS} = 25V$
		2	—	—		$V_{GS} = 10V, V_{DS} = 25V$
Static Drain-to-source On-state Resistance	$R_{DS(ON)}$	—	—	8	Ω	$V_{GS} = 4.5V, I_D = 150\text{ mA}$
		—	—	7		$V_{GS} = 10V, I_D = 1A$
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1	%/°C	$V_{GS} = 4.5V, I_D = 150\text{ mA}$ (Note 2)
AC PARAMETER (Note 2)						
Forward Transconductance	$G_{FS}$	400	—	—	mmho	$V_{DS} = 25V, I_D = 500\text{ mA}$
Input Capacitance	$C_{ISS}$	—	—	110	pF	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1\text{ MHz}$
Common Source Output Capacitance	$C_{OSS}$	—	—	60	pF	
Reverse Transfer Capacitance	$C_{RSS}$	—	—	23	pF	
Turn-on Delay Time	$t_{d(ON)}$	—	—	10	ns	$V_{DD} = 25V,$ $I_D = 1A,$ $R_{GEN} = 25\Omega$
Rise Time	$t_r$	—	—	15	ns	
Turn-off Delay Time	$t_{d(OFF)}$	—	—	20	ns	
Fall Time	$t_f$	—	—	15	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	$V_{SD}$	—	—	1.8	V	$V_{GS} = 0V, I_{SD} = 500\text{ mA}$ (Note 1)
Reverse Recovery Time	$t_{rr}$	—	300	—	ns	$V_{GS} = 0V, I_{SD} = 500\text{ mA}$ (Note 2)

**Note 1:** All DC parameters are 100% tested at  $25^\circ\text{C}$  unless otherwise stated. Pulse test: 300  $\mu\text{s}$  pulse, 2% duty cycle.

**2:** Specification is obtained by characterization and is not 100% tested.

## P-CHANNEL ELECTRICAL CHARACTERISTICS

Electrical Specifications: T <sub>A</sub> = T <sub>J</sub> = 25°C unless otherwise specified.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
DC PARAMETER (Note 1 unless otherwise specified)						
Drain-to-source Breakdown Voltage	BV <sub>DSS</sub>	-200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -2 mA
Gate Threshold Voltage	V <sub>GS(th)</sub>	-1	—	-2.4	V	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -1 mA
Change in V <sub>GS(th)</sub> with Temperature	ΔV <sub>GS(th)</sub>	—	—	4.5	mV/°C	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -1 mA (Note 2)
Gate-to-source Shunt Resistor	R <sub>GS</sub>	10	—	50	kΩ	I <sub>GS</sub> = 100 μA
Gate-to-Source Zener Voltage	VZ <sub>GS</sub>	13.2	—	25	V	I <sub>GS</sub> = -2 mA
Zero-gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-10	μA	V <sub>DS</sub> = Maximum rating, V <sub>GS</sub> = 0V
		—	—	-1	mA	V <sub>DS</sub> = 0.8 Maximum rating, V <sub>GS</sub> = 0V, T <sub>A</sub> = 125°C (Note 2)
On-state Drain Current	I <sub>D(ON)</sub>	-1	—	—	A	V <sub>GS</sub> = -4.5V, V <sub>DS</sub> = -25V
		-2	—	—		V <sub>GS</sub> = -10V, V <sub>DS</sub> = -25V
Static Drain-to-source On-state Resistance	R <sub>DS(ON)</sub>	—	—	10	Ω	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -150 mA
		—	—	8		V <sub>GS</sub> = -10V, I <sub>D</sub> = -1A
Change in R <sub>DS(ON)</sub> with Temperature	ΔR <sub>DS(ON)</sub>	—	—	1	%/°C	V <sub>GS</sub> = -10V, I <sub>D</sub> = -200 mA (Note 2)
AC PARAMETER (Note 2)						
Forward Transconductance	G <sub>FS</sub>	400	—	—	mmho	V <sub>DS</sub> = -25V, I <sub>D</sub> = -500 mA
Input Capacitance	C <sub>ISS</sub>	—	—	200	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -25V, f = 1 MHz
Common Source Output Capacitance	C <sub>OSS</sub>	—	—	55	pF	
Reverse Transfer Capacitance	C <sub>RSS</sub>	—	—	30	pF	
Turn-on Delay Time	t <sub>d(ON)</sub>	—	—	10	ns	V <sub>DD</sub> = -25V, I <sub>D</sub> = -1A, R <sub>GEN</sub> = 25Ω
Rise Time	t <sub>r</sub>	—	—	15	ns	
Turn-off Delay Time	t <sub>d(OFF)</sub>	—	—	20	ns	
Fall Time	t <sub>f</sub>	—	—	15	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V <sub>SD</sub>	—	—	-1.8	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = -500 mA (Note 1)
Reverse Recovery Time	t <sub>rr</sub>	—	300	—	ns	V <sub>GS</sub> = 0V, I <sub>SD</sub> = -500 mA (Note 2)

**Note 1:** All DC parameters are 100% tested at  $25^\circ\text{C}$  unless otherwise stated. Pulse test: 300  $\mu\text{s}$  pulse, 2% duty cycle.

**2:** Specification is obtained by characterization and is not 100% tested.

## TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, for all specifications $T_A = T_J = +25^\circ\text{C}$ .						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Operating Ambient Temperature	$T_A$	-55	—	+150	$^\circ\text{C}$	
Storage Temperature	$T_S$	-55	—	+150	$^\circ\text{C}$	
<b>PACKAGE THERMAL RESISTANCE</b>						
8-lead VDFN	$\theta_{JA}$	—	44	—	$^\circ\text{C/W}$	Note 1
8-lead SOIC	$\theta_{JA}$	—	101	—	$^\circ\text{C/W}$	Note 1

**Note 1:** 1 oz., four-layer, 3" x 4" PCB



# TC6320

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## 2.0 PIN DESCRIPTION

Table 2-1 and Table 2-2 show the description of pins in TC6320 8-lead VDFN and 8-lead SOIC, respectively. Refer to [Package Types](#) for the location of pins.

**TABLE 2-1: 8-LEAD VDFN PIN FUNCTION TABLE**

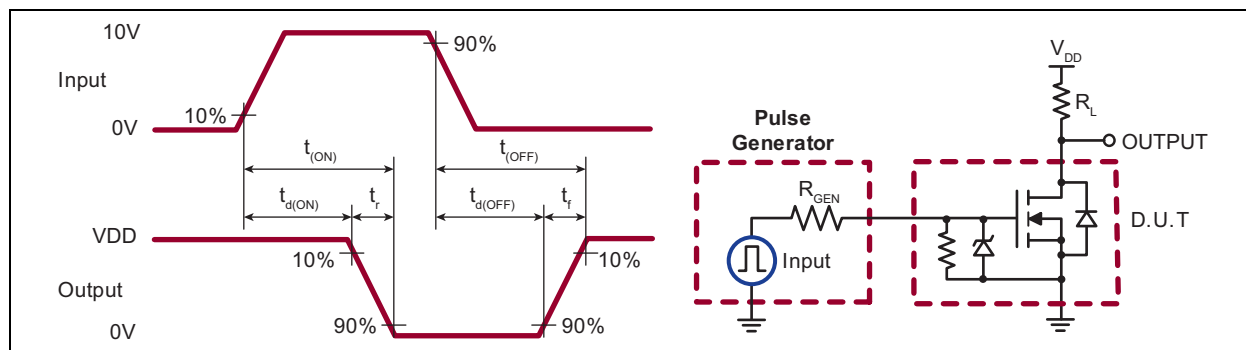
Pin Number	Pin Name	Description
1	SN	Source N-channel
2	GN	Gate N-channel
3	GP	Gate P-channel
4	SP	Source P-channel
5	DP	Drain P-channel
6	DP	Drain P-channel
7	DN	Drain N-channel
8	DN	Drain N-channel

**TABLE 2-2: 8-LEAD SOIC FUNCTION TABLE**

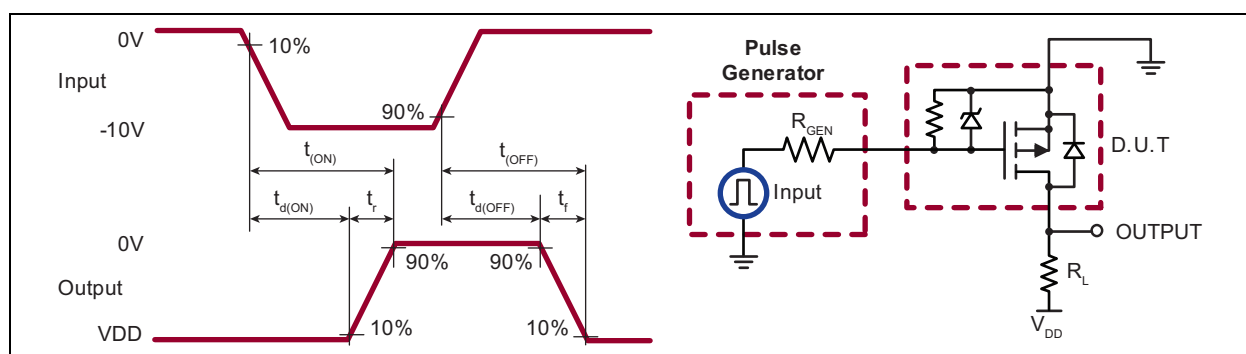
Pin Number	Pin Name	Description
1	SN	Source N-channel
2	GN	Gate N-channel
3	SP	Source P-channel
4	GP	Gate P-channel
5	DP	Drain P-channel
6	DP	Drain P-channel
7	DN	Drain N-channel
8	DN	Drain N-channel

## 3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 and Figure 3-2 illustrate the switching waveforms and test circuits for TC6320.



**FIGURE 3-1:** N-Channel Switching Waveforms and Test Circuit.



**FIGURE 3-2:** P-Channel Switching Waveforms and Test Circuit.

## PRODUCT SUMMARY

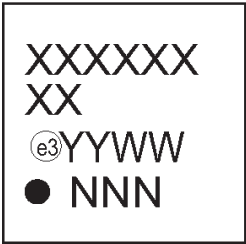
$BV_{DSS}/BV_{DGS}$ (V)		$R_{DS(ON)}$ (Maximum) ( $\Omega$ )	
N-Channel	P-Channel	N-Channel	P-Channel
200	-200	7	8

# TC6320

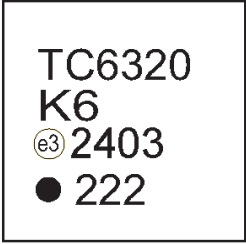
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

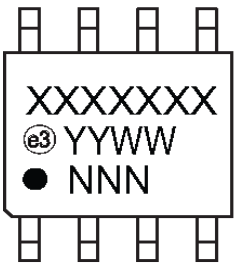
8-lead VDFN



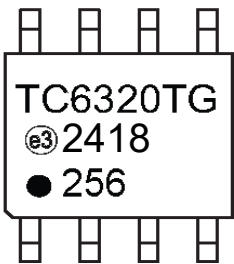
Example



8-lead SOIC



Example



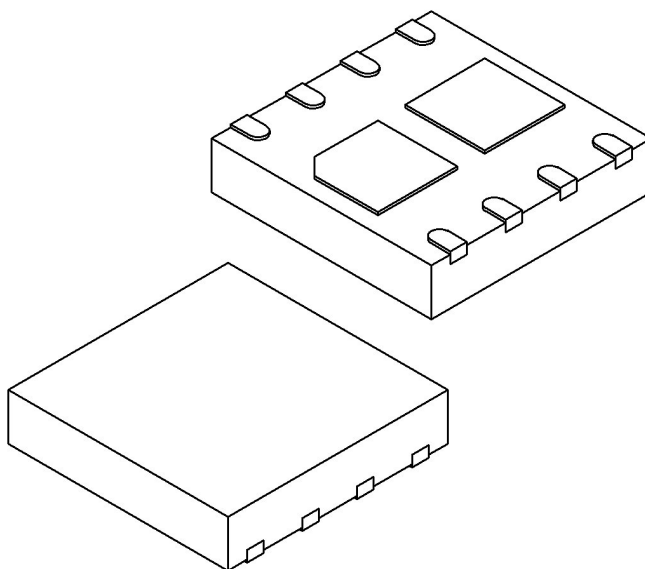
<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. The package may or not include the corporate logo.	



# TC6320

## 8-Lead Very Thin Plastic Quad Flat, No Lead Package (8RX) - 4x4x0.9 mm Body [VQFN] With Dual 1.45mm Exposed Pads

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	1.00 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	–	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	4.00 BSC		
Exposed Pad Length (X2)	D2	1.35	1.45	1.55
Overall Width	E	4.00 BSC		
Exposed Pad Width (X2)	E2	1.35	1.45	1.55
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.40	0.50	0.60
Exposed Pad to Exposed Pad	K1	0.50 REF		
Terminal to Exposed Pad	K2	0.775 REF		

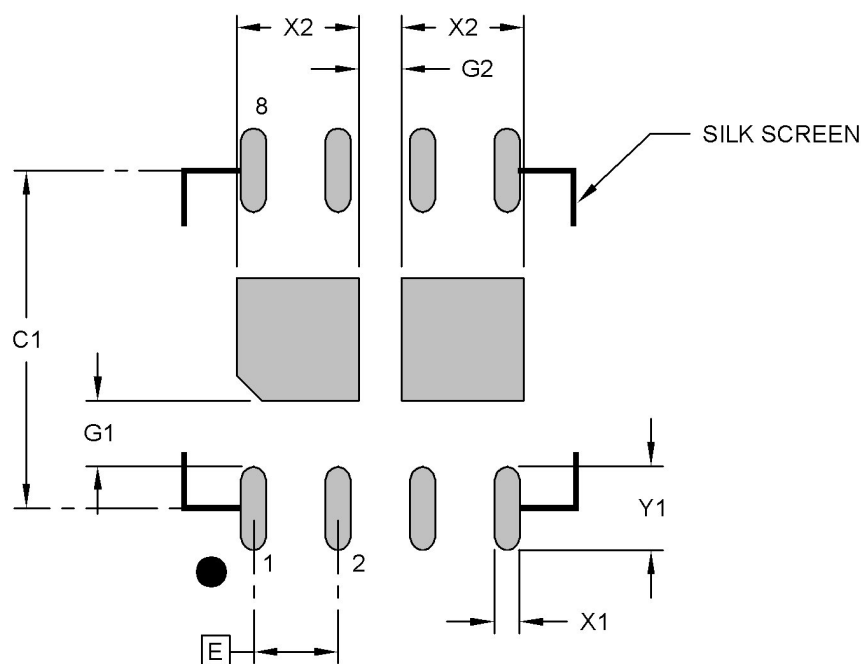
**Notes:**

- Pin 1 visual index feature may vary but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-285 Rev A Sheet 2 of 2

## 8-Lead Very Thin Plastic Dual Flat, No Lead Package (8RX) - 4x4x0.9 mm Body [VDFN] With Dual 1.45mm Exposed Pads

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Contact Pitch	E		1.00 BSC		
Center Pad Width (X2)	X2				1.45
Center Pad Length (X2)	Y2				1.45
Contact Pad Spacing	C1			4.00	
Contact Pad Width (X8)	X1				0.30
Contact Pad Length (X8)	Y1				1.00
Contact Pad to Center Pad (X8)	G1		0.775		
Center Pad to Center Pad	G2		0.50		

**Notes:**

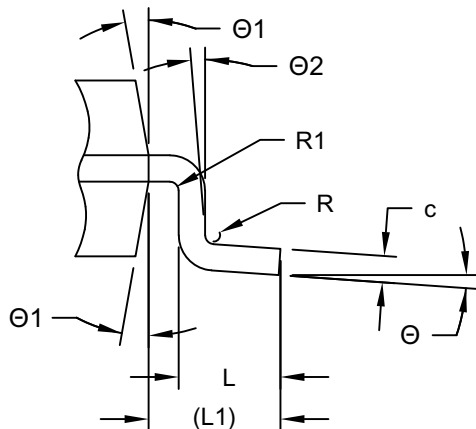
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2285 Rev A

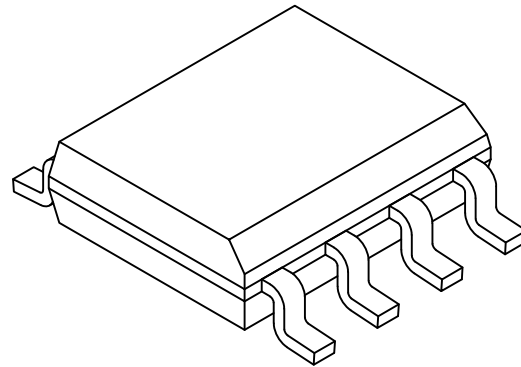


## 8-Lead Small Outline Integrated Circuit (4CX) - 3.90 mm Body [SOIC] Supertex Legacy Package TG

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	1.35	-	1.75
Standoff	A1	0.10	-	0.25
Molded Package Height	A2	1.25	-	1.65
Overall Length	D	4.90 BSC		
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Index Chamfer	h	0.25	-	0.50
Terminal Width	b	0.31	0.41	0.51
Terminal Thickness	c	0.17	-	0.25
Terminal Length	L	0.40	-	1.00
Footprint	L1	1.04 REF		
Terminal Bend Radius	R	0.07	-	-
Terminal Bend Radius	R1	0.07	-	-
Lead Angle	Θ	0°	-	8°
Mold Draft Angle	Θ1	5°	-	15°
Lead Angle	Θ2	0°	-	-

**Notes:**

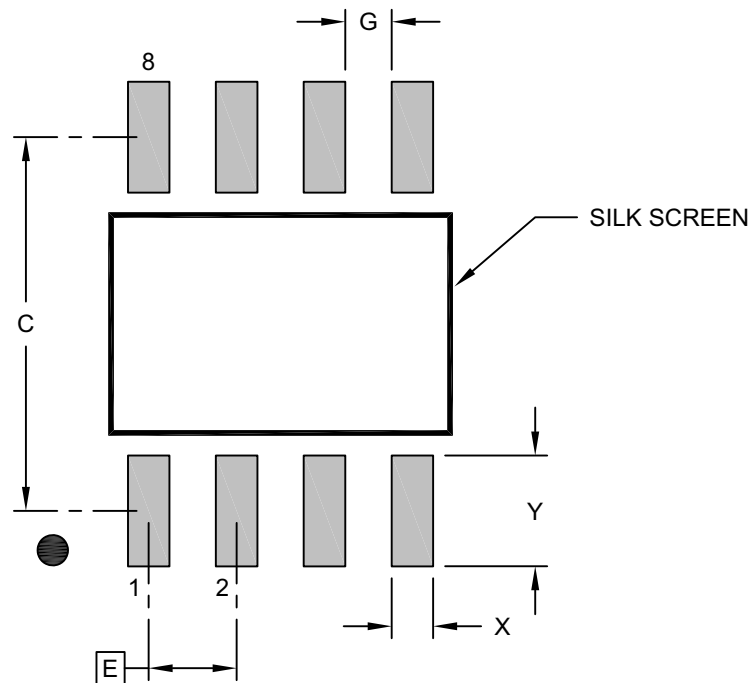
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.



# TC6320

## 8-Lead Small Outline Integrated Circuit (4CX) - 3.90 mm (.150 In.) Body [SOIC] Supertex Legacy Package TG

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (Xnn)	X			0.60
Contact Pad Length (Xnn)	Y			1.60
Contact Pad to Contact Pad (Xnn)	G	0.67		

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2267 Rev A

## APPENDIX A: REVISION HISTORY

### Revision B (June 2024)

- Modified [Section “Package Types”](#) from 5-lead DFN to 8-lead VDFN.
- Updated [Section 4.1 “Package Marking Information”](#) with the latest Package Drawings.

### Revision A (October 2017)

- Converted Supertex Doc# DSFP-TC6320 to Microchip DS20005697A.
- Changed the package marking format.
- Changed the quantity of the 8-lead DFN K6 package from 3000/Reel to 3300/Reel.
- Changed the quantity of the 8-lead SOIC TG package from 2000/Reel to 3300/Reel.
- Minor text changes throughout the document.

# TC6320

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>					
Device	Package Options		Environmental		Media Type
<div> <div> Device: TC6320 = N-Channel and P-Channel Enhancement-Mode MOSFET Pair </div> <div> Packages: K6 = 8-lead (4x4) VDFN TG = 8-lead SOIC </div> <div> Environmental: G = Lead (Pb)-free/RoHS-compliant Package </div> <div> Media Type: (blank) = 3300/Reel for a K6 Package = 3300/Reel for a TG Package </div> </div>					
<b>Examples:</b> <div> a) TC6320K6-G: N-Channel and P-Channel Enhancement-Mode MOSFET Pair, 8-lead (4x4) VDFN, 3300/Reel </div> <div> b) TC6320TG-G: N-Channel and P-Channel Enhancement-Mode MOSFET Pair, 8-lead SOIC, 3300/Reel </div>					

# TC6320

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NOTES:

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**Note the following details of the code protection feature on Microchip products:**

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
  - Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
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  - Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.
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