Product Change Notification / SYST-17AFLW716

Date:

22-Jul-2024

Product Category:

8-Bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

PIC16(L)F18326/18346 Family Silicon Errata and Data Sheet Clarifications

Affected CPNs:

SYST-17AFLW716_Affected_CPN_07222024.pdf
SYST-17AFLW716_Affected_CPN_07222024.csv

Notification Text:

SYST-17AFLW716

Microchip has released a new Document for the PIC16(L)F18326/18346 Family Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at PIC16(L)F18326/18346 Family Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change:

Added Silicon rev. A4.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity.

Change Implementation Status: Complete

Date Document Changes Effective: 22 Jul 2024

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC16(L)F18326/18346 Family Silicon Errata and Data Sheet Clarifications

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC16F18326-E/7NVAO
PIC16F18326-E/P
PIC16F18326-E/SL
PIC16F18326-E/SLVAO
PIC16F18326-E/ST
PIC16F18326-E/STVAO-VW
PIC16F18326-E/JQ
PIC16F18326-E/JQVAO
PIC16F18326-I/P
PIC16F18326-I/SL
PIC16F18326-I/ST
PIC16F18326-I/JQ
PIC16F18326T-I/7NV02
PIC16F18326T-I/SL
PIC16F18326T-I/ST
PIC16F18326T-I/JQ
PIC16F18326T-E/7NV05
PIC16F18326T-E/7NV08
PIC16F18326T-E/7NV08-BW
PIC16F18326T-E/7NVAO
PIC16F18326T-E/SLVAO
PIC16F18326T-E/ST
PIC16F18326T-E/STV01
PIC16F18326T-E/STVAO
PIC16F18326T-E/JQVAO
PIC16LF18326-E/P
PIC16LF18326-E/SL
PIC16LF18326-E/ST
PIC16LF18326-E/STVAO
PIC16LF18326-E/JQ
PIC16LF18326-E/JQVAO
PIC16LF18326-I/P
PIC16LF18326-I/SL
PIC16LF18326-I/ST
PIC16LF18326-I/JQ
PIC16LF18326T-I/7N
PIC16LF18326T-I/7NV03
PIC16LF18326T-I/7NVAO
PIC16LF18326T-I/SL
PIC16LF18326T-I/ST
PIC16LF18326T-I/JQ024
PIC16LF18326T-I/JQ
PIC16LF18326T-E/7NVAO
PIC16LF18326T-E/STVAO
PIC16LF18326T-E/JQVAO
PIC16F18346-E/SS

PIC16F18346-E/SSV10
PIC16F18346-E/SSVAO
PIC16F18346-E/SO
PIC16F18346-E/P
PIC16F18346-E/GZ
PIC16F18346-E/GZVAO
PIC16F18346-I/SSC03
PIC16F18346-I/SS
PIC16F18346-I/SSVAO
PIC16F18346-I/MLC01
PIC16F18346-I/ML
PIC16F18346-I/SO
PIC16F18346-I/P
PIC16F18346-I/PREL
PIC16F18346-I/GZC01
PIC16F18346-I/GZ
PIC16F18346T-I/6NXV06
PIC16F18346T-I/SSC03
PIC16F18346T-I/SS
PIC16F18346T-I/SSVAO
PIC16F18346T-I/SSVAO-VW
PIC16F18346T-I/MLC01
PIC16F18346T-I/ML
PIC16F18346T-I/MLV07
PIC16F18346T-I/SO
PIC16F18346T-I/GZC01
PIC16F18346T-I/GZ
PIC16F18346T-I/GZVAO
PIC16F18346T-E/SS
PIC16F18346T-E/SSV09
PIC16F18346T-E/SSVAO
PIC16F18346T-E/MLVAO
PIC16F18346T-E/GZ
PIC16LF18346-E/SS
PIC16LF18346-E/SSVAO
PIC16LF18346-E/SO
PIC16LF18346-E/P
PIC16LF18346-E/GZ
PIC16LF18346-I/SS
PIC16LF18346-I/SO
PIC16LF18346-I/P
PIC16LF18346-I/GZ
PIC16LF18346T-I/SS
PIC16LF18346T-I/SO
PIC16LF18346T-I/GZ025
PIC16LF18346T-I/GZ026
PIC16LF18346T-I/GZ
PIC16LF18346T-E/SS
PIC16LF18346T-E/SSVAO

PIC16LF18346T-E/MLVAO
PIC16LF18346T-E/GZ
PIC16LF18346T-E/GZVAO

PIC16(L)F18326/18346

PIC16(L)F18326/18346 Family
Silicon Errata and Data Sheet Clarifications

The PIC16(L)F18326/18346 family devices that you have received conform functionally to the current device data sheet (DS40001839**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F18326/18346 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F18326/18346 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			
		A1	A2	A3	A4
PIC16F18326	30A4h	2001h	2002h	2003h	2003h
PIC16LF18326	30A6h	2001h	2002h	2003h	2003h
PIC16F18346	30A5h	2001h	2002h	2003h	2003h
PIC16LF18346	30A7h	2001h	2002h	2003h	2003h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC16(L)F183XX Memory Programming Specification"* (DS40001738) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A1	A2	A3	A4
Oscillators	Fail-Safe Clock Monitor (FSCM)	1.1	The FSCM may fail to trigger with 4x PLL enabled.	X			
Host Synchronous Serial Port Module (MSSP2)	I^2C Communication	2.1	Acknowledge failure on LF devices only.	X			
Electrical Specifications	V_{DD} Parameter	3.1	VDDMIN specifications are changed for LF devices only.	X	X	X	X
	ADC Offset Error	3.2	ADC Offset Error specification changed.	X	X	X	X
	FVR Accuracy	3.3	FVR output voltage may be higher than specified in the data sheet.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Oscillators

1.1 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor may fail to trigger with the loss of the external clock signal when the 4x PLL is enabled. This includes all external clock modes: LP, XT, HS, ECL, ECM and ECH.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X							

2. Module: Host Synchronous Serial Port Module (MSSP2)

2.1 I^2C Communication

When using the MSSP2 to perform I^2C communication and the voltage for V_{DD} is above 3.0 volts, the Acknowledge signal (ACK) does not always occur after the second address byte is received, as expected. This issue exhibits itself when the MSSP2 is configured either for 7-bit or 10-bit addressing and in either Host or Client mode.

The issue occurs more frequently when using 10-bit addressing in Client mode and the lower address bits (A7-A0) are transmitted by the Host on the SDA line.

Work around

Do not exceed 3.0 volts on V_{DD} when using LF device.

Affected Silicon Revisions

A1	A2	A3	A4				
X							

3. Module: Electrical Specifications

3.1 VDD Parameter

VDDMIN at -40°C to +25°C = 2.3V.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

TABLE 3: SUPPLY VOLTAGE

PIC16LF18326/18346			Standard Operating Conditions (Unless Otherwise Stated)				
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
D002	VDD		1.8	—	3.6	V	FOSC ≤ 16 MHz, +25°C < TA ≤ +125°C
D002	VDD		2.3 2.5	— —	3.6 3.6	V V	FOSC ≤ 16 MHz, -40°C ≤ TA ≤ +25°C FOSC > 16 MHz

3.2 ADC Offset Error

The table containing the Offset Error specification (AD04:EOFF) for the Analog-to-Digital Converter is modified. The updated value for Offset Error specification is +/- 3.0 LSb.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

3.3 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are:

- FVR01 (1X gain setting)
- FVR02 (2X gain setting)
- FVR03 (4X gain setting)

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001839**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev G Document (07/2024)

Added Silicon rev. A4.

Rev F Document (09/2021)

Added Silicon issue 3.3 FVR Accuracy.

Rev E Document (11/2020)

Updated Table 2; added Table 3 and Section 3.2 ADC Offset Error.

Rev D Document (01/2020)

Added Silicon rev. A3.

Data Sheet Clarifications:

Removed Modules 1 and 2 (Data Sheet updated).

Rev C Document (01/2017)

Silicon Errata Issues:

Added Silicon rev. A2.

Data Sheet Clarifications:

Changed Module 1 Memory to Analog-to-Digital.

Rev B Document (01/2017)

Data Sheet Clarifications:

Added Module 2: Comparator.

Rev A Document (08/2016)

Initial release of this document.

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