

PH7030L

N-channel TrenchMOS™ logic level FET

Rev. 03 — 04 March 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low thermal resistance
- Logic level gate drive
- SO8 equivalent area footprint
- Low on-state resistance.

1.3 Applications

- DC-to-DC converters
- Portable appliances
- Switched-mode power supplies
- Notebook computers.

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $I_D \leq 68$ A
- $P_{tot} \leq 62.5$ W
- $R_{DSon} \leq 7.9$ mΩ

2. Pinning information

Table 1: Pinning - SOT669 (LFAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBL286</p>	<p>MBB076</p>
4	gate (g)		
mb	mounting base; connected to drain (d)		

SOT669 (LFAK)



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3. Ordering information

Table 2: Ordering information

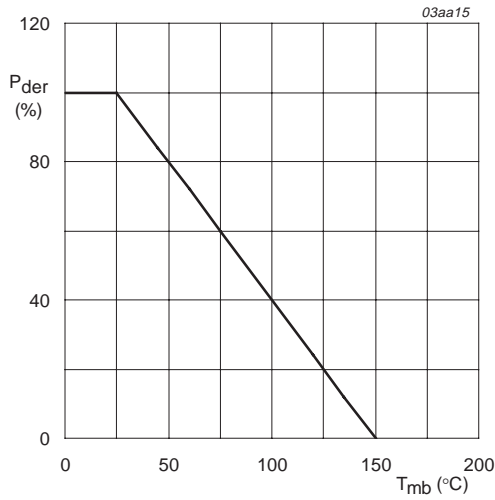
Type number	Package		Version
	Name	Description	
PH7030L	LFPAK	Plastic single-ended surface mounted package; 4 leads	SOT669

4. Limiting values

Table 3: Limiting values

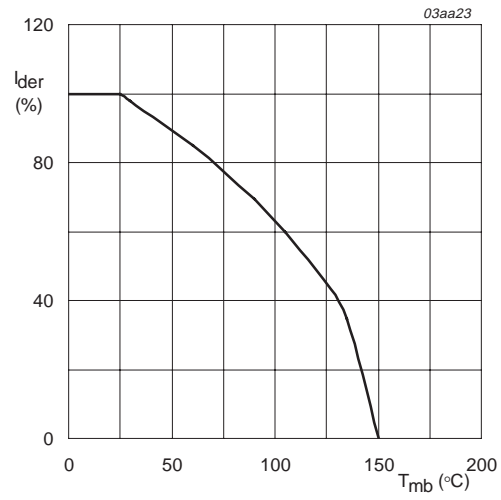
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2 and 3	-	68	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2	-	43	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	220	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	150	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 33.9\text{ A};$ $t_p = 0.15\text{ ms}; V_{DD} \leq 30\text{ V}; V_{GS} = 10\text{ V};$ starting $T_j = 25\text{ °C}$	-	115	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

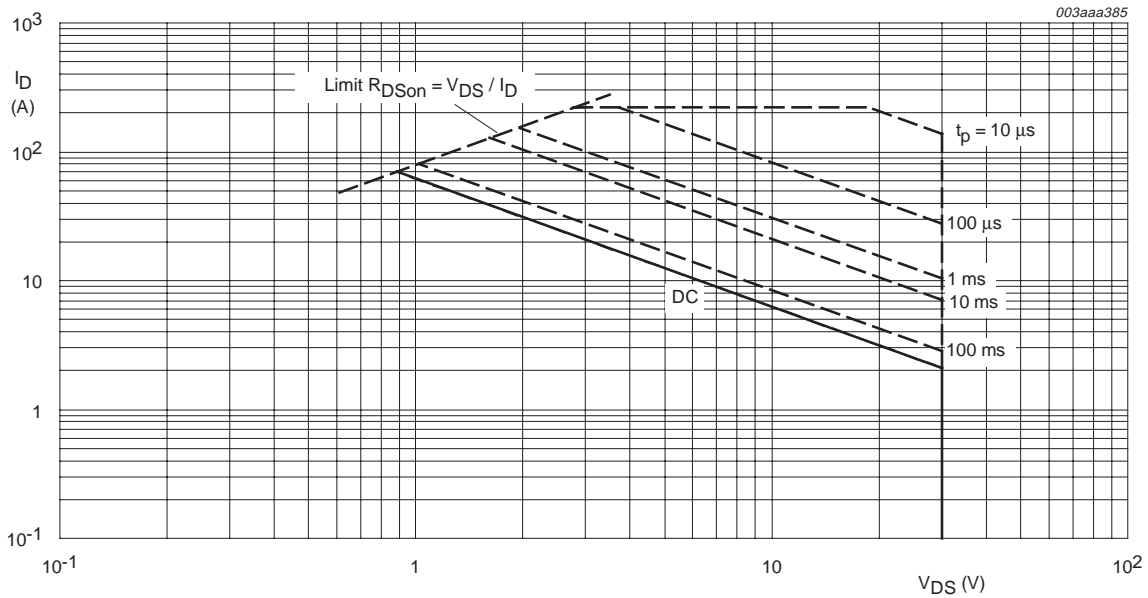
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



V_{GS} ≥ 10 V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

5.1 Transient thermal impedance

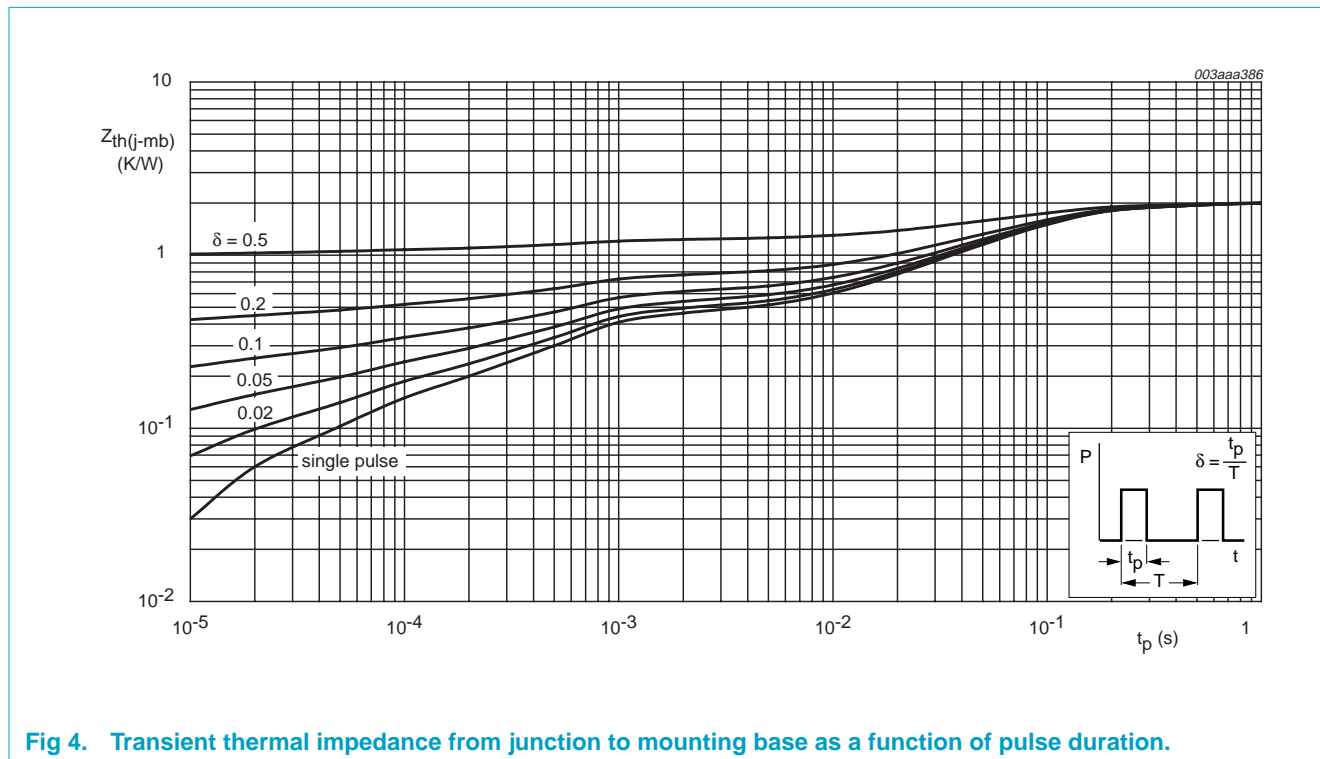


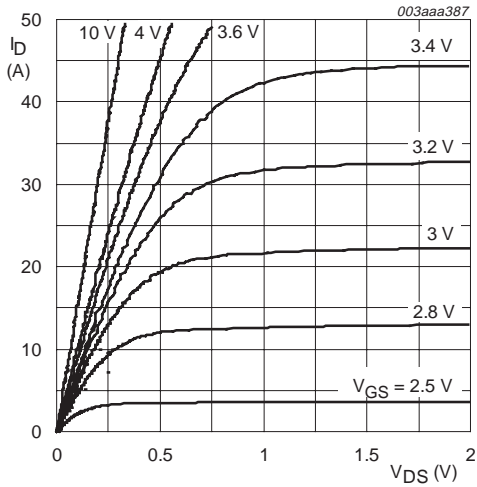
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

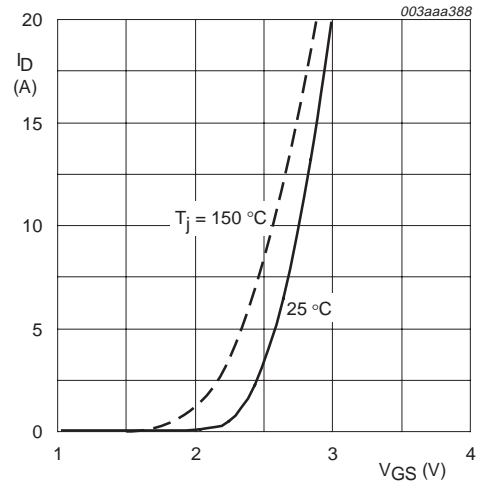
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9				
		$T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 150\text{ °C}$	0.6	-	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	-	0.06	1	μA
		$T_j = 150\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 15\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	20	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 10\ \text{A}$; Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	6.9	7.9	m Ω
		$T_j = 150\text{ °C}$	-	11.7	13.2	m Ω
		$V_{GS} = 5\ \text{V}$; $I_D = 10\ \text{A}$	-	8.7	10	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 20\ \text{A}$; $V_{DD} = 10\ \text{V}$; $V_{GS} = 5\ \text{V}$; Figure 13	-	12	-	nC
Q_{gs}	gate-source charge		-	4.1	-	nC
Q_{gd}	gate-drain (Miller) charge		-	3.2	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 10\ \text{V}$; $f = 1\ \text{MHz}$; Figure 11	-	1362	-	pF
C_{oss}	output capacitance		-	544	-	pF
C_{rss}	reverse transfer capacitance		-	260	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 10\ \text{V}$; $I_D = 10\ \text{A}$; $V_{GS} = 4.5\ \text{V}$; $R_G = 4.7\ \Omega$	-	24	-	ns
t_r	rise time		-	38	-	ns
$t_{d(off)}$	turn-off delay time		-	34	-	ns
t_f	fall time		-	21	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 10\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12	-	0.81	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\ \text{A}$; $dI_S/dt = -100\ \text{A}/\mu\text{s}$; $V_{DS} = 20\ \text{V}$	-	11	-	ns



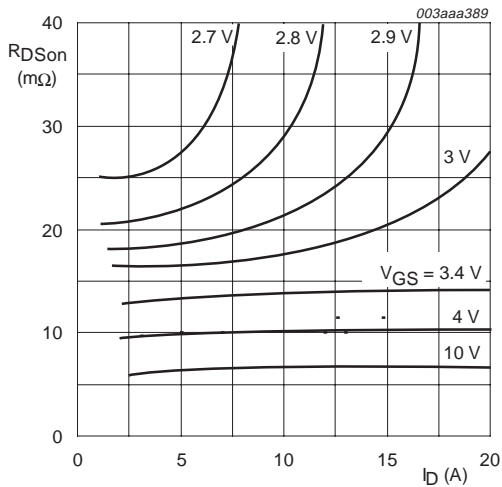
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



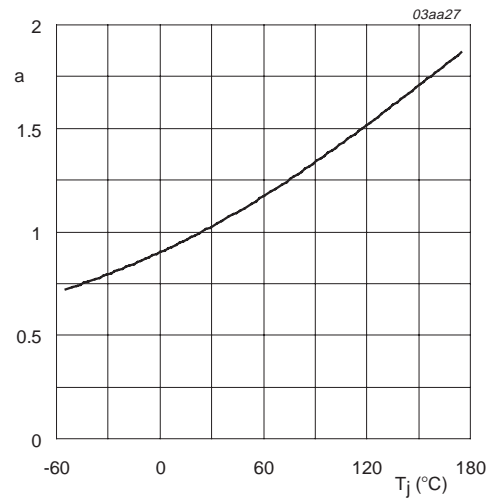
T_j = 25 °C and 150 °C; V_{DS} > I_D × R_{DSon}

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



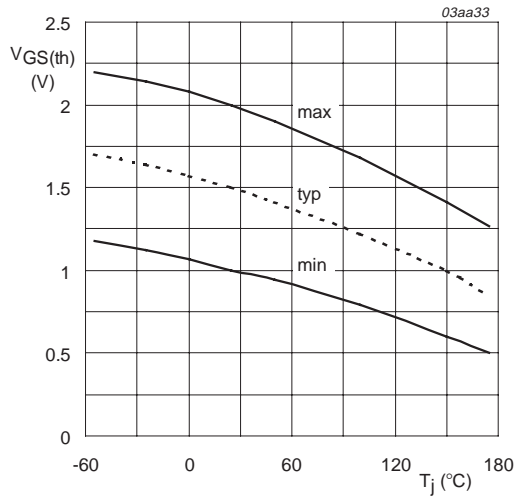
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



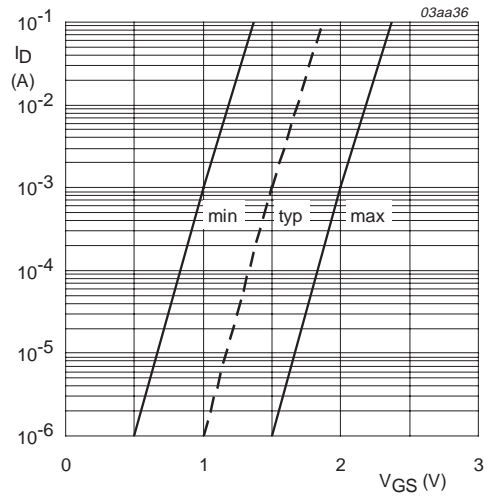
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



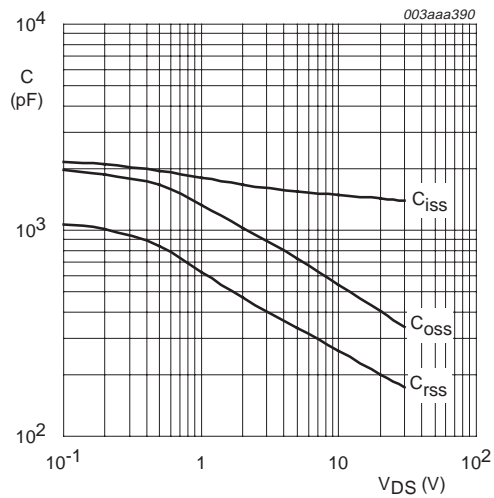
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



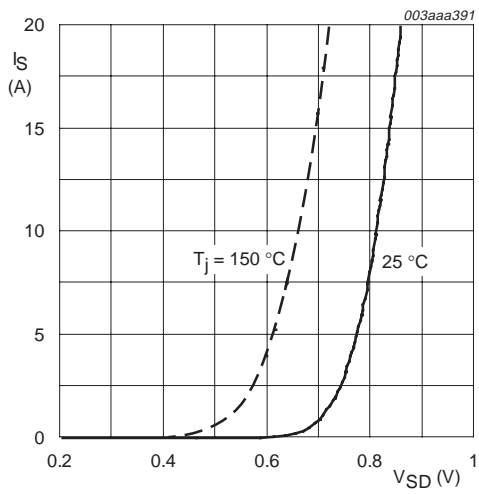
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



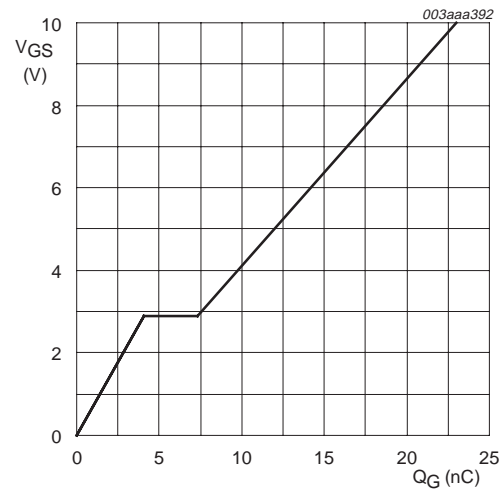
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25^\circ\text{C}$ and 150°C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 20\text{ A}$; $V_{DD} = 10\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

Plastic single-ended surface mounted package (Philips version LFFPAK); 4 leads

SOT669

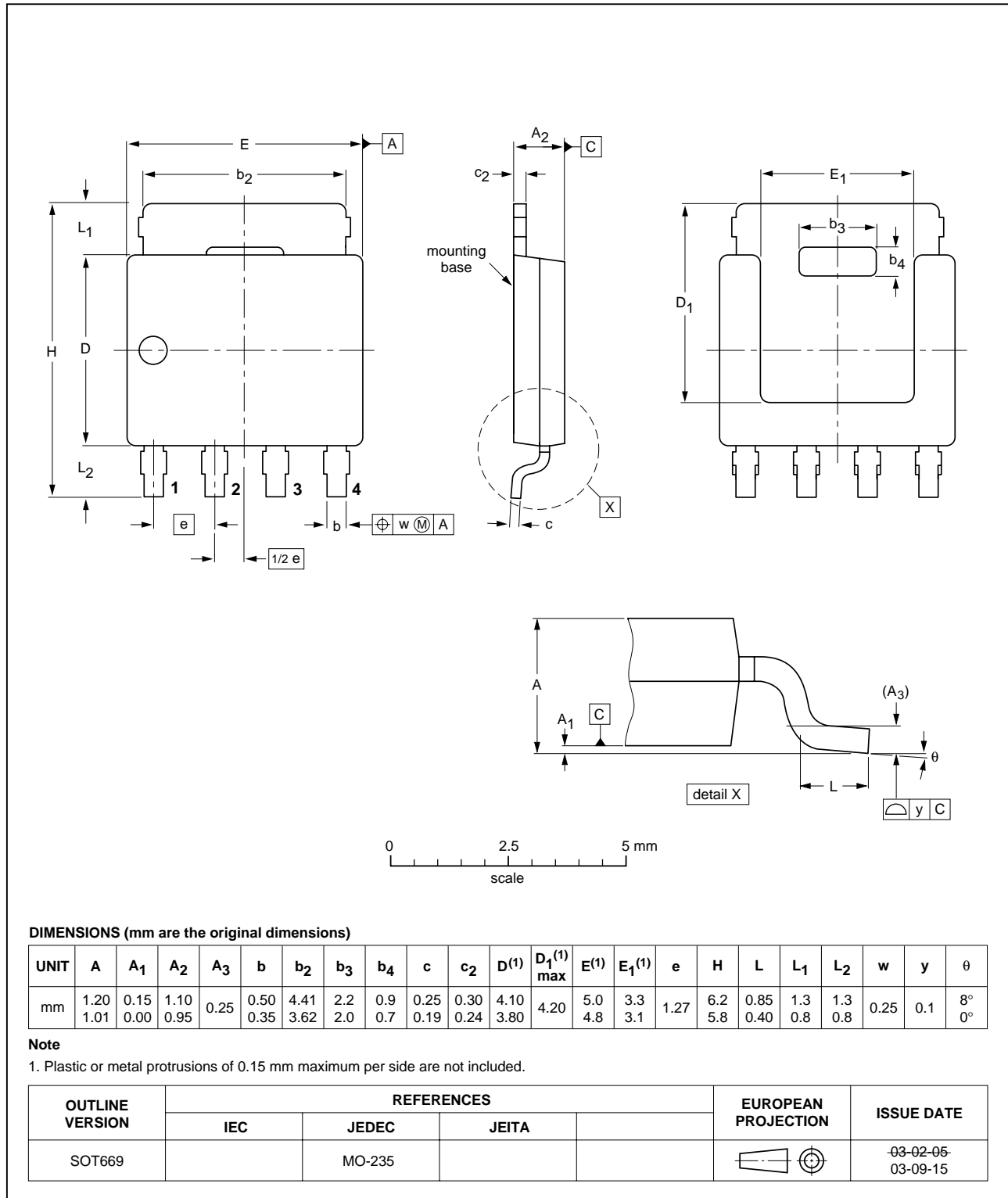


Fig 14. SOT669 (LFFPAK).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
03	20040304	-	Product data (9397 750 12944) Modifications: <ul style="list-style-type: none"> • Table 5 “Characteristics” t_r data revised.
02	20030918	-	Product data (9397 750 11946) Modifications: <ul style="list-style-type: none"> • Section 3 “Ordering information” added on page 2. • Section 1.4 “Quick reference data” and Table 3 “Limiting values”, I_D data revised. • Section 1.4 “Quick reference data” and Table 5 “Characteristics”, R_{DSon} data revised. • Section 4 “Limiting values”, V_{GS} data revised. • Table 5 “Characteristics”, $Q_{g(tot)}$, Q_{gs}, Q_{gd} and V_{SD} data revised. • Figure 3, 4, 7, 8 and 13 updated.
01	20030502	-	Product data (9397 750 11405).

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