

N-Channel 80 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	80
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0058
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5$ V	0.0068
Q_g typ. (nC)	19.1
I_D (A)	78.4
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SIR586DP-T1-RE3
Alternate manufacturing location	SIR586DP-T1-BE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	80	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	78.4	A
	$T_C = 70$ °C	62.7	
	$T_A = 25$ °C	20.7 ^{b, c}	
	$T_A = 70$ °C	16.6 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	200	A
Continuous source-drain diode current	$T_C = 25$ °C	64.9 ^a	
	$T_A = 25$ °C	4.5 ^{b, c}	
Single pulse avalanche current	I_{AS}	30	
Single pulse avalanche energy	$L = 0.1$ mH E_{AS}	45	mJ
Maximum power dissipation	$T_C = 25$ °C	71.4	W
	$T_C = 70$ °C	45.7	
	$T_A = 25$ °C	5.0 ^{b, c}	
	$T_A = 70$ °C	3.2 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	$t \leq 10$ s	R_{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.4	1.75	

Notes

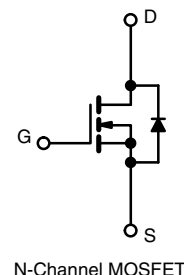
- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W
- $T_C = 25$ °C

FEATURES

- TrenchFET® Gen V power MOSFET
- Very low $R_{DS} \times Q_g$ figure-of-merit (FOM)
- Tuned for the lowest $R_{DS} \times Q_{oss}$ FOM
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converters
- OR-ing and hot swap switch
- Power supplies
- Motor drive control
- Battery management



N-Channel MOSFET



RoHS
COMPLIANT
HALOGEN
FREE

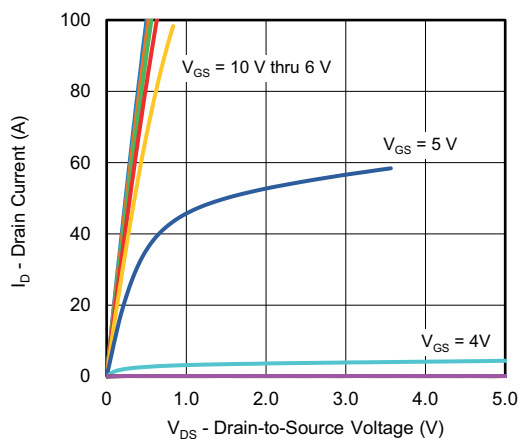
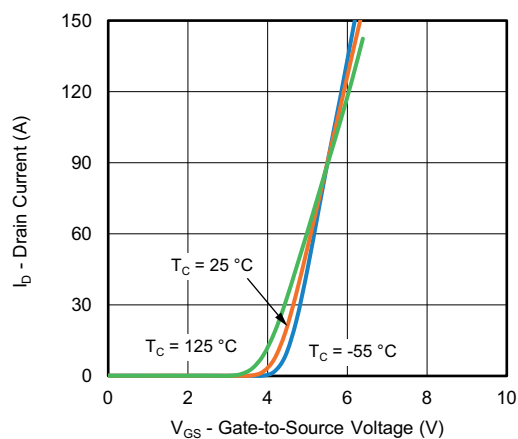
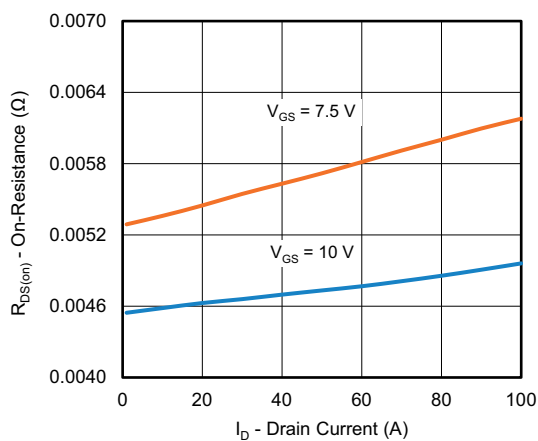
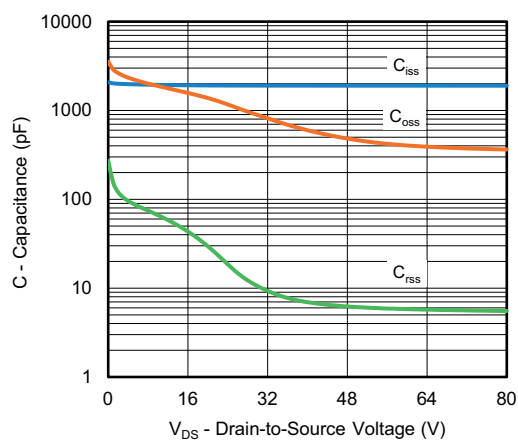
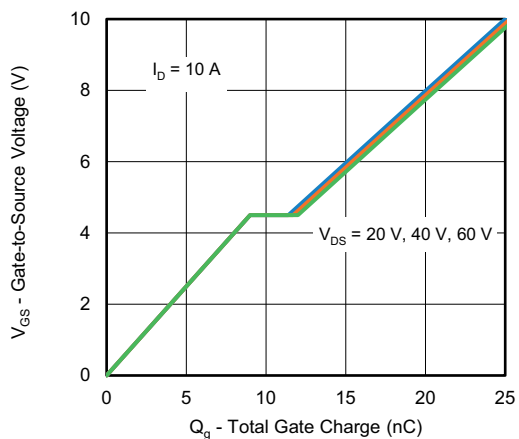
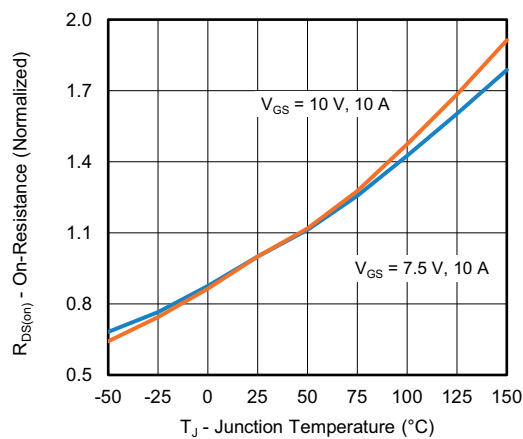


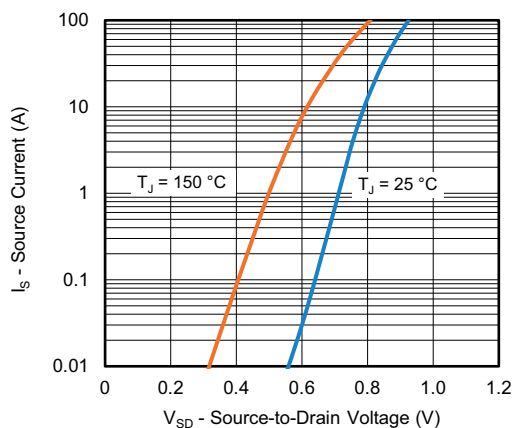
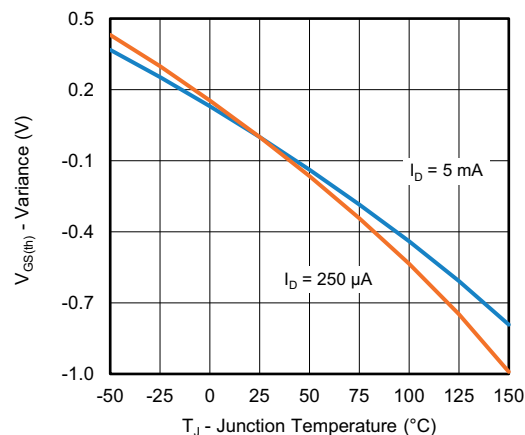
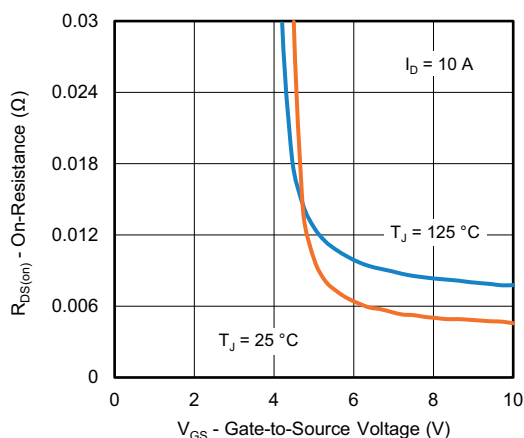
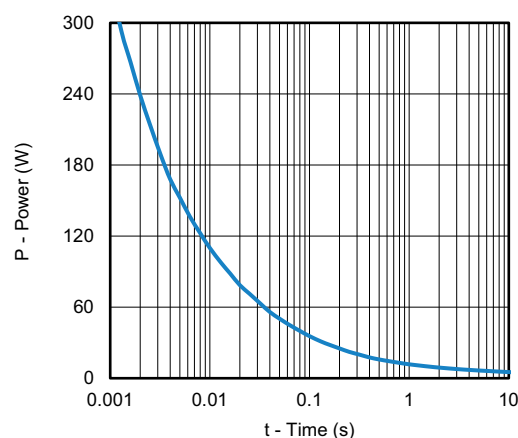
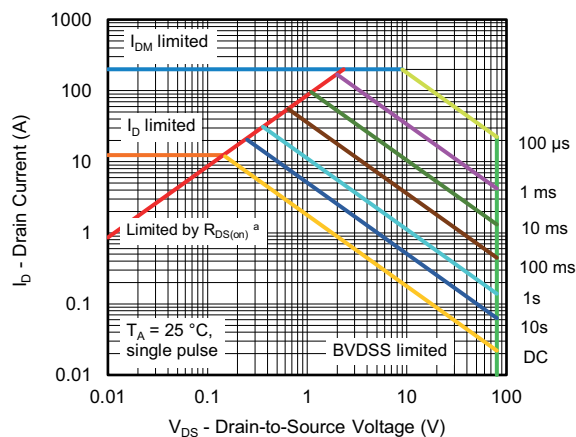
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA	80	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	44	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-6.7	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	-	4	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 64 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 64 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A	-	0.0046	0.0058	Ω
		V _{GS} = 7.5 V, I _D = 10 A	-	0.0053	0.0068	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 10 A	-	41	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz	-	1905	-	pF
Output capacitance	C _{oss}		-	600	-	
Reverse transfer capacitance	C _{rss}		-	7.1	-	
Total gate charge	Q _g	V _{DS} = 40 V, V _{GS} = 10 V, I _D = 10 A	-	25.3	38	nC
		V _{DS} = 40 V, V _{GS} = 7.5 V, I _D = 10 A	-	19.1	29	
Q _{gs}	-		9	-		
Q _{gd}	-		2.7	-		
Output charge	Q _{oss}	V _{DS} = 40 V, V _{GS} = 0 V	-	58.2	-	
Gate resistance	R _g	f = 1 MHz	0.4	1.0	1.8	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	14	28	ns
Rise time	t _r		-	6	12	
Turn-off delay time	t _{d(off)}		-	20	40	
Fall time	t _f		-	7	14	
Turn-on delay time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω, I _D ≅ 10 A, V _{GEN} = 7.5 V, R _g = 1 Ω	-	16	32	
Rise time	t _r		-	7	14	
Turn-off delay time	t _{d(off)}		-	19	38	
Fall time	t _f		-	8	16	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	64.9	A
Pulse diode forward current	I _{SM}		-	-	200	
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.77	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	47	94	ns
Body diode reverse recovery charge	Q _{rr}		-	47	94	nC
Reverse recovery fall time	t _a		-	21	-	ns
Reverse recovery rise time	t _b		-	26	-	

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

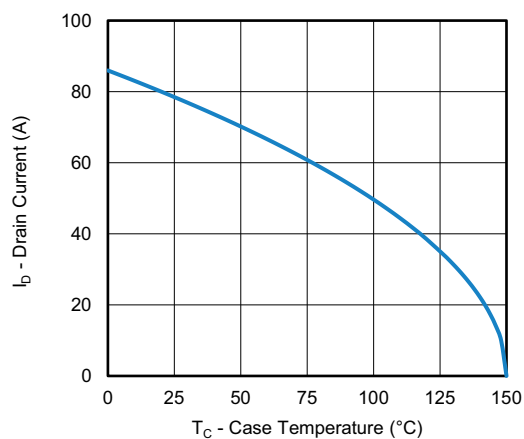
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient
Note

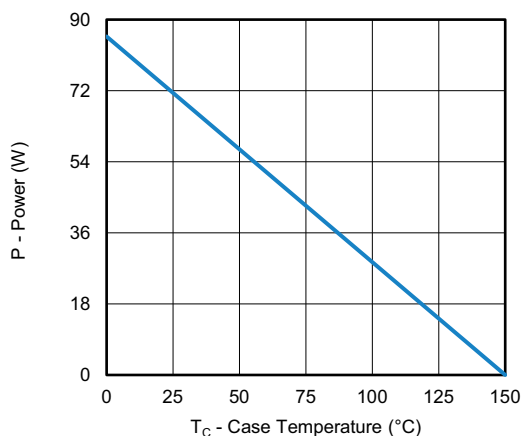
- a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



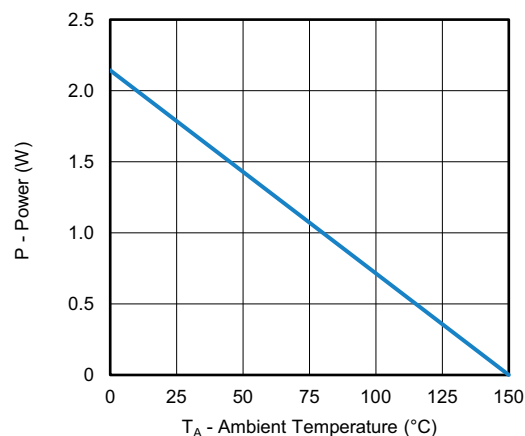
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case



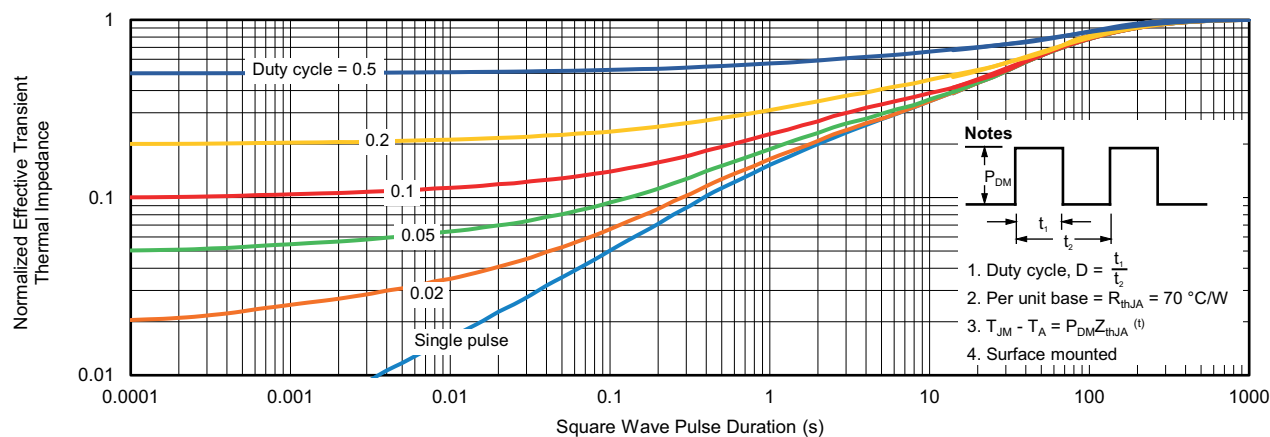
Power, Junction-to-Ambient

Note

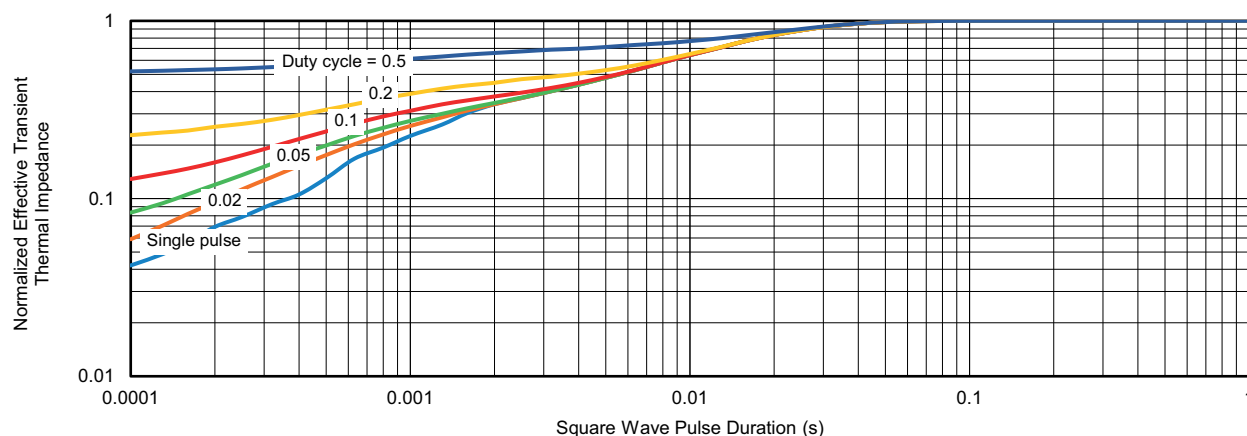
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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