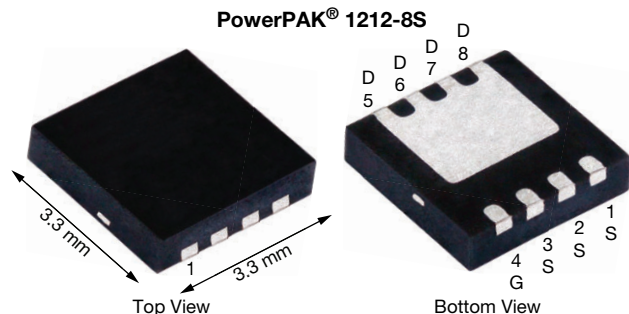


N-Channel 40 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00265
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.00395
Q_g typ. (nC)	18.5
I_D (A)	109
Configuration	Single

FEATURES

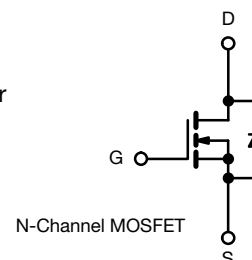
- TrenchFET® Gen IV power MOSFET
- Very low Q_g and Q_{oss} reduce power loss and improve efficiency
- Optimized Q_g , Q_{gd} , and Q_{gd}/Q_{gs} ratio reduces switching related power loss
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- Synchronous buck converter
- High power density DC/DC
- Load switching



ORDERING INFORMATION	
Package	PowerPAK 1212-8S
Lead (Pb)-free and halogen-free	SiSS10ADN-T1-GE3
Alternate manufacturing location	SiSS10ADN-T1-BE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	40		
Gate-source voltage	V_{GS}	+20 / -16		V
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	109		A
	$T_C = 70$ °C	86.8		
	$T_A = 25$ °C	31.7 ^{b, c}		
	$T_A = 70$ °C	25 ^{b, c}		
Pulsed drain current ($t = 100$ μ s)	I_{DM}	150		
Continuous source-drain diode current	$T_C = 25$ °C	51.6		
	$T_A = 25$ °C	4.3 ^{b, c}		
Single pulse avalanche current	$L = 0.1$ mH	30		
Single pulse avalanche energy	E_{AS}	45		mJ
Maximum power dissipation	$T_C = 25$ °C	56.8		W
	$T_C = 70$ °C	36		
	$T_A = 25$ °C	4.8 ^{b, c}		
	$T_A = 70$ °C	3 ^{b, c}		
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) ^c		260		

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	21	26	°C/W
Maximum junction-to-case (drain)	R_{thJC}	1.7	2.2	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W
- $T_C = 25$ °C

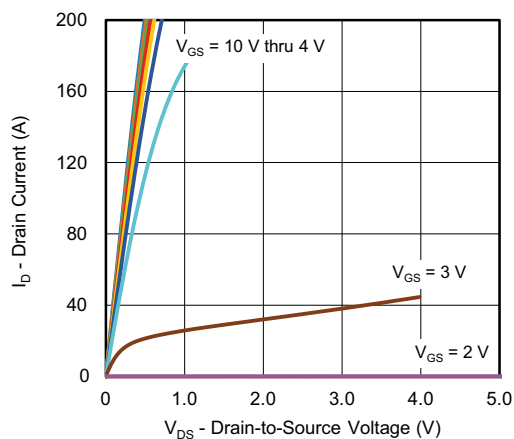
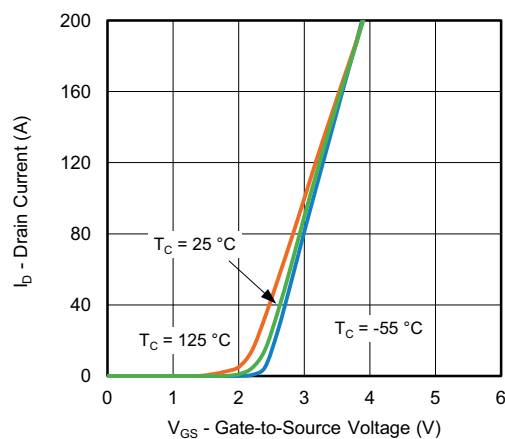
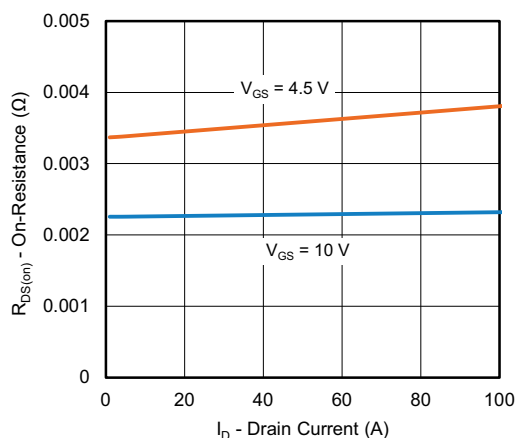
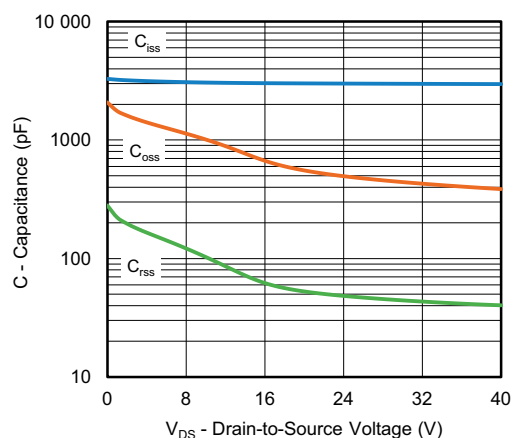
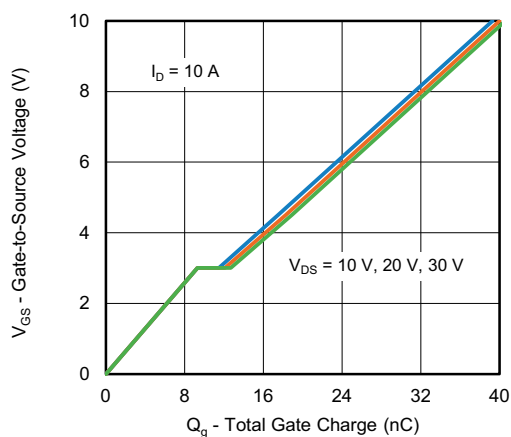
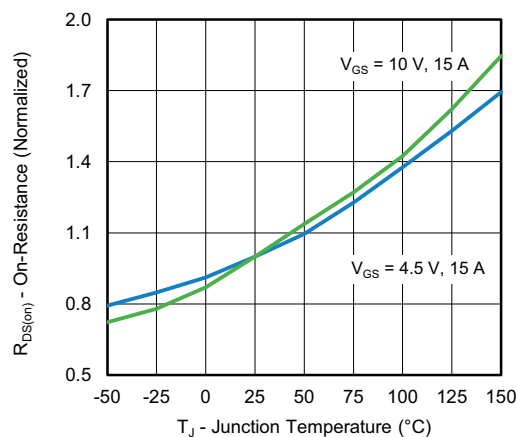


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	25	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	-6	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.1	-	2.4	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A	-	0.00220	0.00265	Ω
		V _{GS} = 4.5 V, I _D = 10 A	-	0.00330	0.00395	
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 15 A	-	80	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	3030	-	pF
Output capacitance	C _{oss}		-	550	-	
Reverse transfer capacitance	C _{rss}		-	52	-	
C _{rss} /C _{iss} ratio			-	0.018	0.036	
Total gate charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 10 A	-	40.5	61	nC
		V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 10 A	-	18.5	28	
Q _{gs}	-		9.3	-		
Q _{gd}	-		2.8	-		
Output charge	Q _{oss}	V _{DS} = 20 V, V _{GS} = 0 V	-	21.5	-	
Gate resistance	R _g	f = 1 MHz	0.5	1.4	2.5	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 1 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	13	26	ns
Rise time	t _r		-	5	10	
Turn-off delay time	t _{d(off)}		-	30	60	
Fall time	t _f		-	5	10	
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 1 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	28	56	
Rise time	t _r		-	66	132	
Turn-off delay time	t _{d(off)}		-	30	60	
Fall time	t _f		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	51.6	A
Pulse diode forward current (t _p = 100 μs)	I _{SM}		-	-	150	
Body diode voltage	V _{SD}	I _S = 5 A	-	0.73	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	29	58	ns
Body diode reverse recovery charge	Q _{rr}		-	17	34	nC
Reverse recovery fall time	t _a		-	14	-	ns
Reverse recovery rise time	t _b		-	15	-	

Notes

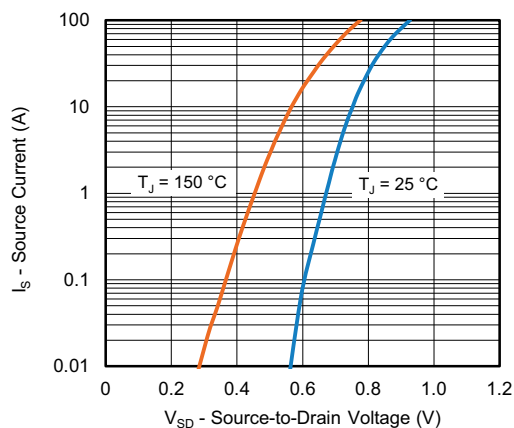
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

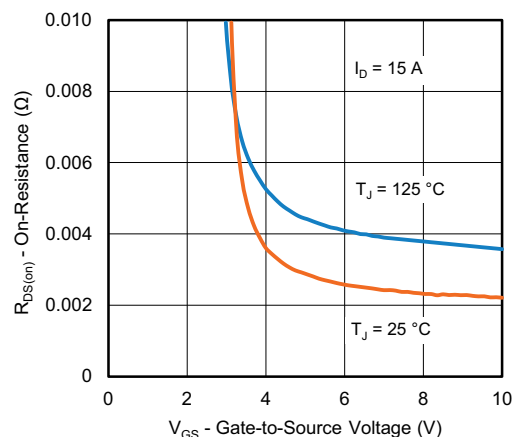
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



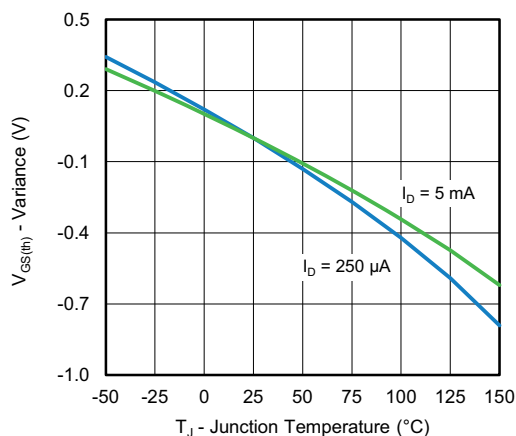
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



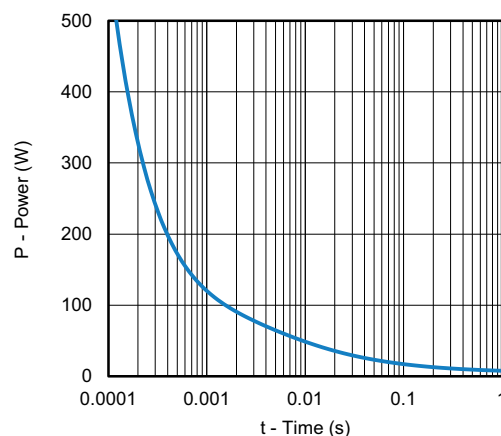
Source-Drain Diode Forward Voltage



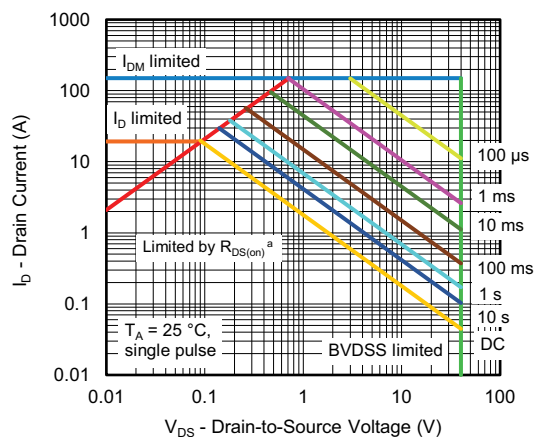
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



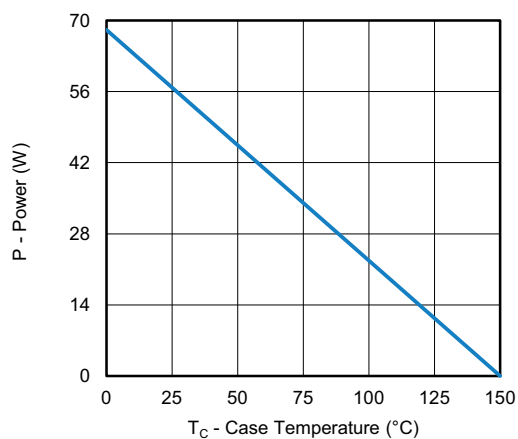
Safe Operating Area

Note

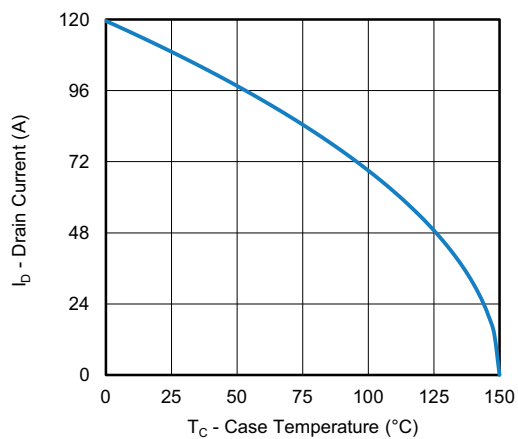
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



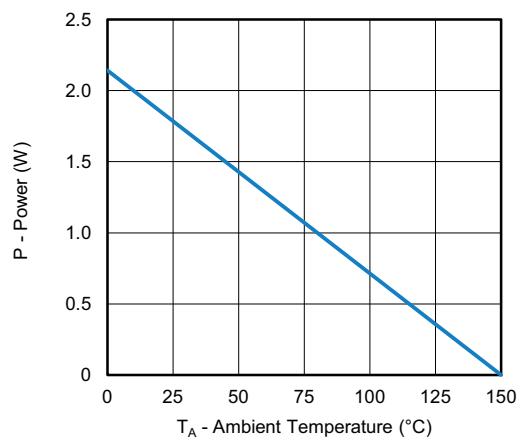
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Power, Junction-to-Case



Current Derating ^a



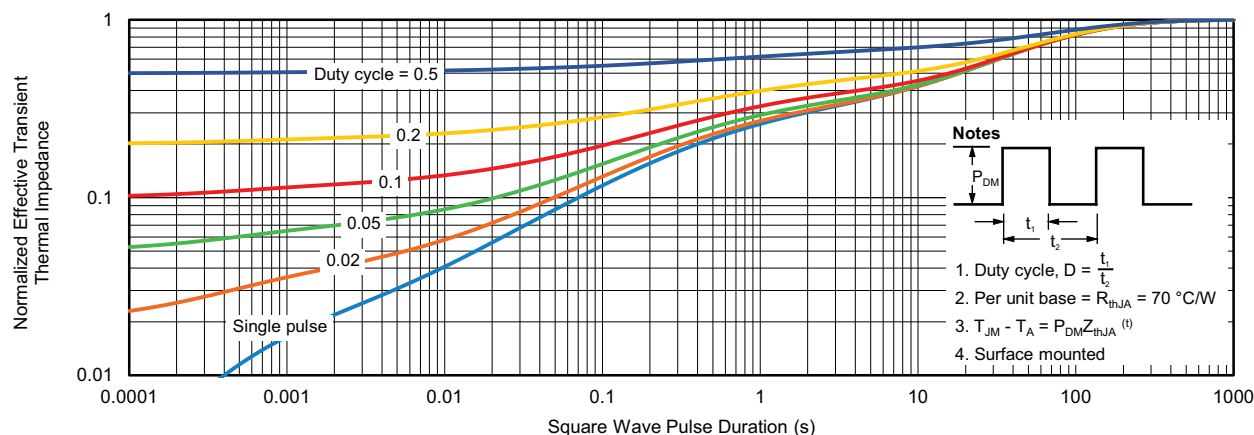
Power, Junction-to-Ambient

Note

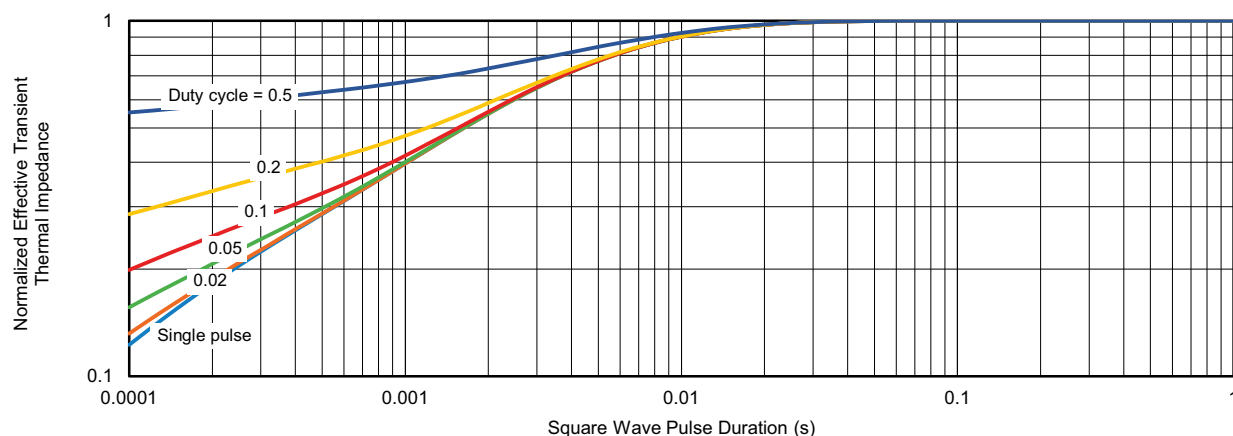
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



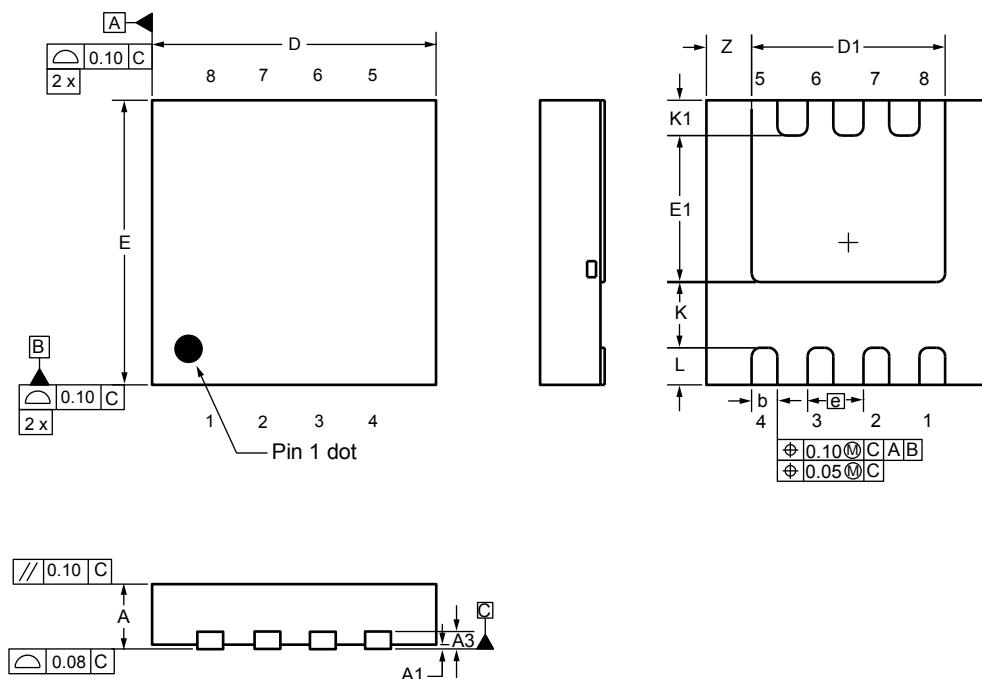
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

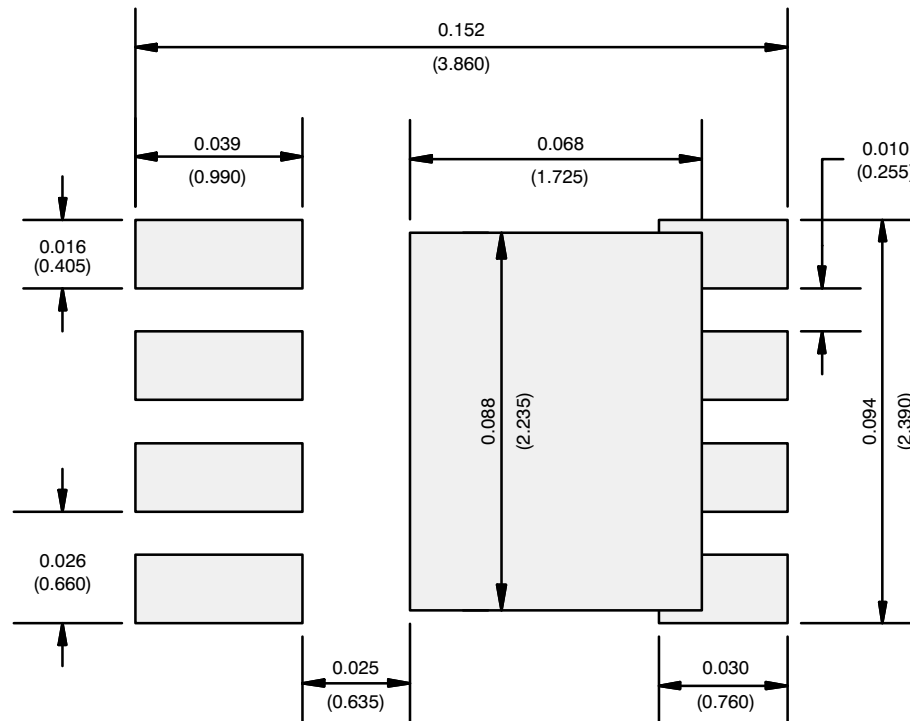
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Case Outline for PowerPAK® 1212-8S



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.67	0.75	0.83	0.026	0.030	0.033
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		
ECN: C20-0862-Rev. B, 20-Jul-2020						
DWG: 6008						

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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