

**R9C1T18/R Series / Power Module**

1.5W / 8.5V-18VDC / 36 Pin SSOP Package

**FEATURES**

- 1.5W isolated DC/DC converter
- Programmable asymmetrical output voltages
- 8.5 - 18VDC input voltage range
- For IGBT/Si/SiC/Cascode GaN gate drive bias voltages
- High 5kVAC/1min reinforced isolation / 1.4kVDC working voltage
- High dV/dt immunity with 150kV/μs CMTI
- Full load 1.5W from -40°C to +120°C
- Less than 3.5pF isolation capacitance
- Compact 7.5x12.83mm SMD package
- 3 year warranty



Dimensions (LxWxH): 12.83 x 7.5 x 3.55mm (0.51 x 0.30 x 0.14 inch)  
0.1g (0.0032 oz)

**APPLICATIONS****SAFETY & EMC****DESCRIPTION**

The R9C1T18/R 1.5W isolated DC/DC converter is a versatile solution designed for isolated gate bias voltages, particularly for transistors such as IGBTs, Si and SiC MOSFETs, and Cascode GaNs. This compact converter features a wide input voltage range of 8.5 - 18VDC and programmable asymmetrical output voltages, ensuring precise control and performance optimization for power electronics applications. With high 5kVAC/1min isolation, 1.4kVDC working voltage, high 150kV/μs CMTI, and remarkable stability up to 150°C (>0.5W), it offers superior reliability, even under harsh high power, high frequency switching environments. The ultra-low isolation capacitance, less than 3.5pF, ensures minimal noise propagation across the isolation barrier. All of these exceptional features are packaged in a compact 7.5 x 12.83mm SMD form factor, making it an ideal choice for all isolated gate bias voltage needs.

**SELECTION GUIDE**

Part Number	Input Voltage Range [VDC]	Output Voltage Range <sup>(1)</sup> [VDC]	Output Current max. [mA]	Efficiency typ. [%]
R9C1T18/R	8.5 - 18	$V_{OUT+} = 2.5 - 15.5$ $V_{OUT-} = (-2.5) - (-15.5)^{(2)}$ $V_{TOTAL} = 15 - 18$	$I_{OUT+} = +100\text{mA}$ $I_{OUT-} = -12\text{mA}$	52

Note1:  $V_{OUT+}$  and  $V_{OUT-}$  can be set from 2.5VDC to 15.5VDC or -2.5VDC to -15.5VDC respectively but the total must be within the range of 15VDC to 18VDC. For more information see „Typical Application“ below.

Note2: For  $V_{OUT-}$  between 0V and -2.5V please contact techsupport@recom-power.com

**ABSOLUTE MAXIMUM RATINGS** (measured @  $T_{AMB} = 25^{\circ}\text{C}$ , nom.  $V_{IN}$ , full load and after warm-up unless otherwise stated)

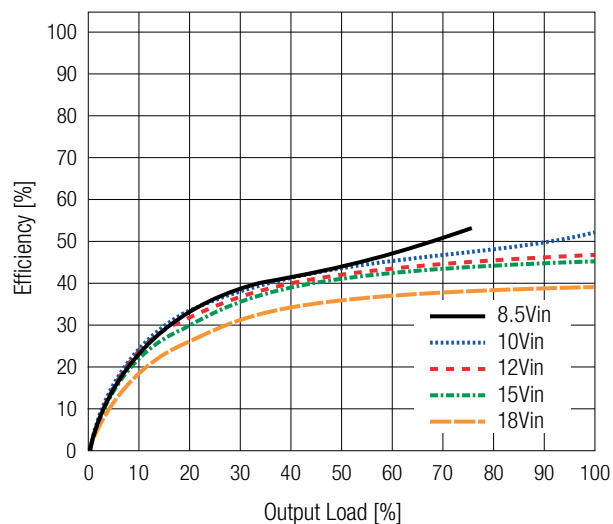
Parameter	Symbol	Min.	Typ.	Max.
Absolute maximum voltage	$V_{IN}$ to PGND	-0.3VDC		32VDC
	CTRL, PG to PGND	-0.3VDC		7VDC
	$V_{OUT+}$ , COM, FBV $_{OUT+}$ , FBV $_{OUT-}$ to $V_{OUT-}$	-0.3VDC		32VDC
Maximum internal power losses <sup>(3)</sup>	$T_{AMB} = +25^{\circ}\text{C}$			2.45W
Maximum output power	$V_{TOTAL} = V_{OUT+}$ to $V_{OUT-}$ , $T_{AMB} = +25^{\circ}\text{C}$			2.5W
Junction Temperature		-40°C		+150°C
Storage Temperature		-65°C		+150°C

Note3: Exceeding maximum allowable power dissipation causes the device to enter thermal shut down which protects the device from permanent damage.

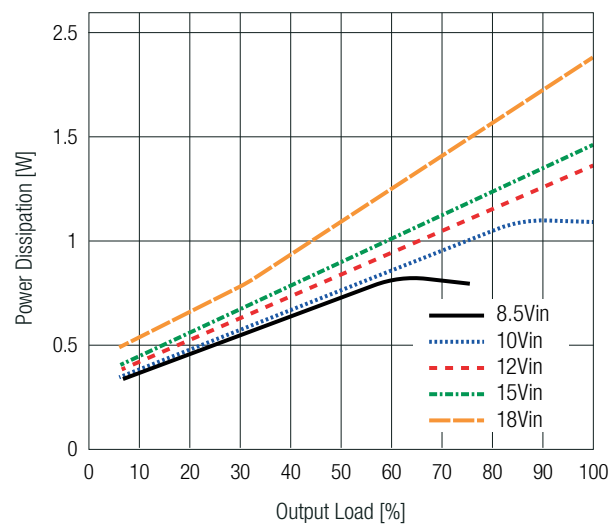
**BASIC CHARACTERISTICS** (measured @  $T_{AMB} = 25^{\circ}\text{C}$ , nom.  $V_{IN}$ , full load and after warm-up unless otherwise stated)

Parameter	Symbol	Condition	Min.	Typ.	Max.
Input Voltage Range	$V_{IN}$	refer to „Derating Graph“	8.5VDC	15VDC	18VDC
Under Voltage Lockout (UVLO)		rising	7.8VDC	8.2VDC	8.5VDC
		falling	7VDC	7.4VDC	7.7VDC
Over Voltage Lockout (OVLO)		rising	11.4VDC	22VDC	23.1VDC
		falling	19VDC	20VDC	21VDC
Soft Start Time				3ms	
Standby Current	$I_Q$	$V_{CTRL} = 5\text{VDC}$ , $V_{IN} = 8\text{VDC}$ to 18VDC, no load			40mA
Quiescent Current		$V_{CTRL} = 0\text{VDC}$ , $V_{IN} = 8\text{VDC}$ to 18VDC			600μA
Output Power					1.5W
Power Dissipation		refer to „Power Dissipation“			2.36W
Switching Frequency		$V_{IN} = 15\text{VDC}$		15MHz	

Efficiency vs. Output current

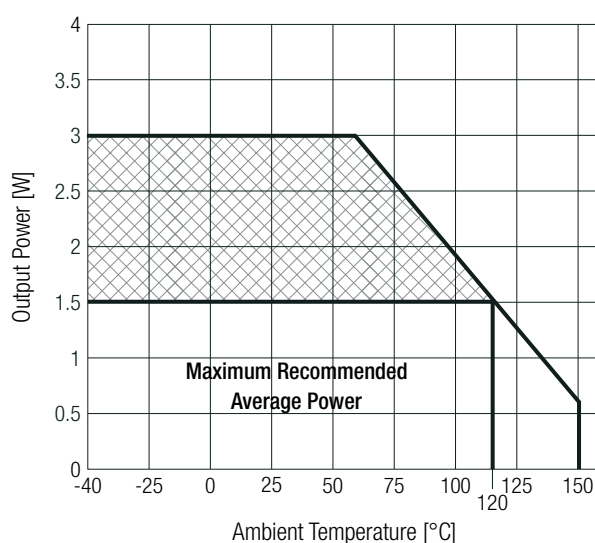


Power Dissipation

**REGULATIONS**

Parameter	Symbol	Condition	Min.	Typ.	Max.
Feedback Voltage <sup>(4)</sup>	$V_{FB}$	FBV $_{OUT+}$ or FBV $_{OUT-}$ to $V_{OUT-}$	0VDC	2.5VDC	5.5VDC
		$V_{OUT+}$ to $V_{OUT-}$ in regulation	2.4675VDC	2.5VDC	2.5325VDC
Feedback $V_{OUT+}$ Hysteresis		hysteresis at the FBV $_{OUT+}$ pin	9mV	10mV	12.3mV
Output Voltage Accuracy		0.1% of FB resistors	-1.3%		1.3%

Note4: For isolated gate driver applications, one positive and one negative output are needed. In this case,  $V_{OUT+}$  to  $V_{OUT-}$  is the total output voltage, and the middle point becomes the reference point. Because the total voltage between  $V_{OUT+}$  and  $V_{OUT-}$  is always regulated through the FBV $_{OUT+}$  feedback, the COM pin only must regulate the middle point voltage so that it can give the correct positive and negative voltages. The COM control is achieved through FBV $_{OUT-}$  pin as described in „Adjustability“ section.

**BASIC CHARACTERISTICS** (measured @  $T_{AMB} = 25^{\circ}\text{C}$ , nom.  $V_{IN}$ , full load and after warm-up unless otherwise stated)
**Derating Graph**

Note5: Exceeding maximum allowable power dissipation causes device to enter thermal shutdown which protects device from permanent damage.

Note6: Keep the average power at 1.5W max. or peak power 3W for 5 seconds max.

Note7: Test with Recom 50x50mm standard EVM board with 70μm copper, double layer

**ADJUSTABILITY**

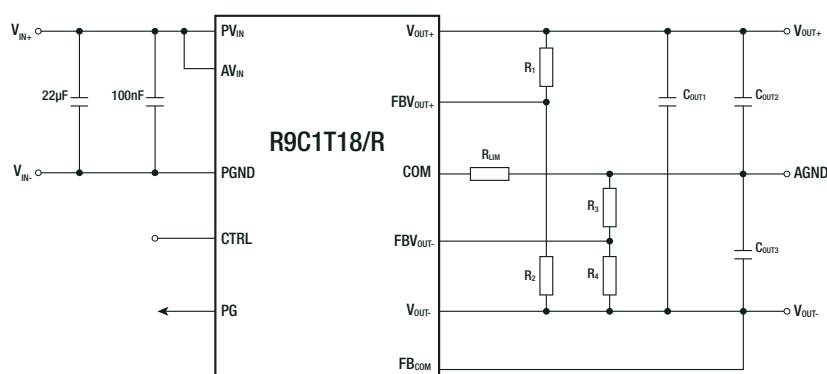
Parameter	Condition	Min.	Typ.	Max.
Output Voltage Trimming	$V_{OUT+}$ to $V_{OUT-}$	15VDC		18VDC
	AGND to $V_{OUT-}$	2.5VDC		$V_{OUT+}$ to $V_{OUT-}$

The R9C1T18/R module creates two regulated outputs. It can be configured as a single output converter,  $V_{OUT+}$  to  $V_{OUT-}$  only, or a dual-output converter,  $V_{OUT+}$  to  $V_{OUT-}$  and COM to  $V_{OUT-}$ . Even though the module uses  $V_{OUT-}$  as the reference point to create two positive output voltages, the outputs can use COM as the reference point and become a positive and a negative output.

These two outputs are controlled independently through hysteresis control. Furthermore, the  $V_{OUT+}$  to  $V_{OUT-}$  is the main output, and COM to  $V_{OUT-}$  uses the main output as its input to create a second regulated output voltage.

**Typical Application**

$V_{TOTAL} = 15\text{-}18\text{VDC}$ ,  $P_{MAX} = 1.5$  watts

**Example**

To set the device into dual configuration, for example to +13/-5V, start to define main output voltage as the sum of both desired voltages (13V + 5V = 18V). 18V are  $V_{OUT+}$  to  $V_{OUT-}$ . Then set the negative output.

+13/-5  $V_{TOTAL} = 18\text{VDC}$ ,  $V_{OUT-} = -5\text{VDC}$

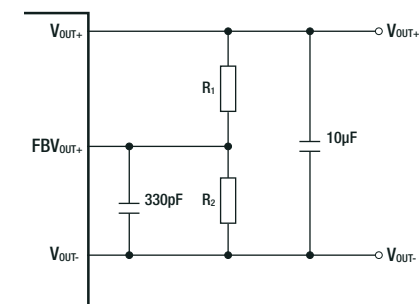
+15/-3  $V_{TOTAL} = 18\text{VDC}$ ,  $V_{OUT-} = -3\text{VDC}$

+12/-5  $V_{TOTAL} = 17\text{VDC}$ ,  $V_{OUT-} = -5\text{VDC}$

Note8: Set  $V_{TOTAL}$  first and afterwards  $V_{OUT-}$ .  $V_{TOTAL}$  must be between 15VDC and 18VDC

**TRIM FUNCTION****Setting the Main Output - Single Configuration**

The  $V_{OUT+}$  to  $V_{OUT-}$  output is the primary module output, regulated by the sensed voltage on  $FBV_{OUT+}$  pin. The  $V_{OUT+}$  to  $V_{OUT-}$  voltage is sensed through a voltage divider ( $R_1$  and  $R_2$ ). When  $FBV_{OUT+}$  voltage is below the turn-off threshold (approx. 10mV above the 2.5V reference), the power stage operates, raising the output voltage. Once the output reaches the turn-off threshold, the power stage turns off, causing the voltage to drop due to load current. When the output voltage falls below the turn-on threshold (approx. 10 mV below the 2.5V reference), the power stage is reactivated. Precise voltage reference and hysteresis control ensure accurate regulation. For enhanced noise immunity, add a 330pF capacitor between  $FBV_{OUT+}$  and  $V_{OUT-}$  pins, avoiding excessive capacitance to prevent output voltage ripple or stability issues. If only a single output is required, connect  $FBV_{OUT-}$  to  $FBV_{OUT+}$  and leave COM pin open.

**Calculation**

$$R_1 = \frac{(V_{OUT+} - V_{ref})}{V_{ref}} \times R_2$$

**Example**

$$R_1 = \frac{(18V - 2.5V)}{(2.5V)} \times 11k\Omega = \mathbf{68k2\Omega}$$

Recommended resistor values for common  $V_{OUT+}$ :

$V_{OUT+}$ [VDC]	$R_2$ [ $\Omega$ ]	$R_1$ [ $\Omega$ ]
15	11k	54k9
16		59k
17		63k4
18		68k1

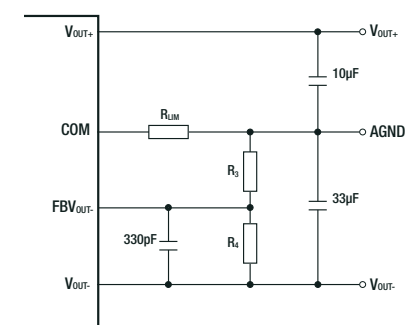
\*(according to E96)

**Setting the Second Output - Dual Configuration**

For isolated gate drivers,  $V_{OUT+}$  to  $V_{OUT-}$  provides the regulated total voltage with the midpoint as the reference. The COM pin regulates the midpoint voltage for accurate positive and negative outputs based on  $FBV_{OUT+}$  feedback.

In Figure below, COM to  $V_{OUT-}$  is monitored through  $R_3$  and  $R_4$  on  $FBV_{OUT-}$ . A 330pF capacitor on  $FBV_{OUT-}$  filters noise. Charging resistor activation, controlled by  $FBV_{OUT-}$ , raises COM to  $V_{OUT-}$  voltage. After reaching the stop charging threshold, the charging resistor turns off. The discharge resistor, with a 20mV hysteresis, is then controlled by  $FBV_{OUT-}$ .

The COM to  $V_{OUT-}$  regulator protects against prolonged high-side FET activation during a COM to  $V_{OUT-}$  short. It monitors COM pin voltage, adjusting the high-side FET duty ratio. If COM pin voltage is below 0.645V while  $FBV_{OUT-}$  is under 2.48V, a 20% duty ratio control overrides normal hysteresis. When COM pin voltage exceeds 0.73V, duty ratio control is disabled, and normal operation resumes.

**Calculation**

$$R_3 = \frac{(V_{OUT-} - V_{ref})}{V_{ref}} \times R_4$$

**Example**

$$R_3 = \frac{(5V - 2.5V)}{2.5V} \times 49k9\Omega = \mathbf{49k9\Omega}$$

Recommended resistor values for common  $V_{OUT-}$ :

$V_{OUT-}$ [VDC]	$R_4$ [ $\Omega$ ]	$R_3$ [ $\Omega$ ]
3	49k9	10k
4		30k1
5		49k9

\*(according to E96)

Note9: To achieve -2.5V on the  $V_{OUT-}$  output remove  $R_4$  and use a value between 10k $\Omega$  and 100k $\Omega$  for  $R_3$ .

**CAPACITOR SELECTION**

For CIN place a 10-μF or more and a 0.1-μF high-frequency decoupling capacitor in parallel close to VIN pins. A capacitance greater than 10μF can be used to reduce the voltage ripple when the series impedance from the voltage source to the VIN pins is large. For COUT1 add a 2.2μF or more and a 100nF capacitor for high-frequency decoupling of VOUT+ to VOUT-. Place the capacitors close to the VOUT+ and VOUT- pins. A capacitance greater than 2.2μF can be used to reduce the output voltage ripple. The selection of COUT2 and COUT3 is based on the gate charge requirement for the gate driver load, the charge balancing during the start-up, and the expected maximum current loading. COUT2 and COUT3 capacitors should be placed close to the load. Calculate COUT2 first.

**Minimal COUT2 Calculation**

$$C_{OUT2}^{(9)} = \frac{Q}{V_{out+} * \frac{V_{pp}}{100}}$$

Parameter		Unit
Q	gate charge	nC
V <sub>pp</sub>	accepted Ripple	%
V <sub>OUT+</sub>	output voltage +	VDC

Recommended COUT2 value is about 10 times higher than the calculated minimum. For simplification, it is recommended to use values for COUT2 between 2.2μF and 10μF. Use the following simplified formula to calculate minimal value of COUT3:

$$C_{OUT3} = \frac{V_{out+}}{V_{out-}} \times 1.1 \times C_{OUT2}$$

**Example +15/-3 Outputs**

$$C_{OUT2} = \frac{55nC}{15V * \frac{1\%}{100}} = 0.366\mu F \quad \text{selected COUT2} = 4.7\mu F$$

$$C_{OUT3} = \frac{V_{OUT+}}{V_{OUT-}} \times 1.1 \times C_{OUT2}$$

$$C_{OUT3} = \frac{15VDC}{3VDC} \times 1.1 \times 4.7\mu F = 25.85\mu F \quad \text{user selected COUT3} = 3 \times 10\mu F$$

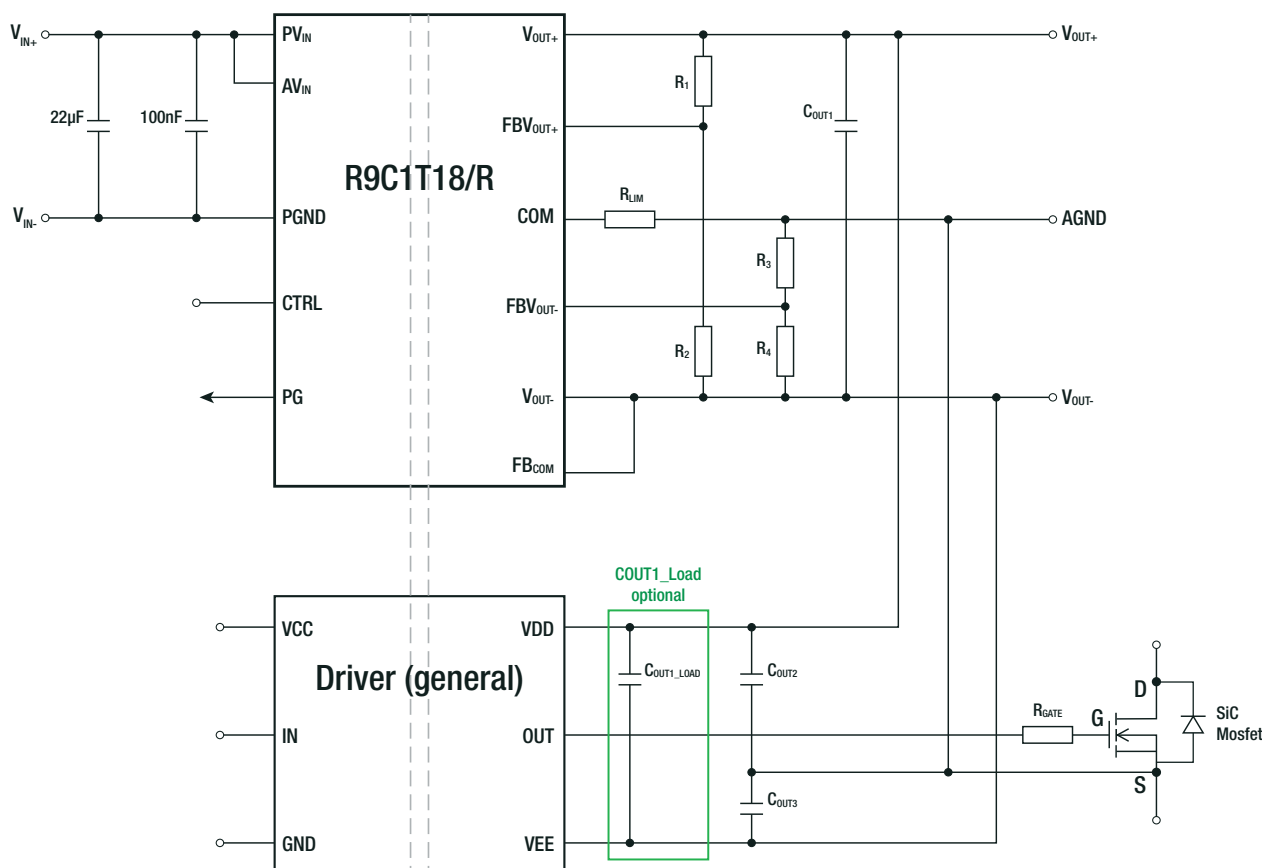
Parameter		Value
Q	gate charge	55nC
V <sub>pp</sub>	accepted Ripple	1%
V <sub>OUT+</sub>	output voltage +	15VDC
V <sub>OUT-</sub>	output voltage -	3VDC

CIN	min. COUT1 (VOUT+ to VOUT-)	VOUT+ to COM	VOUT- to COM	recommended COUT2	recommended COUT3
10μF + 100nF	2.2μF + 100nF	12VDC	5VDC	4.7μF	15μF
10μF + 100nF	2.2μF + 100nF	15VDC	3VDC	4.7μF	3x10μF

Note10:  $(V_{OUT+}/V_{OUT-}) * 1.1$  defines the minimal COUT3 to COUT2 ratio. Consider all capacitance connected to VOUT+ to COM in the system as COUT2 and then calculate the minimal COUT3. If COUT3 in the system is lower than the calculated minimum, the device may not start.

### CAPACITOR SELECTION

#### Typical gate drive application



In order to reduce the number of capacitors needed for COUT2 and COUT3, an additional capacitor COUT1\_LOAD can be added at the load (driver circuit in the figure above) between VOUT+ and VOUT- rails.

COUT1_LOAD value [µF]	COUT2 value [%]	COUT3 value [%]
Not used	100%	100%
4.7µF	60%	60%
10µF	40%	40%
22µF	30%	30%

For +15V/-3V configuration without using COUT1\_LOAD capacitor the recommended values of COUT2 = 4.7µF and COUT3 = 3 x 10µF. By using 10µF as COUT1\_LOAD, the value of COUT2 can be reduced to 40% of its original value. COUT2 can be then reduced from 4.7µF to 2.2µF. The minimal ratio of COUT3 to COUT2 has to be fulfilled, so the same equation as before applies to COUT3 calculation.

#### Example

$$C_{OUT3} = \frac{V_{OUT+}}{V_{OUT-}} \times 1.1 \times C_{OUT2}$$

$$C_{OUT3} = \frac{15VDC}{3VDC} \times 1.1 \times 2.2\mu F = 12.1\mu F$$

The closest higher value is 15µF. The number of COUT3 capacitors have been reduced from 3 pieces to 1 piece. In total the design contains 1 capacitor less.

**DEFINING RLIM**

When the device has been configured to dual positive or dual negative configuration, set up the RLIM resistor as the maximum load current ( $I_{OUT\_max}$ ) needed for  $V_{OUT-}$  to COM path using following equation:

**Calculation**

$$R_{LIM} = \frac{V_{OUT-}}{I_{OUT\_max}} - R_{LIM\_internal}$$

\*  $R_{LIM\_internal} = 30\Omega$

\*  $I_{OUT\_max}$  = depends on application

**Example  $R_{LIM}$  for  $V_{OUT-} = 5VDC$** 

$$R_{LIM} = \frac{5V}{12mA} - 30\Omega = 383\Omega$$

\*  $I_{OUT\_max}$  has been defined as 12mA for the target application

When the device has been configured to dual output configuration with one positive and one negative output, set up the RLIM resistor using following equation:

**Calculation**

$$R_{LIM}^{(11)} = \frac{V_{OUT-}}{38 \times V_{OUT-} \times C_{OUT3} + 0.005} - R_{LIM\_internal}$$

**Example RLIM for  $V_{OUT-} = 5V$  and  $C_{OUT3} = 40\mu F$** 

$$R_{LIM} = \frac{5V}{38 \times 5V \times 0.00004F + 0.005} - 30\Omega = 367\Omega$$

\* selected RLIM 10% lower=332 Ohm

Note11: The equation assumes 15% tolerance of the  $C_{OUT3}$  capacitor and certain response time to transient conditions and load for the driver circuit. Higher value of the limiting resistor can be used in case the power losses have to be minimized. Contact RECOM for further assistance to calculate the right RLIM value for your application.

**CONTROL FUNCTION**

Parameter	Condition	Min.	Typ.	Max.
Control Pin Voltage	CTRL pin to PGND	0VDC		5.5VDC
ON/OFF CTRL	rising			2.1VDC
	falling	0.8VDC		
Input Current	no load			40mA
	full load		190mA	
Input Current of CTRL Pin	$V_{CTRL} = 5.0V$		5 $\mu A$	18 $\mu A$

**POWER GOOD OPERATING CONDITIONS**

Parameter	Condition	Min.	Typ.	Max.
PowerGood threshold	PG of negated	90% of $V_{FB}$		110% of $V_{FB}$
PowerGood pin voltage	PG pin to PGND	0VDC		5.5VDC
Primary side soft start time out	Timer begins when $V_{IN} > UVLO$ and CTRL= High and reset when Powergood pin indicates Good		16ms	

**AGND REGULATIONS HYSTERESIS**

Parameter	Condition	Min.	Typ.	Max.
Feedback regulation reference voltage	AGND to $V_{OUT-}$	2.4675VDC	2.5VDC	2.5325VDC
COM pin Short Charge comparator rising threshold to exit PWM	rising		0.73VDC	
On-Time during COM pin Short Charge PWM mode	COM pin < 0.645VDC, while $FBV_{OUT-}$ pin < 2.48VDC		1.2 $\mu s$	
Off-Time during COM pin Short Charge PWM mode	COM pin < 0.645VDC, while $FBV_{OUT-}$ pin < 2.48VDC		5 $\mu s$	

**OUTPUT UNDER VOLTAGE LOCKOUT**

Parameter	Condition	Min.	Typ.	Max.
UVLO rising threshold ( $V_{OUT+}$ to $V_{OUT-}$ )	Voltage at $FBV_{OUT+}$		0.9VDC	
UVLO hysteresis ( $V_{OUT+}$ to $V_{OUT-}$ )	Voltage at $FBV_{OUT+}$		0.2VDC	

**OUTPUT OVER VOLTAGE LOCKOUT**

Parameter	Condition	Min.	Typ.	Max.
OVLO rising threshold	Voltage from $V_{OUT+}$ to $V_{OUT-}$ , rising	29.45VDC	31VDC	32.55VDC
OVLO falling threshold	Voltage from $V_{OUT+}$ to $V_{OUT-}$ , falling	27.55VDC	29VDC	30.45VDC

**COMMON MODE TRANSIENT IMMUNITY (CMTI)**

Parameter	Condition	Min.	Typ.	Max.
Common Mode Transient Immunity				$\pm 150V/ns$

# R9C1T18/R Series / Power Module

## 1.5W / 8.5V-18VDC / 36 Pin SSOP Package

### PROTECTIONS

Parameter	Condition	Min.	Typ.	Max.
Over Power Protection (OPP)				latch-off
Over Temperature Protection <sup>(12)</sup> (OTP)				latch-off
Over Temperature Shutdown Setpoint			160°C±10°C	
Over Temperature Shutdown Hysteresis	cool down after latch-off before restart is enabled		20°C±5°C	

Note12: The R9C1T18/R integrates power stages with over-temperature protection. If temperatures exceed limits, it stops switching and enters a latch-off protection mode.

### THERMAL OPERATING CONDITIONS

Parameter	Condition	Min.	Typ.	Max.
Thermal Impedance	junction to case		28.5K/W	
	junction to board		25.9K/W	
	junction to ambient, refer to „Note7“		52.3K/W	
ESD	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001			±2kV
	Charged-device model (CDM), per JEDEC specification JESD22-C101			±500V
Moisture Sensitive Level			Level 3, 260°C, 168hrs	

### ISOLATION CAPABILITIES

Parameter	Condition	Min.	Typ.	Max.
Comparative tracking index (CTI)	DIN EN 60112 (VDE 0303-11); IEC 60112			600VDC
Overvoltage Category	Rated mains voltage ≤ 300 VRMS			I-IV
	Rated mains voltage ≤ 600 VRMS			I-IV
	Rated mains voltage ≤ 1000 VRMS			I-III
Isolation Voltage <sup>(13)</sup>	tested in qualification			5kVAC/1min.
	tested in production			6kVAC/1sec.
Repetitive peak isolation voltage	AC voltage (bipolar)			1.4kVp
Working isolation voltage <sup>(14)</sup>	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test			1000VRMS
	DC voltage			1.4kVDC
Transient isolation voltage	tested in qualification			7kVp/1min.
	tested in production			8.4kVp/1sec.
Impulse voltage	waveform per IEC 62368-1			7.6kVp
Surge isolation voltage	waveform per IEC 62368-1			10kVp
Isolation Resistance	input to output	VIO= 500VDC, TA= 25°C	1000GΩ	
		VIO= 500VDC, 100°C ≤ TA ≤ 125°C	100GΩ	
		VIO= 500VDC at TS= 150°C	1GΩ	
Isolation Capacitance	input to output			3.5pF
Internal Clearance	transformer power isolation	120μm		
	capacitive signal isolation	15.4μm		
External Clearance		8mm		

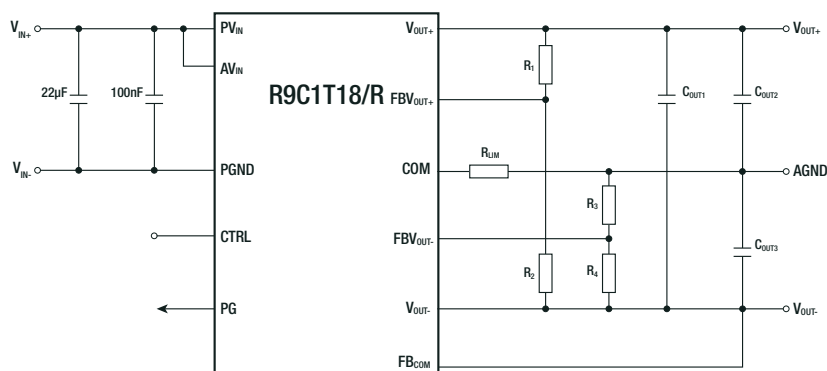
Note13: High voltage isolation testing of a barrier component can degrade isolation capability. RECOM therefore strongly advises against repeated high-voltage isolation testing. If required, reduce specified retest voltage by 20%.

Note14: When the insulation in the R9C1T18/R series is not used as a safety barrier, i.e. provides functional isolation only, continuous or switched voltages across the barrier up to 1.4kVp are sustainable. This is established by measuring the partial discharge inception voltage in accordance with IEC60270. Please contact techsupport@recom-power.com for further information.

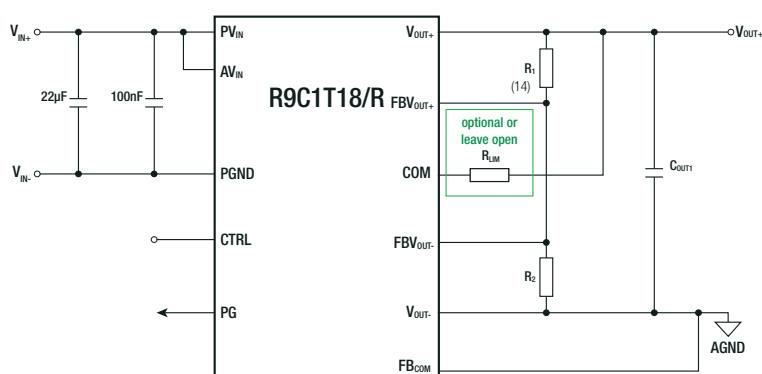


### APPLICATION INFORMATION

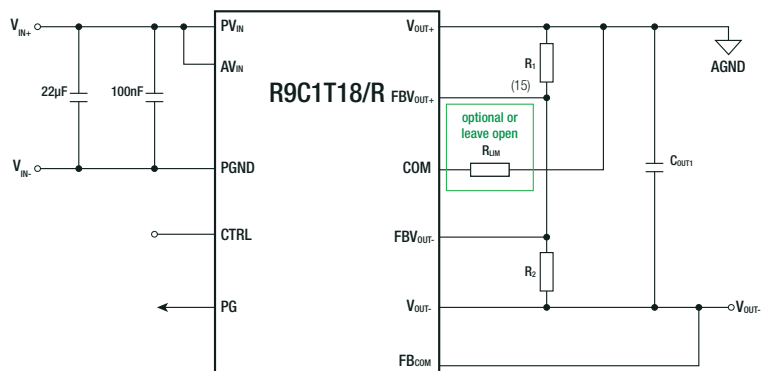
#### Dual Output (one positive, one negative)



#### Single Output (positive)

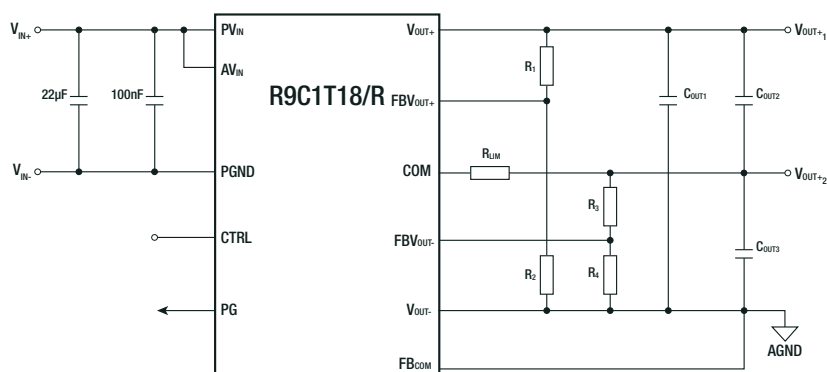


#### Single Output (negative)



Note15: Use  $R_{LIM}$  only for very low load cases (<15mA) and when very high switching frequency is used (>250kHz) the  $R_{LIM}$  value should be at least 1k $\Omega$ .

#### Dual Output (both positive)

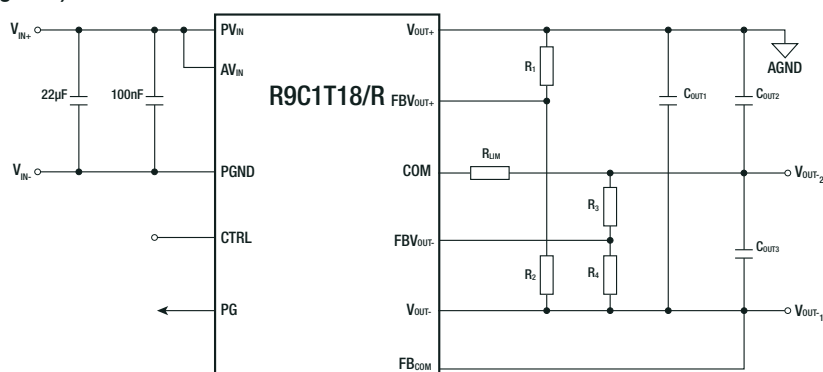


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1.5W / 8.5V-18VDC / 36 Pin SSOP Package

## APPLICATION INFORMATION

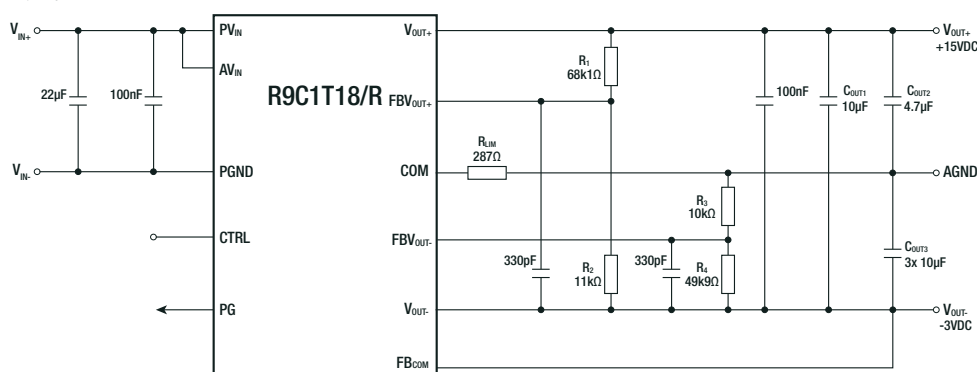
### Dual Output (both negative)



## APPLICATION EXAMPLES

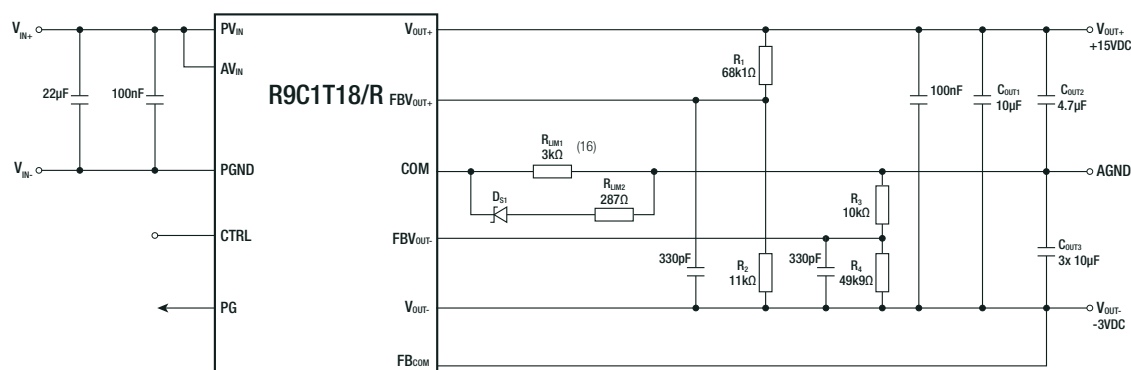
### Dual Output (one positive, one negative)

$V_{OUT+} = 15VDC$ ,  $V_{OUT-} = 3VDC$ ,  $V_{TOTAL} = 18VDC$



### Dual Output (one positive, one negative) - RDR configuration

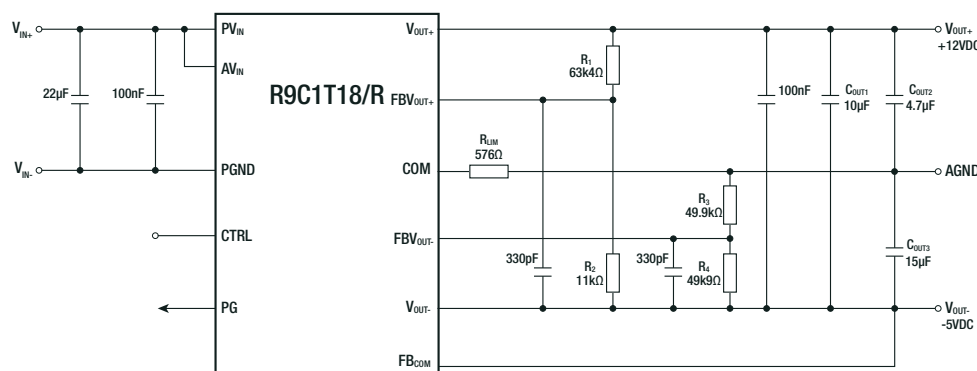
$V_{OUT+} = 15VDC$ ,  $V_{OUT-} = 3VDC$ ,  $V_{TOTAL} = 18VDC$



Note16: Using a Schottky diode and a resistor in parallel with a resistor allows programming the charge and discharge current independently. This RDR configuration greatly reduces power losses of the device.

### Dual Output (one positive, one negative)

$V_{OUT+} = 12VDC$ ,  $V_{OUT-} = 5VDC$ ,  $V_{TOTAL} = 17VDC$





**DIMENSION & PHYSICAL CHARACTERISTICS****Pad Information**

Pad #	Function	Description
1, 2, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18	PGND	Primary side power ground. Place several vias to copper pours for thermal relief.
3	PG	Power good open-drain output. Low when UVLO, OVLO, UVP, OVP, and OTP are not triggered.
4	CTRL	Pull high to enable the device. Connect to ground to disable the device.
6	AV <sub>IN</sub>	Primary side analog input. Connect a 330pF ceramic capacitor between AV <sub>IN</sub> and pin 5. Connect pin6 to pin7.
7	PV <sub>IN</sub>	Primary side power input. Connect a 0.1µF and a 22µF ceramic capacitor to pin 8.
19, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 36	V <sub>OUT-</sub>	Secondary side negative output voltage.
28, 29	V <sub>OUT+</sub>	Secondary side positive output voltage. Connect a 10µF and 0.1µF ceramic capacitor between V <sub>OUT+</sub> and V <sub>OUT-</sub> .
32	COM	Connect current limiting resistor to COM node of circuit. See application example or „Defining RLIM“ section.
33	FBV <sub>OUT-</sub>	FBV <sub>OUT</sub> Feedback (COM – V <sub>OUT-</sub> ) output voltage sense pin used to set the output (COM – V <sub>OUT-</sub> ) voltage.
34	FBV <sub>OUT+</sub>	FBV <sub>OUT</sub> Feedback (V <sub>OUT+</sub> – V <sub>OUT-</sub> ) output voltage sense pin used to set the output (V <sub>OUT+</sub> – V <sub>OUT-</sub> ) voltage.
35	FB <sub>COM</sub>	Use as reference for FBV <sub>OUT+</sub> and FBV <sub>OUT-</sub> .

**LAYOUT GUIDELINES**

The R9C1T18/R integrated isolated power solution simplifies system design and reduces board area usage. Follow these guidelines for proper PCB layout to achieve optimal performance:

- Place decoupling capacitors as close as possible to the device pins. On the primary side, place the capacitors between pin 7 (power V<sub>IN</sub>) and pins 8–18 (power GND). Optionally, place a capacitor between pin 6 (analog V<sub>IN</sub>) and pins 1, 2, and 5 (analog GNDP). Always put lower values and smaller packages as close to the IC pins as possible.
- For the isolated secondary side, place the capacitors between pin 28, 29 (V<sub>OUT+</sub>) and pins 19–25, 30–31, 35–36 (V<sub>OUT-</sub>). Put capacitors between V<sub>OUT+</sub> and V<sub>OUT-</sub> close to the IC.
- The capacitors between V<sub>OUT+</sub>/COM and COM/V<sub>OUT-</sub> should be placed near the output device (gate driver input).
- Connection of Feedback circuit to FB<sub>COM</sub> (pin 35) should be separated from V<sub>OUT-</sub> plane. Use one short trace to connect this pin to the feedback low-side resistors. Place FB resistors and capacitors close to each other and close to the IC.
- Separate the traces from the COM pin and the FB<sub>V<sub>OUT-</sub></sub> pin while routing. If possible, use a via near the FB<sub>V<sub>OUT-</sub></sub> pin to route the feedback connection through a different layer.
- Sense connections should be connected to the capacitors at the output device (gate drivers).
- The package of the module dissipates heat through the GNDP and V<sub>OUT-</sub> pins. Ensure sufficient copper around the IC, preferably connected to the ground plane through multiple vias, is present on the GNDP and V<sub>OUT-</sub> pins. A minimum of four layers and using 2oz copper in internal layers are recommended for optimal thermal PCB design.
- We recommend connecting the V<sub>IN</sub>, GND, V<sub>OUT+</sub>, and V<sub>OUT-</sub> pins to internal ground or power planes through multiple vias. Alternatively, make the traces connected to these pins as wide as possible to minimize losses.
- Pay close attention to the spacing between the primary side and the output signals on the outer layers of the PCB. The effective creepage and clearance of the system are reduced if the gap between the primary and isolated sides is smaller than that of the R9C1T18/R package pins. Avoid placing any traces under the module.

**R9C1T18/R Series / Power Module****1.5W / 8.5V-18VDC / 36 Pin SSOP Package****EMC FILTERING SUGGESTIONS ACCORDING TO EN55032**

The successful EMC filtering of the R9C1T18/R requires the selection of suitable components, correct PCB layout, and mechanical shielding of the application where the module is used. Here are some additional notes for the PCB layout:

- Optionally, inner layers can be used to create a high-frequency bypass capacitor between GNDP and VOUT- to mitigate radiated emissions. Overlapping these layers can be beneficial for reducing radiated emissions. However, this solution might not be suitable for applications requiring fast dV/dt switching. Suitable core thickness and material can help set the correct minimum allowed capacitance between primary and secondary side.
- If the isolation requirements permit, place the internal ground power plane (GNDP) under the module package area. This can serve as partial shielding for the device, helping to reduce radiated emissions.
- If the primary side and isolated secondary output ground planes cannot overlap (as per previous notes), mechanical shielding may be necessary to meet EN55032 Class B requirements. We recommend connecting the metal shielded box to the primary GND.

**PACKAGING INFORMATION**

Parameter	Type		Value
Packaging Dimension (LxWxH)	Suffix -R: tape and reel	reel diameter + width	330.2mm + 24.4mm height 13inch + 0.96inch height
	Suffix -CT: moisture barrier bag		100 x 150 x 30 mm 3.94 x 5.90 x 1.18 inch
	Suffix -R: tape and reel		750pcs
Packaging Quantity	Suffix -CT: moisture barrier bag		10pcs
Storage Temperature Range			-40°C to +125°C
Storage Humidity	non-condensing		5% - 95% RH max.

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