

OLED DISPLAY MODULE

Product Specification

CUSTOMER	Standard	
PRODUCT NUMBER	DD-128128FC-5B	
CUSTOMER APPROVAL		Date

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Elijah Ebo	Anthony Perkins	Bazile Peter
Date: 02/04/08	Date:02/04/08	Date: 02/04/08

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	02 April 08			First Issue	

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1 MAIN FEATURES

ITEM	CONTENTS
Display Format	128 (RGB) x 128 Dots
Overall Dimensions	33.8 x 34.00 x 1.60 mm
Colour	262,144 Colour
Active Area	26.855 x 26.864 mm
Viewing Area	28.855 x 28.864 mm
Display Mode	Passive Matrix (1.50")
Driving Method	1/128 duty
Driver IC	SSD1355
Operating temperature	-30 ~ +70
Storage temperature	-40 ~ +80

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2 MECHANICAL SPECIFICATION

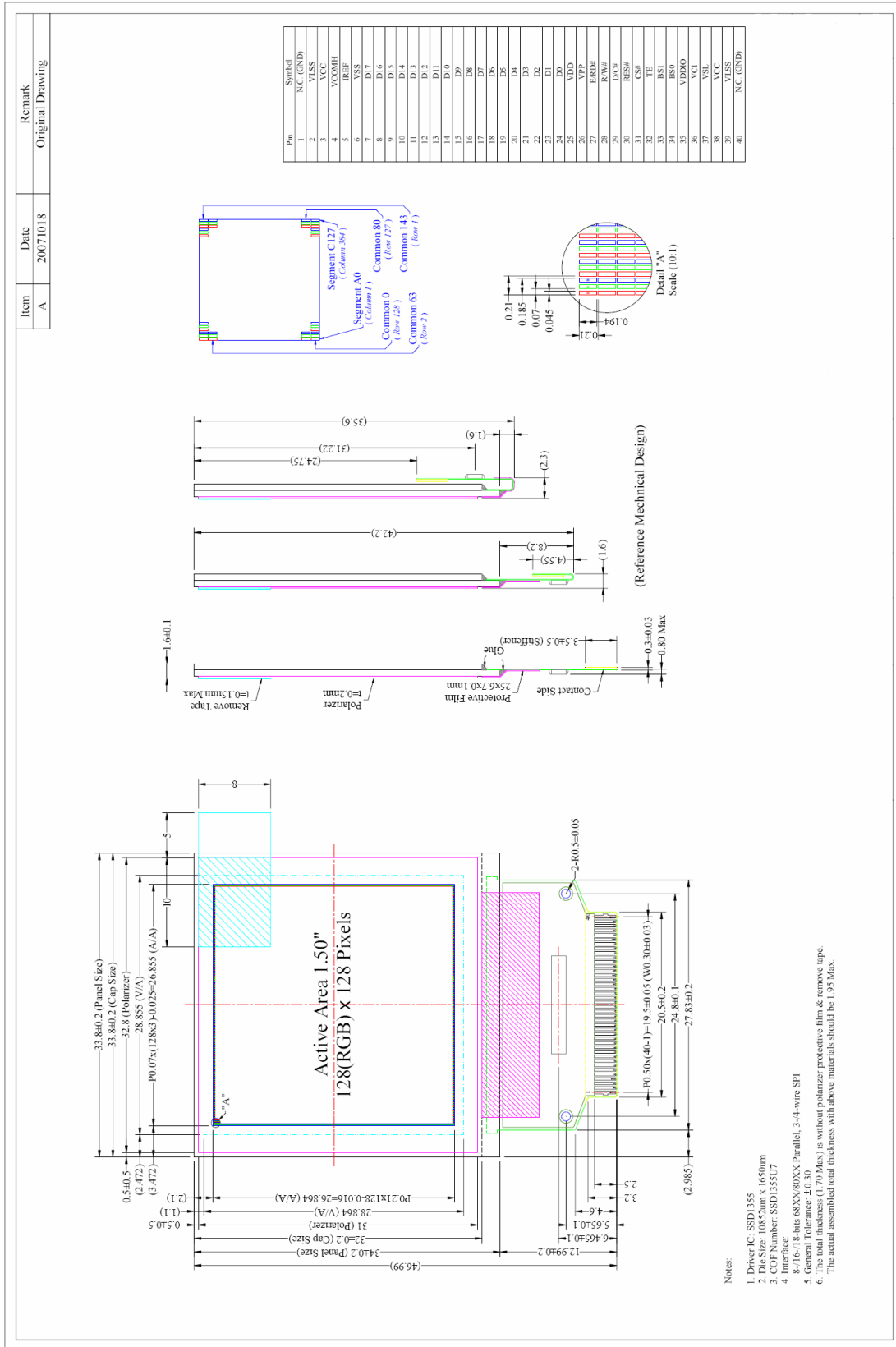
2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	128 (RGB) x 128	Dots
Overall Dimensions	33.8 x 34.00 x 1.60	mm
Viewing Area	28.855 x 28.864	mm
Active Area	26.855 x 26.864	mm
Dot Size	0.045 x RGB x 0.194	mm
Dot Pitch	0.07 x RGB x 0.21	mm
Weight	3.85	g
IC Controller/Driver	SSD1355 (COF)	

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2.2 MECHANICAL DRAWING



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3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Min	Max	Unit	Note
Supply Voltage for Operation	V _{CI}	-0.3	4	V	Note 1, 2
Supply Voltage for Logic	V _{DD}	-0.5	2.75	V	
Supply Voltage for I/O Pins	V _{DDIO}	-0.5	V _{CI}	V	
Supply Voltage for Display	V _{CC}	-0.5	16	V	
Operating Current for V _{CC}	I _{CC}	-	35	mA	
Operating Temperature	T _{op}	-30	70	°C	
Storage Temperature	T _{stg}	-40	80	°C	
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of “VSS=0V”.

Note 2: When this module is used beyond above absolute maximum ratings, permanent damage to the module may occur. Also for normal operations it's desirable to use this module under the conditions according to Section 3.2 “Electrical Characteristics”. If this module is used beyond these conditions the module may malfunction and the reliability could deteriorate.

3.2 ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V _{CI}	Ta = 25°C	2.4	2.8	3.5	V
Supply Voltage for Logic	V _{DD}	Ta = 25°C	2.4	2.5	2.6	V
Supply Voltage for I/O pins	V _{DDIO}	Ta = 25°C	1.6	1.8	V _{CI}	V
Supply Voltage for Display	V _{CC}	Ta = 25°C	14.5	15	15.5	V
High Level Input	V _{IH}		0.8xV _{DDIO}	-	V _{DDIO}	V
Low Level Input	V _{IL}		0	-	0.2xV _{DDIO}	V
High Level Output	V _{OH}	I _{out} =100μA,3.3MHz	0.9xV _{DDIO}	-	V _{DDIO}	V
Low Level Output	V _{OL}	I _{out} =100μA,3.3MHz	0	-	0.1xV _{DDIO}	V
Operating Current for V _{CI}	I _{CI}	Note 1		500	625	μA
		Note 2		500	625	μA
Operating Current for V _{CC}	I _{CC}	Note 1		18.7	23.4	mA
		Note 2		32.5	40.6	mA
Sleep Mode Current for V _{CI}	I _{CI, SLEEP}			1	5	μA
Sleep Mode Current for V _{CC}	I _{CC, SLEEP}			1	5	μA

Note 1 V_{CI} = 2.8V, V_{CC} = 15V, 50% Display area turned on.

Note 2 V_{CI} = 2.8V, V_{CC} = 15V, 100% Display area turned on

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3.3 INTERFACE PIN ASSIGNMENT

No.	Symbol	I/O	Function
1	N.C. (GND)	-	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.
2	VLSS	I	Ground of Analogue Circuit This is an analogue ground pin. It should be connected to VSS
3	VCC	I	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. It must be connected to external source.
4.	VCOMH	I	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
5	IREF	I	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 13.5 μ A
6	VSS	I	Ground of Logic Circuit This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
7~24	D17~D0	I/O	Host Data Input/output Bus These pins are 18-bit bi-directional data bus to be connected to the microprocessors data bus. When serial mode is selected, D1 will be serial data input SDIN. Unused pins must be connected to VSS.
25	VDD	I	Power Supply for Core Logic Circuit This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.
26	VPP	I	Power Supply for Non-Volatile OTP Memory Programming This is the NVM programming voltage supply pin. It must be connected to VDD.
27	E/RD#	I	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.

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28	R/W#	I	<p>Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write(WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin will be the serial clock input SCLK.</p>															
29	D/C#	I	<p>Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D17~D0 is treated as display data. When the pin is pulled low, the input at D17~D0 will be transferred to the command register. For detail relationship to MCU signals, please refer to the Timing Characteristics Diagrams.</p>															
30	RES#	I	<p>Power Reset for Controller and Driver This pin is reset signal input.. When the pin is low, initialization of the chip is executed.</p>															
31	CS#	I	<p>Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</p>															
32	TE	O	<p>Tearing Effect SYNC Output To synchronize the MCU to the frame display writing. Do not connect if not used</p>															
33 34	BS1 BS0	I	<p>Communicating Protocol Select These pins are MCU interface selection input. See the following table:</p> <table border="1"> <thead> <tr> <th></th> <th>BS0</th> <th>BS1</th> </tr> </thead> <tbody> <tr> <td>3-wire SPI</td> <td>1</td> <td>0</td> </tr> <tr> <td>4-wire SPI</td> <td>0</td> <td>0</td> </tr> <tr> <td>68XX-parallel (8-/16-/18-bit)</td> <td>1</td> <td>1</td> </tr> <tr> <td>80XX-parallel (8-/16-/18-bit)</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>Set the command 36h for the MCU bus interface as SPI/8-bit (Default) or 16-/18-bit.</p>		BS0	BS1	3-wire SPI	1	0	4-wire SPI	0	0	68XX-parallel (8-/16-/18-bit)	1	1	80XX-parallel (8-/16-/18-bit)	0	1
	BS0	BS1																
3-wire SPI	1	0																
4-wire SPI	0	0																
68XX-parallel (8-/16-/18-bit)	1	1																
80XX-parallel (8-/16-/18-bit)	0	1																
35	VDDIO	I	<p>Power Supply for I/O Pin This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D17, control signals...) are pulled high, they should be connected to VDDIO.</p>															
36	VCI	I	<p>Power Supply for Operation This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.</p>															
37	VSL	I	<p>Voltage Output Low Level for SEG Signal This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.</p>															
38	VCC	I	<p>Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. It must be connected to external source.</p>															
39	VLSS	I	<p>Ground of Analog Circuit This is an analog ground pin. It should be connected to VSS</p>															

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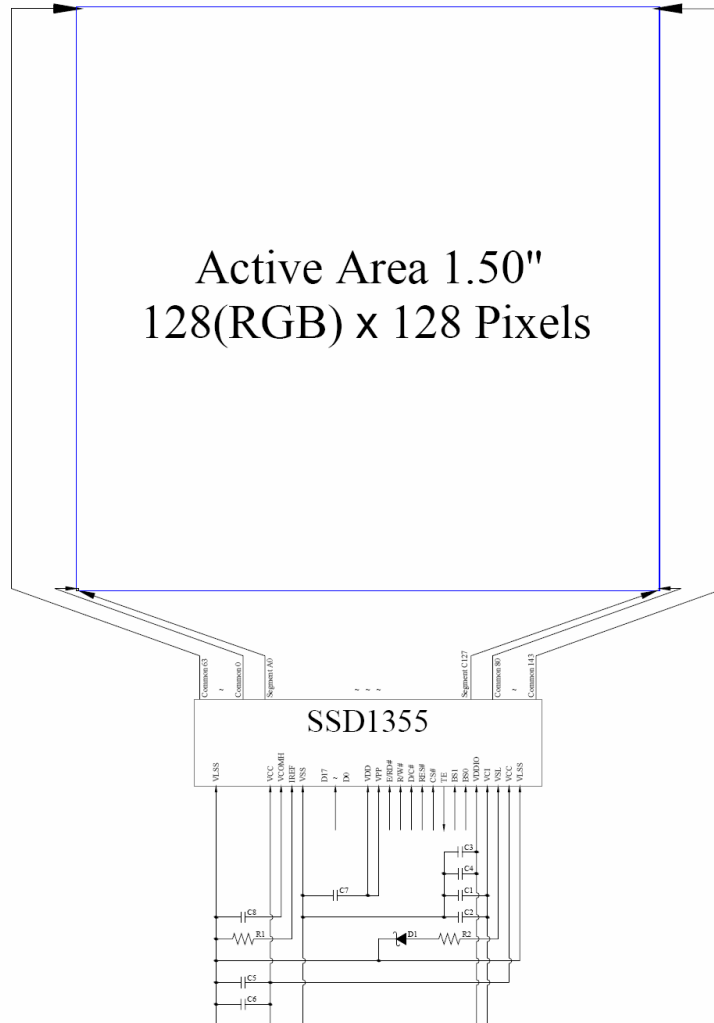
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40	N.C.(GND)	-	<p>Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.</p>
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3.4 BLOCK DIAGRAM



MCU Interface Selection: BS0 and BS1

Pins connected to MCU interface □ D17~D0, E/RD#, R/W#, D/C#, RES#, and CS#

- C1,C3,C5: 0.1μF
- C2,C4: 4.7μF
- C6: 10μF
- C7: 1uF
- C8: 4.7 uF / 25V Tantalum Capacitor
- R1: 680k Ω, $R1 = (\text{voltage at IREF} - VSS) / IREF$
- R2: 50 Ω, 1/4W
- D1: ≤1.4V, 0.5W

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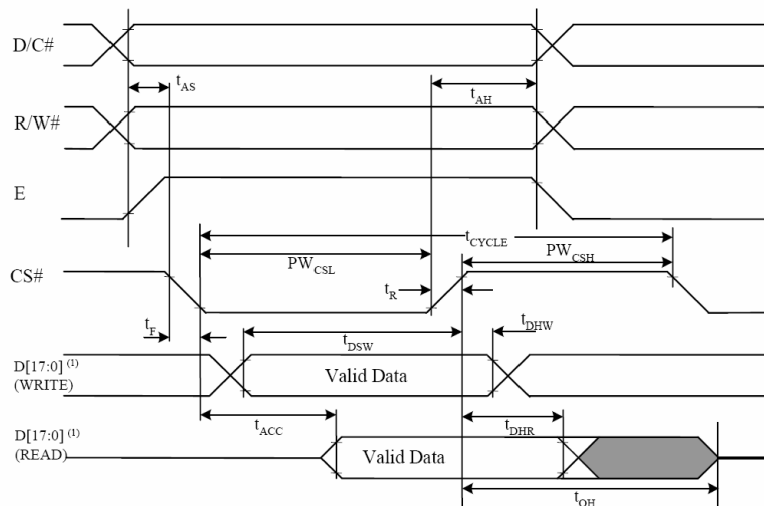
3.5 TIMING CHARACTERISTICS

3.5.1 AC CHARACTERISTICS

3.5.2 68XX-Series MPU Parallel Interface Timing Characteristics

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	300	-	ns
Address Setup Time	t_{AS}	10	-	ns
Address Hold Time	t_{AH}	0	-	ns
Write Data Setup Time	t_{DSW}	40	-	ns
Write Data Hold Time	t_{DHW}	7	-	ns
Read Data Hold Time	t_{DHR}	20	-	ns
Output Disable Time	t_{OH}	-	70	ns
Access Time	t_{ACC}	-	140	ns
Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	PW_{CSL}	120 60	-	ns
Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	PW_{CSH}	60 60	-	ns
Rise Time	t_{R}	-	15	ns
Fall Time	t_{F}	-	15	ns

($V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$, $V_{\text{DDIO}} = 1.6\text{V}$, $V_{\text{CI}} = 2.8\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



When 8-bit Used: D[7:0] Instead
 When 16-bit Used: D[15:0] Instead
 When 18-bit Used: D[17:0] Instead

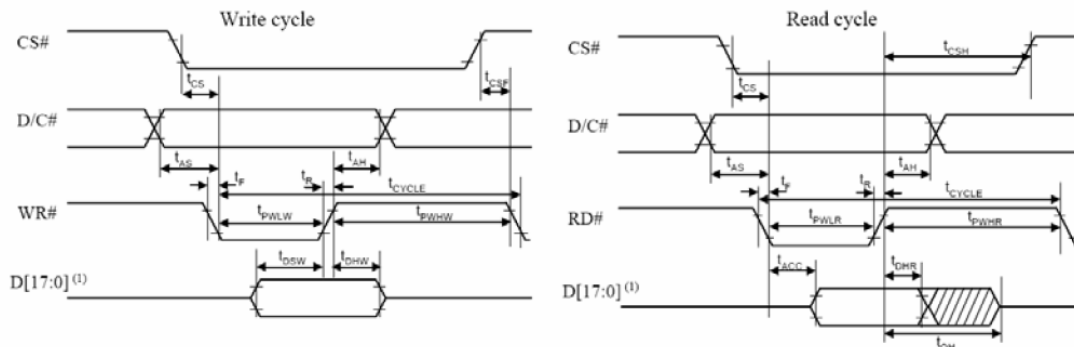
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3.5.3 8080-Series MPU Parallel Interface Timing Characteristics

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	300	-	ns
Address Setup Time	t_{AS}	10	-	ns
Address Hold Time	t_{AH}	0	-	ns
Write Data Setup Time	t_{DSW}	40	-	ns
Write Data Hold Time	t_{DHW}	7	-	ns
Read Data Hold Time	t_{DHR}	20	-	ns
Output Disable Time	t_{OH}	-	70	ns
Access Time	t_{ACC}	-	140	ns
Read Low Time	t_{PWLR}	150	-	ns
Write Low Time	t_{PWLW}	60	-	ns
Read High Time	t_{PWHR}	60	-	ns
Write High Time	t_{PWHW}	60	-	ns
Chip Select Setup Time	t_{CS}	0	-	ns
Chip Select Hold Time to Read Signal	t_{CSH}	0	-	ns
Chip Select Hold Time	t_{CSF}	20	-	ns
Rise Time	t_{R}	-	15	ns
Fall Time	t_{F}	-	15	ns

($V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$, $V_{\text{DDIO}} = 1.6\text{V}$, $V_{\text{CI}} = 2.8\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



* When 8-bit Used: D[7:0] Instead
 When 16-bit Used: D[15:0] Instead
 When 18-bit Used: D[17:0] Instead

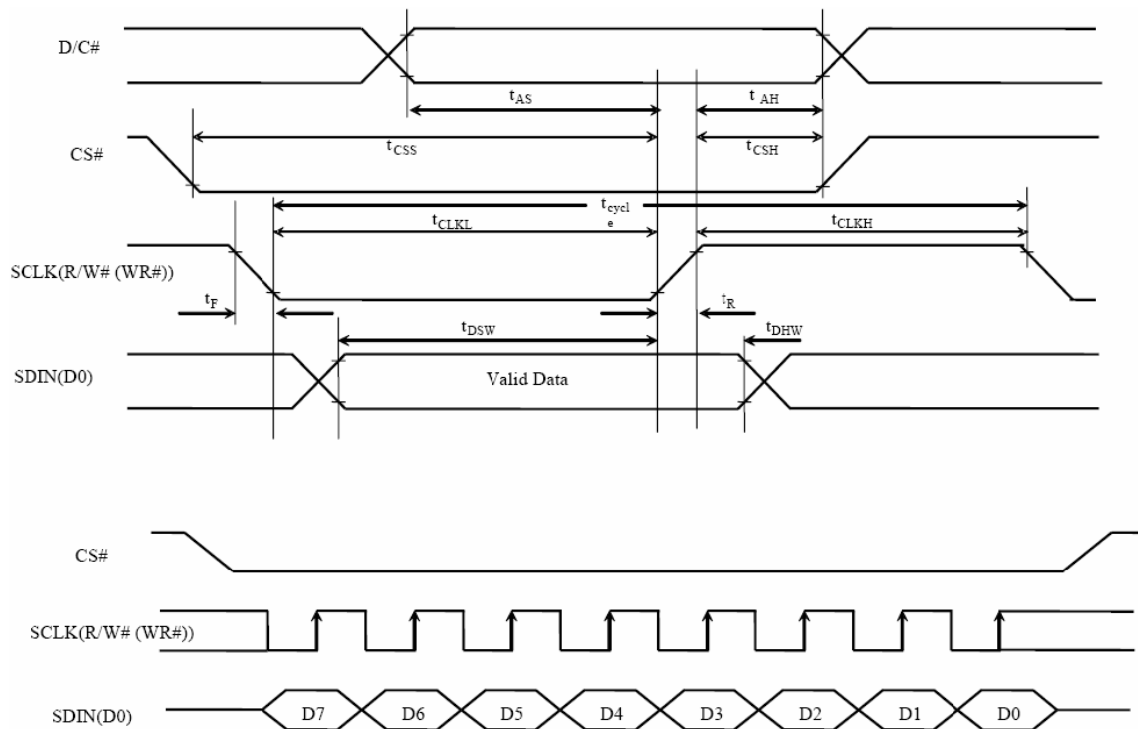
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3.5.4 Serial Interface Timing Characteristics (4-wire SPI)

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	50	-	ns
Address Setup Time	t_{AS}	15	-	ns
Address Hold Time	t_{AH}	15	-	ns
Chip Select Setup Time	t_{CSS}	20	-	ns
Chip Select Hold Time	t_{CSH}	10	-	ns
Write Data Setup Time	t_{DSW}	15	-	ns
Write Data Hold Time	t_{DHW}	15	-	ns
Clock Low Time	t_{CLKL}	20	-	ns
Clock High Time	t_{CLKH}	20	-	ns
Rise Time	t_R	-	15	ns
Fall Time	t_F	-	15	ns

($V_{DD} - V_{SS} = 2.4V$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 2.8V$, $T_a = 25^\circ C$)



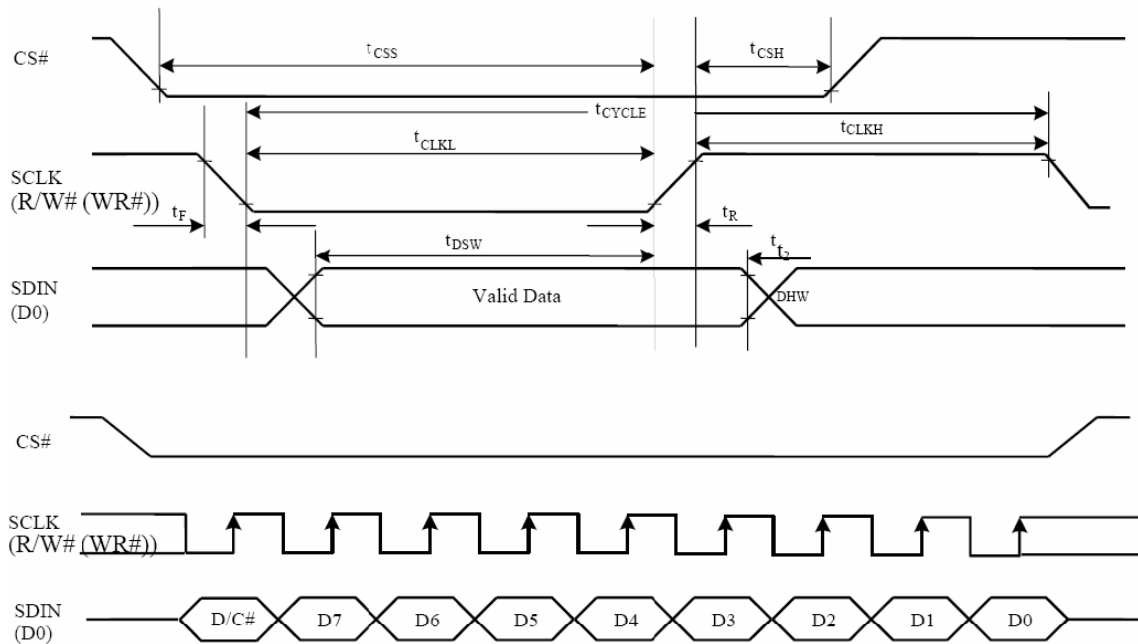
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3.5.5 Serial Interface Timing Characteristics (3-wire SPI)

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	50	-	ns
Address Setup Time	t_{AS}	15	-	ns
Address Hold Time	t_{AH}	15	-	ns
Chip Select Setup Time	t_{CSS}	20	-	ns
Chip Select Hold Time	t_{CSH}	10	-	ns
Write Data Setup Time	t_{DSW}	15	-	ns
Write Data Hold Time	t_{DHW}	15	-	ns
Clock Low Time	t_{CLKL}	20	-	ns
Clock High Time	t_{CLKH}	20	-	ns
Rise Time	t_{R}	-	15	ns
Fall Time	t_{F}	-	15	ns

($V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$, $V_{\text{DDIO}} = 1.6\text{V}$, $V_{\text{CI}} = 2.8\text{V}$, $T_a = 25^\circ\text{C}$)



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4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness(White)	L _{br}	With Polarizer	70	90	-	cd/m ²
C.I.E.(White)	(X)	With Polarizer	0.26	0.30	0.34	-
	(Y)		0.29	0.33	0.37	
C.I.E.(Red)	(X)	With Polarizer	0.60	0.64	0.68	-
	(Y)		0.30	0.34	0.38	
C.I.E.(Green)	(X)	With Polarizer	0.27	0.31	0.35	-
	(Y)		0.58	0.62	0.66	
C.I.E.(Blue)	(X)	With Polarizer	0.10	0.14	0.18	-
	(Y)		0.12	0.16	0.20	
Dark Room Contrast	CR		-	>2000:1	-	-
Viewing Angle			>160	-	-	degree

Optical measurement taken at V_{CI} = 2.8V, V_{CC} = 15V

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5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

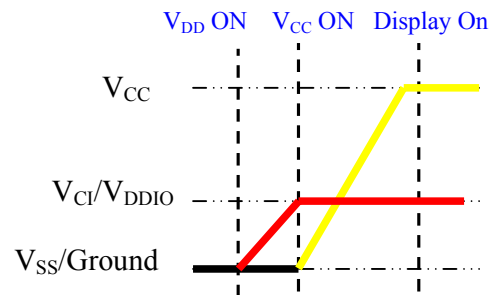
Please refer to the Technical Manual for the SSD1355

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

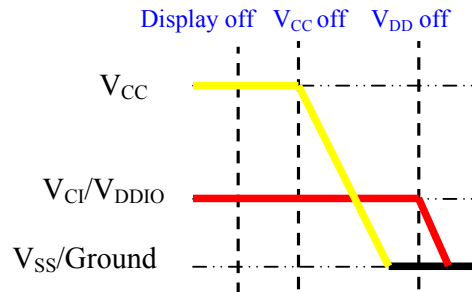
5.2.1 POWER UP SEQUENCE

1. Power up V_{CI} & V_{DDIO}
2. Send Display off command
3. Initialization 4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
(When V_{CC} is stable)
7. Send Display on command



5.2.2 POWER DOWN SEQUENCE

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
(When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{CI} & V_{DDIO}



5.3 RESET CIRCUIT

When RES# input is low, the chip is initialized with the following status:

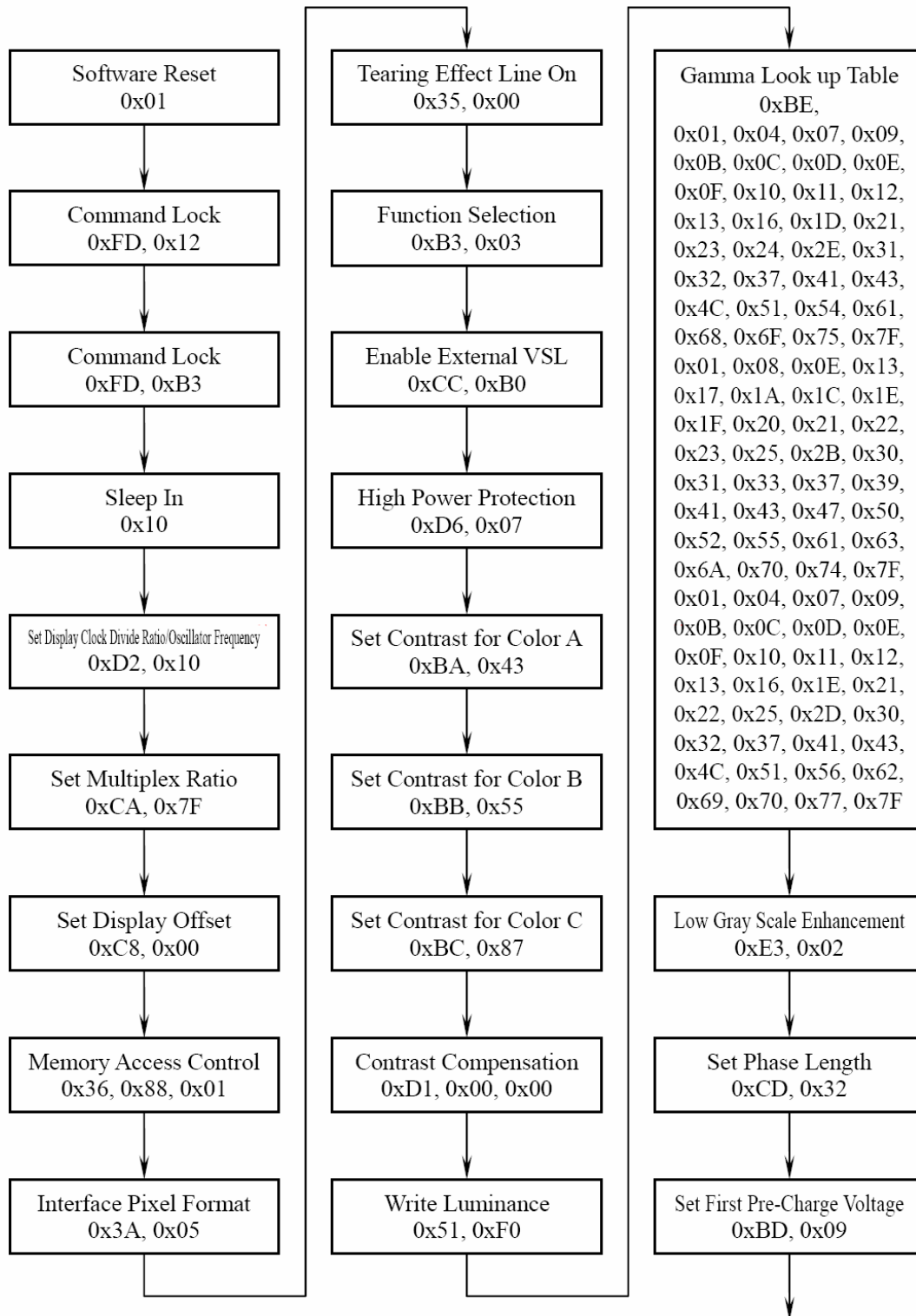
1. Display is off
2. 128(RGB)x160 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Individual contrast control registers of colour A, B, C are set at 80h

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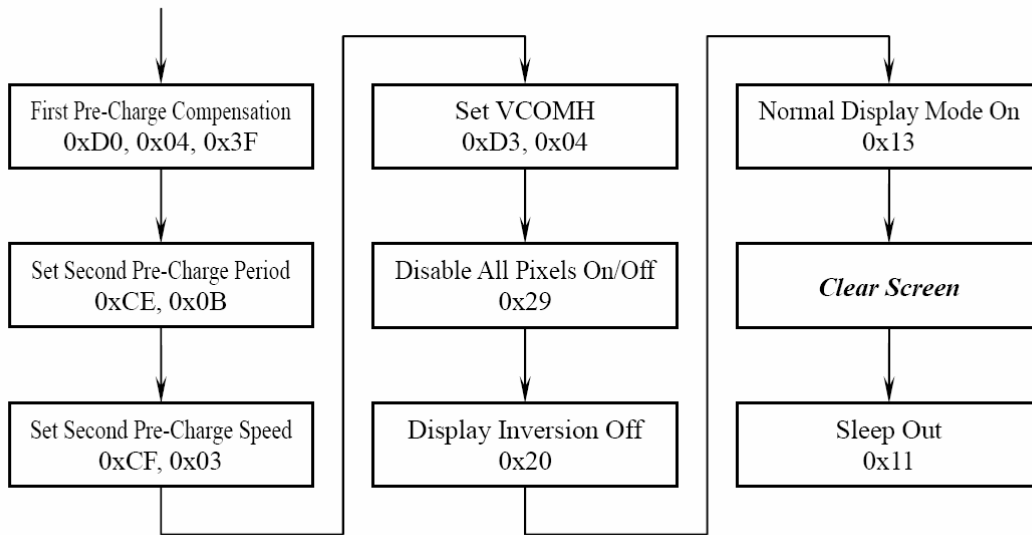
5.4 ACTUAL APPLICATION EXAMPLE

Command usage and explanation of an actual example



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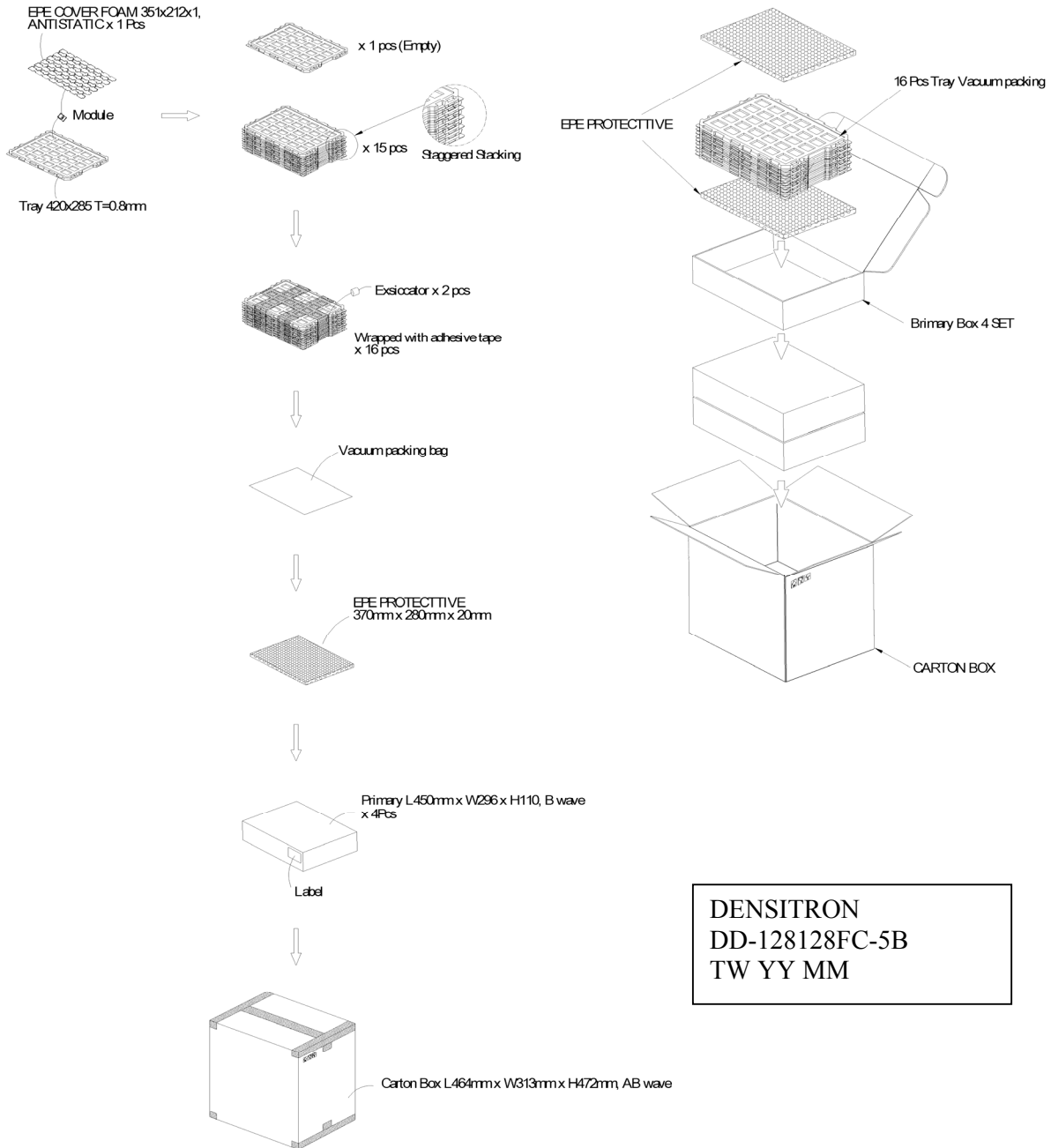
If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

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6 PACKAGING AND LABELLING SPECIFICATION

6.1 LABELLING & MARKING



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7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

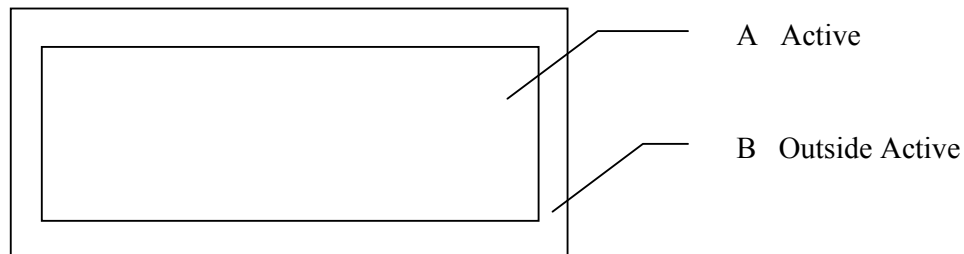
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assemblies standard

7.2.2 Zone definition



7.2.3 Visual inspection

Test and measurement to be conducted under following conditions

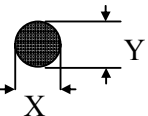
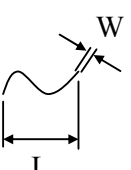
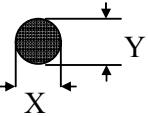
Temperature:	23±5°C
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≥30cm
Distance between the Panel & the lamp:	≥50cm

7.2.4 Standard of appearance inspection

Units: mm

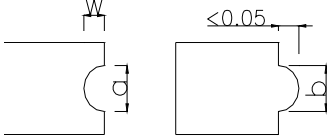
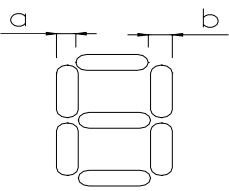
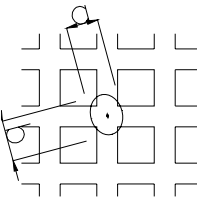
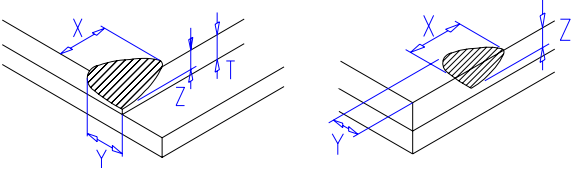
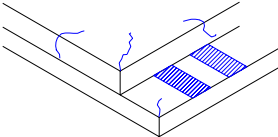
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Class	Item	Criteria																																		
Minor	Packing & Label	Outside & inside package Presence of product no., lot no., quantity																																		
Critical		Product must not be mixed with others and quantity must not be different from that indicated on the label																																		
Major	Dimension	Product dimensions must be according to specification and drawing																																		
Major	Electrical	Product electrical characteristics must be according to specification																																		
Critical	OLED Display	Missing lines, short circuits or wrong patterns on OLED display are not allowed																																		
Minor	Black spot, white spot, dust	<p>Round type: as per following drawing $\varnothing = (X+Y)/2$</p>  <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="3">Acceptable quantity</th> </tr> <tr> <th>Size</th> <th>Zone A</th> <th>Zone B</th> </tr> </thead> <tbody> <tr> <td>$\varnothing < 0.1$</td> <td>Any number</td> <td rowspan="3">Any number</td> </tr> <tr> <td>$0.1 < \varnothing < 0.2$</td> <td>3</td> </tr> <tr> <td>$0.2 < \varnothing < 0.25$</td> <td>1</td> </tr> <tr> <td>$0.25 < \varnothing$</td> <td>0</td> <td></td> </tr> </tbody> </table> <p>Line type: as per following drawing</p>  <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="4">Acceptable quantity</th> </tr> <tr> <th>Length</th> <th>Width</th> <th>Zone A</th> <th>Zone B</th> </tr> </thead> <tbody> <tr> <td>--</td> <td>$W \leq 0.05$</td> <td>Any number</td> <td rowspan="3">Any number</td> </tr> <tr> <td>$L \leq 2.0$</td> <td>$W \leq 0.1$</td> <td>3</td> </tr> <tr> <td>$L > 2.0$</td> <td></td> <td>0</td> </tr> </tbody> </table> <p style="text-align: center;">Total acceptable quantity: 3</p>	Acceptable quantity			Size	Zone A	Zone B	$\varnothing < 0.1$	Any number	Any number	$0.1 < \varnothing < 0.2$	3	$0.2 < \varnothing < 0.25$	1	$0.25 < \varnothing$	0		Acceptable quantity				Length	Width	Zone A	Zone B	--	$W \leq 0.05$	Any number	Any number	$L \leq 2.0$	$W \leq 0.1$	3	$L > 2.0$		0
Acceptable quantity																																				
Size	Zone A	Zone B																																		
$\varnothing < 0.1$	Any number	Any number																																		
$0.1 < \varnothing < 0.2$	3																																			
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--	$W \leq 0.05$	Any number	Any number																																	
$L \leq 2.0$	$W \leq 0.1$	3																																		
$L > 2.0$		0																																		
Minor	Polariser scratch	Scratch on protective film is permitted Scratch on polariser: same as No. 1																																		
Minor	Polariser bubble	<p>$\varnothing = (X+Y)/2$</p>  <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="3">Acceptable quantity</th> </tr> <tr> <th>Size</th> <th>Zone A</th> <th>Zone B</th> </tr> </thead> <tbody> <tr> <td>$\varnothing < 0.5$</td> <td>Any number</td> <td rowspan="2">Any number</td> </tr> <tr> <td>$\varnothing > 0.5$</td> <td>0</td> </tr> </tbody> </table>	Acceptable quantity			Size	Zone A	Zone B	$\varnothing < 0.5$	Any number	Any number	$\varnothing > 0.5$	0																							
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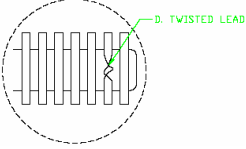
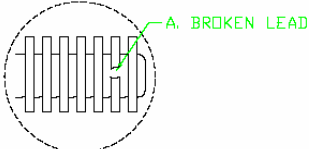
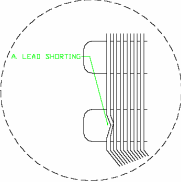
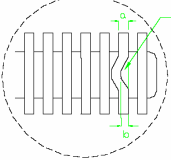
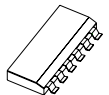
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Class	Item	Criteria																												
Minor	Segment deformation	<p>1b. Pin hole on dot matrix display</p>  <table border="1" data-bbox="1006 357 1380 525"> <thead> <tr> <th colspan="2">Acceptable quantity</th> </tr> <tr> <th>Size</th> <th></th> </tr> </thead> <tbody> <tr> <td>a,b<0.1</td> <td>Any number</td> </tr> <tr> <td>(a+b)/2≤0.1</td> <td>Any number</td> </tr> <tr> <td>0.5<Ø<1.0</td> <td>3</td> </tr> </tbody> </table> <p>Total acceptable quantity: 7</p> <p>2. Segments / dots with different width</p>  <table border="1" data-bbox="1006 714 1380 819"> <thead> <tr> <th colspan="2">Acceptable</th> </tr> </thead> <tbody> <tr> <td>a≥b</td> <td>a/b≤4/3</td> </tr> <tr> <td>a<b</td> <td>a/b>4/3</td> </tr> </tbody> </table> <p>3. Alignment layer defect</p> <p>Ø = (a+b)/2</p>  <table border="1" data-bbox="1006 882 1380 1092"> <thead> <tr> <th colspan="2">Acceptable quantity</th> </tr> <tr> <th>Size</th> <th></th> </tr> </thead> <tbody> <tr> <td>Ø≤0.4</td> <td>Any number</td> </tr> <tr> <td>0.4<Ø≤1.0</td> <td>5</td> </tr> <tr> <td>1.0<Ø≤1.5</td> <td>3</td> </tr> <tr> <td>1.5<Ø≤2.0</td> <td>2</td> </tr> </tbody> </table> <p>Total acceptable quantity: 7</p>	Acceptable quantity		Size		a,b<0.1	Any number	(a+b)/2≤0.1	Any number	0.5<Ø<1.0	3	Acceptable		a≥b	a/b≤4/3	a<b	a/b>4/3	Acceptable quantity		Size		Ø≤0.4	Any number	0.4<Ø≤1.0	5	1.0<Ø≤1.5	3	1.5<Ø≤2.0	2
Acceptable quantity																														
Size																														
a,b<0.1	Any number																													
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1.0<Ø≤1.5	3																													
1.5<Ø≤2.0	2																													
Minor	Panel Chipping	<p>$X \leq 1/6$ Panel length $Y \leq 1$ $Z \leq T$</p> 																												
Minor	Panel Cracking	<p>Cracks not allowed</p> 																												
Minor	Copper exposed (pin or film)	Not allowed if visible by eye inspection																												
Minor	Film or Trace Damage	Not allowed if affect electrical function																												

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Class	Item	Criteria			
Minor	Contact Lead Twist	Not allowed	 <p>D. TWISTED LEAD</p>		
Minor	Contact Lead Broken	Not allowed	 <p>A. BROKEN LEAD</p>		
Minor	Contact Lead Bent	Not allowed if bent lead causes short circuit	 <p>A. LEAD SHORTING</p>		
		Not allowed if bent lead extends horizontally more than 50% of its width	 <p>a b</p>		
Minor	Colour uniformity	Level of sample for approval set as limit sample			
Major		No unmelted solder paste should be present on PCB			
Critical		Cold solder joints, missing solder connections, or oxidation are not allowed			
Minor		No residue or solder balls on PCB are allowed			
Critical		Short circuits on components are not allowed			
Minor	Tray particles			Size	Quantity
			On tray	$\varnothing < 0.2$	Any number
				$\varnothing > 0.25$	4
			On display	$\varnothing \geq 0.25$	2
L = 3	1				

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7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample. After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.

If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

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8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70°C±2, 240 hours	No abnormalities in function and appearance
Low Temperature Operation	-30°C±2, 240 hours	No abnormalities in function and appearance
High Temperature Storage	80°C±2, 240 hours	No abnormalities in function and appearance
Low Temperature Storage	-40°C±2, 240 hours	No abnormalities in function and appearance
High Temperature & High Humidity Storage(Operation)	60°C±2, 90%RH, 120 hours	No abnormalities in function and appearance
Thermal Shock	24 cycle of -40°C 1 Hour, R.T. 5 min, 85°C 1 Hour	No abnormalities in function and appearance

- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5 °C □ 55±15% RH

8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration more than 10,000 hours under ordinary operating conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.

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9 HANDLING PRECAUTIONS

Safety

If the panel breaks, be careful not to get the organic substance in your mouth or in your eyes.
If the organic substance touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design

Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.

Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during OLED cleaning

Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotrifluoroethane.

Do not wipe the display surface with dry or hard materials that will damage the polariser surface.

Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge

As the display uses C-MOS LSI drivers, connect any unused input terminal to V_{DD} or V_{SS} . Do not input any signals before power is turned on.

Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging

Displays use OLED elements, and must be treated as such. Avoid strong shock and drop from a height.

To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation

It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.

Other Precautions

When a display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.

Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored.

Also, there will be no problem in the reliability of the module.

Storage

Store the display in a dark place where the temperature is $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ and the humidity below 50%RH.

Store the display in a clean environment, free from dust, organic solvents and corrosive gases.

Do not crash, shake or jolt the display (including accessories).

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