



650 V 42 mΩ SiC MOSFET

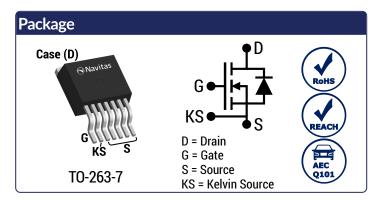
Silicon Carbide MOSFET

Trench-Assisted Planar Technology

 V_{DS} = 650 V $R_{DS(ON)}(Typ.)$ = 42 m Ω $I_{D}(T_{C} = 100^{\circ}C)$ = 39 A

Features

- Gen3F (3rd Generation) Technology
- Most Stable R_{DS(ON)} over Temperature
- Low Coss, Crss and Balanced Ciss/Crss
- Lower Q_{GD} and Balanced R_{G(INT)}
- Electromagnetically Optimized Design
- Robust Body Diode with Low V_F and Low Q_{RR}
- 100% Avalanche (UIL) Tested
- AEC-Q101 Qualified



Advantages

- Superior Performance and Robustness
- Lowest Conduction Losses at all Temperatures
- Lesser Switching Spikes and Lower Losses
- Faster and More Efficient Switching
- Reduced Ringing
- Ease of Paralleling without Thermal Runaway
- Excellent Power Density and System Efficiency
- Enhanced System Reliability

Applications

- xEV OBC & DC-DC
- EV Fast Charging Infrastructure
- Solar / PV
- Energy Storage System
- Server & Telecom Power Supply
- Uninterruptible Power Supply
- Motor Control
- Class D Amplifiers

Absolute Maximum Ratings (At T _C = 25°C Unless Otherwise Stated)						
Parameter	Symbol	Conditions	Values	Unit	Note	
Drain-Source Voltage	$V_{DS(max)}$	V_{GS} = 0 V, I_D = 100 μA	650	V		
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +22	V		
Gate-Source Voltage (Static)	$V_{GS(op)-ON}$	Recommended Operation	15 to 18	V	Note 1	
	$V_{GS(op)\text{-}OFF}$	necommended operation	-5 to -3	V	Note i	
		$T_C = 25^{\circ}C$, $V_{GS} = -5 / +18 V$	56			
Continuous Drain Current	I _D	$T_C = 100$ °C, $V_{GS} = -5 / +18 V$	39	Α	Fig. 16	
		$T_C = 135^{\circ}C$, $V_{GS} = -5 / +18 V$	29			
Pulsed Drain Current	I _{D(pulse)}	$t_P \le 3\mu s$, $D \le 1\%$, $V_{GS} = 18~V$	100	Α	Note 2	
Power Dissipation	P_D	$T_c = 25^{\circ}C$	187	W	Fig. 17	
Non-Repetitive Avalanche Energy	E _{AS}	$L = 36 \text{ mH}, I_{AV} = 3 \text{ A}$	162	mJ		
Operating Junction and Storage Temperature	T_j , T_{stg}		-55 to 175	°C		

Note 1: This product can support 0V turn-off gate drive voltage with optimized PCB layout and gate drive circuit configuration.

Note 2: Pulse Width t_P Limited by T_{j(max)}



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Electrical Characteristics (At T _C = 25°C Unless Otherwise Stated)							
Parameter	Symbol	Conditions	Values Min. Typ. Max.		Max.	Unit	Note
Drain-Source Breakdown Voltage	V _{DSS}	V _{GS} = 0 V, I _D = 100 μA 650		٧			
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V	1 50		μA		
		V _{DS} = 0 V, V _{GS} = 22 V			100	·	
Gate Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V, } V_{GS} = -10 \text{ V}$			-100	nA	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 8 \text{ mA}$	2.2	2.8	4.3	٧	Note 3
Transconductance	~	$V_{DS} = 10 \text{ V, } I_D = 20 \text{ A}$		10.8		0	F: F
Transconductance	G fs	V_{DS} = 10 V, I_D = 20 A, T_j = 175°C	10.5			S	Fig. 5
		$V_{GS} = 18 \text{ V, } I_D = 20 \text{ A}$	42 54 60				Fig. 5-9
Drain-Source On-State Resistance	R _{DS(ON)}	V_{GS} = 18 V, I_D = 20 A, T_j = 175°C				mΩ	
Diani-Source off-State nesistance	HDS(UN)	$V_{GS} = 15 \text{ V, } I_D = 20 \text{ A}$		55			
		$V_{GS} = 15 \text{ V}, I_D = 20 \text{ A}, T_j = 175^{\circ}\text{C}$		68			
Input Capacitance	Ciss			1640			
Output Capacitance	Coss			112		pF	Fig. 12
Reverse Transfer Capacitance	C _{rss}						
Coss Stored Energy	E _{oss}			10		μJ	Fig. 13
Coss Stored Charge	Q_{oss}			71		nC	
Effective Output Capacitance (Energy Related)	C _{o(er)}			125		F	Note 4
Effective Output Capacitance (Time Related)	C _{o(tr)}			178		- pF	Note 4
Gate-Source Charge	Q_{gs}	$V_{DS} = 400 \text{ V}, V_{GS} = -5 / +18 \text{ V}$		13		_	
Gate-Drain Charge	Q_{gd}	I _D = 20 A		16		nC	Fig. 11
Total Gate Charge	Q_g	Per JEDEC JEP-192		55			
Internal Gate Resistance	R _{G(int)}	$V_{GS} = 18 \text{ V, } f = 1 \text{ MHz, } V_{AC} = 25 \text{ mV}$	1.3		Ω		
Turn-On Switching Energy (Body Diode)	E _{On}	T_j = 25°C, V_{GS} = -5/+18V, $R_{G(ext)}$ = 6.8 Ω, L		67		1	Fig. 24-27
Turn-Off Switching Energy (Body Diode)	E _{Off}	= $80.0 \mu H$, $I_D = 20 A$, $V_{DD} = 400 V$	$20 \text{ A, V}_{DD} = 400 \text{ V}$ 34			— μJ	1 lg. 27 21
Turn-On Delay Time	t _{d(on)}			21			
Rise Time	t _r	$V_{DD} = 400 \text{ V}, V_{GS} = -5/+18 \text{ V}$	9			Fig. Oc	
Turn-Off Delay Time	t _{d(off)}	$R_{G(ext)}$ = 6.8 Ω, L = 80.0 µH, I_D = 20 A I_D Timing relative to I_D S, Inductive load I_D		16		ns	Fig. 26
Fall Time	t _f	- Taring relative to VDS, inductive load -		8			

Note 3: Tested after applying 30ms pulse at Vgs= +25V

Note 4: $C_{O(er)}$, a lumped capacitance that gives same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400V. $C_{O(tr)}$, a lumped capacitance that gives same charging times as C_{OSS} while V_{DS} is rising from 0 to 400V.

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Reverse Diode Characteristics							
Parameter	Symbol	Conditions		Values			Note
	Syllibol		Min.	Тур.	Max.	Unit	Note
Diode Forward Voltage	V_{SD}	$V_{GS} = -5 \text{ V, } I_{SD} = 10 \text{ A}$	4.4			٧	Fig. 18-19
	VSD	V_{GS} = -5 V, I_{SD} = 10 A, T_j = 175°C		3.9		V	riy. 10-19
Continuous Diode Forward Current	l _a	V_{GS} = -5 V, T_c = 25°C			30	Α	
	Is	$V_{GS} = -5 \text{ V, } T_c = 100^{\circ}\text{C}$			18	A	
Diode Pulse Current	I _{S(pulse)}	$V_{GS} = -5 V$		72		Α	Note 2
Reverse Recovery Time	t _{rr}	V 5VI 00 4 V 400 V		8		ns	
Reverse Recovery Charge	Qrr	$V_{GS} = -5 \text{ V, } I_{SD} = 20 \text{ A, } V_{R} = 400 \text{ V}$ $dif/dt = 4800 \text{ A/}\mu\text{s, } T_{i} = 25^{\circ}\text{C}$		83		nC	
Peak Reverse Recovery Current	I _{rrm}	uii/ut - 4000 A/μs, 1] - 25 C		17		Α	
Reverse Recovery Time	t _{rr}	V 5VI 00 1 V 100 V		9.5		ns	
Reverse Recovery Charge	Q _{rr}	$V_{GS} = -5 \text{ V, } I_{SD} = 20 \text{ A, } V_{R} = 400 \text{ V}$ $dif/dt = 4800 \text{ A/}\mu\text{s, } T_{i} = 175^{\circ}\text{C}$		158		nC	
Peak Reverse Recovery Current	I _{rrm}	uii/ut - 4000 Α/μs, 1 _j - 175 C		24		Α	

Package Characteristics					
Parameter	Symbol	Conditions	Values	Unit	Note
Max Thermal Resistance, Junction - Case	R _{th} JC-Max	Maximum	0.8	°C/W	Fig. 14
Weight	\mathbf{W}_{T}		1.45	g	
Moisture Sensitivity Level	MSL		1		
EMC Material Group			II		

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Fig 1: Typical Output Characteristics ($T_j = 25$ °C)

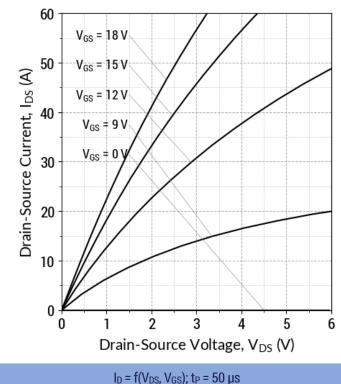
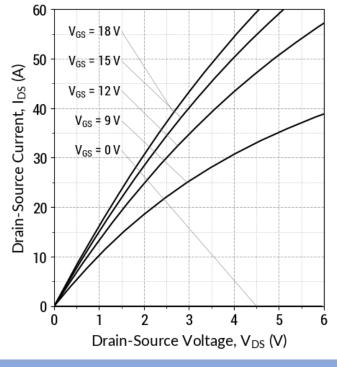
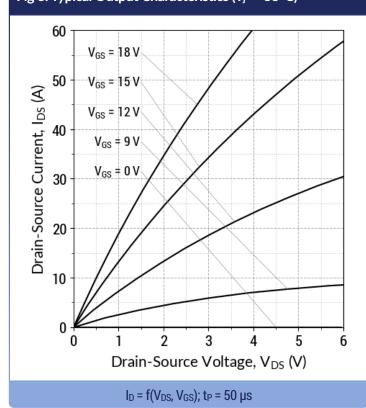


Fig 2: Typical Output Characteristics ($T_j = 175$ °C)



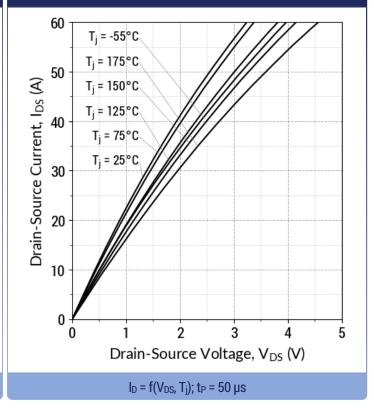
 $I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu s$

Fig 3: Typical Output Characteristics (T_j = -55°C)



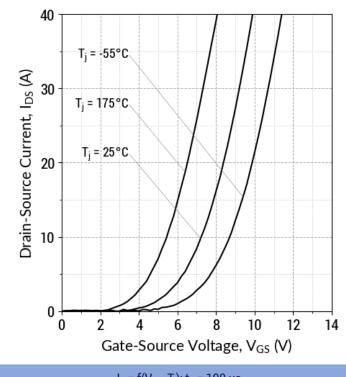
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Fig 4: Typical Output Characteristics (V_{GS} = 18 V)



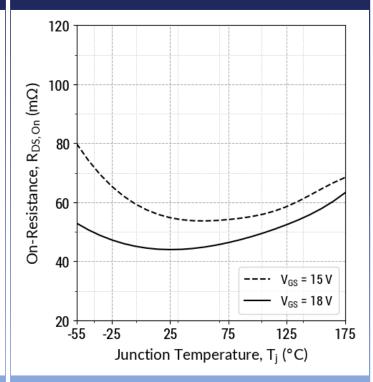
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Fig 5: Typical Transfer Characteristics (V_{DS} = 10 V)



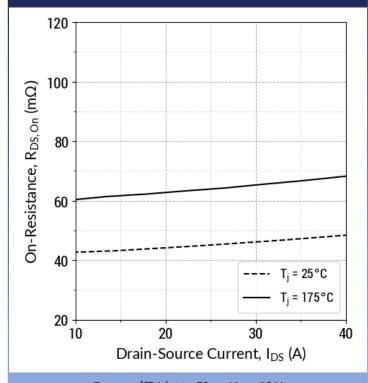
 $I_D = f(V_{GS}, T_j); t_P = 100 \mu s$

Fig 6: Typical R_{DS(ON)} v/s Temperature



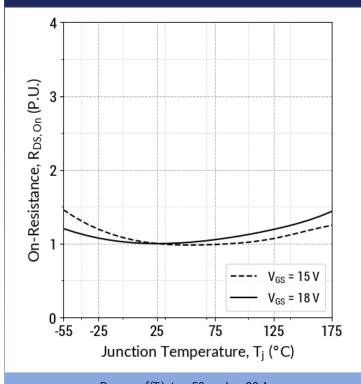
 $R_{DS(ON)} = f(T_j, V_{GS}); t_P = 50 \mu s; I_D = 20 A$

Fig 7: Typical RDS(ON) v/s Drain Current



 $R_{DS(ON)} = f(T_j,I_D)$; $t_P = 50 \mu s$; $V_{GS} = 18 \text{ V}$

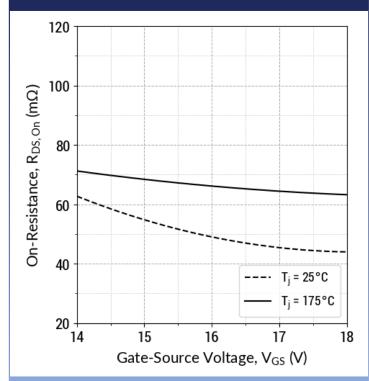
Fig 8: Typical Normalized RDS(ON) v/s Temperature



 $R_{DS(ON)} = f(T_j); t_P = 50 \mu s; I_D = 20 A$

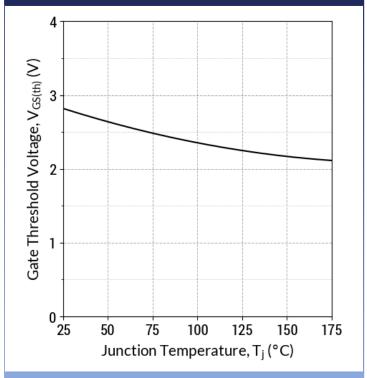
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 $R_{DS(ON)} = f(T_i, V_{GS}); t_P = 50 \mu s; I_D = 20 A$

Fig 10: Typical Threshold Voltage Characteristics



 $V_{GS(th)} = f(T_j)$; $V_{DS} = V_{GS}$; $I_D = 8 \text{ mA}$

Fig 11: Typical Gate Charge Characteristics

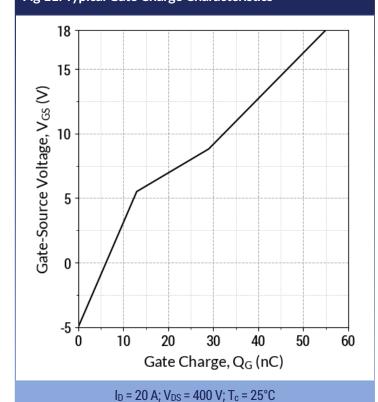
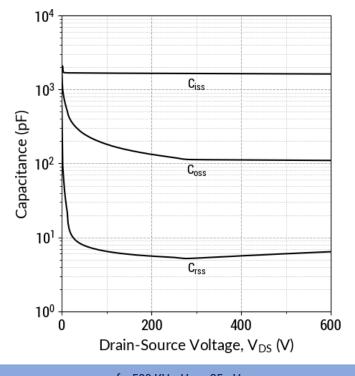


Fig 12: Typical Capacitance v/s Drain-Source Voltage



f = 500 KHz; $V_{AC} = 25 \text{mV}$

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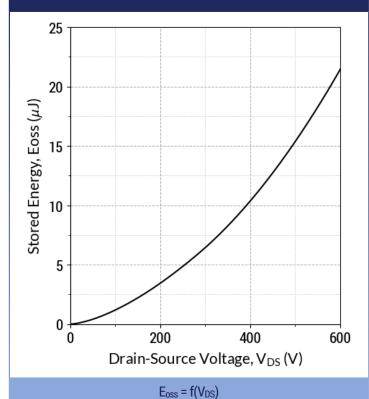
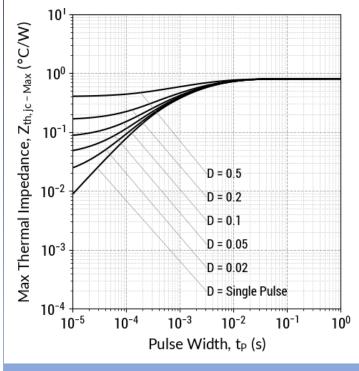


Fig 14: Max. Transient Thermal Impedance



 $Z_{th,ic} = f(t_P,D); D = t_P/T$

Fig 15: Safe Operating Area ($T_c = 25^{\circ}C$)

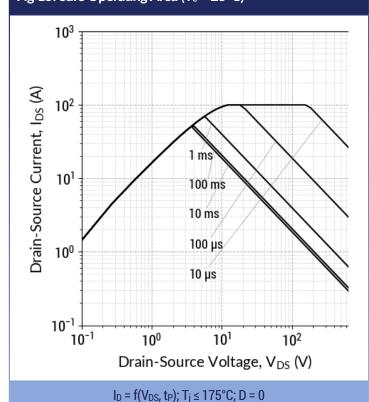
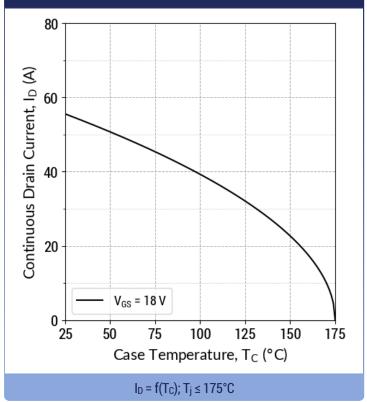
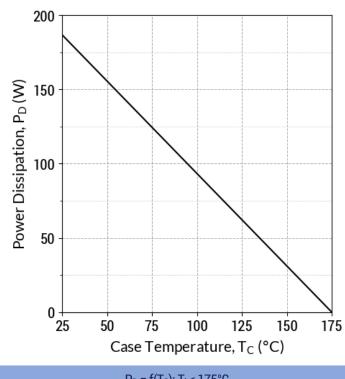


Fig 16: Current De-rating Curve



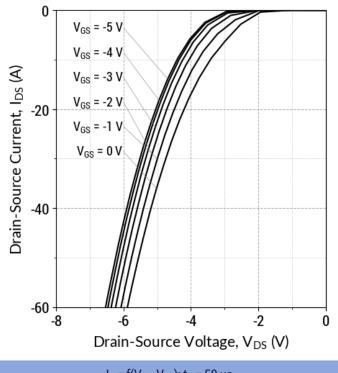
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 $P_D = f(T_C); T_j \le 175^{\circ}C$

Fig 18: Typical Body Diode Characteristics ($T_j = 25$ °C)



 $I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu s$

Fig 19: Typical Body Diode Characteristics ($T_j = 175$ °C)

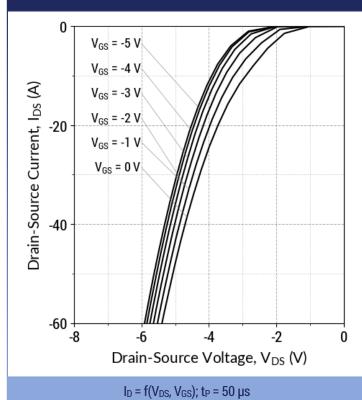
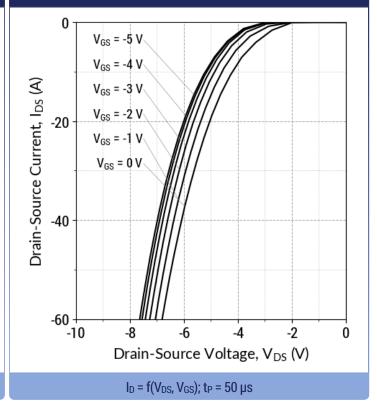


Fig 20: Typical Body Diode Characteristics ($T_j = -55$ °C)



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Fig 21: Typical Third Quadrant Characteristics ($T_j = 25$ °C)

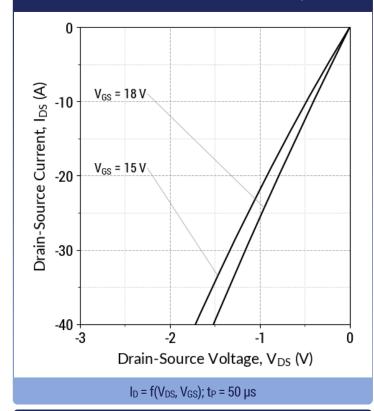


Fig 22: Typical Third Quadrant Characteristics (T_j = 175°C)

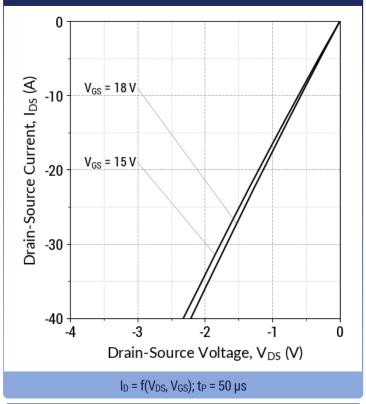


Fig 23: Typical Third Quadrant Characteristics ($T_j = -55$ °C)

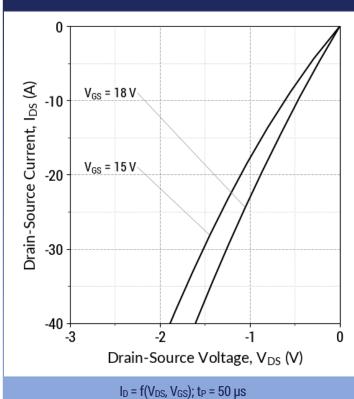
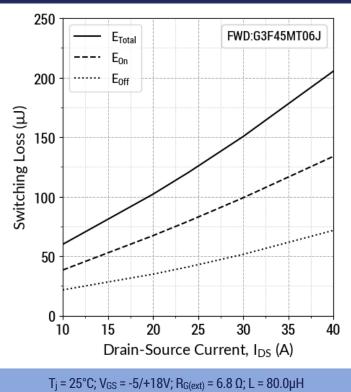
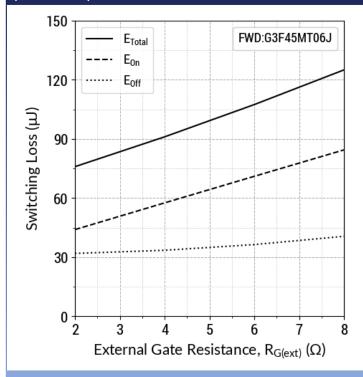


Fig 24: Inductive Switching Energy v/s Drain Current $(V_{DD} = 400V)$



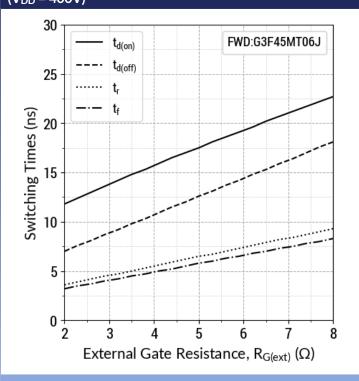
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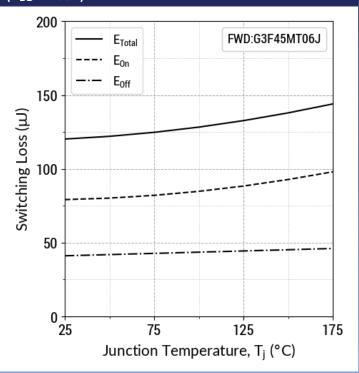
 $T_i = 25$ °C; $V_{GS} = -5/+18V$; $I_{DS} = 20$ A; $L = 80.0 \mu H$

Fig 26: Switching Time v/s $R_{G(ext)}$ ($V_{DD} = 400V$)



 $T_i = 25$ °C; $V_{GS} = -5/+18V$; $I_{DS} = 20$ A; $L = 80.0 \mu H$

Fig 27: Inductive Switching Energy v/s Temperature $(V_{DD} = 400V)$

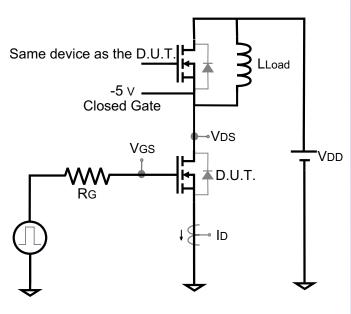


 $T_i = 25^{\circ}C$; $V_{GS} = -5/+18V$; $R_{G(ext)} = 6.8 \Omega$; $I_{DS} = 20 A$; $L = 80.0 \mu H$

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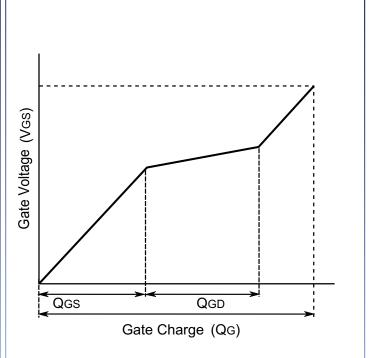


Dynamic Test Circuit

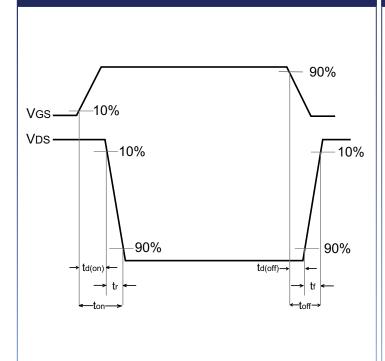


Note: Gate Charge, Switching Time and Energy Circuit

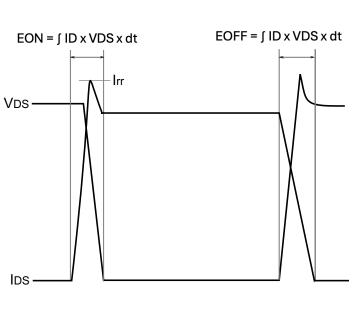
Gate Charge Waveform



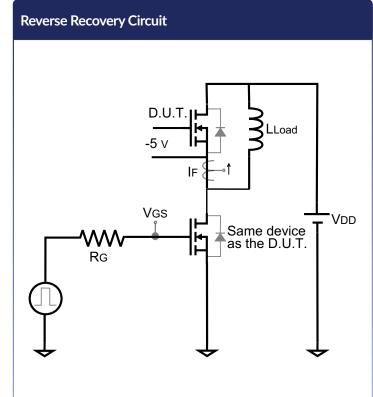
Switching Time Waveform

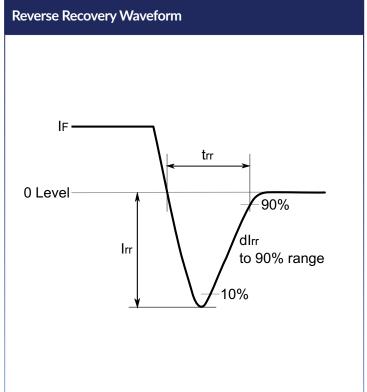


Switching Energy Waveform



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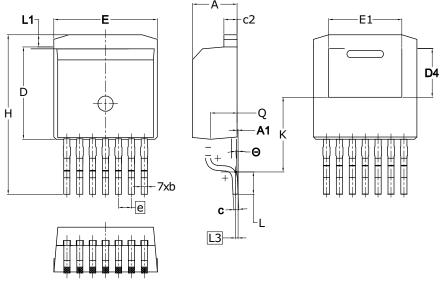
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Package Dimensions

TO-263-7 Package Outline



- All Dimensions Are In mm.
 Dimension D & E Do Not Include Mold Flash.
 These Dimensions Are Measured At The Outermost
- Extreme Of The Plastic Body.

 3. Thermal Pad Contour Optional Within Dimensions E, L1, D4 & E1.

 4. Dimension D4 & E1 Establish A Minmum Mounting Surface for
- The Thermal Pad.

 5. is Exposed Cu.
- 6. There is Exposed Cu and Molding Flash Bleeding At The Pin Which is Close To Package.

	DIMENSIONS				
SYMBOL		11210112			
	MIN.	MAX.			
Α	4.30	4.50			
A1	0.00	0.25			
b	0.50 0.				
С	0.45 0.6				
c2	1.20 1.4				
D	8.93 9				
D4	4.65 4.				
E	10.08 10				
E1	6.82 7.6				
е	1.27 BSC				
Н	15.00 16.0				
К	7.30				
L	1.90 2.5				
L1	1.00 1.40				
L3	0.25 BSC				
Q	2.45 2.75				
Θ	0° 7°				

NOTE

- 1. CONTROLLED DIMENSION IS MILLIMETER.
- 2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.
- 3. THE SOURCE AND KELVIN-SOURCE PINS ARE NOT INTERCHANGABLE. THEIR EXCHANGE MIGHT LEAD TO MALFUNCTION.

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Revision History

Rev 24/Aug: Initial Release (Rev 1.0)

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