Hardware design guidelines for 1EDL8011 high-side driver using EVAL_1EDL8011 Drive Evaluation Board

About this document

Scope and purpose

This document describes the functionality of the 1EDL8011 high-side driver with the EVAL_1EDL8011 Drive Evaluation Board where N-channel MOSFETs are used on the high side to connect or disconnect the power supply. The applications include power tools, robotics, e-bikes, and vacuum cleaners.

EVAL_1EDL8011 Drive Evaluation Board demonstrates how 1EDL8011 operates in undervoltage lockout (UVLO), overcurrent, and soft startup conditions. The four high-side N-channel MOSFETs are connected in parallel to provide the load current.

Intended audience

This document is intended for design engineers and application engineers of power tools, gardening tools, robotics, e-bikes, vacuum cleaners, drones, and multicopters, who aim to provide a cost-effective system solution.

Infineon components featured

- OptiMOS™ 5 IPT039N15N5 150 V 3.9 mΩ 10 mm × 12 mm
- 1EDL8011 high-side MOSFET gate driver (5 mm × 6 mm)

Table of contents

1 Introduction

1.1 High-side gate driver

In power applications, the supply architecture requires a switch to disconnect the main supply rail at the high side when a malfunction occurs. To achieve that functionality, it is common to use a single N-channel MOSFET or back-to-back N-channel FETs in common source configuration. These disconnect switches require a high-side driver and the 1EDL8011 high-side gate driver can be used in these applications to provide:

- Programmable overcurrent protection (OCP) against a short-circuit condition at the load.
- Soft startup to limit the inrush current.
- Shutdown protection when the supply is lower than the UVLO.

1.2 EVAL_1EDL8011 Drive Evaluation Board

This section describes the functions of 1EDL8011 using the EVAL_1EDL8011 Drive Evaluation Board as shown in Figure 1, designed for a power supply from 10 V to 84 V. This board utilizes OptiMOS™ 5 IPT039N15N5 150 V 3.9 mΩ power MOSFETs in TO-Leadless packages (TOLL, 10 mm x 12 mm). Four MOSFETs are placed in parallel to get 50 A of load current. This board can be used to evaluate the 1EDL8011 drive capabilities with different functions of the current limit and various timings, soft startup, and undervoltage lockout. Figure 2 shows the system block diagram of the EVAL_1EDL8011 board.

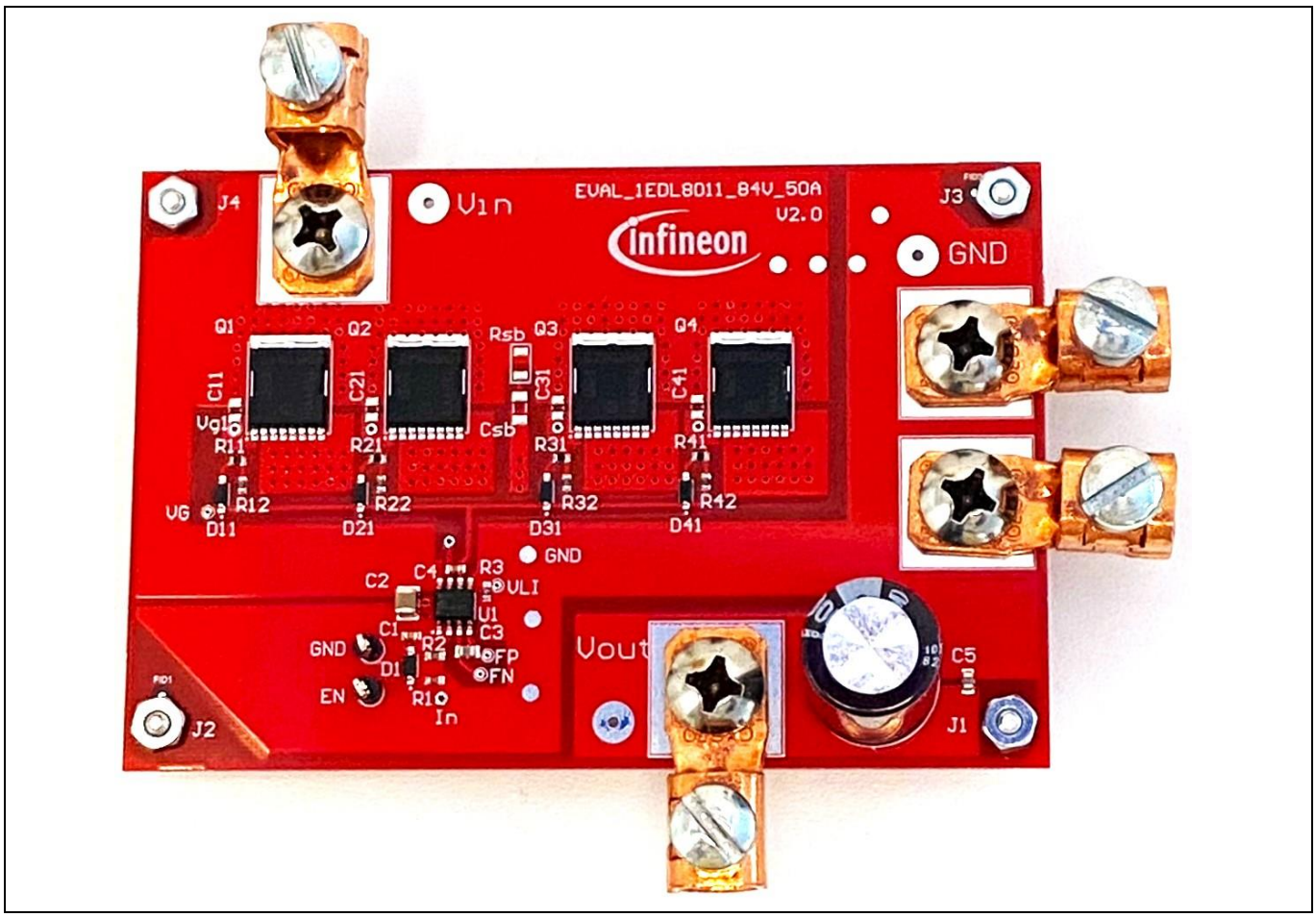

Figure 1 EVAL_1EDL8011 Drive Evaluation Board

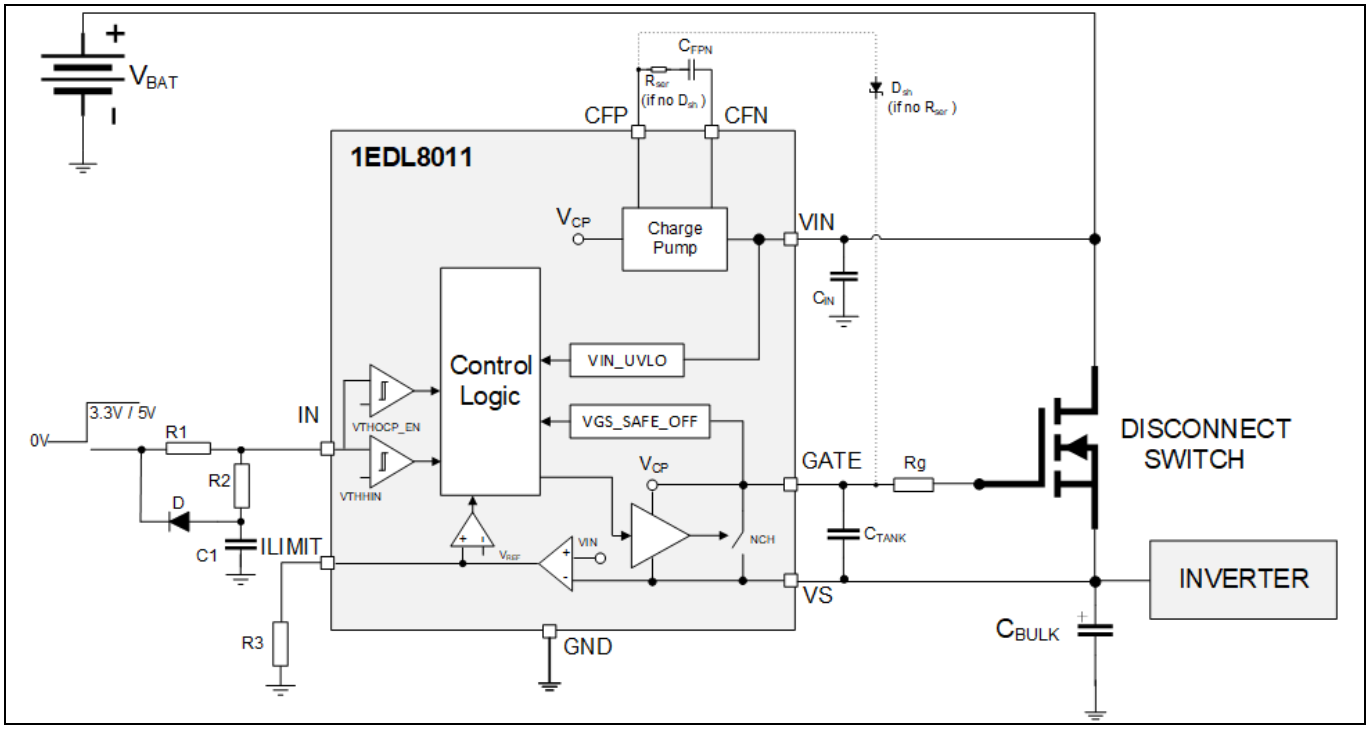

Figure 2 Block diagram

1.3 1EDL8011 startup

Ensure that the following conditions are met to start up the device:

- The IN pin voltage (V_IN) must be higher than $VTHH_{IN}$ (1.15 V minimum) and the input voltage (VIN) must be higher than $V_{VIN\_UVLO\_R}$ (10 V typical). When an RC network is used at the IN pin and the IN pin voltage (V_IN) is higher than $V_{initial}$ (1.4 V typical), the charge pump voltage rises and the MOSFETs will turn on.
- When an RRC network is used at the IN pin, the slew rate of V_IN voltage must be higher than 0.35 V/µs. The high-frequency charge pump (400 kHz) stops when the V_{GS} voltage is higher than 12 V. After that, the gate voltage is supplied from the auxiliary charge pump.
- Another critical parameter during the startup is the blanking time. It is also determined by the external components (R1, R2, and C1) as shown in Figure 2. During the blanking time, the OCP is not triggered. The blanking time is the sum of the blanking time 1 and blanking time 2.

Calculate blanking time 1 as follows:

$$T_{BLANK1} = -\tau\left(1+\frac{a*b}{a+b}\right)*\ln\left[\left(1-\frac{V_{LOOP}}{V\_IN}*\left(1+\frac{a}{b}\right)\right)*\left(1+\frac{1}{a}+\frac{1}{b}\right)\right]$$

Equation 1

Where:

a = R_1/R_2 (10 kΩ /10 kΩ)

b = R_{PD}/R_2 (11 MΩ /10 kΩ)

R_{PD} = IN pin pull-down resistor as shown in Figure 3

τ = $R_2 \times C_1$ (10 kΩ × 100 nF)

V_{LOOP} = 2.6 V

V_{REF} = 1.2 V

V_IN = Voltage to drive at the IN pin (3.3 V in this example)

C_{int} = 1 nF

T_{BLANK1} = 1.72 ms

Calculate blanking time 2 as follows:

$$T_{BLANK2} = \frac{V_{REF}}{V_{LOOP} - V_{CBLANK1}} * R_2 * \sqrt{2 * C_1 * C_{int} * k}$$

Equation 2

and

$$V_{CBLANK1} = V\_IN * \frac{b}{a+b} * [1 - e^{-\frac{T_{BLANK1}}{\tau * \left(1+\frac{a*b}{a+b}\right)}}]$$

Equation 3

$$k = 1.1 + \frac{1\ nF}{1.4 * C_1}$$

Equation 4

Where V_{REF} is 1.2 V and C_{INT} is a 1 nF internal capacitance shown in Figure 3. Blanking times 1 and 2 can be calculated as 1.72 and 0.19 ms, respectively, to provide a total blanking time of 1.91 ms in this example.

1.4 1EDL8011 turn-off

The gate of the MOSFETs will turn off if one of the following conditions occurs:

- The IN pin voltage (V_IN) is less than $VTHL_{IN}$ (1 V maximum)
- The input voltage is less than $V_{VIN\_UVLO\_F}$ (7.5 V typical)
- OCP is triggered

The current limit (I_{LIMIT}) can be calculated by substituting the following terms in equation 5:

- $R_{DS(on)}$ of the MOSFETs
- External R3 as shown in Figure 3
- Number of the MOSFETs in parallel (N)
- Temperature coefficient (k1)

$$I_{LIMIT} = \frac{V_{REF} * N * R_4}{R_{dson} * k1 * R_3}$$

Equation 5

Where V_{REF} is 1.2 V and the internal resistor R4 is 10 kΩ. The product variation of V_{REF} and R4 is less than 25% when the MOSFETs V_{DS} voltage is higher than 100 mV. In this example, when R3 is 182 kΩ, N is 4, k1 is 1.09, and $R_{DS(on)}$ is 3.9 mΩ, I_{LIMIT} can be calculated as 62 A.

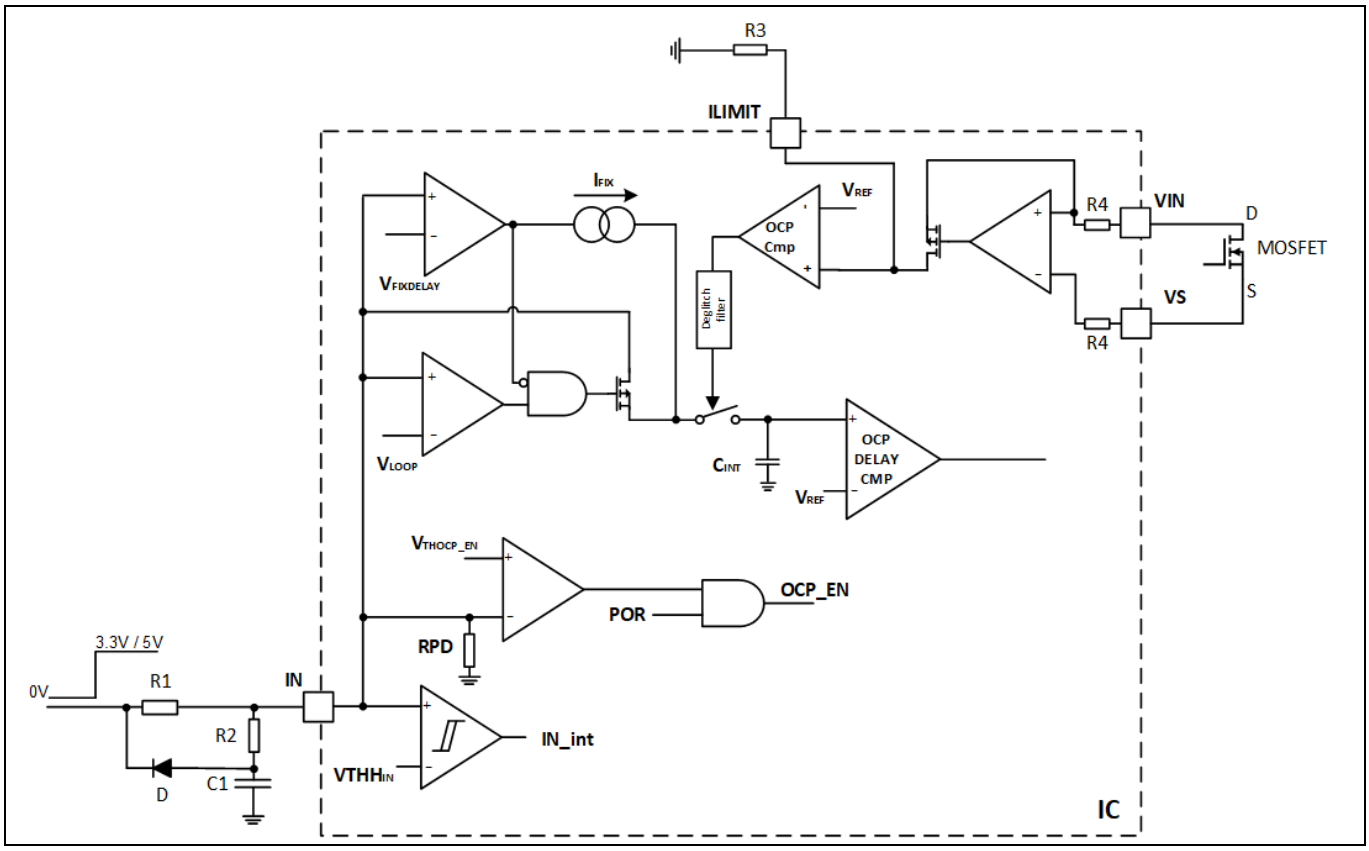

Figure 3 OCP setup

OCP is not triggered if the duration of OCP is shorter than the delay time. Therefore, any current spike that lasts less than the delay time does not trigger the OCP function. The delay time can be set with the external component R1 as shown in Figure 3 and its driver voltage with the following equation:

$$T_{DELAY} = \frac{C_{int} * V_{REF}}{I}$$

Equation 6

Where C_{int} is 1 nF and V_{REF} is 1.2 V. The current (*I*) can be calculated by:

$$I = \frac{V\_IN - V_{LOOP}}{R_1}$$

Equation 7

Where V_IN is 3.3 V or 5 V and V_{LOOP} is 2.6 V. In this example, when R1 is 10 kΩ and V_IN is 3.3 V, the delay time can be calculated as:

$$T_{DELAY} = \frac{1000 * 1.2}{(3.3-2.6)/10} = 17\ \mu s$$

Equation 8

2 Evaluation board specifications

Input and output in operation

- DC input voltage (VIN): 10 V to 84 V
- Maximum input current: 50 A
- Maximum output current: 50 A
- Maximum output continuous power: 4.2 kW

Protection features

- Output overcurrent protection

Maximum component temperature

The maximum allowed component temperatures are as follows:

- Resistors: Less than 100°C
- Ceramic capacitors, film capacitors, and electrolytic capacitors: Less than 100°C
- MOSFET transistors and diodes: Less than 100°C
- ICs: Less than 100°C

Dimensions of the evaluation board

Width: 76 mm, length: 114 mm, and height: 1.6 mm.

Attention: ***The board should be tested only by qualified engineers and technicians.***

3 Evaluation board schematics

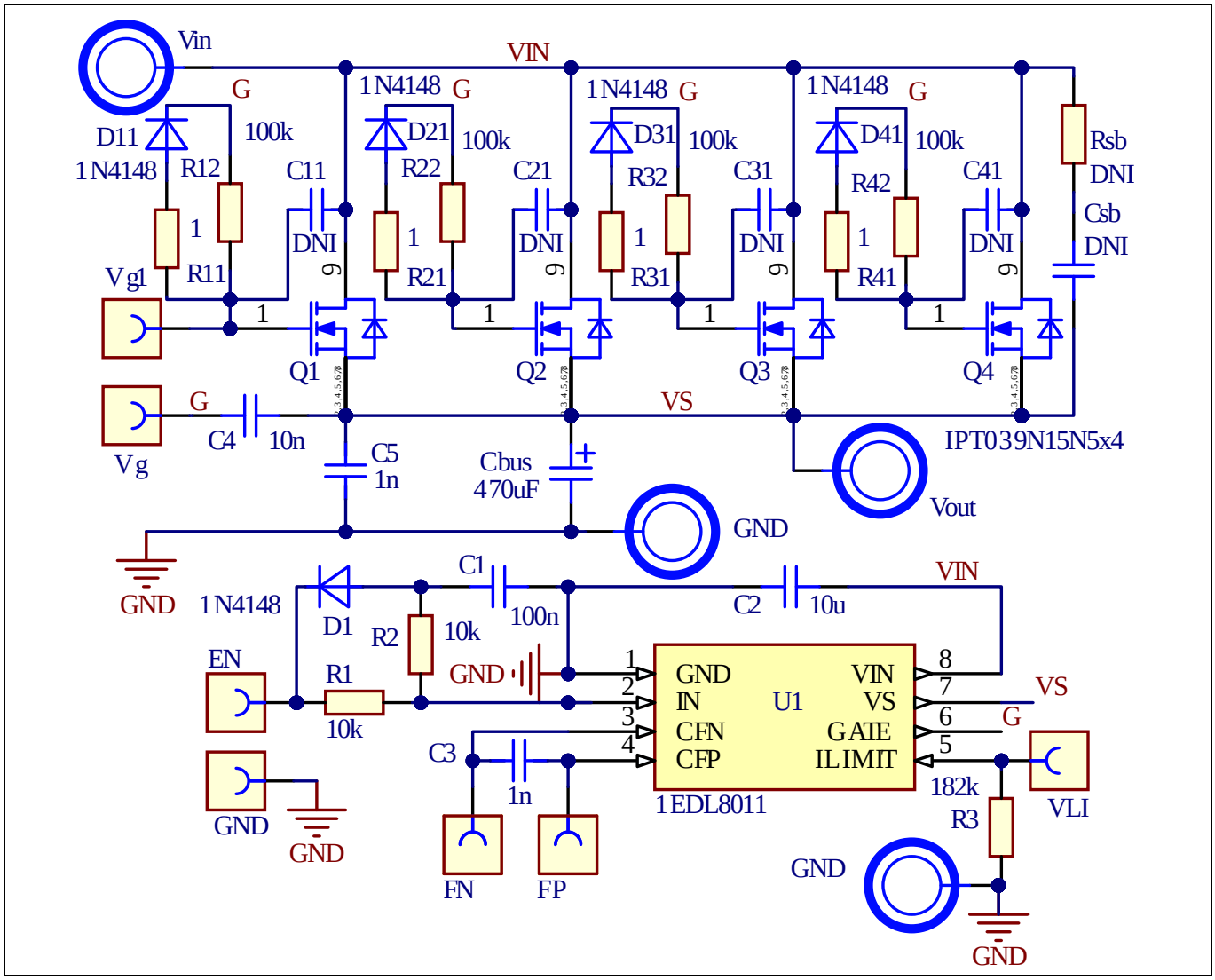

Figure 4 Evaluation board schematics

4 Hardware functional description

1EDL8011 Evaluation Board contains four MOSFETs connected in parallel to maintain device temperature within safe limits. These MOSFETs are driven by 1EDL8011 which consists of an integrated charge pump.

4.1 Charge pump design

Supply for the gate driver is provided by a charge pump with an external flying capacitor (C_{FPN}) connected at CFP and CFN pins. The output of the charge pump is available at the GATE pin to provide direct current sourcing. An external capacitor (C_{TANK}) works in parallel with the MOSFET input capacitance through an external resistor. The C_{TANK} capacitance ($C_{TANK} \geq 10 \times C_{FPN}$) is chosen to minimize the voltage ripple at the GATE pin. The charge pump is enabled as soon as the IN pin is set to HIGH by the enable signal V_IN. The value of C_{FPN} must be less than 10 nF to minimize stresses on internal devices and to avoid damage caused by the inrush current to the charge pump. Based on the value of C_{FPN}, a resistance R_{ser} must be added in series (chosen according to the following table) or a Schottky diode, D_{sh} (20 V, 1 A) must be connected between C_{FPN} and GATE pin (if C_{FPN} > 1 nF).

Table 1 Series resistance corresponding to flying capacitor

C_{FPN} (nF)	R_{ser} (Ω)
≤1	Not required
2.2	25
4.7	50
10	100

4.2 MOSFET turn-on time

The MOSFET turn-on time is measured from the first rising edge of CFN till the gate voltage (V_{GATE} – VS) reaches 10 V. Turn-on time depends on multiple factors like MOSFET input capacitance, drain voltage (VIN), flying capacitor (C_{FPN}), R_{ser}, tank capacitor (C_{TANK}), and external gate resistor Rgon. The plot has been generated using measurements at three input voltages (VIN) 18 V (▲), 40 V (●), and 84 V (■) with a 50 A load and Cbus of 47 µF. The values of R_{ser} and C_{TANK} are changed corresponding to the C_{FPN} value.

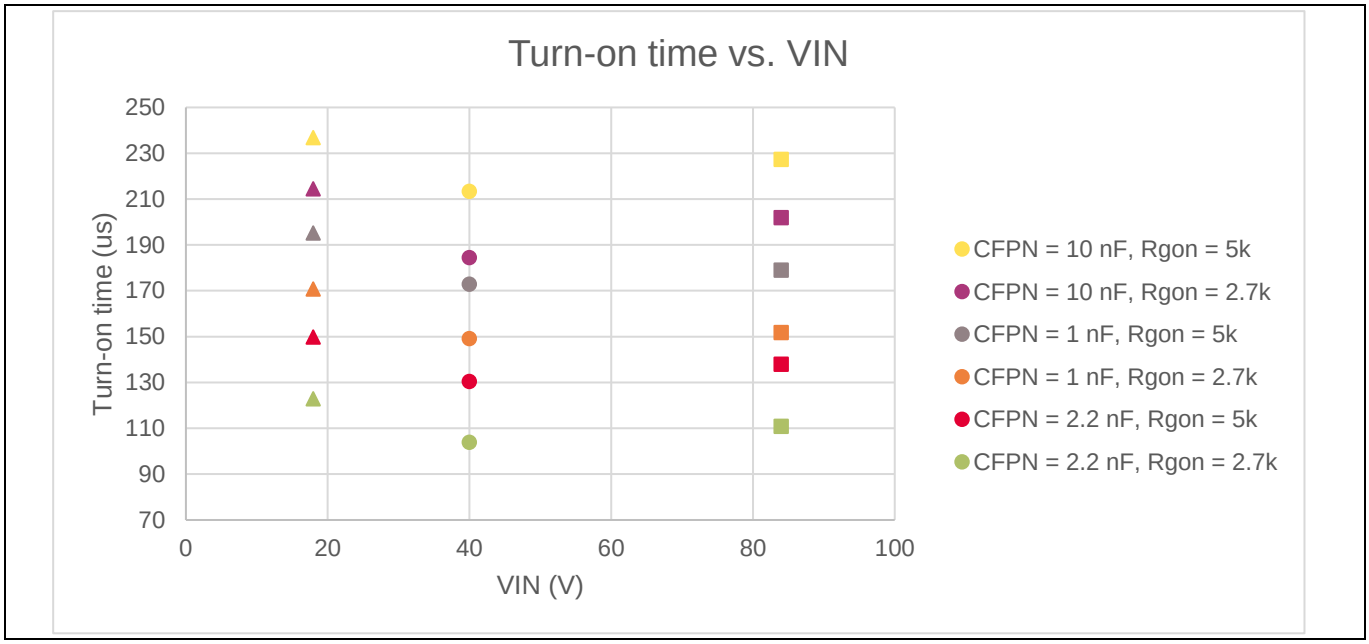

Figure 5 Turn-on time vs. VIN at different input voltages

4.3 MOSFET turn-off time

The MOSFET turn-off time is measured as the time taken for the gate voltage (V_{GATE} – VS) to drop from 12 V to 2 V. The measurements for MOSFET turn-off time are performed with similar test conditions as turn-on time except the Rgoff values.

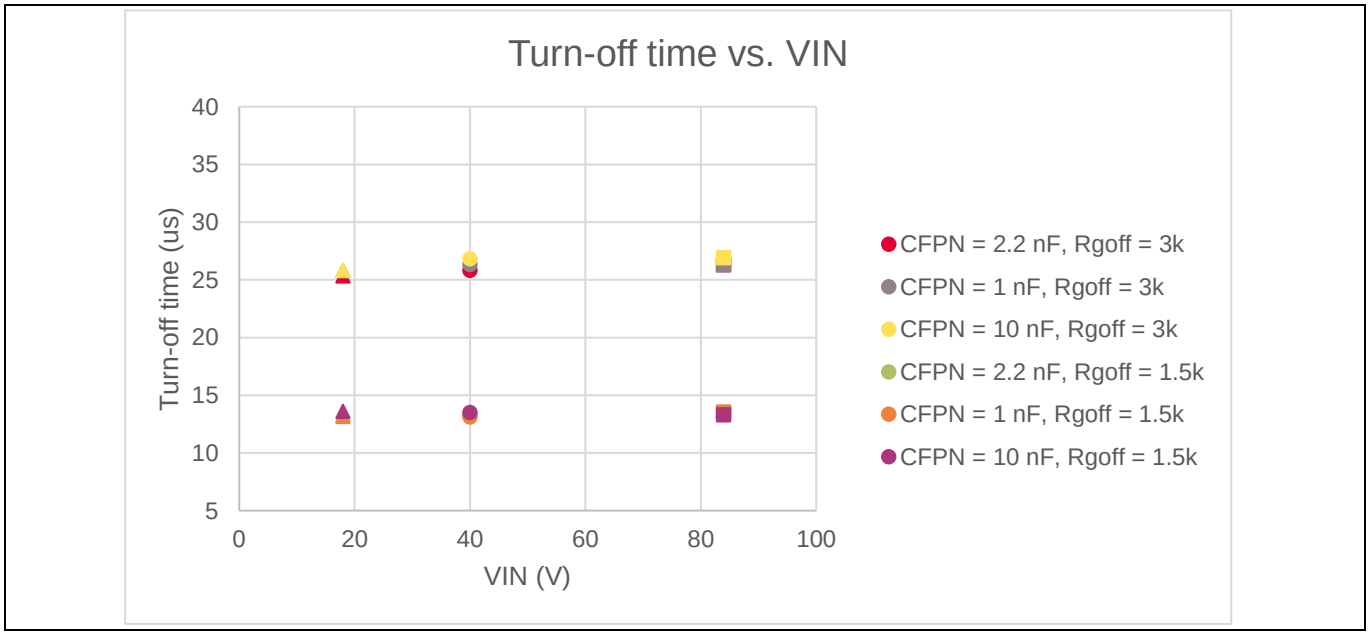

Figure 6 Turn-off time vs. VIN at different input voltages

4.4 Board connections and controls

The following lab equipment is required to test the boards.

Table 2 Equipment required

Item	Equipment type		Description
1	DC power supply 1		84 V, 50 A output
2	Power supply 2	DC	3.3 V, 0.1 A output
3		Pulse generator	3.3 V, 0.1 A output

Figure 7 shows the board connections. The power-up steps are as follows:

1. Connect the DC power supply 1, power supply 2 (or pulse generator), load, and probes (measure the V_{GS} and V_{DS} voltages with differential probes).
2. Set the load current (max. 50 A).
3. Increase the voltage using DC power supply 1 to above UVLO.
4. Turn on the pulse generator. The slew rate must be higher than 0.35 V/µs to start-up properly.

To check UVLO, use the following power-up steps:

1. Connect the DC power supply 1, power supply 2 (DC), load, and probes (measure the V_{GS} and V_{DS} voltages with differential probes).
2. Set load current (max. 50 A).
3. Increase the voltage using DC power supply 2 from 2 V to 3.3 V.
4. Increase the voltage using DC power supply 1 to above UVLO.

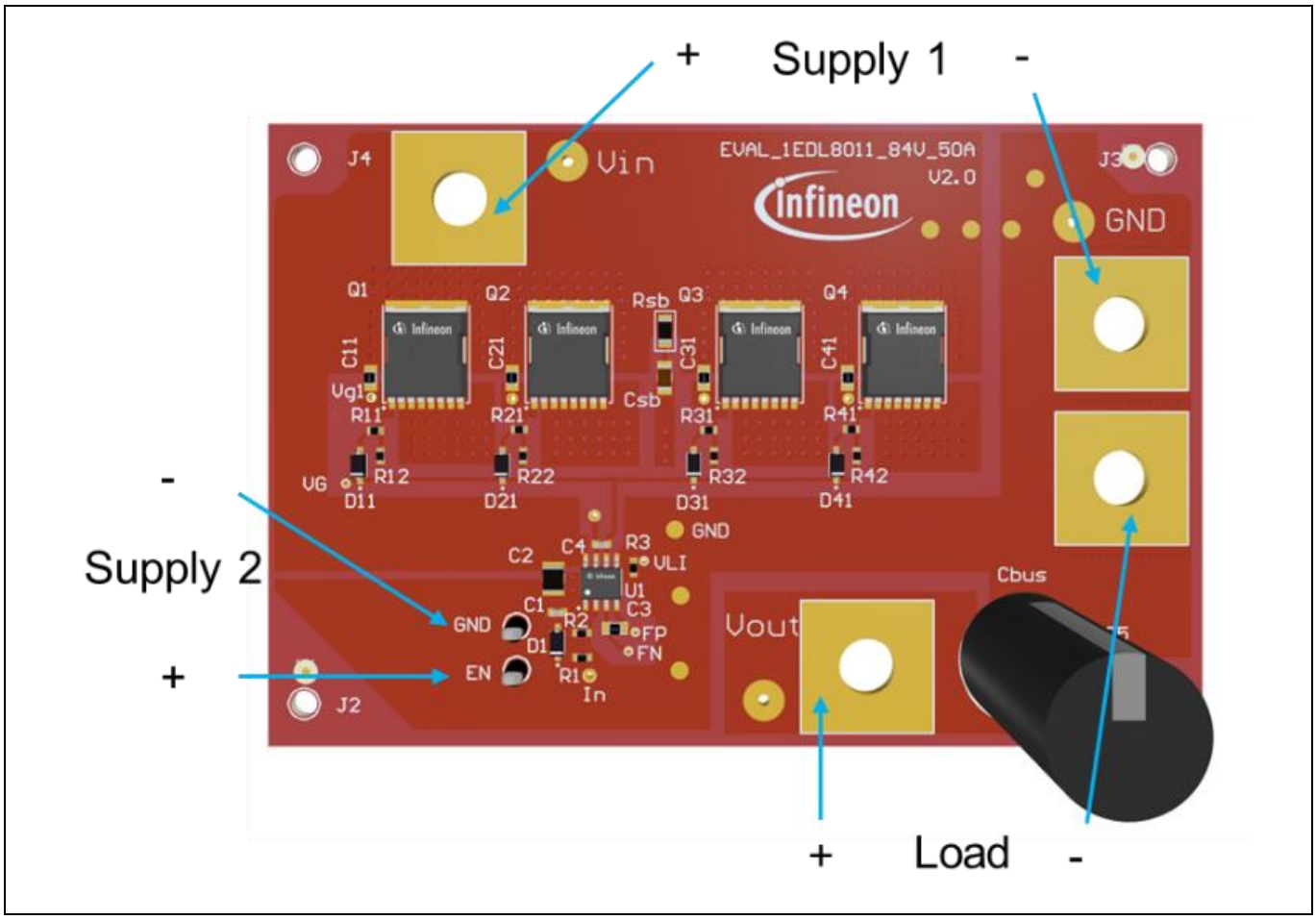

Figure 7 Board connections

5 Bill of materials

Table 3 Bill of materials

Item	Part references	Qty	Type	Value/rating/ tolerance/package/ other	Manufacturer	Part number
1	C1	1	Capacitor	100 nF, 25 V, 20%, 0603, X7R	AVX	06035C104K4Z2A
2	C2	1	Capacitor	10 µF, 100 V, 20%, 1210, X7S	Murata	490-16266-1-ND
3	C3, C5	2	Capacitor	1 nF, 100 V, 20%, 0805, X7R	AVX	478-10422-1-ND
4	C4	1	Capacitor	10 nF, 25 V, 20%, 0603, X7R	Cal-Chip Electronics	GMC10X7R103M25NT
5	Cbus	1	Capacitor	470 µF, 100 V, 20%, 16 x 32 mm, Aluminum	Nichicon	UPW2A471MHD
6	D1, D11, D21, D31, D41	5	Diode	0.3 A, 100 V, SOD123	Diodes	1N4148W-13-F
7	EN, GND	2	Connector	Black bead terminal, assembly 1.32 mm hole	Keystone Electronics	36-5011-ND
8	FN, FP, Vg, Vg1, VLI	5	Test pad	Test pad, SMD, 1.0 mm	–	–
9	J1, J2, J3, J4	4	Standoff	Standoffs & Spacers .375 M/F THRD	Keystone Electronics	36-8400-ND
10	NT1, NT2, NT3, NT4	4	Hex nut	#4-40 Hex nut 0.250" (6.35 mm) 1/4"	B&F Fastener Supply	H216-ND
11	Q1, Q2, Q3, Q4	4	Transistor	N-channel, 150 V, 190 A, 3.9 mΩ, HSOF-8	Infineon Technologies	IPT039N15N5
12	R1, R2	2	Resistor	10 kΩ, 0.1 W, 1%, 0603	Vishay	CRCW060310K0FKEBC
13	R3	1	Resistor	182 kΩ, 0.1 W, 1%, 0603	Bourns Inc.	CR0603-FX-1823ELF
14	R11, R21, R31, R41	4	Resistor	1 Ω, 0.1 W, 1%, 0603	Vishay	CRCW06031R00JNEA
15	R12, R22, R32, R42	4	Resistor	100 kΩ, 0.1 W, 1%, 0603	Vishay	RCA0603100KFKEA
16	T2, T3, Vin, Vout	4	Connector	Connector, 6-14 AWG, 12.7 x 17 mm	Panduit	CXS70-14-C

Bill of materials

Item	Part references	Qty	Type	Value/rating/ tolerance/package/ other	Manufacturer	Part number
17	SW1, SW2, SW3, SW4	4	Connector	Screws	McMaster	91772A537
18	NT5, NT6, NT7, NT8	4	Connector	Nuts	McMaster	91845A029
19	WS1, WS2, WS3, WS4	4	Connector	Washer	McMaster	96551A240
20	U1	1	IC	High-side gate driver, 125 V, 5 x 6 mm	Infineon Technologies	1EDL8011

6 PCB layout

EVAL_1EDL8011 Evaluation Board uses a four-layer PCB with 1 oz. copper for each layer, as shown in Figure 8 to Figure 11. Components are mounted on the top side. The PCB layout is optimized to minimize the unbalanced current flow. This is done by connecting the positive input on the left side and the positive output on the right side. The big polygon of the positive input on the top is used to connect pin 1 of 1EDL8011 to ensure that $R_{DS(on)}$ sensing is accurate. Ensure spacing between high-voltage nodes on the top and bottom layers. Components with switching noises are kept close to each other.

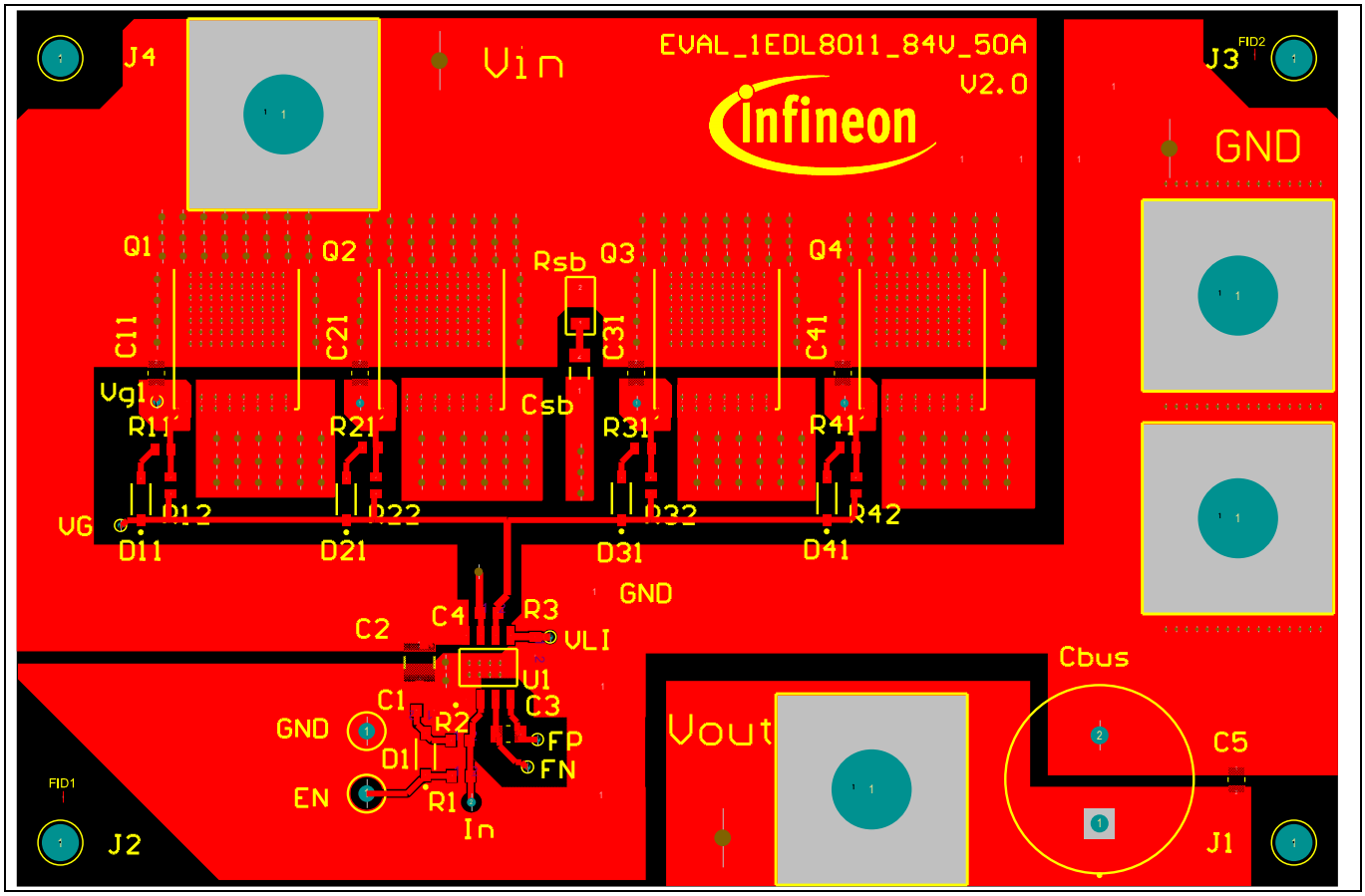

Figure 8 Top layer with silkscreen

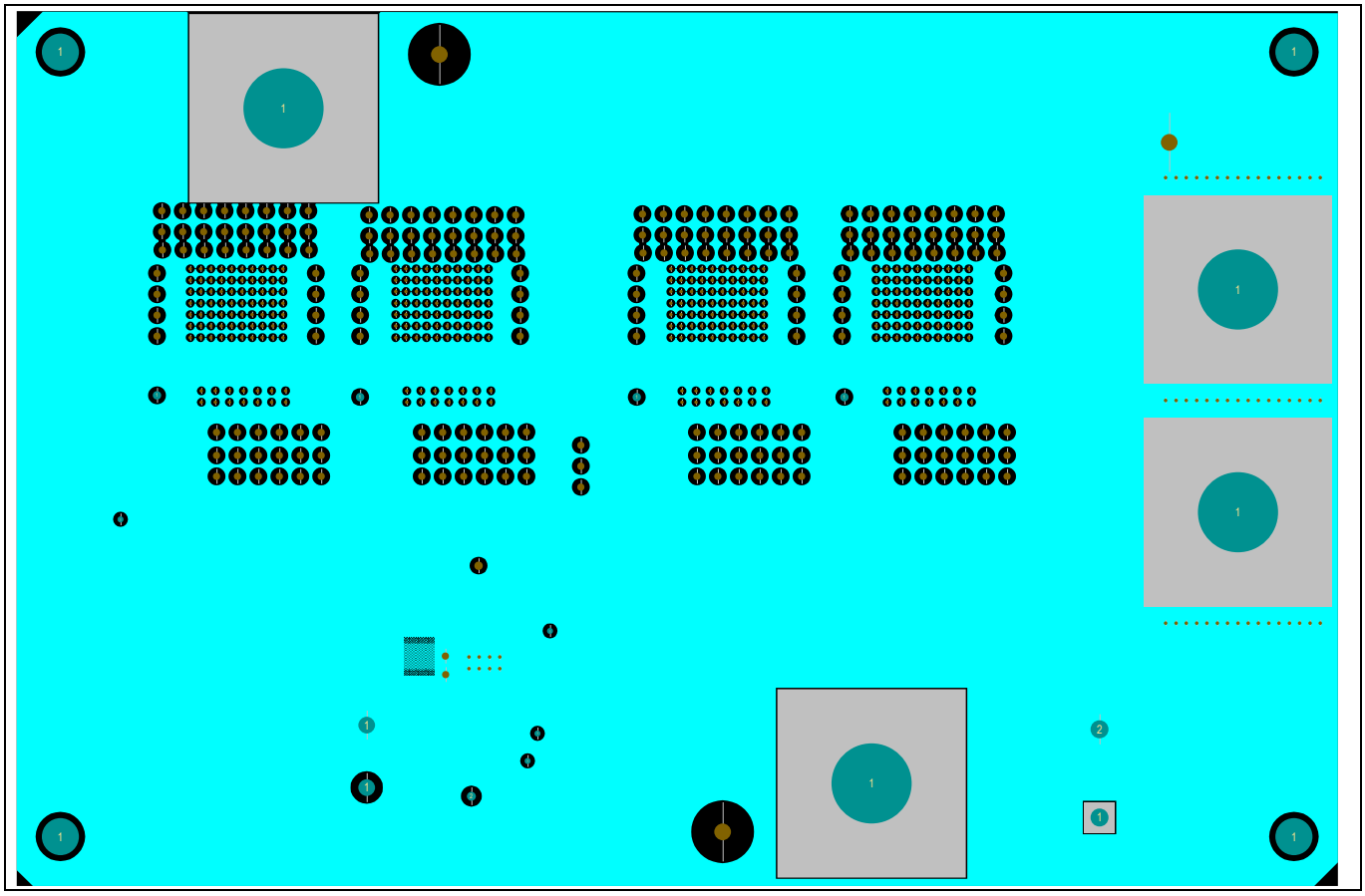

Figure 9 M2 layer

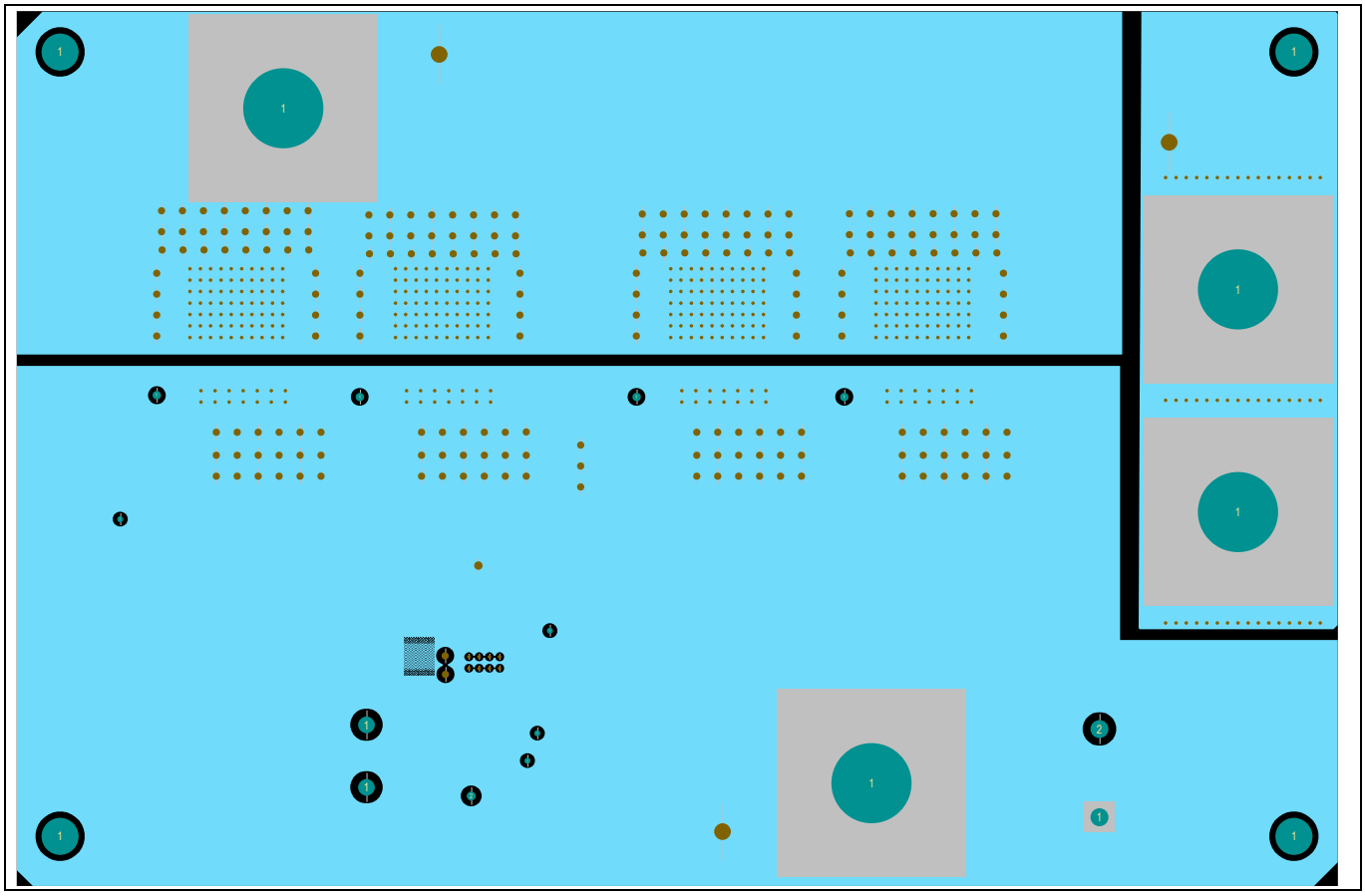

Figure 10 M3 layer

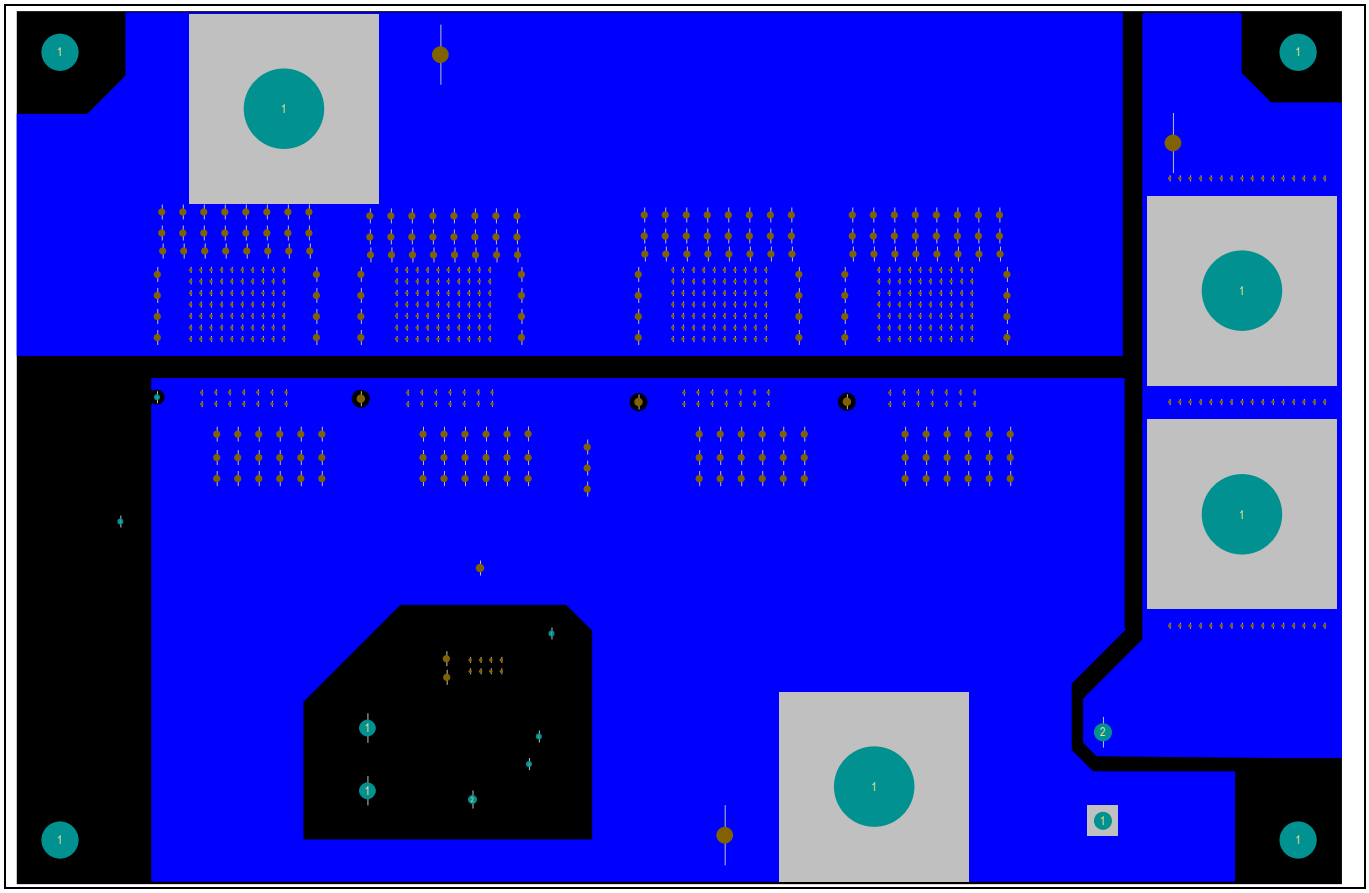

Figure 11 Bottom layer with silkscreen

7 Test results

7.1 Operating waveforms

Figure 12 shows the startup waveforms. VGS1 rises from zero to 10 V within 1.7 ms. Figure 13 shows the OCP triggered at 60 A when the load increases gradually. The triggered current is very close to the chosen OCP setting of 62 A in Section 1.4. The measured turn-off time is 320 ns as shown in Figure 13.

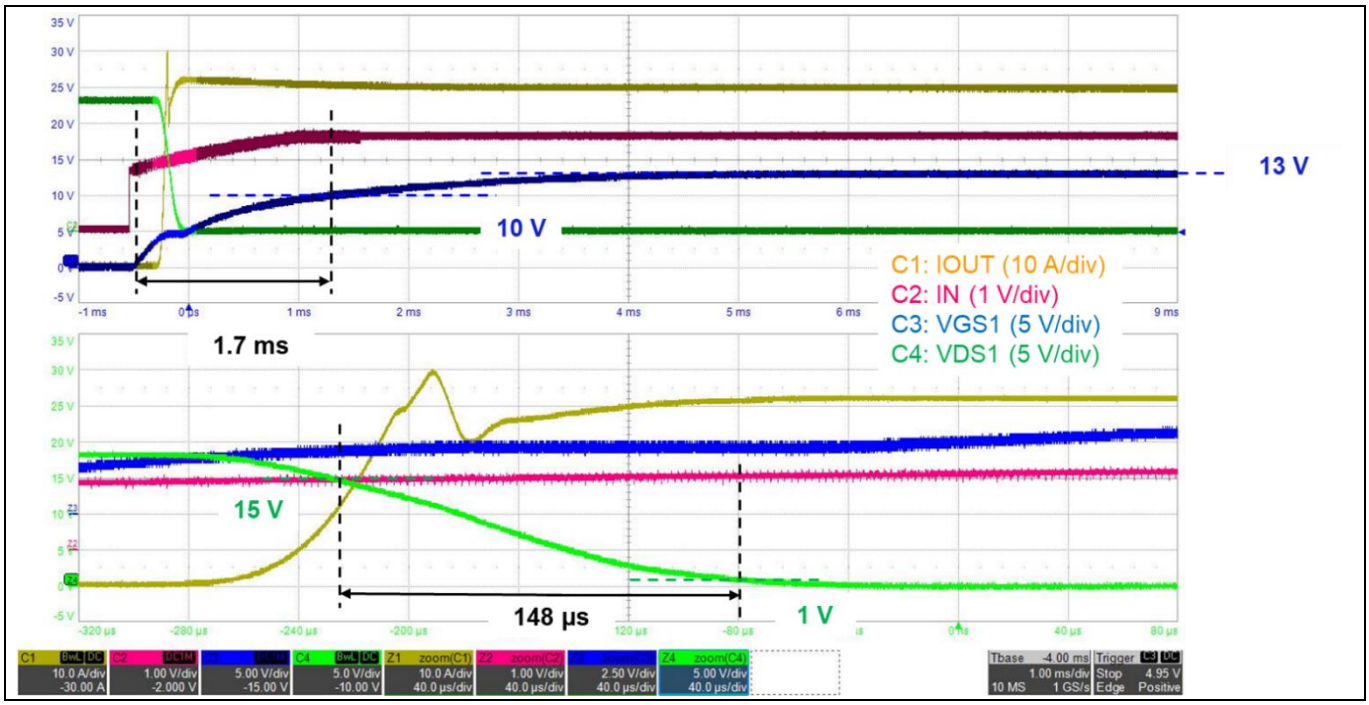

Figure 12 Startup waveforms (18 V VIN 50 A load)

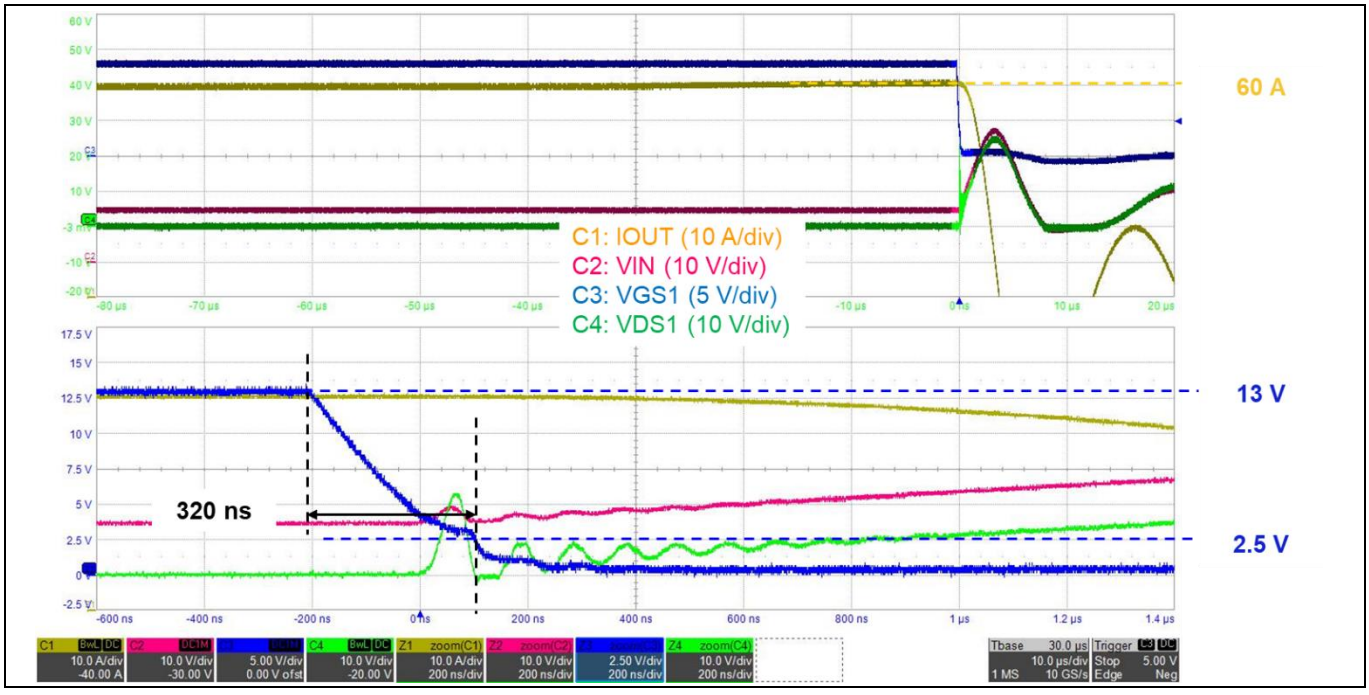

Figure 13 OCP triggered at 60 A with 18 V VIN

Test results

Figure 14 shows the OCP delay time of 24 µs which begins when the current exceeds 60 A, based on the measurement shown in Figure 13. The measured delay time is very close to the calculated value of 17 µs in Section 1.4.

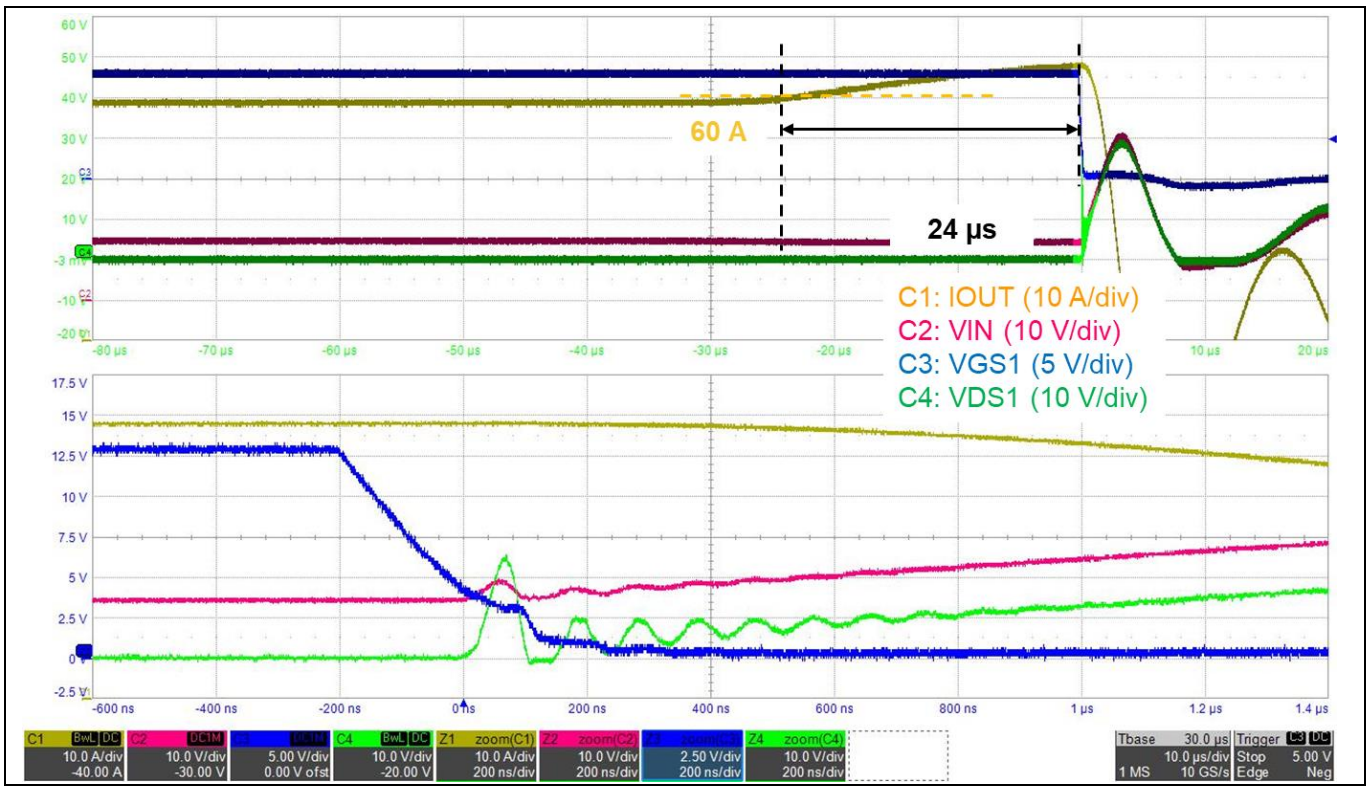

Figure 14 OCP delay time 24 µs with 18 V VIN and current change from 59 A to short

Figure 15 shows the blanking time of 1.7 ms during startup and is approximately equivalent to the calculated value of 1.91 ms in Section 1.3. In the waveforms shown below, the load current of 62 A was chosen to demonstrate the blanking time.

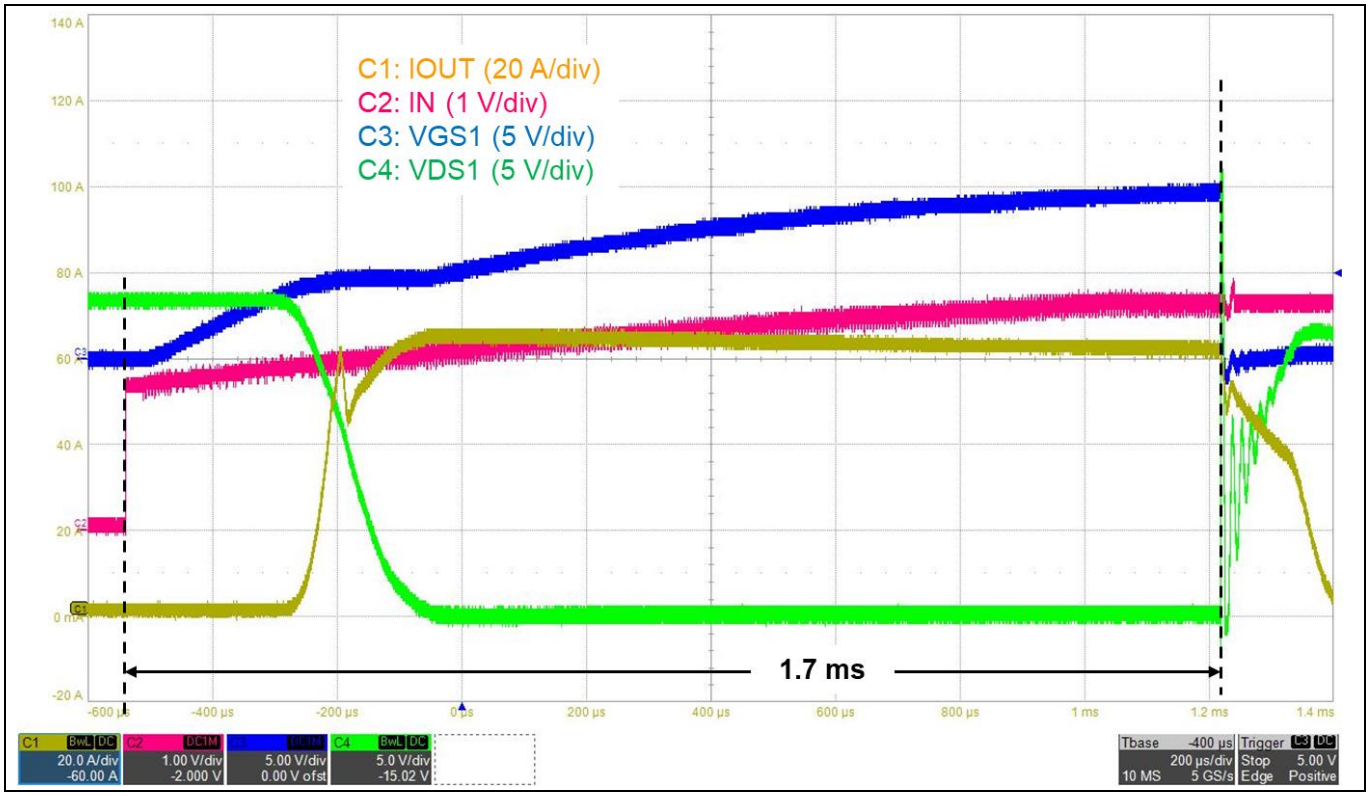

Figure 15 Blanking time waveforms (18 V VIN, 62 A load)

Test results

Figure 16 shows the startup waveforms with voltages at CFP and CFN pins. The voltages at CFP and CFN are DC voltages (18 V and 0 V respectively) after V_{GS} reaches 12 V indicating that the charge pump operating at 400 kHz turns off. When V_{GS} exceeds 12 V, an auxiliary charge pump takes over and continues to maintain the V_{GS} voltage, which minimizes EMI in the application. The flying capacitance CF will have the input voltage VIN across it. V_{GS} is the voltage between the output of the driver (GATE pin) and the source of the MOSFETs. The 1EDL8011 driver can provide a minimum DC current of 5 mA for a V_{GS} voltage of 9 V.

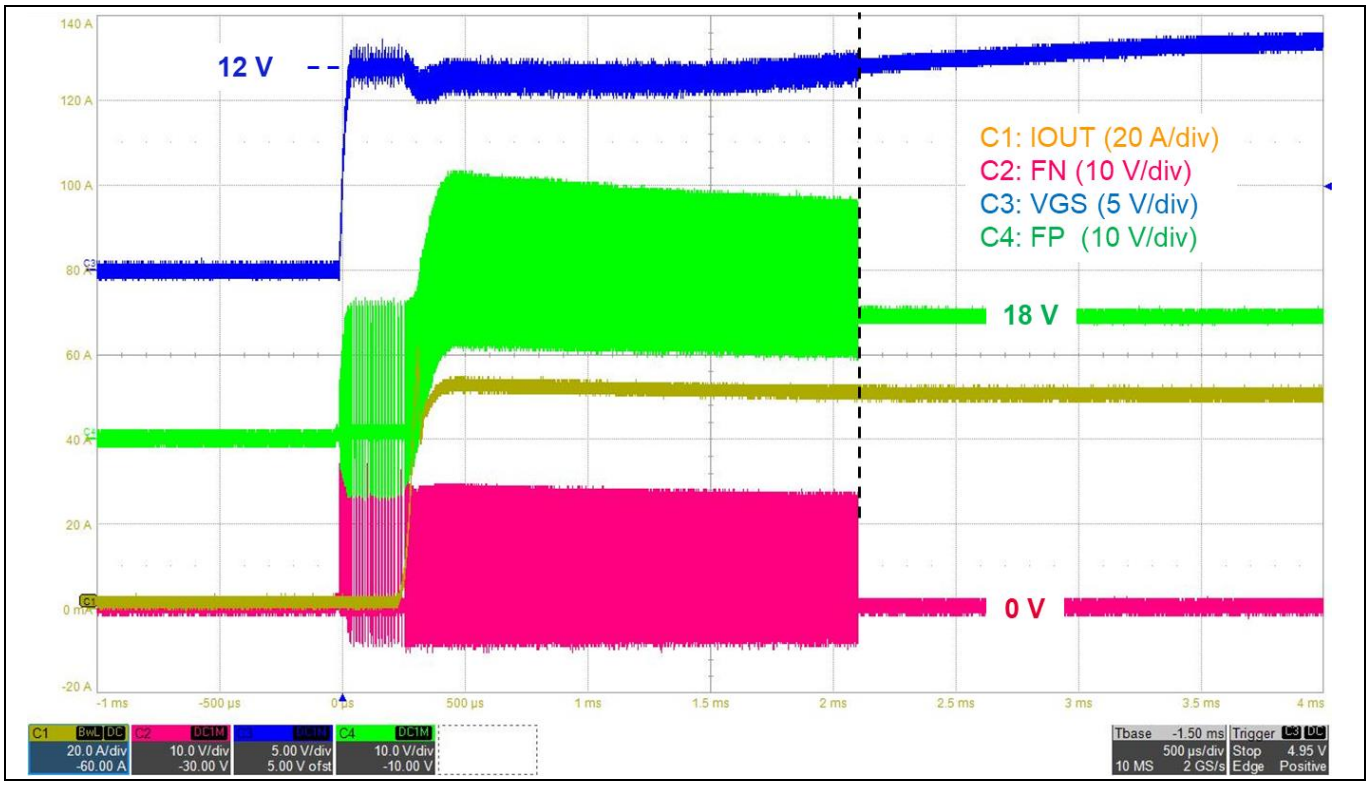

Figure 16 Startup waveforms with voltages at CFP and CFN pins (18 V VIN, 50 A load)

Figure 17 shows the UVLO waveforms when VIN decreases gradually from 18 V. VGS1 turns off when the voltage at the input falls below 7.4 V.

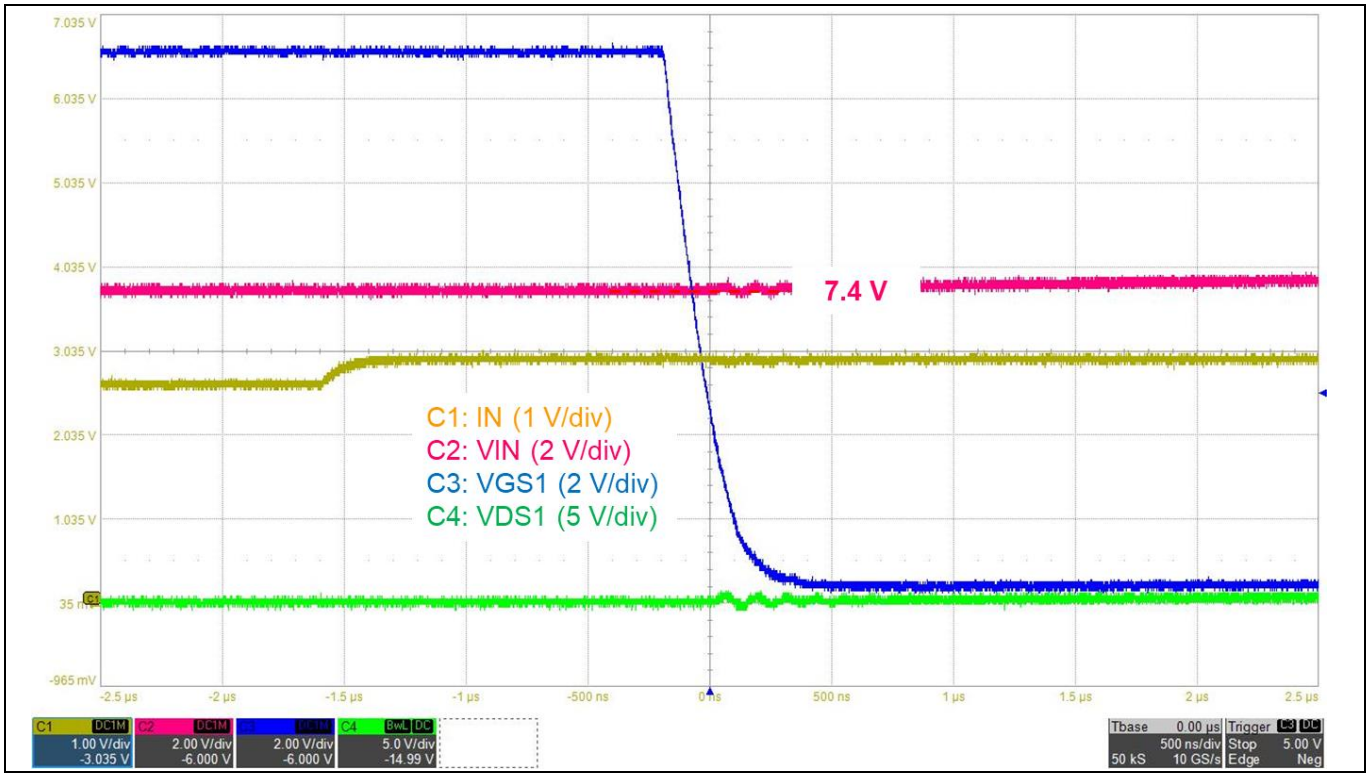

Figure 17 UVLO waveforms (VIN from 18 V to 0 V, 1 A load)

A high input current is expected during startup when the load is short. Figure 18 shows the turn-off waveforms for a 40 V input. The voltage at VIN exhibits a voltage spike of 120 V after turning-off an input current of 120 A due to the leakage inductance between the power supply and the evaluation board. Any voltage spike must be below 125 V, which is the maximum voltage rating of 1EDL8011 driver. The addition of a 470 µF capacitor can reduce the amplitude of the voltage spike even at higher input voltages. This is shown in the turn-off waveforms of Figure 19, where a voltage spike of only 92 V is observed for a 84 V input voltage.

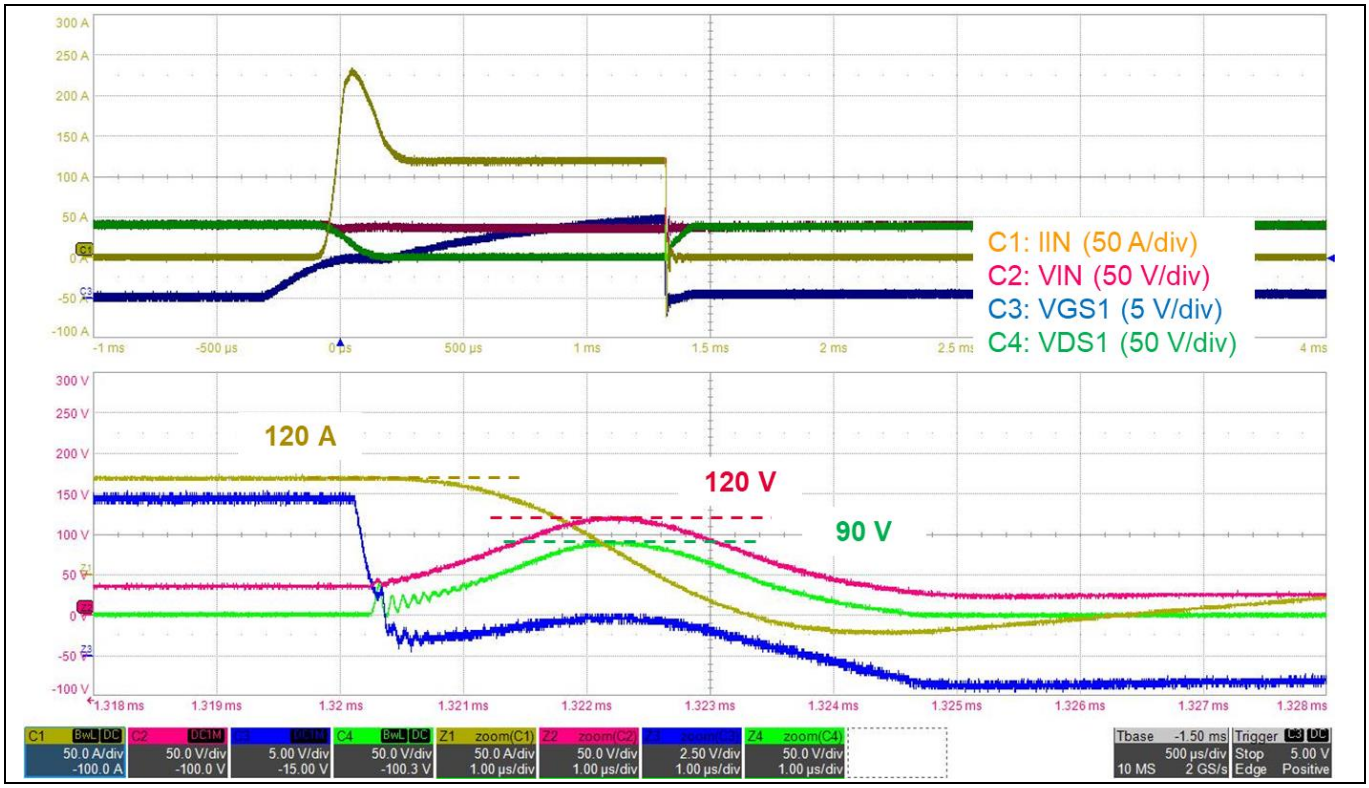

Figure 18 Turn-off waveforms with 40 V VIN and short at load

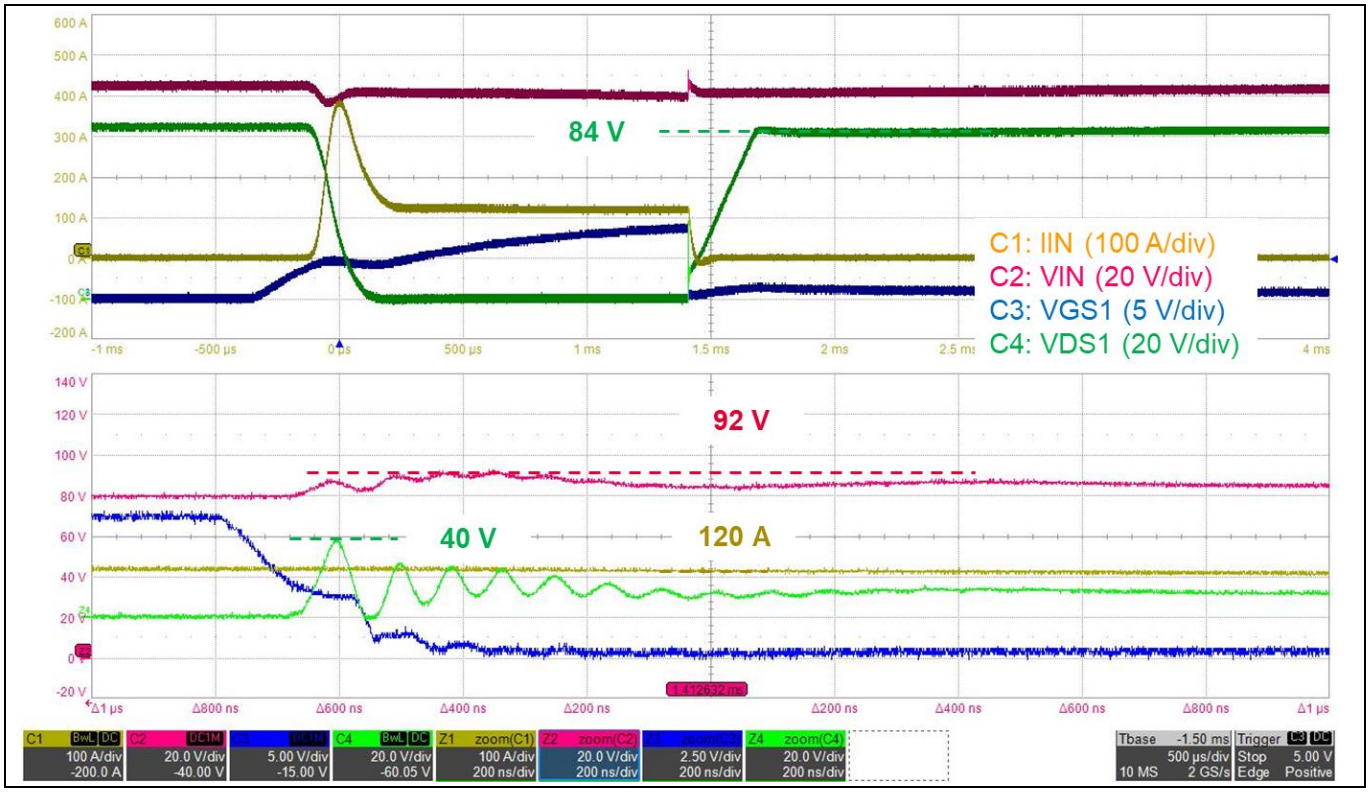

Figure 19 Turn-off waveforms with 84 V VIN and short at load (470 µF added to VIN)

7.2 Thermal measurements

Figure 20 shows the thermal image taken after 15 minutes of operation to allow the component temperatures to rise and reach the thermal steady state. Without any heatsinking or forced air cooling, the maximum case temperature of the MOSFETs reaches 70°C.

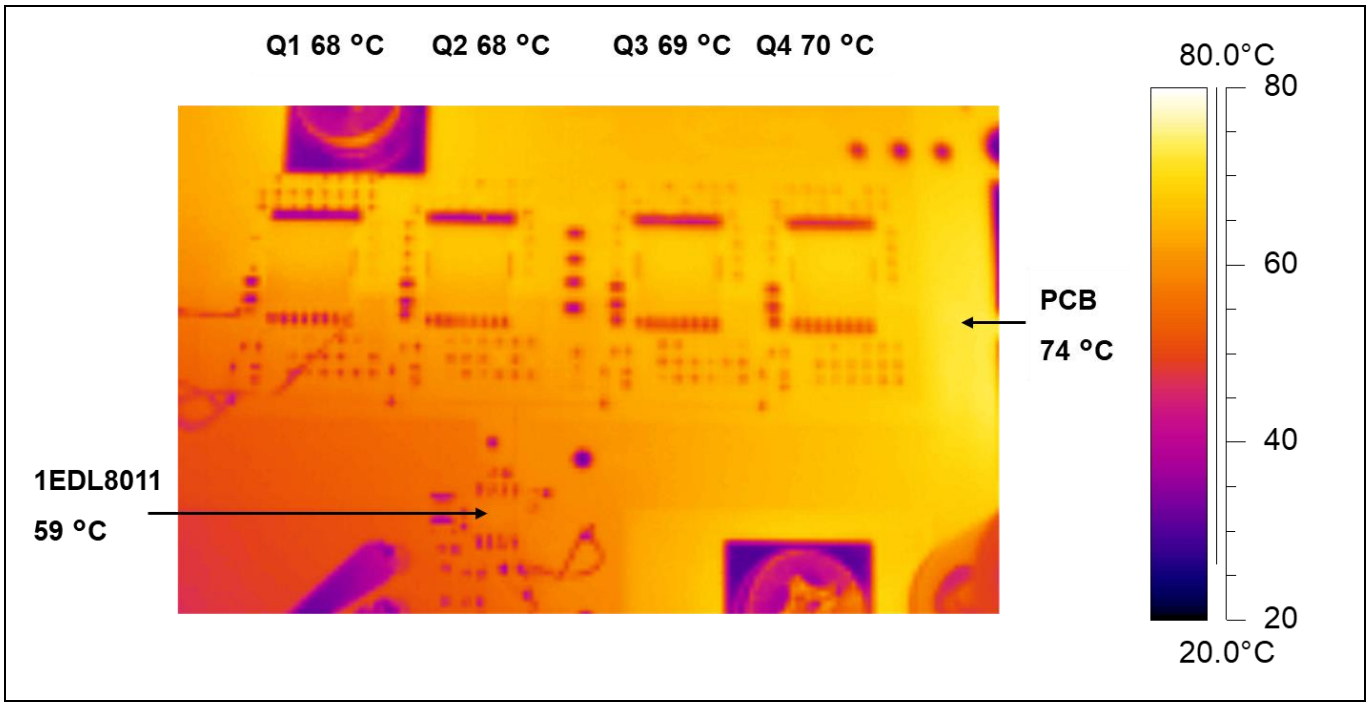

Figure 20 Thermal image after 15 minutes at 18 V VIN at the input and 50 A load

8 Summary

The 1EDL8011 is a high-side driver for high-side MOSFETs used as a switch to provide power to a load. Its VDS sensing provides overcurrent protection (OCP) for the MOSFETs, load, and power source. The OCP blanking and time delay can be adjusted with external components to ensure that the OCP will not be accidently triggered during startup and normal operation. A wide operating input range is achieved with VIN UVLO protection. A safe switch-off mechanism is used to turn-off the MOSFETs before the driver is powered down. An internal charge pump is used to maintain gate drive voltage while minimizing EMI and facilitating operation at low input voltages.

References

Contact Infineon Support to obtain this document.

[1] Infineon Technologies AG; *1EDL8011 datasheet*

Revision history

Document revision	Date	Description of changes
V 1.0	2024-07-16	Initial release

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Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.