microSD 7.1 Specification

(Fx Premium, 3D TLC)

Version 1.0

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1. GENERAL DESCRIPTION

1.1. Introduction

Fx Premium microSD 7.0 card comes with 17-pin interface, designed to operate at PCIe interface with a maximum throughput (logical/ Idea performance) to 985MB/s (Gen3x1 Lane). It can alternate communication protocol between the SD Express mode, SD mode and SPI mode. Backward compatible with UHS-I hosts.

Fx Premium microSD 7.0 card is the first SD card implements PCIe/NVMe interface and protocol. It is the slimmest SSD like storage device with maximum speed of 985MB/s. It is designed for those applications that need extreme high performance like burst mode photo shooting, 8K 10K video recording, mobile devices, VR/AR, drones, gaming application, data-intense wireless communication, mobile computing devices, multi-channel IoT devices and automotive storage.

1.2. Product Overview

- **Flash**
  - 3D TLC
- **Capacity**
  - 128GB up to 256GB
- **Support SD SPI mode**
- **Non-Copyrights Protection Mechanism**
- **Card removal during read operation will never harm the content**
- **Password Protection of cards (optional)**
- **Designed for read intensive and write intensive cards**
- **Write Protect feature using mechanical switch**
- **Built-in write protection features (permanent and temporary) (SD mode only)**
- **Write Protect feature using mechanical switch (Full SD Card only)**
- **Operation voltage range:**
  - VDD1: 2.7V~3.6V, VDD2: 1.70V~1.95V
- **Temperature Range**
  - Operation: -25°C ~ 85°C
  - Storage: -40°C ~ 85°C
- **RoHS Compliant**
- **Bus Speed Mode (use PCIe Differential Interface Lines)**
  - **PCIe with Gen 3 x 1 Lan – Up to 985MB/s**
  - **Gen3 x1 bus, two differential I/O (1 RX/ 1TX) of 8Gbps transfer for each direction (~1.5% overhead due to 128/120 encoding)**
- **Bus Speed Mode (use 4 parallel data lines)**
  - **UHS-I mode**
    - SDR12: SDR up to 25MHz, 1.8V signaling
    - SDR25: SDR up to 50MHz, 1.8V signaling
    - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
    - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104 MB/sec
    - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec

2. PRODUCT SPECIFICATIONS

2.1. Performance

Table 2-1 Performance of microSD (Fx Premium)

Capacity	Sequential (Burst Mode)		Sequential (Sustained Mode)	
	Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)
128GB	810	500	650	60
256GB	810	700	650	60

NOTES:

1. The performance is obtained from CrystalDiskMark
2. Samples are made of 3D TLC Flash.
3. Performance may vary from flash configuration and platform.
4. The PCIe performance was measured by direct connecting to mother board reader
5. The Burst mode size is the 1/8 capacity.

2.2. Power

Table 2-2 Maximum Power Consumption of microSD (Fx Premium)

Capacity	Read (mA)	Write (mA)	Standby (mA)
128GB	400	400	1
256GB	400	400	1

NOTES:

1. Power consumption may vary from flash configuration and platform.

2.3. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The higher the MTBF value, the higher the reliability of the device. The predicted result of FLEXXON's SD Express Series SD is more than 3,000,000 hours.

2.4. Data Retention

- 10 years if > 90% life remaining (@25C)
- 1 year if < 10% life remaining (@25C)

3. ENVIRONMENTAL SPECIFICATIONS

Test Items	Test Conditions
Storage Temperature	-40°C ~ 85°C
Operating Temperature	-25°C ~ 85°C
Storage Humidity	40°C, 93% RH
Operating Humidity	25°C, 95% RH
Shock	500G, Half Sin Pulse Duration 1ms
Vibration	80Hz ~ 2000Hz/20G, 20Hz ~ 80Hz/1.52mm, 3 axis/30min
Drop	150cm free fall, 6 face of each unit
Bending	≥ 10N, Hold 1 min/5 times
Torque	0.15N-m or +/-2.5 deg, Hold 30 seconds/5 times
Salt Spray	Concentration: 3% NaCl, Temperature: 35°C, 24hours
Waterproof	Water temperature: 25°C Water depth: The lowest point of unit is locating 1000mm below surface. Storage for 30 mins
X-Ray	0.1 Gy of medium-energy radiation (70 keV to 140 keV, cumulative dose per year) to both sides of the card Storage for 30 mins
Durability	10,000 times
ESD	Contact: +/- 4KV each item 25 times Air: +/- 8KV 10 times

4. ELECTRICAL SPECIFICATIONS

4.1. DC Characteristics

4.1.1. Bus Operation Conditions

Table 4-1 Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH}=-2mA V_{DD} Min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL}=2mA V_{DD} Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Table 4-2 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 4-3 Threshold Level for 1.8V Signaling

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.58	V	

Table 4-4 Input Leakage Current for 1.8V Signaling

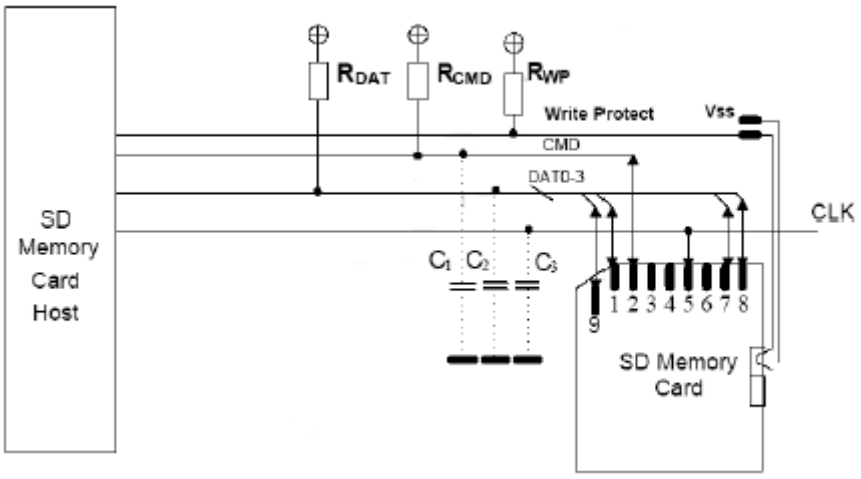
Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

4.1.2. Bus Operation Conditions for PCIe

Table 4-5 Bus Operation Conditions of VDD3

Parameter	Symbol	Min	Max.	Unit	Remarks
Supply Voltage	**V_{DD2}**	1.14	1.3	**V**	-
Capacitance connected to V_{DD2}	**C_{C2}**	-	2	**uF**	-
Host capacitance recommended for V_{DD3}	**C_{h3}**	22	-	**uF**	-

4.1.3. Bus Signal Line Load



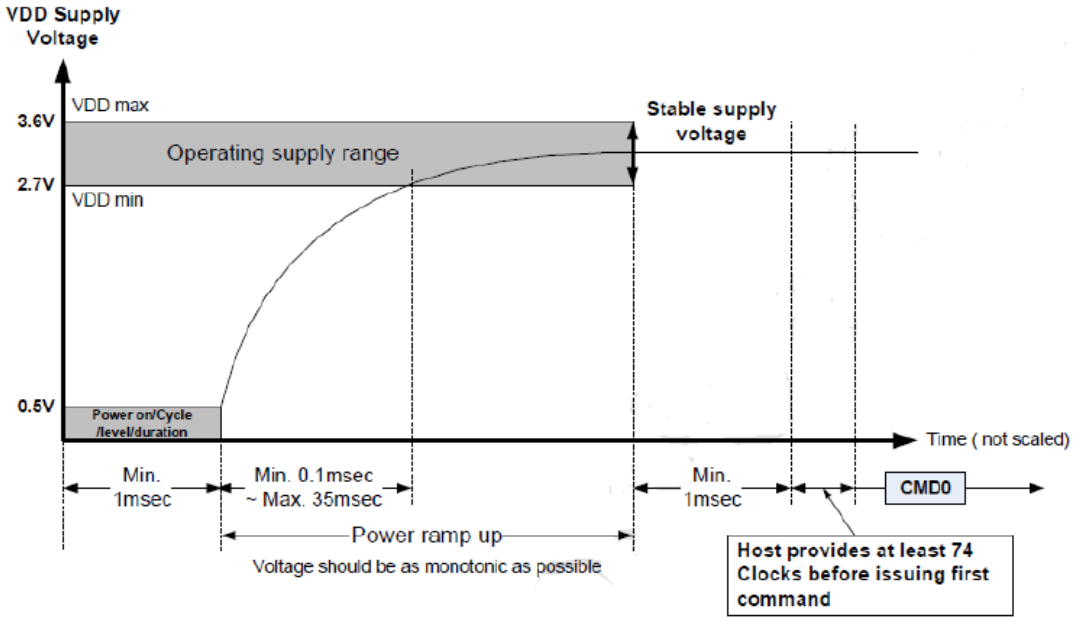
Bus Operation Conditions – Signal Line's Load

Total Bus Capacitance = C_{HOST} + C_{BUS} + N C_{CARD}

Parameter	symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30 pF
Card Capacitance for each signal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

4.1.4. Power Up Time of Host

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V

(2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:

(1) Voltage of power ramp up should be monotonic as much as possible.

(2) The minimum ramp up time should be 0.1ms.

(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

(4) Host shall wait until VDD is stable.

(5) After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

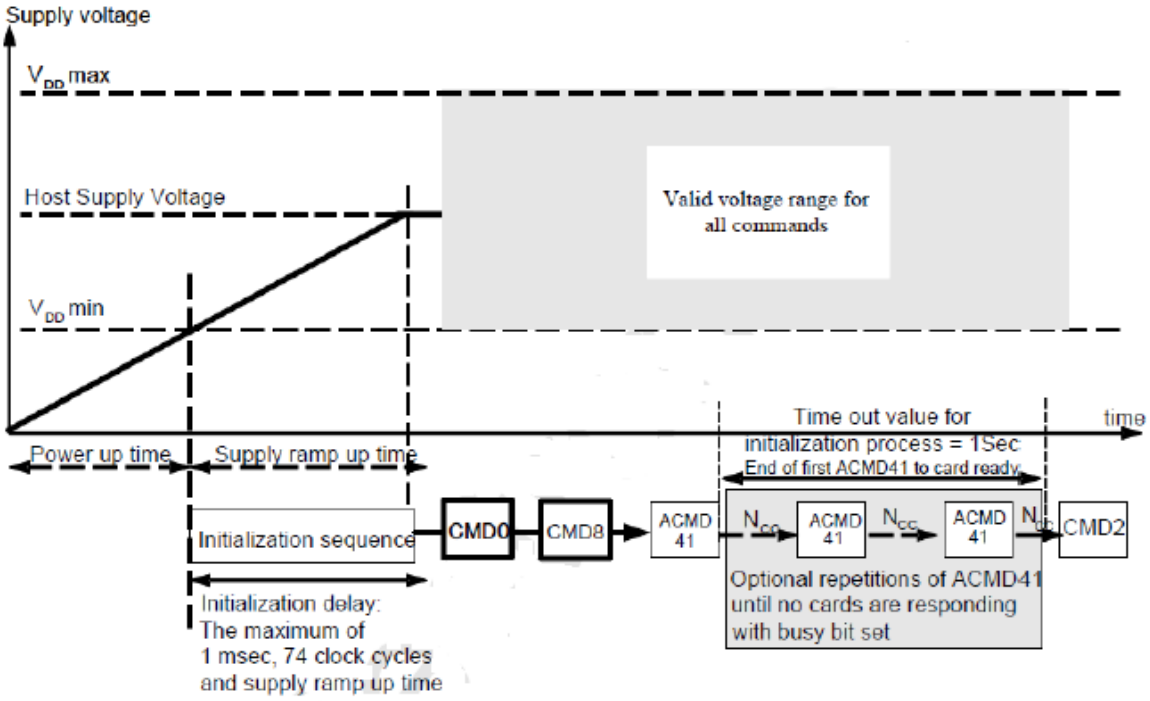
Power Down and Power Cycle

- When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.
- If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State.* To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

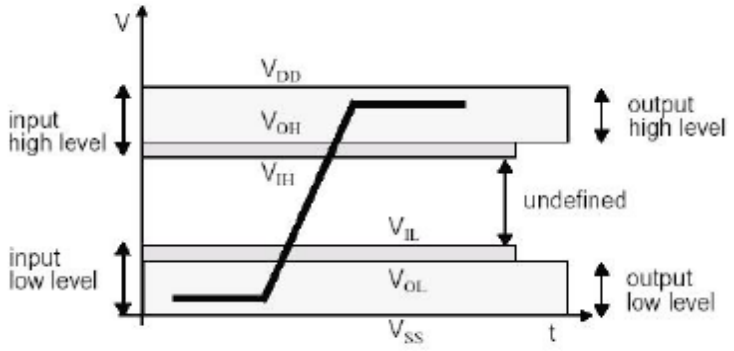
4.1.5. Power Up Time of Card

A device shall be ready to accept the first command within 1ms from detecting VDD min.

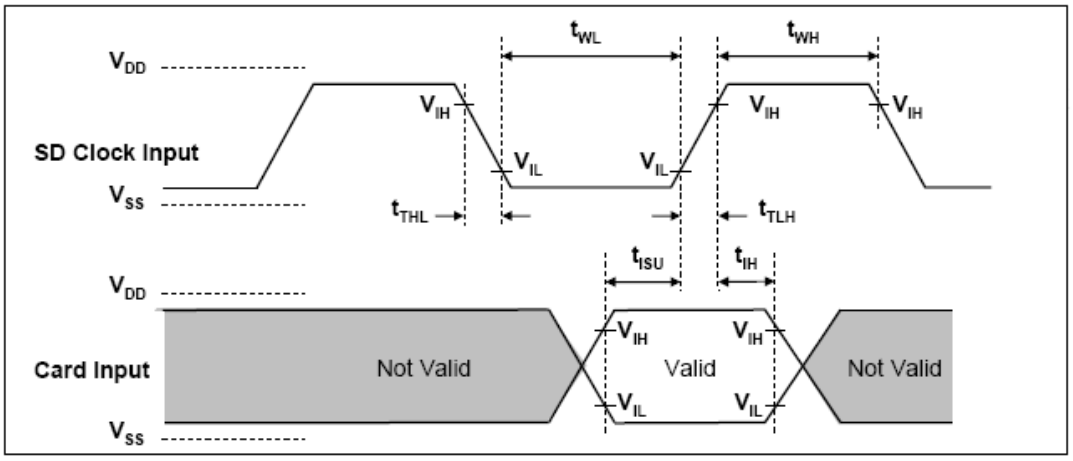
Device may use up to 74 clocks for preparation before receiving the first command.



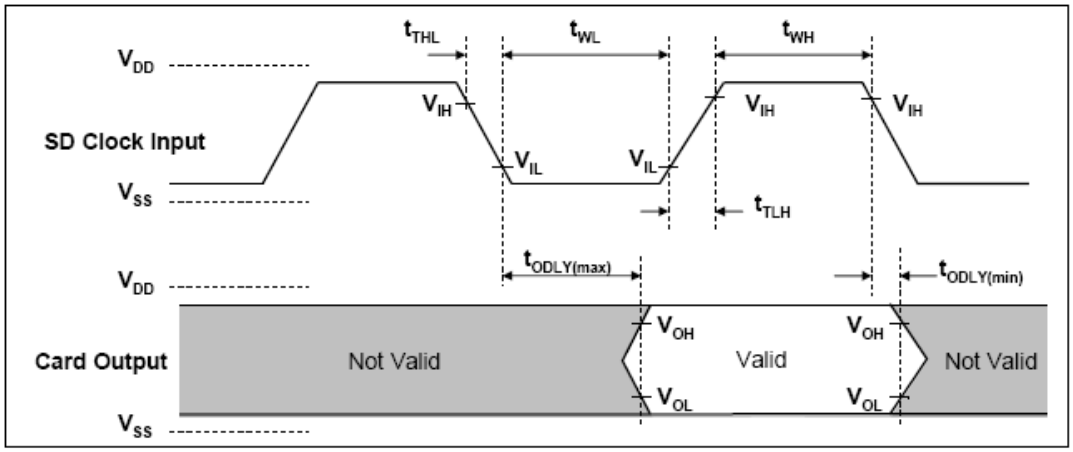
4.2. AC Characteristic



4.2.1. SD Interface timing (Default)



Card Input Timing (Default Speed Card)



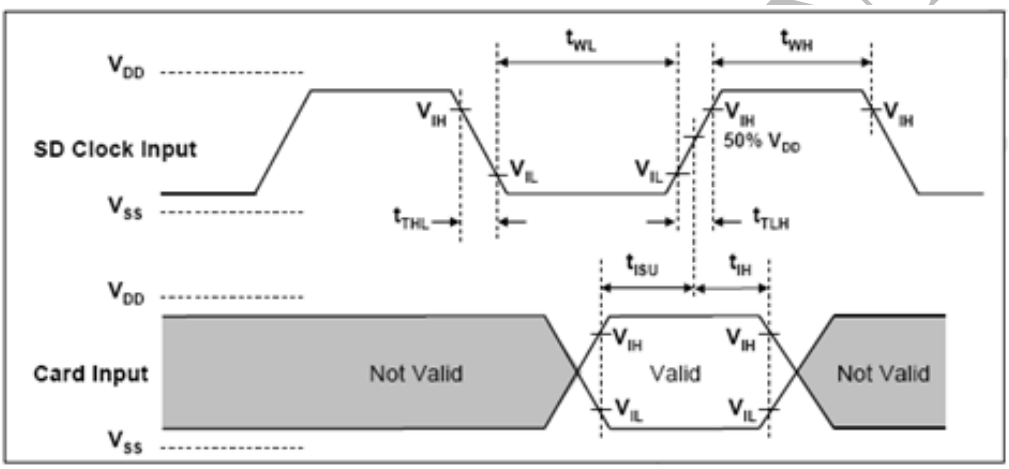
Card Output Timing (Default Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card}≤ 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	$0_{(1)}$/100	400	KHz	C_{card}≤ 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card}≤ 10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card}≤ 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card}≤ 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card}≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card}≤ 10 pF (1 card)

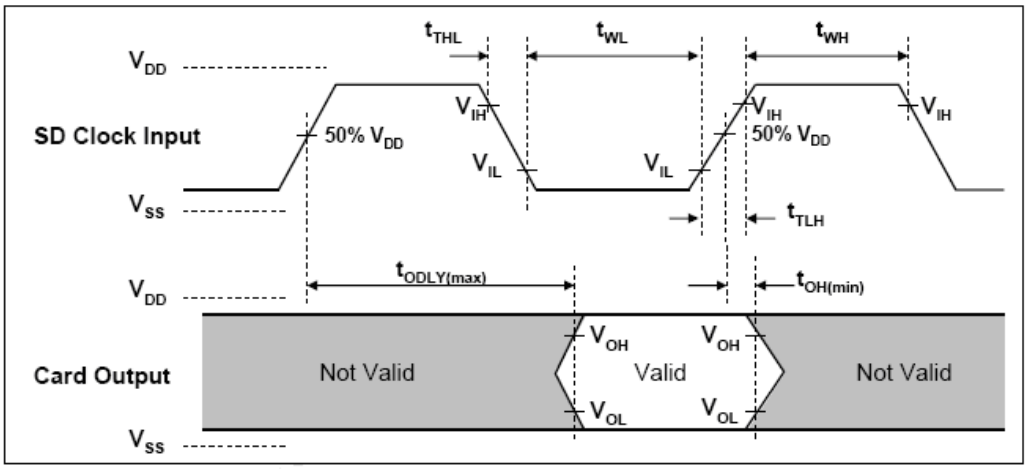
Input hold time	t_{IH}	5		ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L≤ 40 pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L≤ 40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continues clock is required.

4.2.2. SD Interface Timing (High-Speed Mode)



Card Input Timing (High Speed Card)



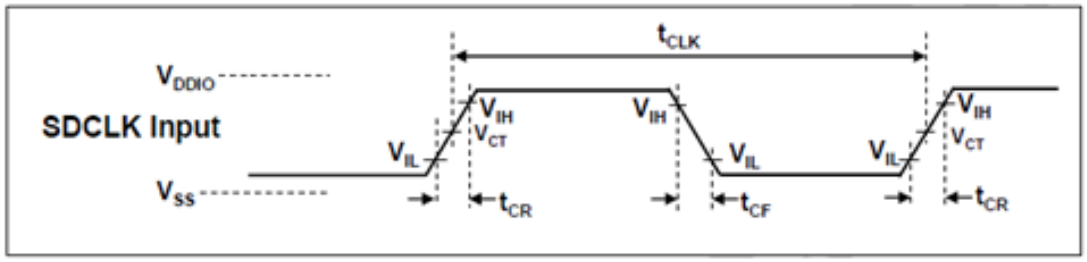
Card Output Timing (High Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{card} ≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L ≤ 40 pF (1 card)
Output Hold time	T_{OH}	2.5		ns	C_L ≤ 15 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL ≤ 15 pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

4.2.3. SD Interface timing (SDR12, SDR25, SDR50 and SDR104 Modes)

Input:

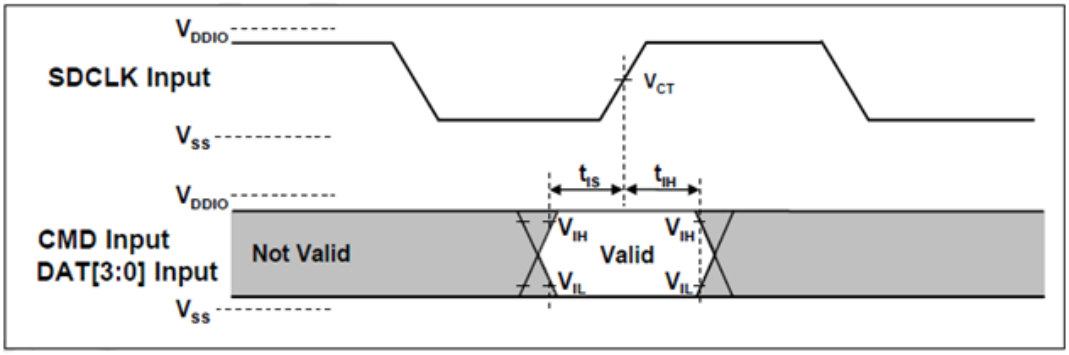


Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	

Clock Signal Timing

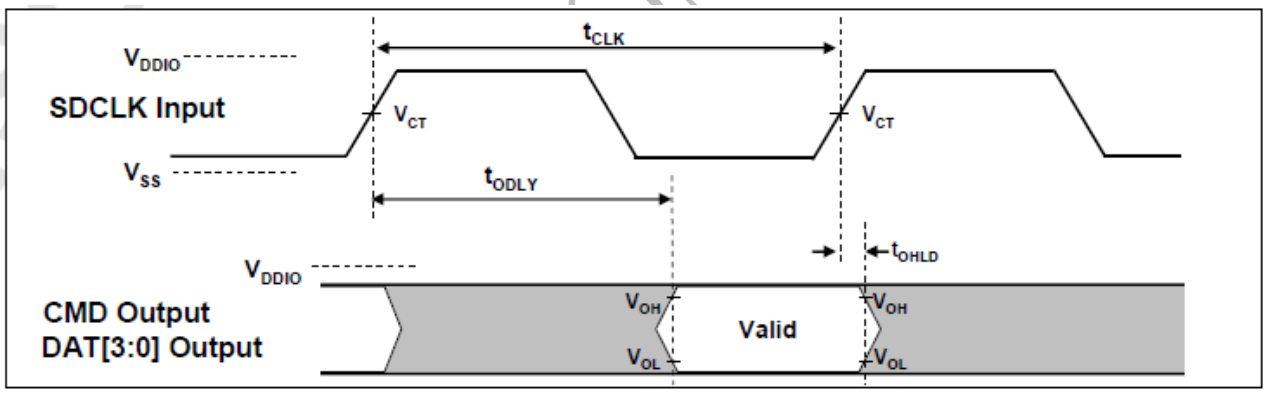
SDR12, SDR25, SDR50 and SDR104 Input Timing:



Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.8	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
t_{IS}	3.00	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.8	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V

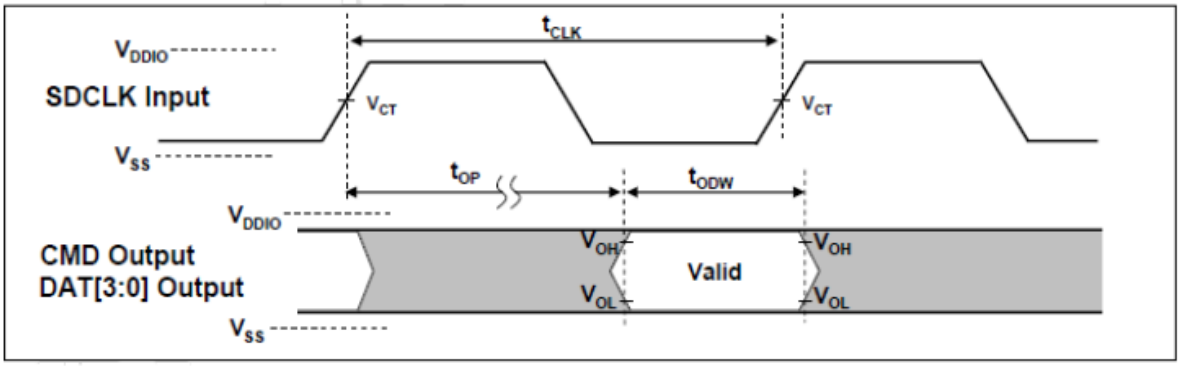
Output* (SDR12, SDR25, SDR50)*:



Output Timing of Fixed Data Window

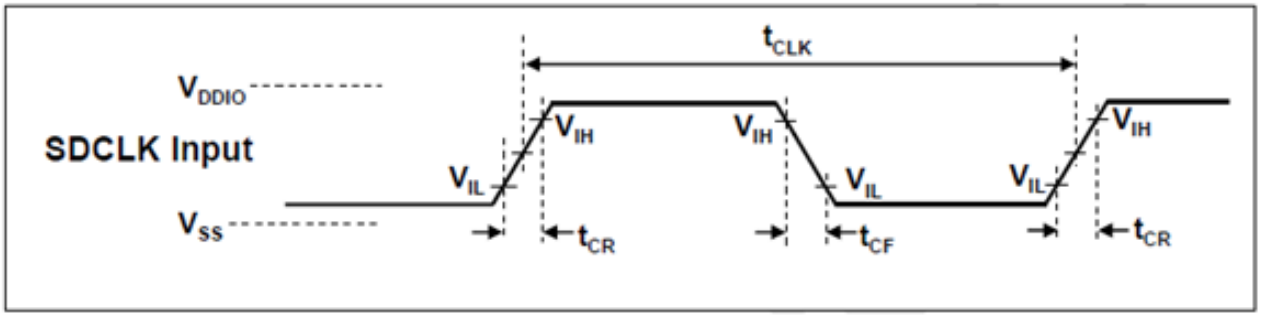
Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12,
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

Output (SDR104 Mode):



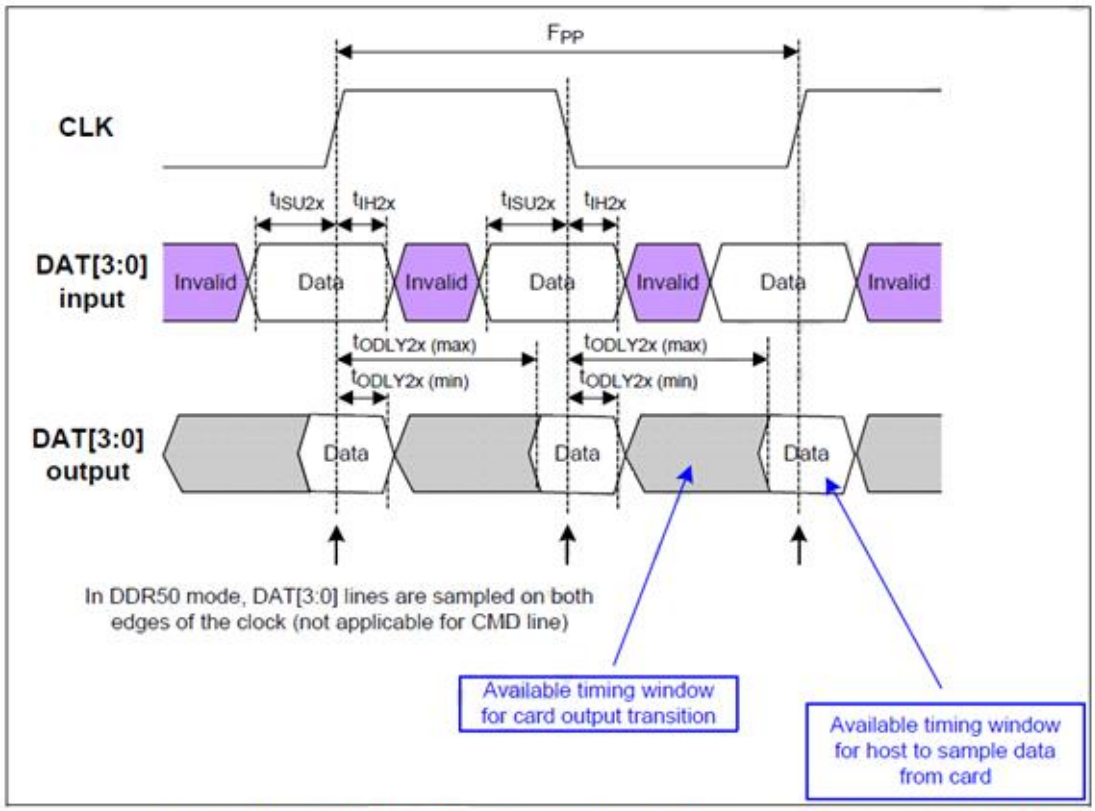
Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
$\triangle t_{OP}$	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

4.2.4. SD Interface timing (DDR50 Mode)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Bus Timings – Parameters Values (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_L≤ 30 pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	C_L≥ 15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤ 25 pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	C_L≥ 15 pF (1 card)

5. PAD ASSIGNMENT

5.1. Pad Assignment and Descriptions

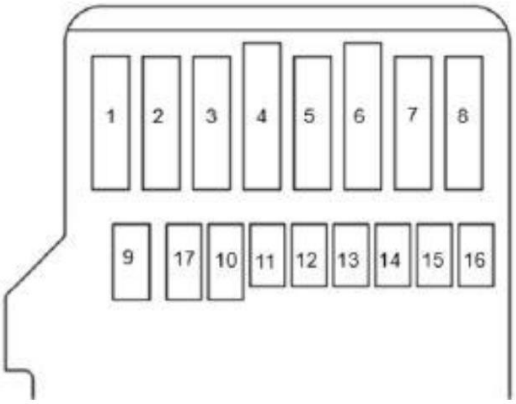


Table 5-1 1-Lane microSD Express Interface Memory Card Pad Assignment

pin	SD Mode			PCIe Mode		
	Name	Type[1]	Description	Name	Type	Description
1	DAT2	I/O	Data Line	DAT2/CLKREQ#	I/O	Data Line/Reference clock request signal.
2	CD/DAT3	I/O	Card Detect/Data Line	CD/DAT3/PERST#	I/O	Card Detect/Data Line/Power Enable Reset
3	CDM	I/O	Command/Response	CMD	I/O	Command/Response
4	V_{DD}	S	Supply voltage (3.3V)	V_{DD1}	S	Supply voltage (3.3V)
5	CLK	I	Clock	CLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O	Data Line	DAT0/REFCLK+	I/O	Data Line/PCIe Ref Clock
8	DAT1	I/O	Data Line	DAT1/REFCLK-	I/O	Data Line/PCIe Ref Clock
9	-	-	Not Used	V_{DD2}	S	Supply voltage (1.8V)
10	-	-	Not Used	V_{SS}	S	Supply voltage ground
11	-	-	Not Used	PCIe_Tx+	I	PCIe transmit lane
12	-	-	Not Used	PCIe_Tx-	I	PCIe transmit lane
13	-	-	Not Used	V_{SS}	S	Supply voltage ground
14	-	-	Not Used	PCIe_Rx-	O	PCIe receive lane
15	-	-	Not Used	PCIe_Rx+	O	PCIe receive lane
16	-	-	Not Used	V_{SS}	S	Supply voltage ground
17	-	-	Not Used	-	-	Not Used

(1) S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers; OD: I/O using Open Drain drivers; IDS: Input Differential Signal; ODS: Output Differential Signal.

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode as well while they are not used. It is defined so in order to keep compatibility to MultiMedia Cards.

(3) At power up, this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode, it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer with SET_CLR_CARD_DETECT (ACMD42) command.

(4) Pin2 and Pin5 shall not be kept open by host in PCIe Mode.

5.2. PCIe Bus

Refer to PCI Express standard defined by the PCI-SIG. The command layer used by the PCIe interface is NM Express(NVMe) and standard defined by the NVM Express.

6. REGISTERS

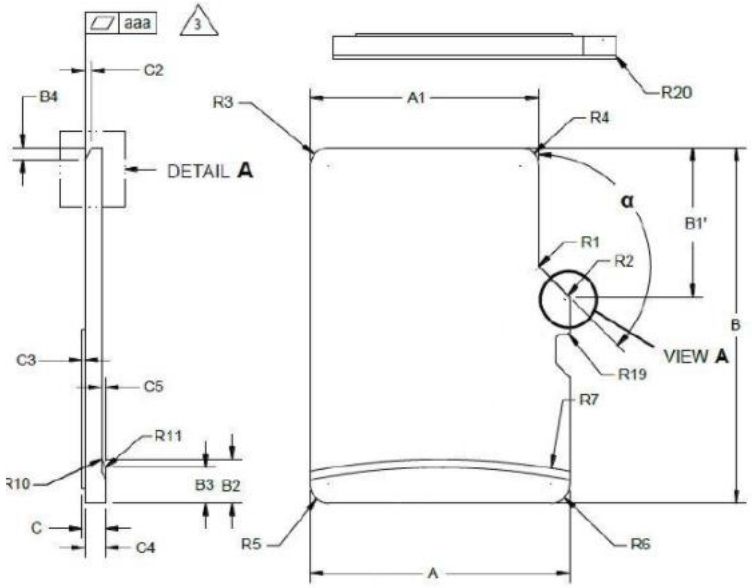
6.1. Card Register

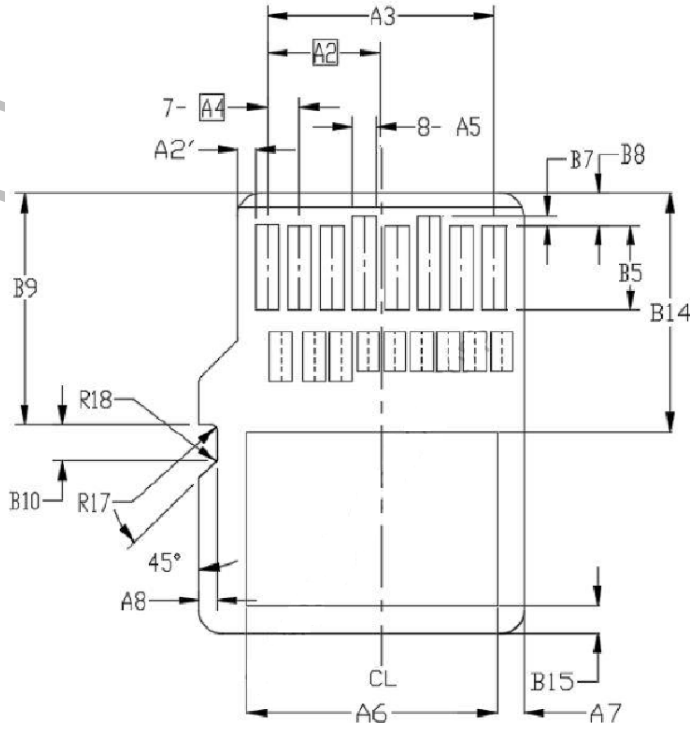
Name	Width	Description
CID	128bit	Card identification number; card individual number for identification.
RCA[1]	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization.
DSR	16bit	Driver Stage Register; to configure the card's output drivers.
CSD	128bit	Card Specific Data; Information about the card operation conditions.
SCR	64bit	SD Configuration Register; Information about the SD Memory Card's Special Features capabilities
OCR	32bit	Operation conditions register.
SSR	512bit	SD Status; Information about the card proprietary features.
CSR	32bit	Card Status; Information about the card status.

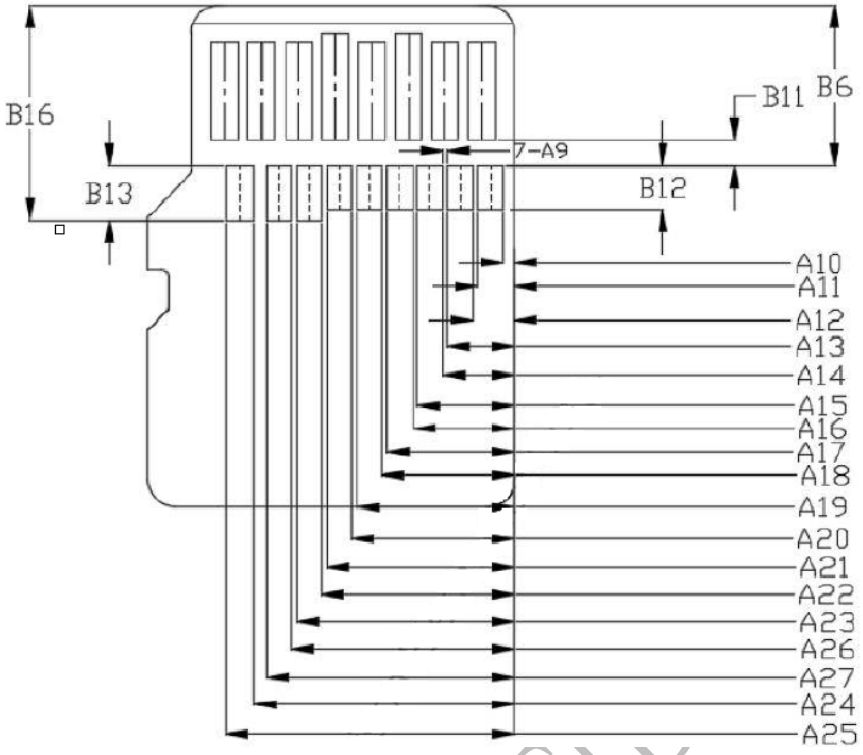
(1) RCA register is not used (or available) in SPI mode.

7. PHYSICAL DIMENSION

Dimension: 15mm(L) x 11mm(W) x 1mm(H)







	COMMON DIMENSION			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.05	-	-	
A10	0.25	0.35	0.45	
A11	1.01	1.11	1.21	
A12	1.16	1.26	1.36	
A13	1.92	2.02	2.12	
A14	2.07	2.17	2.27	
A15	2.83	2.93	3.03	
A16	2.98	3.08	3.18	
A17	3.74	3.84	3.94	
A18	3.89	3.99	4.09	
A19	4.65	4.75	4.85	
A20	4.80	4.90	5.00	
A21	5.56	5.66	5.76	
A22	5.71	5.81	5.91	
A23	6.47	6.57	6.67	
A24	7.75	7.85	7.95	
A25	8.55	8.65	8.75	
A26	6.62	6.72	6.82	
A27	7.38	7.48	7.58	
A28	-	-	0.50	
A29	-	-	0.50	
B	14.90	15.00	15.10	
B1'	6.13	6.23	6.33	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	-	4.75	4.85	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	7.80	7.90	8.00	REF
B10	1.10	1.20	1.30	
B11	-	0.75	-	
B12	-	1.35	-	
B13	-	1.65	-	
B14	9.00	-	-	
B15	0.10			
B16	-	6.40	6.50	
B17	11.40	11.50	11.60	
B18	-	-	0.50	
C	-	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
C4	0.80	-	1.10	
C5	0.15	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.60	0.80	0.90	
R6	0.60	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	4	-	0.15	
α	133°	135°	137°	
β	43°	45°	47°	
aaa	-	-	0.10	

Notes:
1. DIMENSIONS and TOLERANCING per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. COPLANARITY is additive to C1 MAX thickness.
4. All edges shall not be sharp as tested per UL1439 "Test for Sharpness of Edges on Equipment"
5. As B16 is related to connector specification, this length will be defined in next version.

8. ORDERING INFORMATION

Capacity	MPN
128GB	FDMM128GBC-5700
256GB	FDMM256GBC-5700

Revision History

Revision	Release Date	Description
1.0	2024/12	First release