Three-Phase Brushless Motor Gate Driver SBC

ATA6847 Data Sheet

Description (Submit Feedback)

The ATA6847 is a Three-Phase Brushless Motor Gate Driver System Basis Chip (SBC) for brushless motor control, designed using advanced SOI technology. In combination with a microcontroller and six discrete power MOSFETs, the SBC forms a brushless DC motor control unit. Through six dedicated parallel inputs, the gate driver units (GDU) can be controlled independently, supporting duty cycle operations from 0% to 100%, due to the implementation of two charge pumps, for low and high-side gate drives. In addition, the circuit provides 5V and 3.3V low dropout voltage regulators, two current-sensing operational amplifiers, an integrated Back-EMF detection module and a window watchdog. The microcontroller controls the ATA6847 using an SPI interface.

Features (Submit Feedback)

General

- Power Supply Voltage Range from 3V to 42V
- Sleep (Deep Sleep) Mode with Maximum 15 µA Current Consumption with Full Wake-up Capability (Local Wake-up)
- 3.3V or 5V Microcontroller Interface
- Up to 4 MHz SPI Bus for Device Configuration and Register Access
- SPI Frame Error Detection
- Dedicated NIRQ Pin for MCU External Interrupt in order to Report Events Directly
- Input-Output Reset Pin (NRES) with Variable Reset Length to Support a Wide Variety of Microcontrollers
- Package: QFN40 with Wettable Flanks and Exposed Pad

Motor Gate Driver Unit (GDU)

- VDH Motor Operating Voltage Range from 4.9V to 32V (Overvoltage Lockout Level)
  - VS Undervoltage
  - VDH Overvoltage Lockout selectable
- Individual Driving of Six External NMOS Transistors or Complementary Driving of Three Half Bridges with Three Pairs of PWM Input Pins
- Maximum Switching Frequency of 50 kHz with 100 nC Gate Charge per MOSFET
- Charge Pumps for Supporting Crank Pulse Voltage Operation and 100% PWM Duty Cycle Control
- MOSFET VGS Undervoltage Monitoring, Configurable Undervoltage Lockout Level
- MOSFET VDS Monitoring, Configurable Short Circuit Detection Levels
- Cross Conduction Protection Timer
- Programmable Deadtime Insertion or Adaptive Deadtime Control
- Failure Detection Blanking Time for All Protection Features
- Configurable Fault Filter Times for VGSUV, ILIM and SCP

Current Sense Amplifier (CSA)

- Two Integrated High-performance CSA with Configurable Gain and Output Offset
- One Advanced Power Stage Current Limitation Using OpAmp Output and Integrated DAC

Back-EMF Detection

- Back-EMF Feedback Detector Including Motor Neutral Point Emulation

Voltage Regulators

- VDD1 - 5V/3.3V, 100 mA
  - ±2% accuracy
  - Foldback short circuit limit (I_{VDD1} + I_{VDD2} = 105-135 mA)
  - Short-circuit protection
  - Undervoltage detection
  - Overvoltage protection and detection
- VDD2 - 3.3V, 70 mA
  - ±2% accuracy
  - Current limitation 75 mA
  - Short-circuit protection
  - Undervoltage detection
  - Overvoltage protection and detection
- High-voltage Output INH for Controlling an External Component, Like a Voltage Regulator (VDD2 Not Available in this Variant)

Watchdog

- Window and Time-out Modes
- Optional Cyclic Wake-up in Time-out Mode
- Configurable Period and Reset Pulse Length
- Limp Home (LH) - High-voltage Failure Output

Functional Safety Support

- ISO 26262:2018 Functional Safety Ready up to ASIL B
- IEC 61508:2010 Functional Safety Ready up to SIL 2

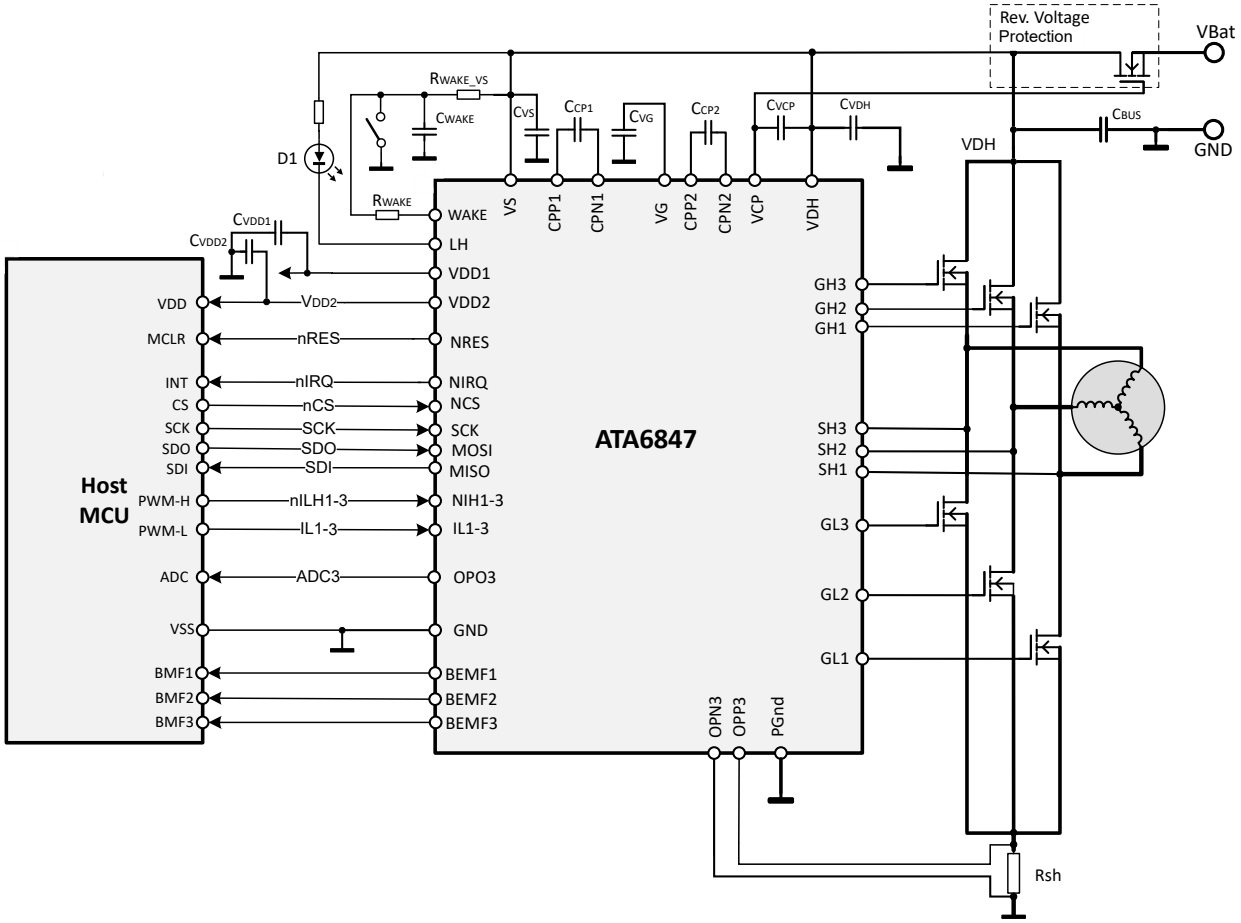
Applications (Submit Feedback)

- Home Appliances using BLDC Motor Control
- Power Tool Motors
- Hobby Aircraft, Boats, Drones or Vehicles

1. Typical Application Circuit(s) (Submit Feedback)

The typical application shows a B-EMF system configuration for a 6-step trapezoidal application and a shunt as a current limit sensor. The application circuit is also suited for a single-shunt FOC application, with the current limitation functionality of the single shunt and detect wind milling via the B-EMF sampler. The charge pump output (VCP) controls the reverse polarity protection N-channel MOSFET.

Figure 1-1. Typical Application Schematic: ATA6847



- R_{WAKE} = 2.7 kΩ
- C_{WAKE} = 100 nF
- R_{WAKE_VS} = 10 kΩ
- C_{VDD1} = C_{VDD2} = 2.2 µF
- R_{NRES} = R_{NIRQ} = 10 kΩ
- C_{VS} = 10 µF || 100 nF
- C_{VDH} = 47 µF || 100 nF
- C_{CP1} = 330 nF
- C_{CP2} = 220 nF
- C_{VG} = C_{VCP} = 3.3 µF

2. Product Family (Submit Feedback)

The name, features and package types of each device are listed in the following table. All devices integrate six dedicated parallel gate drivers and a B-EMF comparator.

Table 2-1. ATA6847 Family Overview

Product Name	VDD1 LDO (Note 1)	VDD2 LDO (Note 1)	INH	OpAmps / OpAmps+ B-EMF (Note 2)	OpAmp output rail, MCU interface voltage [VIO]	Package
ATA6847-5050	5V 100 mA	3.3V 70 mA		2 / 1 + 1	5V	40-VQFN
ATA6847-3333	3.3V 100 mA		x	2 / 1 + 1	3.3V	40-VQFN
ATA6847-5033	5V 100 mA	3.3V 70 mA		2 / 1 + 1	3.3V	40-VQFN

Notes:

1. Sum current (I_{VDD1} + I_{VDD2}) maximum 100 mA
2. Selectable via SPI:
   Two OpAmps or One OpAmp plus One B-EMF sampler

3. Block Diagram (Submit Feedback)

Figure 3-1. ATA6847-5050, ATA6847-5033

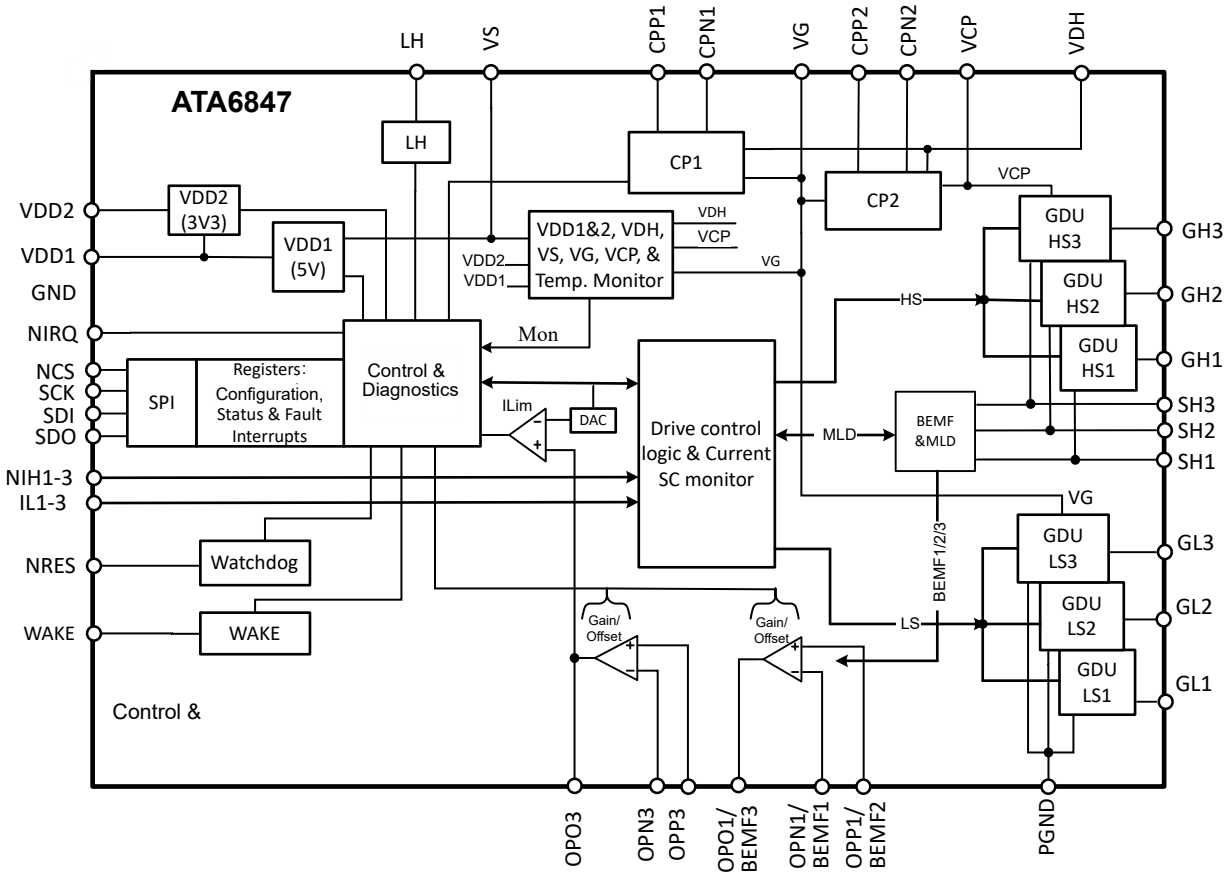
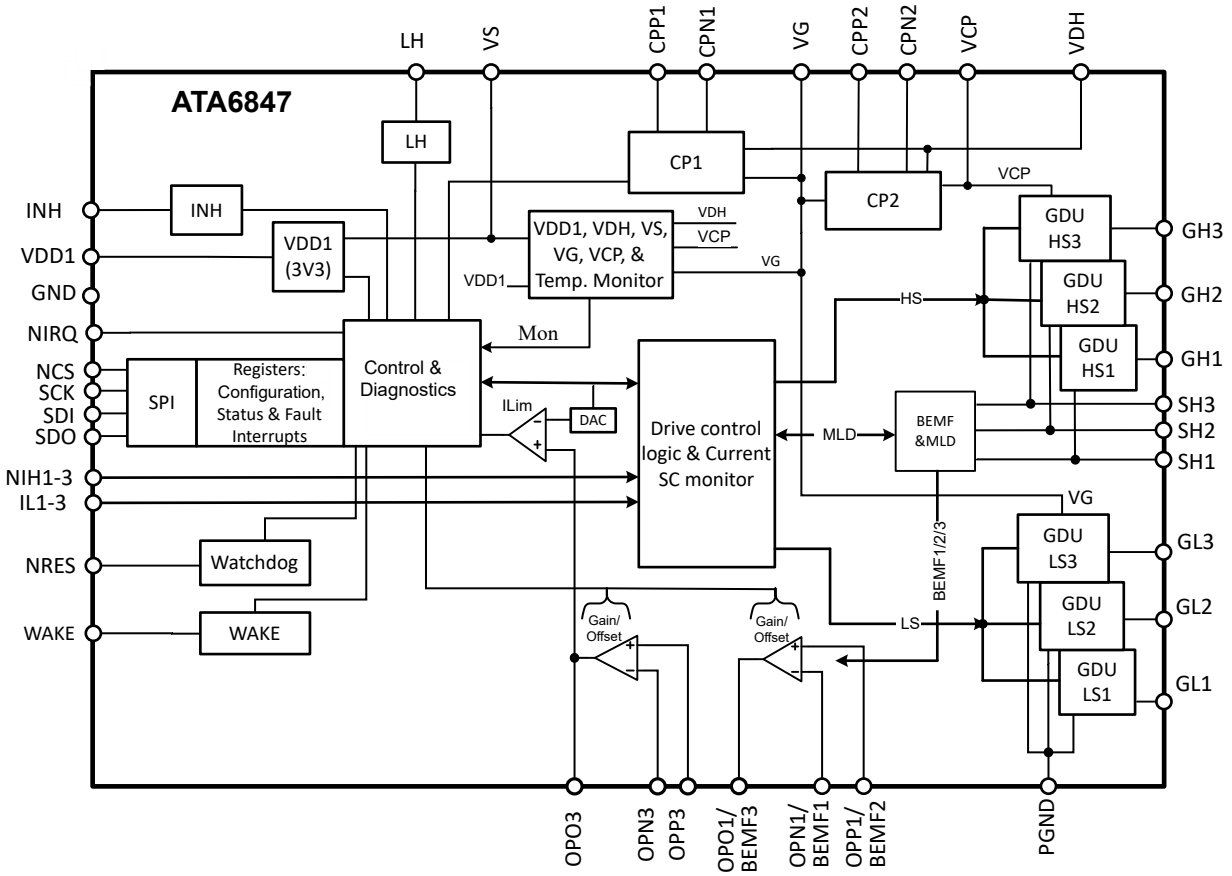


Figure 3-2. ATA6847-3333



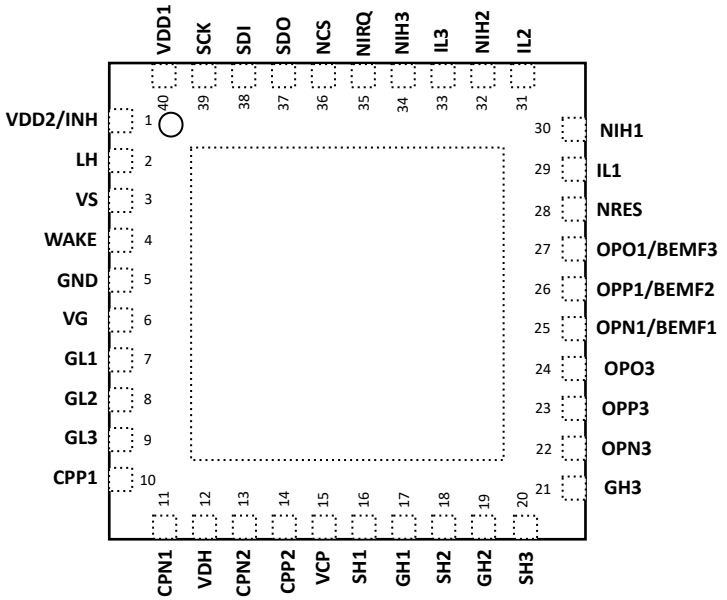
4. Pin Configuration (Submit Feedback)

Pin Name	40 Pin	Pin Description
VDD2 / INH	1	70 mA, 3.3V supply voltage/INH is the high-voltage output designed to control an external voltage regulator.
LH	2	Limp Home – High-voltage failure output, Open drain
VS	3	Battery supply pin
WAKE	4	High-voltage input for local wake-up
GND	5	LDO and analog ground
VG	6	12V gate drive regulator/charge pump 1 output
GL1	7	Gate driver output for low-side MOSFET, phase 1
GL2	8	Gate driver output for low-side MOSFET, phase 2
GL3	9	Gate driver output for low-side MOSFET, phase 3
CPP1	10	Charge pump 1 flying capacitor positive connection 1
CPN1	11	Charge pump 1 flying capacitor negative connection 1
VDH	12	Supply for VG and charge pump, high-side drain-source voltage monitoring reference, reference voltage level for charge pump 2 reservoir capacitor
CPN2	13	Charge pump 2 flying capacitor negative connection 2
CPP2	14	Charge pump 2 flying capacitor positive connection 2
VCP	15	Charge pump 2 reservoir capacitor, gate drive supply of high-side MOSFET gate drivers
SH1	16	Motor connection terminal 1 and phase 1 high-side MOSFET source terminal
GH1	17	Gate driver output for high-side MOSFET, phase 1
SH2	18	Motor connection terminal 2 and phase 2 high-side MOSFET source terminal
GH2	19	Gate driver output for high-side MOSFET, phase 2
SH3	20	Motor connection terminal 3 and phase 3 high-side MOSFET source terminal
GH3	21	Gate driver output for the high-side MOSFET, phase 3
OPN3	22	Current sense OpAmp 3 inverting input
OPP3	23	Current sense OpAmp 3 non-inverting input
OPO3	24	Current sense OpAmp 3 output
OPN1/ BEMF1	25	Current sense OpAmp 1 inverting input/B-EMF feedback phase 1
OPP1/ BEMF2	26	Current sense OpAmp 1 non-inverting input/B-EMF feedback phase 2
OPO1/ BEMF3	27	Current sense OpAmp 1 output/B-EMF feedback phase 3
NRES	28	Input/output pin for resetting microcontroller, pull-up to VIO, active low
IL1	29	Low-side digital driver input – use in direct control mode to activate GL1 or in complementary control mode as enable line for phase 1
NIH1	30	High-side digital driver input – use in direct control mode to activate GH1 or in complementary control mode as PWM input for phase 1, active low
IL2	31	Low-side digital driver input – use in direct control mode to activate GL2 or in complementary control mode as enable line for phase 2
NIH2	32	High-side digital driver input – use in direct control mode to activate GH2 or in complementary control mode as PWM input for phase 2, active low
IL3	33	Low-side digital driver input – use in direct control mode to activate GL3 or in complementary control mode as enable line for phase 3

.....continued		
Pin Name	**40 Pin**	**Pin Description**
NIH3	34	High-side digital driver input – use in direct control mode to activate GH3 or in complementary control mode as PWM input for phase 3, active low
NIRQ	35	Interrupt output, pull-up to VIO, active low
NCS	36	SPI chip-select, active low
SDO	37	SPI Serial Data Output
SDI	38	SPI Serial Data Input
SCK	39	SPI Clock Input
VDD1	40	100 mA, 5V/3.3V supply voltage
PGND	EP	Exposed Thermal Pad: Heat slug, general device ground

4.1 Package (Submit Feedback)

Figure 4-1. 40-VQFN (5x5x0.9 mm^3)



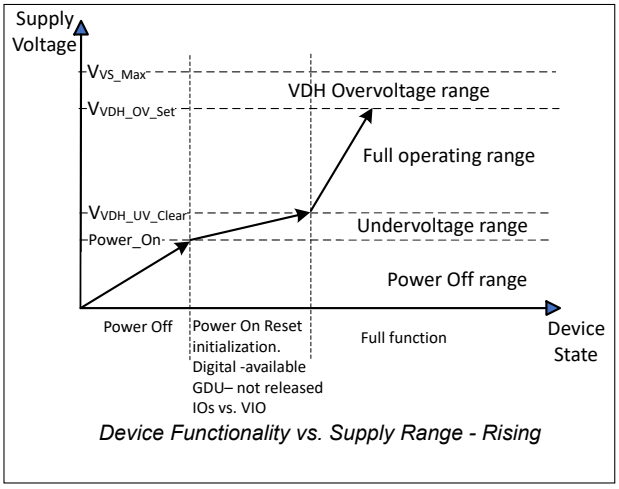
5. Functional Description (Submit Feedback)

Safe operation is assured by a wide variety of integrated diagnostic and protection features.

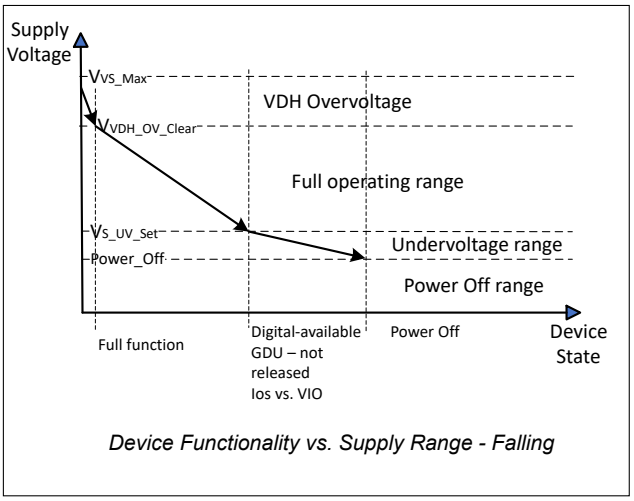
The device has a wide operating voltage range and offers several power-saving operating modes for battery-based applications.

5.1 Supply Voltage Range vs. Device Functionality (Submit Feedback)

Figure 5-1. Device Functionality vs. Supply Range



Device Functionality vs. Supply Range - Rising



Device Functionality vs. Supply Range - Falling

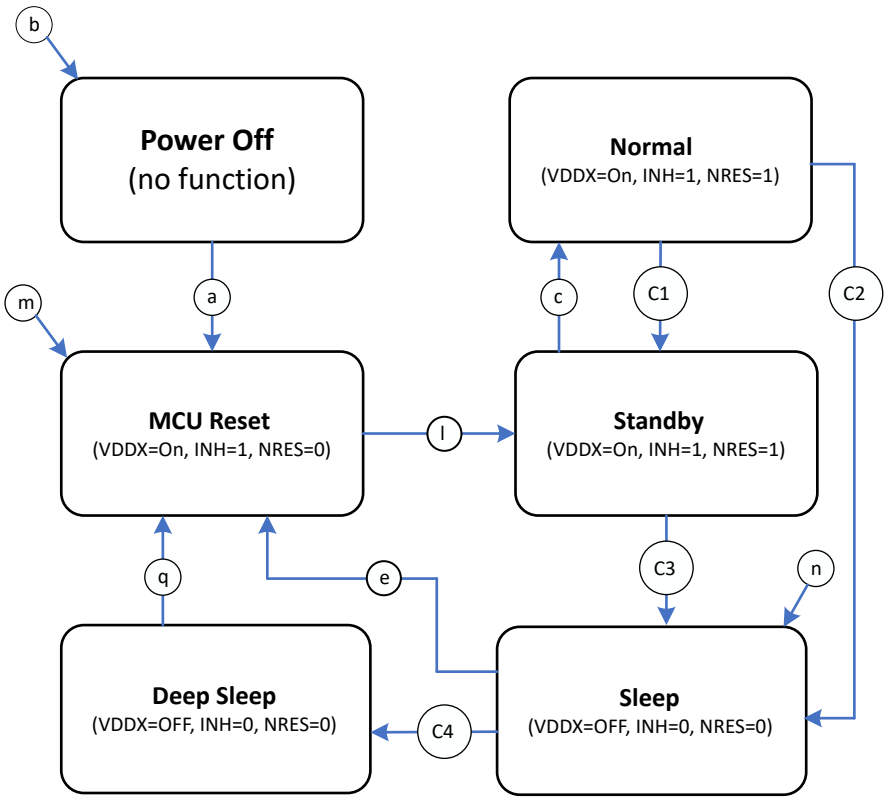
5.2 Device Operating Modes (Submit Feedback)

Initialization

The device mode control unit of the ATA6847 implements six different modes (see Device Operating Modes):

- MCU Reset
- Normal
- Power Off
- Standby
- Deep Sleep
- Sleep

Figure 5-2. Device Operating Modes (DOPM)



- a: $V_{VS} \geq V_{VS\_PWRON}$ (4.2V...4.55V)
- b: $V_{VS} < V_{VS\_PWROFF}$ (2.8V...3V)
- c: DOPM = Normal
- e: Wake-up/interrupt event
- f: DOPM = Standby
- g: DOPM = Sleep
- h: No wake-up and interupt event pending
- j: Illegal DOPM code configuration via SPI
- k: Number of enabled wake-up sources ≥ 1

- l:
  - ATA6847-5050: Reset pulse time expired **&** NRES not driven low externally **&** ((RSTLVL = 0 **&** $V_{VDD1} > V_{VDD1\_UV\_IO\_Clear}$) **||** (RSTLVL = 1 **&** $V_{VDD1} > V_{VDD1\_UV\_Clear}$))
  - ATA6847-3333: Reset pulse time expired **&** NRES not driven low externally **&** $V_{VDD1} > V_{VDD1\_UV\_IO\_Clear}$
  - ATA6847-5033: Reset pulse time expired **&** NRES not driven low externally **&** $V_{VDD2} > V_{VDD2\_UV\_IO\_Clear}$
- m:
  - ATA6847: Watchdog activated **&** any Reset event
  - ATA6847-5050: ($V_{VDD1} < V_{VDD1\_UV\_Set}$ **&** RSTLVL = 1) **||** $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$
  - ATA6847-3333: $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$
  - ATA6847-5033: $V_{VDD2} < V_{VDD2\_UV\_IO\_Set}$
  - ATA6847: NRES pulled low externally
- n: VDDIOOVSD = 1 **&** VDDIO overvoltage has been detected
- p: DOPM = Deep Sleep
- q: Local wake-up has been detected
- r: Local wake-up enabled

- C1 = f **||** j **||** g **&** (!h **||** !k)
- C2 = g **&** h **&** k
- C3 = (g **||** p **&** r) **&** h **&** k
- C4 = p **&** r

Notes: LH (Limp Home) will be activated in MCU Reset mode when:

- A watchdog failure event has been detected. (Watchdog timeout in Sleep mode will not activate LH.)
- The device enters MCU Reset mode due to a VDDx undervoltage event.
- VDDx undervoltage has been detected for longer than t_{Reset} after entering MCU Reset mode, triggered by (e).
- Mode switching triggered by condition a or q will not activate the LH pin.
- If DOPM = Normal mode and the CSCR [CSA1/3EN] bits are set, then CSA1/3 are enabled.

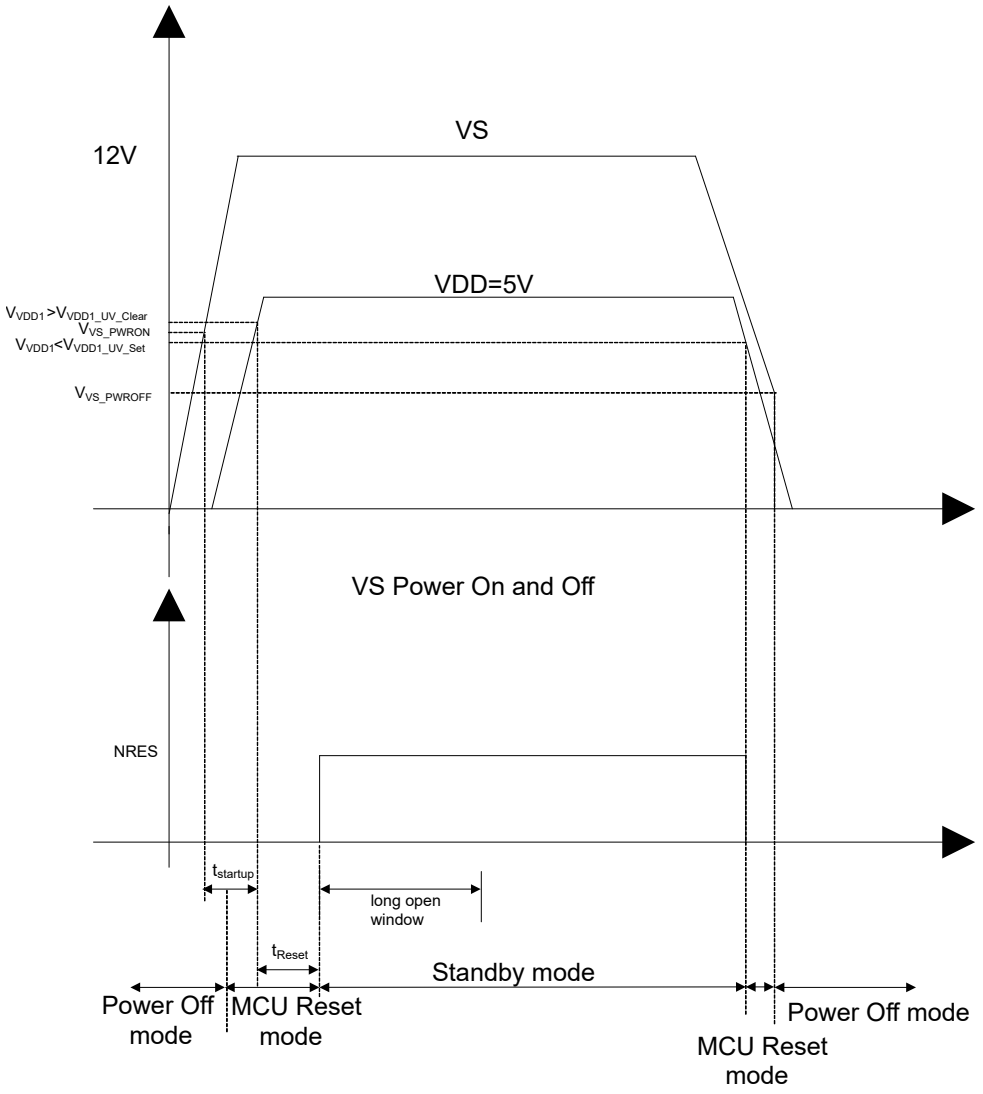
5.2.1 POWER OFF MODE (Submit Feedback)

The ATA6847 is in Power OFF mode as long as the supply voltage of the device (V_{VS}) is lower than the Power OFF Detection Voltage Threshold (V_{VS_PWROFF}).

- The watchdog is inactive.
- The LDO(s) is/are inactive.

As soon as V_{VS} rises above the Power ON Detection Threshold (V_{VS_PWRON}), the device starts transitioning to MCU Reset mode. The device is reset, initialized and the VDDx LDOs are enabled, see Figure 5-3, "Mode Switching During Power ON Start and Power OFF (ATA6847-5050, RSTLVL = ‘1’)".

Figure 5-3. Mode Switching During Power ON Start and Power OFF (ATA6847-5050, RSTLVL = '1')



5.2.2 MCU RESET MODE (Submit Feedback)

The MCU Reset mode is the default mode of the ATA6847 after a Power-on Reset. It is the Reset execution state of the device. This mode ensures that the NRES pin is pulled down for a defined time to allow the microcontroller to be reset in a controlled manner.

The INH pin, if available, is driven high.

In the MCU Reset mode, the gate drive unit is in GDU OFF mode. The SPI is disabled. All registers will be reset. If the mode transition was triggered by the NRES pin being driven externally, the SPI communication is disabled only until t_{Reset} expires. The LDO voltage regulators (VDDx) and the overtemperature detection are active. The watchdog is disabled.

In the MCU Reset mode, the DOPMCR Register cannot be programmed and is set to Standby.

The following events will cause the ATA6847 to transition to the MCU Reset mode:

- From Sleep mode or Deep Sleep mode after detecting a wake-up event or interrupt event.
- After a watchdog timeout or when the watchdog in the Window mode is triggered too early.

- An attempt is made to reconfigure the watchdog control register while the ATA6847 is in Normal mode.
- For the ATA6847-5050: If the RSTLVL bit in the DOPMCR register has been set to '1' and $V_{VDD1} < V_{VDD1\_UV\_Set}$
- For the ATA6847: $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$
- For the ATA6847-5050, ATA6847-5033: $V_{VDD2} < V_{VDD2\_UV\_IO\_Set}$

5.2.2.1 MCU Reset Mode and VDD Undervoltage Events (Submit Feedback)

For ATA6847-5050, if the RSTLVL bit is set to '1' (default), the device will enter MCU Reset mode after detecting a VDD1 undervoltage ($V_{VDD1} < V_{VDD1\_UV\_Set}$).

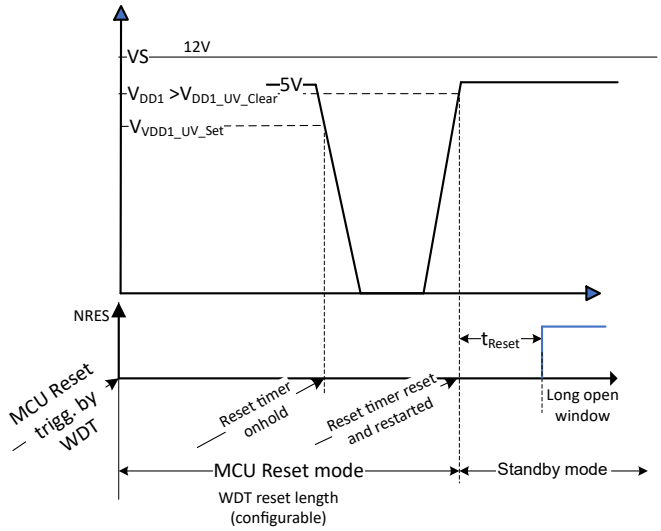
The device will stay in the MCU Reset mode until VDD1 recovers ($V_{VDD1} > V_{VDD1\_UV\_Clear}$) and then resets, restarting the Reset pulse length timer.

If VDD1 undervoltage is detected when the device is in MCU Reset mode, the Reset pulse length timer will remain on hold until VDD1 recovers and will then be reset and restarted.

The ATA6847 device will leave the MCU Reset mode and enter Standby mode after the t_{Reset} time expires (see Device Operating Modes).

For ATA6847-3333 or ATA6847-5050, when the RSTLVL bit is set to '0', the device will enter MCU Reset mode only after Power-on start-up, after detecting a Watchdog Reset event, or after detecting $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$. In this case, the device will start the Reset pulse length timer after the device enters the MCU Reset mode and $V_{VDD1} > V_{VDD1\_UV\_IO\_Clear}$ has been detected. As soon as the timer has expired, the device will transition to Standby mode.

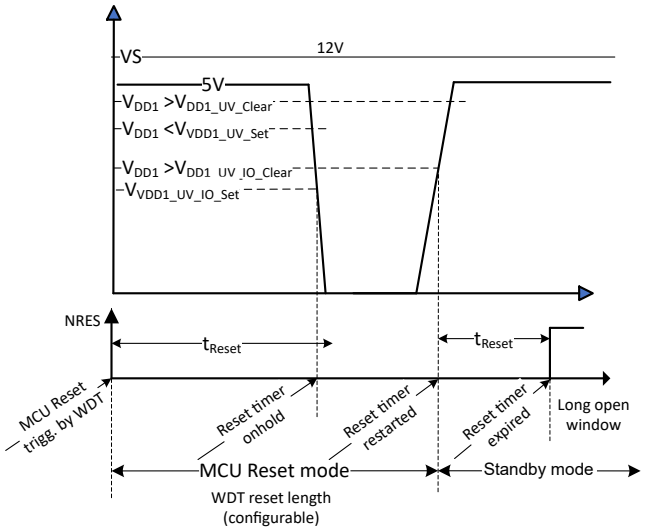
Figure 5-4. VDD1 undervoltage ($V_{VDD1} < V_{VDD1\_UV\_Set}$) in the MCU Reset mode, RSTLVL = '1', ATA6847-5050



5.2.2.2 Reset Input and Output (NRES) (Submit Feedback)

The NRES pin is asserted when the ATA6847 enters MCU Reset mode. The ATA6847 also enters MCU Reset mode when the NRES pin is pulled low externally. The ATA6847 can only exit the MCU Reset mode when the NRES pin is not driven "low" externally.

Figure 5-5. MCU Reset mode during VDD undervoltage ($V_{VDD} < V_{VDD\_UV\_IO\_Set}$) when, RSTLVL = '0', ATA6847-5050



5.2.3 STANDBY MODE (Submit Feedback)

In Standby mode, the gate drive unit is in GDU OFF mode. All available VDDx regulators are active. The INH pin, if available, is driven high. The watchdog is set to active by default.

A transition into Normal mode only can be achieved by setting the DOPM bits to '111'.

The ATA6847 provides various interrupt registers. Register bits (see SIR1 Register to SIR4 Register) are set to '1' by the device if a corresponding event has been detected. The detection of a wake-up or interrupt event is signaled via the NIRQ pin. The NIRQ pin voltage in high level (logic status '1') is the same as VIO voltage and will be forced to low (logic status '0') if an event has been captured and the corresponding interrupt mask bit is not set. The SPI interrupt registers can be read out to determine the corresponding trigger source.

The device will enter Standby mode in the following cases (see Device Operating Modes):

- From MCU Reset mode, after reset pulse length time expired.
- When DOPM is set to Sleep mode and a wake-up event occurs or all wake-up sources are disabled.
- From Normal mode, when DOPM is set to Standby mode via SPI.
- From Normal mode, when an invalid DOPM code was selected.

5.2.3.1 Watchdog during Standby Mode (Submit Feedback)

By default, the watchdog is activated when switching into Standby mode. The watchdog will start in Timeout mode by default. As a safety feature, the watchdog can **only** be configured in Standby mode. The intention is to avoid unwanted watchdog reconfiguration.

After start-up, the microcontroller is expected to initialize the ATA6847 registers. First, the microcontroller must write a valid watchdog trigger sequence (`WDTRIG = 0x55`).

5.2.4 SLEEP MODE (Submit Feedback)

In Sleep mode, all available VDDx regulators are deactivated. The INH pin (if available) is high ohmic. The gate drive unit is in GDU OFF mode (see GDU OPERATION MODES). The device reacts to local wake-up and system interrupt events.

The device exits Sleep mode if a local wake up (WAKE) is detected. It will also exit Sleep mode as soon as an interrupt event or a Watchdog Reset occurs.

The device will enter Sleep mode in the following cases (see Device Operating Modes):

- From **Normal Mode** or **Standby Mode** via the DOPM SPI command `010` = Sleep mode, if no wake-up event is pending and at least one wake-up source is enabled. All interrupt flags must be cleared before the device can enter Sleep mode.
- From all modes when a VIO overvoltage has been detected and the VDDIOOVSD bit is set to '1'.

5.2.5 DEEP SLEEP MODE (Submit Feedback)

The ATA6847 has the lowest current consumption in Deep Sleep mode. All functional blocks are deactivated, except for local wake up and VS Power OFF capture. The INH pin (if available) is high ohmic. All registers are reset.

The Deep Sleep mode can only be entered from Standby or Sleep mode, not directly from Normal mode.

Any interrupt must be cleared before entering Deep Sleep mode.

The local wake up (LOCWUE) must be activated.

Switching into Deep Sleep mode is initiated by setting the DOPM bits in the DOPMCR Register to `001` = Deep Sleep mode.

After detecting a wake-up event, the device is reset, initialized and enters MCU Reset Mode.
The wake-up event initiating the wake up out of the Deep Sleep mode will be registered in the corresponding registers (SIR1 and SIR5 registers).

5.2.6 NORMAL MODE (Submit Feedback)

In Normal mode, the ATA6847 provides full functionality. All available VDDx regulators are active. The INH pin (if available) is driven high.

Depending on the GDUOPM bits and failure detection status, the gate drive unit can be in GDU OFF, GDU Standby or GDU Normal mode (see GDU FSM in GDU OPERATION MODES).

5.2.7 DEVICE OPERATION MODE CONTROL REGISTERS (Submit Feedback)

Register 1: DOPMCR Register – Device Operation Mode Control Register (Address `0x01`)

Bit	7	6	5	4	3	2	1	0
	RSTLVL	**VDDIOOVSD**	—	—	—	**DOPM [2:0]**		
Read/Write	R/W	R/W	U	U	U	R/W	R/W	R/W
Initial Value	1	0	0	0	0	1	0	0

Bit 7 - **RSTLVL** ATA6847-5050: When set to '1', a VDD1 undervoltage ($V_{VDD1} < V_{VDD1\_UV\_Set}$) will trigger a mode switch to MCU Reset mode. When set to '0', $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$ will trigger a mode switch to MCU Reset mode.

This bit is unimplemented for ATA6847-3333 and ATA6847-5033.

Bit 6 - VDDIOOVSD The microcontroller should set the bit '1' to enable a VDD µC supply overvoltage shutdown when VDD (µC supply, the LDO connected to VIO) overvoltage has been detected. VDD µC supply:

- ATA6847-5050 / ATA6847-3333: VIO = VDD1
- ATA6847-5033: VIO = VDD2

Bits 5:3 - **Unimplemented.**

Bits 2:0 - **DOPM [2:0]** Select Device Operating mode (see Device Operating Modes):

'`3'b001`' = Deep Sleep mode

'`3'b010`' = Sleep mode

'3'b100' = Standby mode

'3'b111' = Normal mode

Other = invalid mode selection

5.3 Gate Drive Unit (GDU) (Submit Feedback)

5.3.1 GDU FEATURES (Submit Feedback)

The Gate Drive Unit connects three low-side gate drive outputs (GLx) and three high-side gate drive outputs (GHx) to three gate drive half bridges. For VGSUV monitoring, the high-side gate drivers use as reference the signals between the GHx and SHx pins, whereas the low-side gate drivers use as reference the signals between the GLx and GND pins.

The GDU monitors the voltage drop between drain and source of the MOSFET for short circuit events.

The Slew Rate Control unit optimizes EMC performance. This feature allows the control of the gate drive current injected into external MOSFET gates in four configurable levels. The slew rate of both high-side and low-side gate control are configurable individually to achieve the best trade-off between EMC performance and drive efficiency.

The module combines the following sub-modules:

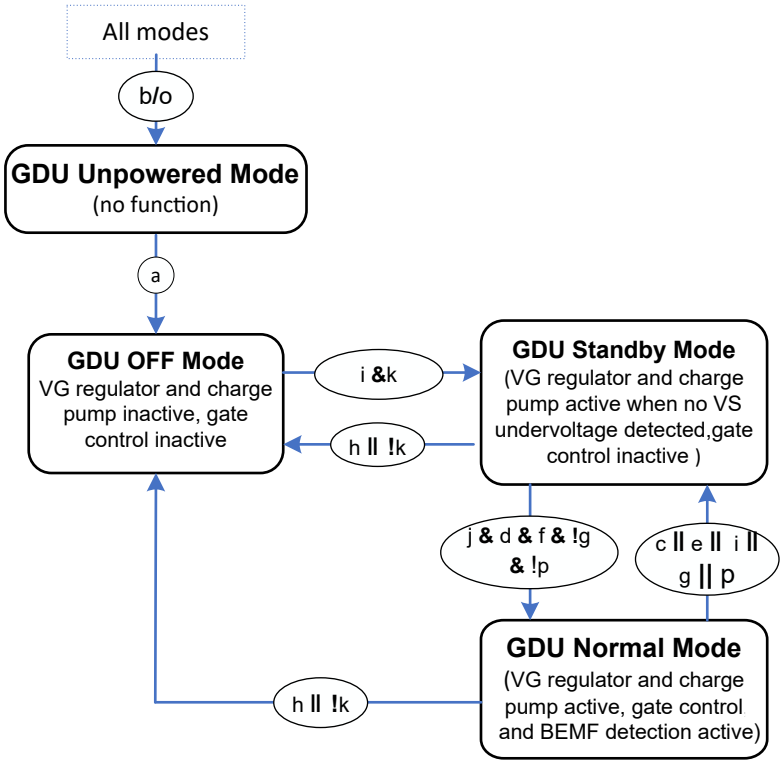
- High-side gate drive unit, including control logic, an adaptive dead-time unit, slew rate control unit, level shifter and gate driver
- Low-side gate drive unit, including control logic, an adaptive dead-time unit, slew rate control unit, level shifter and gate driver
- VDS monitoring unit
- Temperature monitoring sensors

5.3.2 GDU OPERATION MODES (Submit Feedback)

- **GDU OFF mode:** VG, VCP and Gate Control are deactivated.
- **GDU Standby mode:** VG and VCP are active as long as VS undervoltage has not been detected.
- **GDU Normal mode:** VG, VCP and Gate Control are active. Also, if selected, B-EMF is active.

The state diagram is illustrated below.

Figure 5-6. GDU Operating Modes



- a: Power-on Reset
- b: Device in Power Off ($V_{VS} < V_{VS\_PowerOFF}$)
- c: $V_{VG} < V_{VGS\_UV\_Set}$ || ($V_{VCP} - V_{VDH}$) < $V_{VGS\_UV\_Set}$, when VGS undervoltage monitoring is active.
- d: No VG and VCP detected
- e: $V_{VS} < V_{VS\_UV\_Set}$
- f: No VS undervoltage detected
- g: Any GDU related failure registered (overcurrent with ILIMSDEN=1 and/or short circuit event with CSDEN=1 and/or overtemperature shutdown, etc.)
- h: GDUOPM = GDU OFF mode
- i: GDUOPM = GDU Standby mode
- j: GDUOPM = GDU Normal mode and device is in Normal mode
- k: DOPM = Normal mode
- o: Device is in Deep Sleep mode
- p: VDH overvoltage & VDHOVSD = 1

Notes:

- VG and VCP are enabled at GDU transition from Off to Standby (default). The DSR1.GDUS flag is available if GDUOPM = Normal.
- CSA1/3 is available when DOPMCR.DOPM = Normal and CSCR.CSA1/3EN bits are activated.
- GDU = Normal mode can be written in any state of DOPM, but it will not be active if DOPM is switched in Normal mode while GDU = Normal. To activate the GDU, it is necessary to manually switch the GDU back into Standby, and then into Normal.

5.3.3 GDU OPERATION MODE CONTROL REGISTERS (Submit Feedback)

The GOPMCR register is a control register. Therefore, the state of GDU will not be mirrored to this register. GDUOPM bits only define the expected state of the transceiver. In addition to setting up the GDUOPM appropriately, all conditions for entering the corresponding GDU Operation modes must be fulfilled before the mode transition occurs. GDU can also leave the expected Operation mode if the conditions to stay cannot be fulfilled.

Register 2: GOPMCR Register – GDU Operation Mode Control Register (Address 0x03)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	**GDUOPM [2:0]**		
Read/Write	U	U	U	U	U	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	1

Bits 7:3 - Unimplemented.

Bits 2:0 - **GDUOPM [2:0]** Select GDU Operation mode, as shown below:

'3'b001' = GDU OFF mode

'3'b100' = GDU Standby mode

'3'b111' = GDU Normal mode

Other = Invalid mode selection

Register 3: GDUCR1 Register – GDU Control Register 1 (Address 0x05)

Bit	7	6	5	4	3	2	1	0
	CCPT [5:0]						**CCEN**	**BEMFEN**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	1	1	1	1	0

Bits 7:2 - CCPT [5:0] Cross conduction protection timer. The cross conduction protection time can be calculated as follows: t_{CC} = 100 ns × N, N = 0 to 63 [0x00 to 0x3F]. The role of CCPT is the prevention of shoot-through currents in the external MOSFET transistors (see CROSS CONDUCTION PROTECTION).

Bit 1 - CCEN Cross conduction protection enable bit. The CCEN bit enables the cross conduction protection feature. Disabling cross conduction protection leads to disabling both the cross conduction timer and adaptive dead-time generation. If CCEN is set to '0', "direct"/"complementary" Control mode is disabled (COMPEN = '0'). In this case, the MCU will generate PWM signals with the desired dead time between high side and low side.

Bit 0 - BEMFEN Back EMF comparator enable.

BEMFEN = '1' will activate Back EMF detection. The BEMF1, BEMF2 and BEMF3 pins are activated and signal the current ZCD state.

BEMFEN = '0' disables the Back EMF detection. The BEMFx pins are then released for OpAmp1 operation.

In case both the current sense amplifier '1' (CSA1EN = '1') and Back EMF comparator (BEMFEN = '1') are enabled, Back-EMF detection and current sense amplifier 1 will be disabled.

Register 4: GDUCR2 Register – GDU Control Register 2 (Address 0x06)

Bit	7	6	5	4	3	2	1	0
	HSOFF	**LSOFF**	**TSWTO**		**EGBLT**			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	1	0	0	0	1

Bit 7 - HSOFF - High-side gate driver inactive mode state. The microcontroller will set this bit to '0' if high-side gate drivers should become tri-state when GDU is in GDU Standby mode and will set the bit to '1' if high-side gate drivers should be driven low in GDU Standby mode.

Bit 6 - LSOFF - Low-side gate driver inactive mode state. The microcontroller will set this bit to '0' if low-side gate drivers should become tri-state when GDU is in GDU Standby mode and will set the bit to '1' if low-side gate drivers should be driven low in GDU Standby mode.

Bits 5:4 - TSWTO - Forces switch delay time control bits. For the definition of the delay, refer to CROSS CONDUCTION PROTECTION. Force to switch delay is set in ns, as shown below:

'2'b00' = 225

'2'b01' = 475

'2'b10' = 975

'2'b11' = 1975

Bits 3:0 - EGBLT - The edge blanking time control bits. The edge blanking time can be configured as shown in Current Limitation Detection/Short Circuit Detection Time. Edge blanking time starts after the cross conduction time expires and the corresponding gate control input becomes active (NIHx = '0' or ILx = '1'). VDS monitoring is blanked out during this time.

Register 5: GDUCR3 Register – GDU Control Register 3 (Address 0x07)

Bit	7	6	5	4	3	2	1	0
	ADDTHS		**ADDTLS**		**HSSRC**		**LSSRC**	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bits 7:6 - ADDTHS - Adaptive dead-time configuration bits (high side). Can be set as shown below:

'2'b00' = disabled

'2'b01' = 50-160 ns

'2'b10' = 150-210 ns

'2'b11' = 300-360 ns

Bits 5:4 - ADDTLS - Adaptive dead-time configuration bits (low side). Can be set as shown below:

'2'b00' = disabled

'2'b01' = 50-160 ns

'2'b10' = 150-210 ns

'2'b11' = 300-360 ns

Bits 3:2 - HSSRC - High-side slew rate control bits. Can be set as shown below (**Note 1**):

'2'b00' = Full speed

'2'b01' = 50% of full speed

'2'b10' = 25% of full speed

'2'b11' = 12.5% of full speed

Bits 1:0 - LSSRC - Low-side slew rate control bits. Can be set as shown below (**Note 1**):

'2'b00' = Full speed

'2'b01' = 50% of full speed

'2'b10' = 25% of full speed

'2'b11' = 12.5% of full speed

Note 1: Pay attention to the impact of the slew rate when handling negative voltage at phase pins.

Register 6: GDUCR4 Register – GDU Control Register 4 (Address 0x08)

Bit	7	6	5	4	3	2	1	0
	COMPEN	**VDHOVSD**	**UVVGSEN**	**UVVGSLVL**	**VGSUVFLT [3:0]**			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	1	1	1	1	0	0	0

Bit 7: COMPEN - Complementary control enable bit. The microcontroller shall set this bit to '1' if the complementary control of external MOSFETs is activated and set this bit to '0' if the external MOSFETs are controlled individually (direct) with the six gate control input signals (NIHx and ILx).

Bit 6: VDHOVSD - VDH overvoltage shutdown enable bit. The microcontroller shall set this bit to '1' when a VDH overvoltage event triggers a shutdown of the VG and VCP regulator (triggers transition from GDU Normal mode to GDU Standby mode). The microcontroller shall set this bit to '0' if a VDH overvoltage event will not trigger a shutdown of VG and VCP regulator.

Bit 5: UVVGSEN - VGS undervoltage detection enable bit. The microcontroller shall set this bit to '1' when VGS monitoring is active and set the bit to '0' when it is not. Effectively, the bit enables/disables both VCP and VG monitoring.

Bit 4: UVVGSLVL - VGS/VG undervoltage detection level selection. The microcontroller shall set this bit to '1' when the higher detection level ($V_{VGS\_UV\_Set\_H}$) is used and set this bit to '0' if the lower detection level ($V_{VGS\_UV\_Set\_L}$) is used.

Bits 3-0: VGSUVFLT [3:0] - VGS undervoltage filter time ($t_{VGS\_UV\_Blank}$). The filter time can be configured as follows: 770 ns × N, N = 1 to 16 [0x0 to 0x0F]. Filter time starts after an undervoltage event has been detected (comparator output changes to high). If VG and VCP voltage rise above the detection threshold during filter time, filter time will be reset and it will be restarted after VGS undervoltage occurs again.

Table 5-1. Current Limitation Detection/Short Circuit Detection Time

ILIMFLT [3:0], SCFLT [3:0], EGBLT [3:0]	Blanking/Filter time (ns), typical (±5%)
4'b0000	0
4'b0001	250
4'b0010	500
4'b0011	750
4'b0100	1000
4'b0101	1250
4'b0110	1500
4'b0111	1750

.....continued

ILIMFLT [3:0], SCFLT [3:0], EGBLT [3:0]	Blanking/Filter time (ns), typical (±5%)
4'b1000	2000
4'b1001	2500
4'b1010	3000
4'b1011	3500
4'b1100	4000
4'b1101	5000
4'b1110	6000
4'b1111	8000

5.4 Charge Pumps (CP1 and CP2) (Submit Feedback)

The ATA6847 supports 100% duty cycle operation by using two charge pumps. CP1 supplies the low-side gate drivers. Its input voltage is generated from the battery supply pin VDH. CP2 supplies the high-side gate drivers. It is generated out of the charge pump output of VG. Each charge pump (CP1 and CP2) charges from its input supply via an external flying capacitor into an external storage capacitor. VG is the output pin of CP1, whereas VCP is the output pin of CP2.

After the GDU transition into Standby mode, CP1 is turned on if VS < VCP_START and turned off if VS > VCP_STOP. In case VS > VCP_STOP, a 12V LDO has been included to limit VG voltage to 12V.

The second charge pump, CP2, provides the high-side gate driver biasing, being active when the GDU is in Standby or Normal mode.

The module monitors the output voltages and delivers the undervoltage detection event, notified in the SIR3 Register, VCPUV and VGUV bits.

CP2 output may serve as a control output pin for a reverse voltage polarity protection MOSFET, see Figure 1-1.

5.5 Low Dropout Voltage Regulator (VDD1) (Submit Feedback)

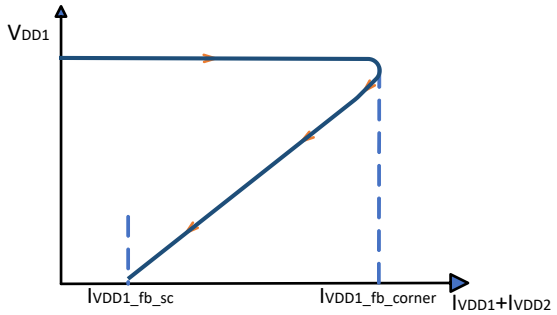
Depending on the product, the VDD1 pin has a nominal voltage output level of 5V or 3.3V, see Product Family.

The voltage regulator needs an external capacitor to compensate and smooth any disturbances. It is recommended to use an MLC capacitor connected in parallel to a 100 nF ceramic capacitor.

During a short circuit at VDD1, the output current is limited to $I_{VDD1\_fb\_sc}$. In case the LDO temperature exceeds the T_{OT_sdwn} threshold, the VDD1 output will be switched off. As soon as the junction temperature decreases below $T_{OT\_release}$, the regulator will be switched on again.

Exceeding the maximum sum load current of VDD1 and VDD2 [I_{VDD1} + I_{VDD2}] beyond the output current foldback corner threshold $I_{VDD1\_fbcorner}$ leads to a current limitation of LDO1. The current is getting limited down to the foldback short circuit limit $I_{VDD1\_fb\_sc}$ with decreasing load resistance. This feature reduces the dissipated power in overloading or short circuit conditions, and prevents LDO damage. This principle is illustrated in the Principle Foldback Current Waveform (Figure 5-7).

Figure 5-7. Principle Foldback Current Waveform



A proper connection between the exposed pad and a heat sink is recommended for sufficient power dissipation.

If the supply voltage (VS) is below the nominal output voltage of VDD1, the foldback current limitation is disabled and replaced with the standard current limitation ($I_{VDD1lim}$).

5.6 Low Dropout Voltage Regulator (VDD2) (Submit Feedback)

ATA6847-5050, and ATA6847-5033 provide a voltage regulator with an output voltage of V_{VDD2} = 3.3V. The VDD2 is powered from the 5V output of the VDD1 regulator. The maximum output current is limited to $I_{VDD2lim}$.

The ATA6847-3333 provides an inhibit output pin, **INH**. The purpose of the INH pin is to control external devices, such as external voltage regulators.

When inactive, the INH pin output level is high ohmic. When active, the INH voltage is on VS level.

5.7 Current Sense Amplifier (CSA) (Submit Feedback)

The ATA6847 provides two fully integrated operational amplifiers, tailored for measuring power stage currents by sensing currents across the shunt resistors. The gain and output offset voltage are configurable by setting the corresponding bits in the CSCR register via the SPI interface.

Optionally, the CSAs can be disabled.

The CSA output voltage range is adapted to the VIO voltage.

The CSA3 output voltage can be monitored with the ILim module, see OUTPUT CURRENT LIMITATION.

Register 7: CSCR Register – Current Sensing OpAmp Control Register (Address 0x0C)

Bit	7	6	5	4	3	2	1	0
	CSA3EN	—	**CSA1EN**	—	**OFFSET**		**GAIN**	
Read/Write	R/W	U	R/W	U	R/W	R/W	R/W	R/W
Initial Value	1	0	1	0	0	0	0	0

Bit 7 - CSA3EN Enable current sense amplifier 3. The CSA is enabled when the device is in Standby/Normal mode and the corresponding enable bit is set to '1'. All current sense amplifiers will need a maximum of 20 µs to settle their output voltage after the enable signal is set to '1'.

Bit 6 - Unimplemented.

Bit 5 - CSA1EN Enable current sense amplifier 1. The CSA is enabled when the device is in Standby/Normal mode and the corresponding enable bit is set to '1'. If current sense amplifier 1 (CSA1EN = '1') is enabled and BEMFEN (in GDUCR1) is enabled, then both Back EMF detection and current sense amplifier 1 will be disabled. All current sense amplifiers will need a maximum of 20 µs to settle their output voltage after the enable bit is set to '1'.

Bit 4 - Unimplemented.

Bits 3:2 - OFFSET Current sensing amplifier output offset set point.

'2'b00'= V_{VIO}/16

'2'b01'= V_{VIO}/8

'2'b10'= V_{VIO}/4

'2'b11'= V_{VIO}/2

Bits 1:0 - **GAIN** Current sensing OpAmp gain set point.

'2'b00'= 8

'2'b01'= 16

'2'b10'= 32

'2'b11'= 64

5.8 Back EMF Sampler and Back EMF Detection (Submit Feedback)

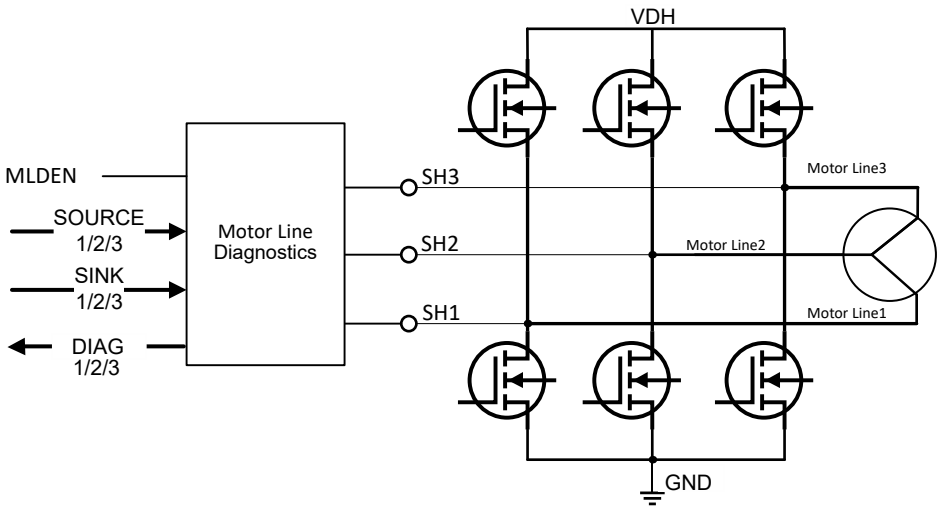
The ATA6847 comes with a fully-integrated B-EMF detection module, which converts the motor phase voltages into digital feedback signals. The B-EMF unit includes a resistor network and three high-speed, Zero-Cross Detection comparators (ZCD). The scaled phase signals VSHx are compared with the emulated motor neutral point voltage for estimating the virtual zero crossing. The ZCD comparator outputs provide three digital feedback signals via the BEMF1, BEMF2 and BEMF3 pins.

B-EMF detection is activated using the GDUCR1 Register.

5.9 Motor Line Diagnostics (Submit Feedback)

While the motor is not in operation, the B-EMF module can be used for motor line diagnostics. GDU must be in GDU Standby mode. Motor line (SHx) short to GND, short to VDH and open load can be evaluated, see Motor Line Diagnostics Setup. The MLDCR register is used to control the motor line diagnostics. As soon as the diagnostics are activated, the outputs of the diagnostics comparators will continuously update the MLDRR register. Enabling the motor line diagnostics disables the NIHX and ILx PWM input pins.

Figure 5-8. Motor Line Diagnostics Setup



Motor Line Short to GND and Supply Test and Motor Line Open Connection Test show the motor clamp short to GND, short to V_{BUS} or open load failure detection.

Figure 5-9. Motor Line Short to GND and Short to VDH Test

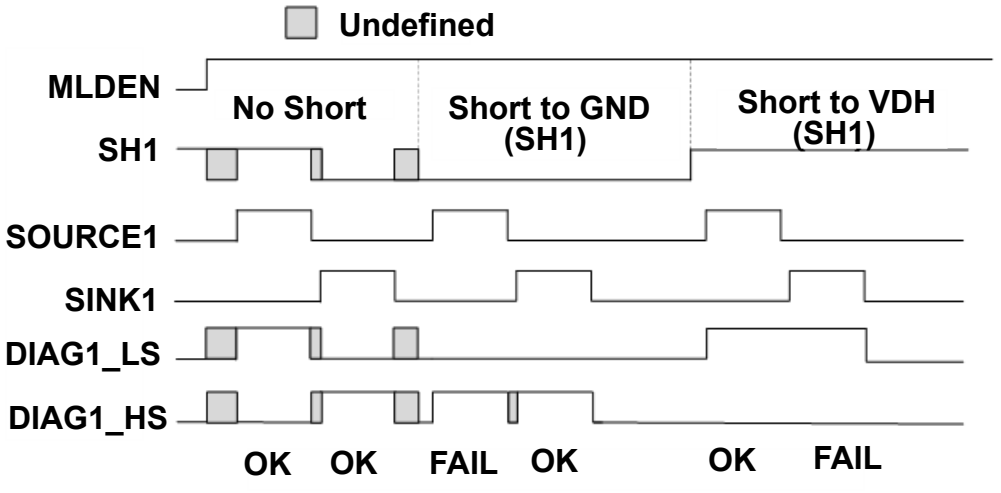
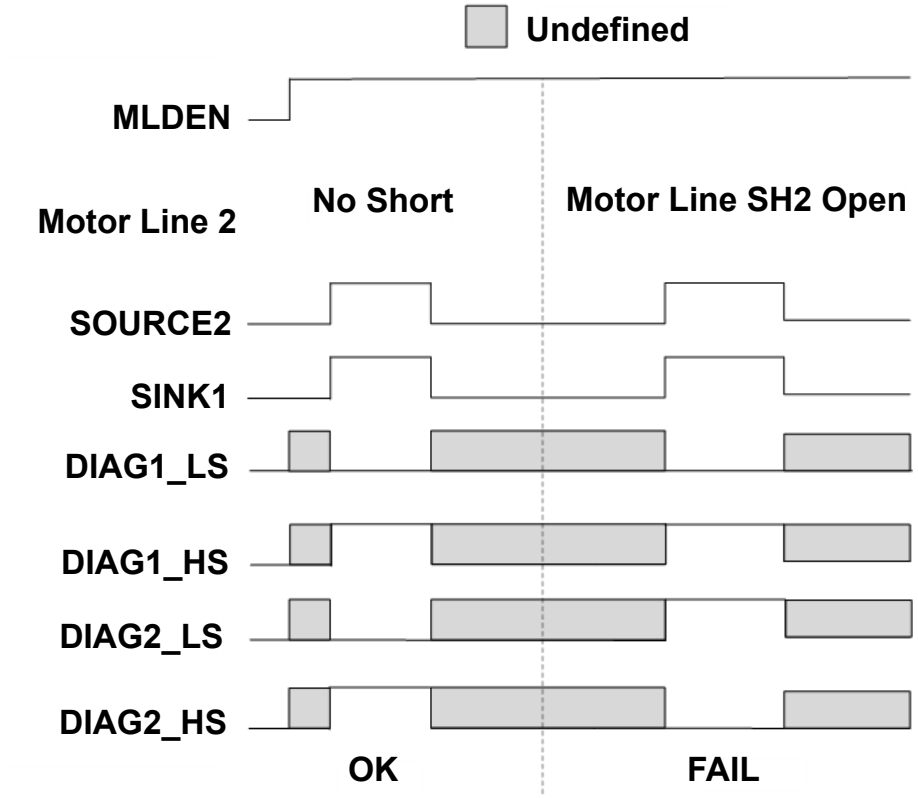


Figure 5-10. Motor Line Open Load Test.



A sufficient delay time is required before evaluating the MLDRR register, accounting for parasitic board and power MOSFET capacitances, and limited current capability of the diagnostics current sources.

Motor line diagnostics can be activated when VS is within the valid operating range, the ATA6847 is in Normal mode and the GDU is in GDU Standby mode.

5.9.1 MOTOR LINE DIAGNOSTICS CONTROL REGISTERS (Submit Feedback)

Register 8: MLDCR Register – Motor Line Diagnostics Control Register (Address 0x0E)

The motor line diagnostics circuitry is controlled by the MLDCR register.

Bit	7	6	5	4	3	2	1	0
	—	**SOURCE3**	**SINK3**	**SOURCE2**	**SINK2**	**SOURCE1**	**SINK1**	**MLDEN**
Read/Write	U	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 - Unimplemented.

Bit 6 - SOURCE3 Enables source current source 3 if SOURCE3 = '1' and disables source current Source 3 if SOURCE3 = '0'.

Bit 5 - SINK3 Enables sink current source 3 if SINK3 = '1' and disables sink current Source 3 if SINK3 = '0'.

Bit 4 - SOURCE2 Enables source current source 2 if SOURCE2 = '1' and disables source current Source 2 if SOURCE2 = '0'.

Bit 3 - SINK2 Enables sink current source 2 if SINK2 = '1' and disables sink current Source 2 if SINK2 = '0'.

Bit 2 - SOURCE1 Enables source current source 1 if SOURCE1 = '1' and disables source current Source 1 if SOURCE1 = '0'.

Bit 1 - SINK1 Enables sink current source 1 if SINK1 = '1' and disables sink current Source 1 if SINK1 = '0'.

Bit 0 - MLDEN Enables (MLDEN = '1', default) and disable (MLDEN = '0') motor-line diagnostics only in GDU Standby mode.

Register 9: MLDRR Register – Motor Line Diagnostics Results Register (Address 0x12)

The motor-line diagnostics results can be read from the MLDRR register. The register is accessed via SPI. The results are available after each change in the MLDCR register.

Bit	7	6	5	4	3	2	1	0
	—	—	**DIAG3_HS**	**DIAG3_LS**	**DIAG2_HS**	**DIAG2_LS**	**DIAG1_HS**	**DIAG1_LS**
Read/Write	U	U	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

Bits 7:6 - Unimplemented.

Bits 5:0 - DIAGx_HS, DIAGx_LS Diagnostics results register bits. Interpret the results as described in Motor Line Short to GND and Short to VDH Test and Motor Line Open Load Test.

5.10 Wake-up Sources (Submit Feedback)

5.10.1 LOCAL WAKE-UP VIA WAKE PIN (Submit Feedback)

The ATA6847 provides a high-voltage input pin (WAKE) with the purpose of waking up the device.

The local wake up is active after enabling it via the LOCWUE bit.

A local wake-up request is detected when a falling edge has been detected on the WAKE pin and the logic level on the pin has been stable for at least t_{local_wu}. The event will be signaled via the NIRQ pin in all Device Operation Modes (DOPM).

In Deep Sleep mode the local wake up is always active, independent of the LOCWUE bit value, as all SPI registers are cleared upon entering Deep Sleep mode. However, Deep Sleep mode cannot be entered without LOCWUE = '1'.

5.10.2 WAKE-UP CONTROL REGISTER (Submit Feedback)

Register 11: WUCR Register – Wake-up Control Register (Address 0x04)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	**LOCWUE**
Read/Write	U	U	U	U	U	U	U	R/W
Initial Value	0	0	0	0	0	0	0	1

Bits 7:1 - Unimplemented.

Bit 0 - LOCWUE Local wake-up enable. Setting this bit to '1' will enable the local wake up via the WAKE pin, while setting the bit to '0' will disable it.

5.11 Watchdog (Submit Feedback)

The watchdog is used to monitor the proper function of the microcontroller and to trigger a Reset, if the microcontroller stops serving the watchdog due to a lock-up in the software or other malfunction. The NRES pin is pulled to Low when a watchdog Reset event is detected.

5.11.1 WATCHDOG BEHAVIOR DURING POWER-ON AND AFTER MCU RESET (Submit Feedback)

For a safe start-up, the microcontroller must issue a watchdog trigger command, followed by the configuration of the watchdog via the WDCR registers. Following this, the device enters Device Standby mode. As soon as the ATA6847 enters Standby mode, the watchdog starts with a long open window (t_{LW}). **Within this long open window, the watchdog must be triggered.** If the watchdog trigger is missing, the watchdog will generate a Reset via the NRES pin. In case of a correct first trigger within the long open window time, the watchdog starts its normal operation.

The watchdog cannot be disabled and configured in the following cases:

- After the power-on of the device and before it receives the first trigger in long open window mode.
- In all other cases when the watchdog is enabled and the device moves from MCU Reset mode to Standby mode, before the watchdog receives the first trigger.

If the WDLW bit from the Watchdog Control Register 1 is set to '1' (default value), the watchdog timer will always be reset when the Reset pulse time expires and starts the long open window after the device enters Standby mode. Otherwise, the watchdog will continue with its normal operation immediately, and skip the long window.

5.11.2 WATCHDOG REGISTERS AND FEATURES (Submit Feedback)

The built-in watchdog is activated by default and starts after powering on the device. The watchdog can be reconfigured or disabled only after power-on AND the first trigger.

The watchdog supports two operating modes:

- Window mode

  In Window mode, a watchdog trigger event within the watchdog trigger window resets the watchdog timer.

  The Window Mode is only available in Normal mode.

- Time-out mode

  In Time-out mode, the watchdog can be triggered any time within the trigger range by a watchdog trigger.

Figure 5-11. Window Watchdog in Window Mode

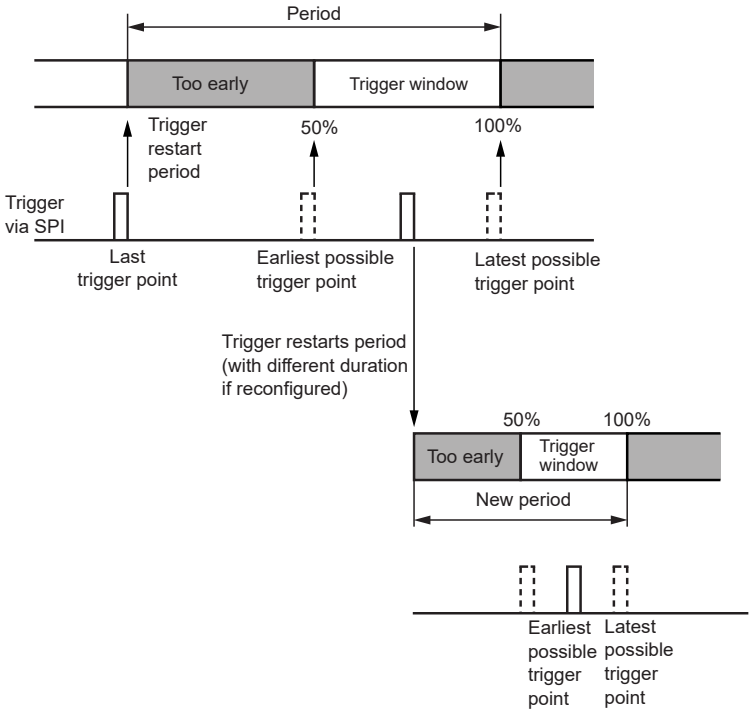
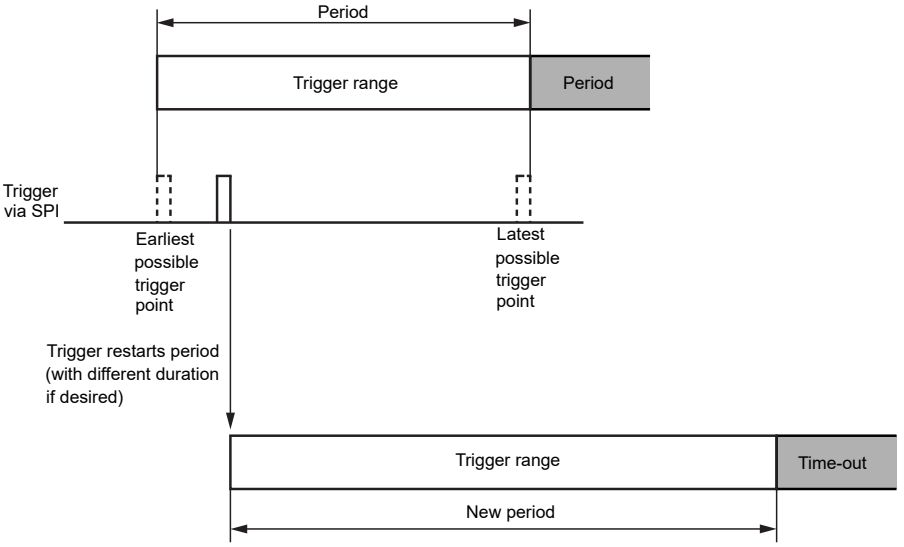


Figure 5-12. Window Watchdog in Time-out Mode



In order to avoid unwanted configuration of the watchdog, the ATA6847 only allows configuration of the watchdog (write access to WDCR1 and WDCR2 registers) when the device is in Standby mode.

Every write access to the WDCR1 and WDCR2 registers via SPI will reset the Watchdog Timer and immediately apply the changes.

If Window mode is selected (WDC = 100), the watchdog will remain in (or switch to) Time-out mode until the device enters Normal mode (Window mode is only supported when the device is in Normal mode).

Any attempt to configure the watchdog (write access to WDCR1 Register and WDCR2 Register) while the device is not in Standby mode will trigger a Reset of the microcontroller, and the device will set the ILLCON bit in the Watchdog Status register, WDSR (illegal watchdog configuration).

The ATA6847 watchdog supports eight watchdog periods. The watchdog period is programmable via the Watchdog Period bits (WWDP) in the Watchdog Control Register 2 (WDCR2). The selected period is valid for both Window and Time-out modes. The default watchdog period value is 128 ms.

A watchdog trigger event (an SPI write access to the WDTRIG register with the pattern (01010101) resets the Watchdog Timer. The Watchdog Reset pulse width is configured via the WRPL bits in the WDCR2 Register.

Register 12: WDCR1 Register – Watchdog Configuration Register 1 (Address 0x21)

Bit	7	6	5	4	3	2	1	0
	WDC			**WDPRE**		—	**WDLW**	—
Read/Write	R/W	R/W	R/W	R/W	R/W	U	R/W	U
Initial Value	0	1	0	0	0	0	1	0

Bits 7:5 - WDC Watchdog mode control:

001 = OFF mode

010 = Time-out mode (default)

100 = Window mode

Bits 4:3 - WDPRE Watchdog period control:

00 = Watchdog prescale factor 1 (default)

01 = Watchdog prescale factor 1.5

10 = Watchdog prescale factor 2.5

11 = Watchdog prescale factor 3.5

Bit 2 - Unimplemented.

Bit 1 - WDLW

If the bit is set to '1': After LH is released, the WDT is reset, and the first trigger window is long (t_{LW}).

If the bit is set to '0': After LH is released, the WDT is reset, and the first trigger window is standard (as configured by WDPRE and WWDP).

Bit 0 - Unimplemented.

Register 13: WDCR2 Register – Watchdog Configuration Register 2 (Address 0x22)

Bit	7	6	5	4	3	2	1	0
	WWDP				**WRPL**			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	1	0	0	0	0	0	1

Bits 7:4 - WWDP Watchdog period configuration (ms, prescale factor = 1, ± 20%):

1000 = 8

0001 = 16

0010 = 32

0011 = 64

0100 = 128 (default)

1101 = 256

1110 = 1024

0111 = 4096

Bits 3:0 - WRPL Watchdog reset pulse length (ms, ± 20%):

1000 = 1.25

0001 = 4.3 (default)

0010 = 11.25

1011 = 22.5

0100 = 45

1101 = 67.5

1110 = 112.5

0111 = 170

The watchdog is an important safety mechanism that must be configured correctly. Two mechanisms are provided to prevent watchdog parameters from being changed by mistake.

- All configuration bitfields in the registers WDC, WWDP and WRPL have a hamming distance of at least two for valid states.
- Reconfiguration protection: The configuration is only possible in Standby mode.

Having a hamming distance of at least two for all valid states for the control bitfields, WDC, WWDP and WRPL, ensures that a single bit error cannot cause the watchdog to be configured incorrectly (at least two bits must be flipped to reconfigure WDC, WWDP or WRPL). If an attempt is made to write an invalid code to the WDCR1 register or WDCR2 register, the SPI write to the WDCRx register is ignored and the CACC bit in the Watchdog Status register is set.

Register 14: WDSR Register – Watchdog Status Register (Address 0x23)

Bit	7	6	5	4	3	2	1	0
	OFF	**CACC**	**ILLCON**	**TRIGS**	**OF**	**OFSLP**	**ETRIG**	—
Read/Write	R	R/W	R/W	R	R/W	R/W	R/W	U
Initial Value	0	0	0	0	0	0	0	0

Bit 7 - OFF Value is '1' when Watchdog is OFF.

Bit 6 - CACC Corrupted write access to the watchdog configuration registers.

Bit 5 - ILLCON An attempt is made to reconfigure the watchdog control register while the device is not in Standby mode.

Bit 4 - TRIGS The device sets this bit to '1' if the Window mode watchdog is in the first half of the window and sets it to '0' if the Window mode watchdog is in the second half of the window. If the WD is not in Window mode, this bit will always be set to '0'.

Bit 3 - OF Watchdog overflow (Time-out/Window mode in Standby or Normal mode).

Bit 2 - OFSLP Watchdog overflow in Sleep mode (Time-out mode).

Bit 1 - ETRIG Watchdog triggered too early (Window mode).

Bit 0 - Unimplemented.

Writing '1' to the corresponding bit of the watchdog status register will reset the bit.

A microcontroller Reset is triggered immediately in response to an illegal watchdog configuration (configuration of the watchdog in Normal or Sleep mode), an incorrect Watchdog Trigger event in Window mode (watchdog overflow or triggered too early) or when the watchdog overflows in Time-out mode. If a Reset is triggered by the window watchdog the Window Watchdog Reset Event register will be set. The device will enter the µC Reset mode and enter Standby mode after the Reset is finished.

If a Reset is triggered by the watchdog, the respective Reset event register will be set. The device will enter the MCU Reset mode, followed by Standby mode, after the Reset takes place.

If there is a corrupted write access to the watchdog configuration registers and/or an illegal configuration of watchdog control register occurred when the watchdog is in OFF mode, the corresponding status register bit will be set.

If the fault register bits (CACC, ILLCON, OF, OFSLP and ETRIG bits) are not reset to zero before enabling the window watchdog, an MCU Reset will be triggered immediately after enabling the watchdog.

Register 15: WDTRIG Register – Watchdog Trigger Register (Address 0x20)

Bit	7	6	5	4	3	2	1	0
	WDTRIG							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

A watchdog trigger is an 8-bit wide SPI pattern written to the WDTRIG register.

A valid watchdog trigger event resets the watchdog timer. The only valid trigger pattern is **0b01010101**.

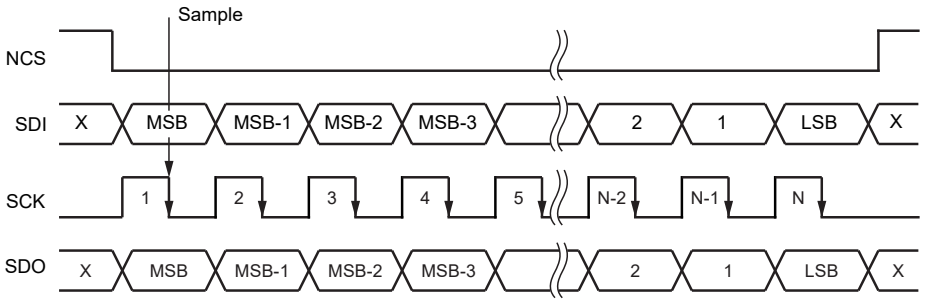
5.12 Serial Peripheral Interface (SPI) (Submit Feedback)

The SPI is used to communicate with a host microcontroller. The ATA6847 is configured and operated using SPI transfers. SPI transfers are disabled in Sleep and Deep Sleep modes.

The SPI allows full-duplex data transfer. Status information is returned when new control data are shifted in. The interface also offers read-only access, allowing registers to be read back without changing the register content.

Bit sampling is performed on the falling edge of the clock pin (SCK) and data is shifted in/out on the rising edge (see the figure below).

Figure 5-13. SPI Timing Protocol.



The SPI data is stored in dedicated 8-bit registers, and each register is assigned a unique 7-bit address. Sixteen bits must be transmitted to the device for a single register write operation.

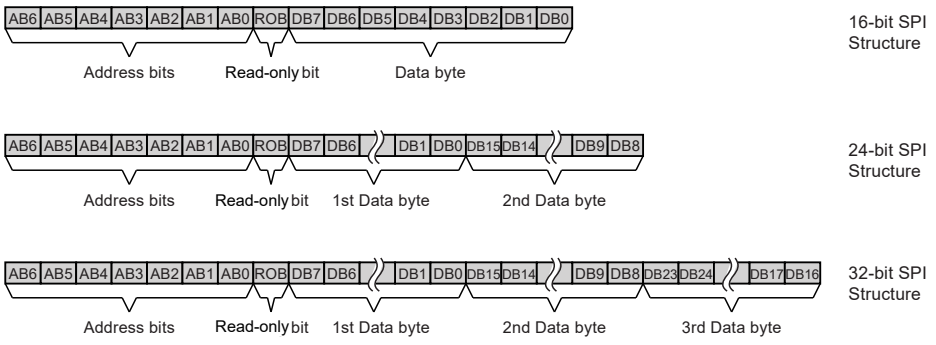
The **first byte** contain the 7-bit address along with a 'read/write' bit (the LSB). The read/write bit must be '0' to indicate a write operation. If this bit is '1', a read operation is performed and any data after this bit is ignored.

The **second byte** contain the data meant to be written to the register. The contents of the addressed register(s) are returned via the SDO pin, while a read or write operation is performed.

For faster programming, 16, 24 and 32-bit read and write operations are supported. For 24 and 32-bit operations, the register address is automatically incremented: once for a 24-bit operation and twice for a 32-bit operation.

Attempting to write to a non-existing register is not prohibited. If the available address space is exceeded during a write operation, the data beyond the valid address range is ignored without generating an SPI failure event.

Figure 5-14. SPI Transfer Data Structure



The number of transmitted SPI bits is monitored during SPI transfers. If the number of bits is not equal to 16, 24 or 32, the transfer is aborted.

An SPI failure event is captured (SPIF = '1', see SIR1 Register) if the SPI failure detection is enabled (SPIFECE = '1') and at least one of the following SPI failures is detected:

- SPI clock count error: only 16, 24 and 32-bit commands are valid for both read and write operation
- Illegal DOPM code (see DOPMCR Register)
- Attempted write access to locked register

If more than 32 bits are clocked in on the SDI pin during a read and write operation, the data stream on the SDI pin is looped back on the SDO pin from bit 33 onwards.

5.12.1 Register Summary (Submit Feedback)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	DOPMCR	RSTLVL	VDDIOOVSD	—	—	—	DOPM [2:0]		
0x03	GOPMCR	—	—	—	—	—	GDUOPM [2:0]		
0x04	WUCR	—	—	—	—	—	—	—	LOCWUE
0x05	GDUCR1	CCPT [5:0]						CCEN	BEMFEN
0x06	GDUCR2	HSOFF	LSOFF	TSWTO		EGBLT			
0x07	GDUCR3	ADDTHS		ADDTLS		HSSRC		LSSRC	
0x08	GDUCR4	COMPEN	VDHOVSD	UVVGSEN	UVVGSLVL	VGSUVFLT [3:0]			
0x09	ILIMCR	ILIMEN	ILIMFLT				ILIMSDEN	—	—
0x0A	ILIMTH	—	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0
0x0B	SCPCR	SCSDEN	SCFLT [3:0]				SCTHSEL [2:0]		
0x0C	CSCR	CSA3EN	—	CSA1EN	—	OFFSET		GAIN	
0x0E	MLDCR	—	SOURCE3	SINK3	SOURCE2	SINK2	SOURCE1	SINK1	MLDEN
0x0F	RWPCR	—	—	—	—	—	—	—	WP0
0x10	DSR1	SMTS	VDD2OTPWS	VDD1OTPWS	GDUOTPWS	—	GDUS	—	—
0x11	DSR2	—	VDD2OVS	VDD1OVS	VDD2UVS	VDD1UVHS	VDD1UVLS	VGUVS	VCPUVS
0x12	MLDRR	—	—	DIAG3_HS	DIAG3_LS	DIAG2_HS	DIAG2_LS	DIAG1_HS	DIAG1_LS
0x13	SIR1	VSUPF	WAKE	SYS	ILIM	LDOF	OVTF	VDSSC	VGSUV
0x14	SIR2	—	VDD2OV	VDD1OV	VDD2UV	VDD1UVH	VDD1UVL	—	—
0x15	SIR3	VGUV	VCPUV	SCHS3	SCHS2	SCHS1	SCLS3	SCLS2	SCLS1
0x16	SIR4	OVTSDVDD2	OVTSDVDD1	OVTSDGDU	—	OVTPWVDD2	OVTPWVDD1	OVTPWGDU	—
0x17	SIR5	VDHOV	VSUV	LOCWU	—	SPIF	PWRON	SYSERR	OSCF
0x18	SIECER1	GSCECE	VDHOVECE	ILIMECE	—	—	VSUVECE	SPIFECE	OVTPWECE
0x19	SIECER2	—	—	—	VDD2UVECE	VDD1UVHECE	VDD1UVLECE	VDD2OVECE	VDD1OVECE
0x20	WDTRIG	WDTRIG							
0x21	WDCR1	WDC			WDPRE		—	WDLW	—
0x22	WDCR2	WWDP				WRPL			
0x23	WDSR	OFF	CACC	ILLCON	TRIGS	OF	OFSLP	ETRIG	—

5.13 Diagnostics and Protections (Submit Feedback)

5.13.1 SLEEP MODE PROTECTION (Submit Feedback)

All interrupt bits must be cleared before the device transitions into Sleep or Deep Sleep mode. Otherwise, the device will switch to Standby mode in response to a Go-to-Sleep or Go-to-Deep-Sleep command (if DOPM = Sleep or Deep Sleep, see Device Operating Modes).

5.13.2 VS SUPPLY UNDERVOLTAGE PROTECTION (Submit Feedback)

If $V_{VS} < V_{VS\_UV\_Set}$ has been detected, the device will:

- Switch the GDU to GDU Standby mode, if it was in GDU Normal mode.
- Set the status register bit, VSUV (see SIR5 Register).
- In case the event capture enable register bit (VSUVECE) is set to '1' (see SIECER1 Register), an NIRQ interrupt will be generated.

5.13.3 VDH SUPPLY OVERVOLTAGE PROTECTION (Submit Feedback)

The VDH supply overvoltage protection is active when setting the VDHOVSD bit to '1'. If a $V_{VDH} > V_{VDH\_OV\_Set}$ event occurs, the device will switch the GDU to GDU Standby mode (when in GDU Normal mode) and the Charge Pump will be deactivated (as long as the overvoltage condition is valid).

If the VDHOVSD bit is set to '0', the device will not react to the overvoltage event, the GDU will remain in Normal mode and the Charge Pump will keep operating. Only an NIRQ interrupt event will be generated, presuming the VDHOVECE bit is set to '1'.

The device will set the status register bit (VDHOV, see the SIR1 Register), presuming the VDHOVECE bit is set to '1', and an NIRQ interrupt event will be generated. Set the VDHOVECE bit to '0' to disable VDH overvoltage event capture.

VDH overvoltage monitoring is only active in Normal mode.

5.13.4 VDD1/VDD2 UNDERVOLTAGE AND OVERVOLTAGE PROTECTION (Submit Feedback)

The ATA6847 provides various levels of VDD1 and VDD2 undervoltage monitoring. The feature is enabled by the RSTLVL bit.

If an undervoltage event has been detected at the VDD1 or VDD2 pin, the following will happen:

- The status bit VDDxUV (x = 1 or 2) and/or VDD1UVL will be set.
- The NIRQ pin will be asserted if the corresponding interrupt event capture enable register bit is set (see SIR2 Register).
- The device will switch to MCU Reset mode, causing the GDU to switch into GDU Standby mode.

If an overvoltage event has been detected on the microcontroller supply for longer than the overvoltage detection debouncing time, $t_{VDD1\_OV\_deb}$ or $t_{VDD2\_OV\_deb}$, the device is forced into Sleep mode, given that VDDIOOVSD is set to '1'. A number of actions are taken while switching into Sleep mode:

- All previously captured system interrupt events are cleared before the device switches to Sleep mode.
- Local wake up is enabled.
- Status bit SMTS is set to '1' (See DSR1 Register).
- The status register bit VDDIOOVSD (see #DOPMCR) will be set, presuming the VDD1OVECE or VDD2OVECE bit is set to '1'.
- The NIRQ pin will be asserted. Setting the VDD1OVECE and/or VDD2OVECE bits to '0' will disable VDD1 and/or VDD2 overvoltage event capture, respectively.

VDD1 and VDD2 overvoltage monitoring are active in Normal mode.

5.13.5 VGS MONITORING AND EXTERNAL MOSFET PROTECTION (Submit Feedback)

The ATA6847 monitors the gate supply voltage for each of the low and high-side external MOSFETs. The VG pin buffers the low-side gate supply voltage, whereas the VCP pin buffers the high-side gate supply voltage. The device provides two undervoltage detection thresholds, valid for both low and high-side gate supply voltages. The used threshold can be selected via the UVVGSLVL bit (see GDUCR4 Register).

A gate supply undervoltage condition for the low-side gate drivers occurs if $V_{VG} - V_{GND} < V_{VGS\_UV\_Set\_x}$.

A gate supply undervoltage condition for the high-side gate drivers occurs if $V_{VCP} - V_{VDH} < V_{VGS\_UV\_Set\_x}$.

In both cases:

- The GDU will be switched into GDU Standby mode.
- The gate control inputs NIHx and ILx are ignored.
- The according status register bit(s) VGUV and/or VCPUV will be set (see the SIR3 register).
- The NIRQ pin will be asserted.

The external MOSFET gate source (VGS) undervoltage monitoring is active as soon as the VG and VCP regulators are enabled, and the UVVGSEN bit is set (see GDUCR4 Register). Both the VG and VCP regulators start operating when the transition to GDU Normal mode occurs. Transitioning to GDU Standby mode is not possible unless VG and VCP are within the valid range. The status of both VG and VCP output regulators can be seen in the DSR2 register (see DSR2 Register).

The VGS undervoltage event capturing is active in GDU Standby mode and GDU Normal mode. In GDU Standby mode, the VGS undervoltage event is filtered with $t_{VGS\_U\_V\_Blank\_ADOO}$, ensuring the VG and VCP regulators ramp up properly. The delay filter is activated only once, when both VG and VCP regulators are activated. In case the VG and/or VCP regulator/s are not able to reach the requested voltage level (undervoltage level) within the filter time, NIRQ will be asserted.

UVVGSEN	VGS Monitoring
0	VGS monitoring deactivated – GDU state machine ignores all VGS UV events.
1	VGS monitoring activated – GDU switches into GDU Normal mode only if no VGS undervoltage has been detected.

5.13.6 OUTPUT CURRENT LIMITATION (Submit Feedback)

The ATA6847 provides an output current limitation feature for monitoring the external power MOSFETs sum current. The output of OpAmp3 is internally connected to a comparator. The limitation voltage is set in the ILIMTH Register. The limitation feature is active in Device Normal mode, as soon as it is activated via the ILIMEN bit, see the ILIMCR Register below.

On a current limitation event, different reactions can be configured, as following:

- If the ILIMSDEN bit is set to '1' (latched behavior), the interrupt event is latched and the GDU will switch into GDU Standby mode.
- If the ILIMSDEN bit is set to '0' (unlatched behavior), GDU Normal mode is maintained, but the six GHx and GLx gate driver outputs are deactivated until ILIM condition is resolved.

The interrupt register bit "ILIM" (see SIR1 Register) will be set, and an interrupt will be generated under the following conditions:

- Unlatched fault handling (ILIMEN = '1' AND ILIMSDEN = '0') and ILIMECE bit is set to '1'; or
- Latched fault handling (ILIMEN = '1' AND ILIMSDEN = '1')

The interrupt register bit "ILIM" will be cleared under the following conditions:

- When any of the six gate driver outputs become active while the unlatched fault handling is enabled; or
- When the ILIM bit is set to '1' via SPI.

The ATA6847 will ignore any current limitation event if the ILIMEN bit is set to '0'.

The current limitation detection delay filter can be configured using ILIMFLT in the ILIMCR Register. The following table explains the ILIM control bits in more detail:

ILIMEN	ILIMECE	ILIMSDEN	Device Behavior
0	0/1	0	No action on current limitation events
0	0/1	1	No action on current limitation events
1	1	0	Interrupt generation, unlatched automatic fault handling, interrupt event delay is inactive as soon as the interrupt bit is reset by the gate control.
1	0	0	No interrupt, unlatched automatic fault handling
1	0/1	1	Interrupt generation and latched fault handling

Register 16: ILIMCR Register – Current Limitation Control Register (Address 0x09)

Bit	7	6	5	4	3	2	1	0
	ILIMEN	**ILIMFLT**				**ILIMSDEN**	—	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	U	U
Initial Value	1	1	0	0	0	1	0	0

Bit 7 - ILIMEN Current limitation enable bit. Set to '1' activates the current limitation, whereas set to '0' deactivates it.

Bits 6:3 - ILIMFLT Current limitation filter time bits. The filter times are configured according to Current Limitation Detection/Short Circuit Detection Time. The filter time starts after the current limitation threshold has been reached. If the sensed current drops below the detection threshold during the filter time, the filter time will be reset and restarted.

Bit 2 - ILIMSDEN Current limitation shutdown enable bit. If set to '1', it will switch to GDU Standby mode and disable all gate drive outputs when a current limitation event has been detected, whereas if set to '0', the GDU stays in Normal mode. In the latter case, the unlatched automatic fault handling is activated.

Bits 1:0 - Unimplemented.

Register 17: ILIMTH Register – Current Limitation Threshold Register (Address 0x0A)

Bit	7	6	5	4	3	2	1	0
	—	**DAC6**	**DAC5**	**DAC4**	**DAC3**	**DAC2**	**DAC1**	**DAC0**
Read/Write	U	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 - Unimplemented.

Bits 6:0 - DACx Current limitation threshold DAC input.

Formula to calculate the current threshold through the external power MOSFETs:

$$V_{ILIM\_TH} = \frac{V_{VIO}}{128} \sum_{x=0}^{6} DAC_x \times 2^x$$

5.13.7 VDS DRAIN-SOURCE VOLTAGE MONITORING AND POWER STAGE SHORT CIRCUIT PROTECTION (Submit Feedback)

Short circuits in the half-bridge circuitry are monitored by sensing the voltage drop across the drain source of the external high-side and low-side MOSFETs. Comparators monitor the voltage drop between the drain (VDH) and the source terminals (SHx) of the external high-side MOSFET transistors, as well as between the external low-side MOSFET transistors drain (SHx) and source (GND). The voltage drop is monitored during the ON phase of the MOSFET, according to the ILx and NIHx pins.

The voltage drop is compared with the reference voltage. As soon as one of the drain-source voltage drops exceed the V_{SCREF} threshold, a short circuit in this branch is detected.

The Short Circuit Reference Threshold (V_{SCREF}) can be configured via SPI, using the SCTHSEL [2:0] bits (see table Short Circuit Detection Threshold).

The following actions occur in case of a short circuit event. The corresponding interrupt register will be set according to the SIR3 Register. The short circuit event will be signaled at the interrupt output pin (NIRQ). The GDU will be switched to GDU Standby mode, and all gate driver outputs will be disabled if SCSDEN bit is set to '1'. If the SCSDEN bit is set to '0', the device will only indicate the event at the NIRQ pin and the gate control will not be disabled.

To prevent false short circuit triggering, a VDS Drain-Source Short Circuit event is blanked out with the edge blanking time using the EGBLT bits (GDUCR2 register). Furthermore, the VDS short circuit event is filtered, and the filter time can be configured using the SCFLT[3:0] bits (see the SCPCR Register).

Register 18: SCPCR Register – Short Circuit Protection Control Register (address 0x0B)

Bit	7	6	5	4	3	2	1	0
	SCSDEN	**SCFLT [3:0]**				**SCTHSEL [2:0]**		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	1	0	0	0	0	0	0

Bit 7 - SCSDEN Short circuit shutdown enable. Set to '1', all gate driver outputs are disabled as soon as a short circuit failure has been detected. Set to '0', the short circuit event will only be indicated through the NIRQ pin.

Bits 6:3 - SCFLT [3:0] Short circuit filter time. The filter time needs to be configured according to Current Limitation Detection/Short Circuit Detection Time. The filter time starts after the edge blanking time (t_{EG_Blank}) expired and a V_{DS} voltage larger than V_{SCREF} has been detected. If the sensed voltage drops below the detection threshold during the filter time, the filter timer will be reset and will restart when another short circuit event occurs.

Bits 2:0 - SCTHSEL [2:0] Short circuit detection threshold.

Table 5-2. Short Circuit Detection Threshold (V_{SCREF})

SCTHSEL [2:0]	V_{SCREF} [mV]
3'b000	125
3'b001	250
3'b010	500
3'b011	750
3'b100	1000
3'b101	1250
3'b110	1500
3'b111	1750

5.13.8 TEMPERATURE MONITORING AND OVERTEMPERATURE PROTECTION (Submit Feedback)

The device offers two overtemperature detection thresholds, a pre-warning and a shutdown threshold. Thermal sensors are placed at different locations on the die: VDD1 LDO, VDD2 LDO and GDU.

If the temperature of one or more of the thermal sensors exceeds the overtemperature pre-warning threshold ($T_J > T_{OT\_PREW\_Set}$), the device will set the common pre-warning bit (OTPWS = '1', see DSR1 Register) and the corresponding interrupt bits (VDD1OTPWS and/or VDD2OTPWS and/or GDUOTPWS, see DSR1 Register). An overtemperature pre-warning interrupt will be generated at the NIRQ pin when the corresponding interrupt event capture enable register is set (see SIECER1 Register). The OTPWS bit is not latched and will be set to '0' as soon as the temperature of all monitored circuit parts decreases below the overtemperature protection pre-warning threshold.

If the temperature of one or more of the thermal sensors exceeds the overtemperature shutdown threshold (T_{OT_sdwn}), the overtemperature shutdown protection will be triggered for the corresponding circuit parts. This will trigger the following events:

- The VDD1 regulator is disabled in case the VDD1 regulator overtemperature shutdown has been triggered.
- The VDD2 regulator, if available, is disabled when the VDD2 regulator overtemperature shutdown has been triggered.
- The GDU is switched to GDU Standby mode when the GDU overtemperature shutdown has been triggered.
- At the same time, the corresponding overtemperature shutdown interrupt register will be set (see SIR4 Register).
- NIRQ pin will be asserted.

Wake-up events are still detected in case of overtemperature occurrence. A wake-up event will be signaled by asserting the NIRQ pin.

5.13.9 INTERRUPT/WAKE-UP EVENT DELAY (NIRQ) (Submit Feedback)

Frequent interrupt or wake-up events can require significant microcontroller processing time because the NIRQ pin is asserted each time an interrupt/wake-up event is generated. Therefore, the device incorporates an interrupt/wake-up delay timer (td_evt_cap) to limit the frequency of interrupt events.

When one of the event capture status bits is cleared, the NIRQ pin is deasserted, and the event delay timer starts. If further events occur while the event delay timer is running, the relevant status bits are set and NIRQ stays deasserted. As soon as the event timer expires, and one or more events are pending, the NIRQ pin is asserted again to alert the microcontroller.

We use microcontroller often in this DS without host. Using host is only required when we talk about the SPI “master”.

This way, the microcontroller is interrupted only once to process several events, rather than several times to process each individual event. If the microcontroller has cleared all active event capture bits before the event delay timer expires, the NIRQ pin remains deasserted, presuming no new or pending events occurred.

The event capture registers can be read at any time.

5.13.10 PROTECTION AND FAULT EVENT REGISTERS (Submit Feedback)

There are several types of registers:

- System Interrupt Event Capture Enable Registers used for interrupt configuration: SIECER1 and SIECER2
- System Interrupt Registers used for diagnostics feedback: SIR1-SIR5

- Device Status Registers used for hardware fault status feedback: DSR1 and DSR2

The registers are accessible via the SPI interface.

Register 19: SIECER1 Register – System Interrupt Event Capture Enable Register (Address 0x18)

Bit	7	6	5	4	3	2	1	0
	GSCECE	**VDHOVECE**	**ILIMECE**	—	—	**VSUVECE**	**SPIFECE**	**OVTPWECE**
Read/Write	R/W	R/W	R/W	U	U	R/W	R/W	R/W
Initial Value	1	1	1	0	0	1	1	1

Bit 7 - GSCECE General short circuit failure event capture enable bit. Default value '1'. By clearing the **GSCECE** bit, the short circuit fault capture for all branches of the external MOSFET bridge will be disabled.

Bit 6 - VDHOVECE VDH overvoltage failure event capture enable ($V_{VDH} > V_{VDH\_OV\_Set}$). The VDHOVECE bit set to '1' enables the VDH overvoltage event capture, whereas set to '0' disables the VDH overvoltage capture.

Bit 5 - ILIMECE Current limitation event capture enable register. Set to '1' enables the current limitation event capture, whereas set to '0' disables it.

Bits 4:3 - Unimplemented.

Bit 2 - VSUVECE VS undervoltage failure event capture enable ($V_{VS} < V_{VS\_UV\_Set}$). Set to '1' enables the VS undervoltage event capture, whereas set to '0' disables it.

Bit 1 - SPIFECE SPI failure event capture enable register. Set to '1' enables the SPI failure interrupt, whereas set to '0' disables it.

Bit 0 - OVTPWECE Overtemperature pre-warning event capture enable. Set to '1' enables the overtemperature pre-warning event capture, whereas set to '0' disables it.

Register 20: SIECER2 Register – System Interrupt Event Capture Enable Register (Address 0x19)

Bit	7	6	5	4	3	2	1	0
	—	—	—	**VDD2UVECE**	**VDD1UVHECE**	**VDD1UVLECE**	**VDD2OVECE**	**VDD1OVECE**
Read/Write	U	U	U	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	1	1	1	1	1

Bits 7:5 - Unimplemented.

Bit 4 - VDD2UVECE VDD2 undervoltage event capture enable ($V_{VDD2} < V_{VDD2\_UV\_Set}$). Set to '1' – enables the VDD2 undervoltage event capture. Set to '0' – disables it.

Bit 3 - VDD1UVHECE VDD1 undervoltage ($V_{VDD1} < V_{VDD1\_UV\_Set}$) event capture enable. Set to '1' – enables the VDD1 undervoltage event capture. Set to '0' – disables it.

Bit 2 - VDD1UVLECE VDD1 IO undervoltage ($V_{VDD1} < V_{VDD1\_IO\_UV\_Set}$) event capture enable. Set to '1' – enables the VDD1 IO undervoltage event capture. Set to '0' – disables it.

Bit 1 - VDD2OVECE VDD2 overvoltage event capture enable ($V_{VDD2} < V_{VDD2\_OV\_Set}$). Set to '1' – enables the VDD2 overvoltage event capture. Set to '0' – disables it.

Bit 0 - VDD1OVECE VDD1 overvoltage event capture enable ($V_{VDD1} < V_{VDD1\_OV\_Set}$). Set to '1' – enables the VDD1 overvoltage event capture. Set to '0' – disables it.

Register 21: SIR1 Register – System Interrupt Register 1 (Address 0x13)

The SIR1 register shows the overall failure interrupt events. The bits are not latched, except for bit 4 (ILIM). The state of these flags is the result of the OR-ed operation with the latched bits from SIR2, SIR3 and SIR4. The SIR1 bits will be automatically cleared after clearing the corresponding SIR2-SIR5 bits.

Bit	7	6	5	4	3	2	1	0
	VSUPF	**WAKE**	**SYS**	**ILIM**	**LDOF**	**OVTF**	**VDSSC**	**VGSUV**
Read/Write	R	R	R	R/W	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

Bit 7 - VSUPF IC supply failure event interrupt. Will be set to '1' if SIR5[7] and/or SIR5[6] bits are set to '1'. The bit is reset to '0' when both SIR5[7] and SIR5[6] are cleared.

Bit 6 - WAKE Wake-up event interrupt. Will be set to '1' if SIR5[5] and/or SIR5[4] bits are set to '1'. This bit is reset to '0' when SIR5[5] is cleared.

Bit 5 - SYS System event interrupt. Will be set to '1' if SIR5[3:1] and/or SIR5[4] bits are set to '1'. This bit is reset to '0' when SIR5[5] is cleared.

Bit 4 - ILIM Power stage current limitation interrupt. Will be set to '1' if a power stage current limitation event has been detected. The bit is reset to '0' by writing a '1' to the bit or, when unlatched current limitation handling has been enabled, the ILIM bit will be cleared when any of the six gate control driver outputs are activated.

Bit 3 - LDOF LDO failure event interrupt. Will be set to '1' if any SIR2 register bits are set to '1'. The bit is reset to '0' when all of the SIR2 register bits are reset to '0'.

Bit 2 - OVTF Overtemperature failure event interrupt. Will be set to '1' if any of the SIR4 register bits are set to '1'. The bit is reset to '0' when all of the SIR4 register bits are reset to '0'.

Bit 1 - VDSSC Drain-Source monitoring VDS short circuit interrupt. Will be set to '1' if a VDS short circuit failure has been detected by at least one bit in SIR3[5:0] (at least one bit is set to '1'). The bit is reset to '0' when all the bits in SIR3[5:0] are cleared.

Bit 0 - VGSUV Gate-Source monitoring VGS undervoltage interrupt. Will be set to '1' if a VGS undervoltage failure has been detected by at least one bit in SIR3[7:6] (at least one bit is set to '1'). The bit is reset to '0' when both bits in SIR3[7:6] are cleared.

Register 22: SIR2 Register – System Interrupt Register 2 (Address 0x14)

Bit	7	6	5	4	3	2	1	0
	—	**VDD2OV**	**VDD1OV**	**VDD2UV**	**VDD1UVH**	**VDD1UVL**	—	—
Read/Write	U	R/W	R/W	R/W	R/W	R/W	U	U
Initial Value	0	0	0	0	0	0	0	0

Bit 7 - Unimplemented.

Bit 6 - VDD2OV VDD2 overvoltage event interrupt. Will be set to '1' if an overvoltage event has been detected at the VDD2 pin **AND** the VDD2OVECE bit set to '1'. The bit is reset to '0' by writing a '1' to it.

Bit 5 - VDD1OV VDD1 overvoltage event interrupt. Will be set to '1' if an overvoltage event has been detected at the VDD1 pin **AND** the VDD1OVECE bit is set to '1'. The bit is reset to '0' by writing a '1' to it.

Bit 4 - VDD2UV VDD2 undervoltage event interrupt. Will be set to '1' if an undervoltage event has been detected at the VDD2 pin **AND** the VDD2UVECE bit is set to '1'. The bit is reset to '0' by writing a '1' it.

Bit 3 - VDD1UVH VDD1 undervoltage event interrupt ($V_{VDD1} < V_{VDD1\_UV\_Set}$). Will be set to '1' if an undervoltage event has been detected at the VDD1 pin **AND** the VDD1UVHECE bit is set to '1'. The bit is reset to '0' by writing a '1' to it.

Bit 2 - VDD1UVL VDD1 undervoltage event interrupt ($V_{VDD1} < V_{VDD1\_IO\_UV\_Set}$). Will be set to '1' if an undervoltage has been detected at the VDD1 pin **AND** the VDD1UVLECE bit is set to '1'. The bit is reset to '0' by writing a '1' to it.

Bits 1:0 - Unimplemented.

Register 23: SIR3 Register – System Interrupt Register 3 (Address 0x15)

Bit	7	6	5	4	3	2	1	0
	VGUV	**VCPUV**	**SCHS3**	**SCHS2**	**SCHS1**	**SCLS3**	**SCLS2**	**SCLS1**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit 7 - VGUV VG undervoltage interrupt ($(V_{VG} - V_{GND}) < V_{VGS\_UV\_Set\_x}$). Will be set to '1' if a VG undervoltage event has been detected. The bit is reset to '0' by writing a '1' to it.

Bit 6 - VCPUV VCP undervoltage interrupt ($(V_{VCP} - V_{VDH}) < V_{VGS\_UV\_Set\_x}$). Will be set to '1' if a VCP undervoltage event has been detected. The bit is reset to '0' by writing a '1' to it.

Bits 5:3 - SCHSx Power stage high-side external MOSFET short circuit interrupt. Will be set to '1' if a short circuit has been detected for the corresponding external MOSFET. The bit is reset to '0' by writing a '1' to it.

Bits 2:0 - SCLSx Power stage low-side external MOSFET short circuit interrupt. Will be set to '1' if a short circuit has been detected for the corresponding external MOSFET. The bit is reset to '0' by writing a '1' to it.

Register 24: SIR4 Register– System Interrupt Register 4 (Address 0x16)

Bit	7	6	5	4	3	2	1	0
	OVTSDVDD2	**OVTSDVDD1**	**OVTSDGDU**	**—**	**OVTPWVDD2**	**OVTPWVDD1**	**OVTPWGDU**	**—**
Read/Write	R/W	R/W	R/W	U	R/W	R/W	R/W	U
Initial Value	0	0	0	0	0	0	0	0

Bit 7 - OVTSDVDD2 VDD2 regulator overtemperature shutdown interrupt. Set to '1' if the VDD2 regulator junction temperature exceeds the overtemperature shutdown threshold (T_{OT_sdwn}). The bit is reset to '0' by writing a '1' to it.

Bit 6 - OVTSDVDD1 VDD1 regulator overtemperature shutdown interrupt. Set to '1' if the VDD1 regulator junction temperature exceeds the overtemperature shutdown threshold (T_{OT_sdwn}). The bit is reset to '0' by writing a '1' to it.

Bit 5 - OVTSDGDU GDU overtemperature shutdown interrupt. Set to '1' when GDU junction temperature exceeds the overtemperature shutdown threshold T_{OT_sdwn}. The bit is reset to '0' by writing a '1' to it.

Bit 4 - Unimplemented.

Bit 3 - OVTPWVDD2 VDD2 regulator overtemperature prewarning interrupt. Set to '1' if the VDD2 regulator junction temperature exceeds the overtemperature prewarning threshold $T_{OT\_PREW\_Set}$ **AND** the OVTPWECE bit is set to '1'. The bit is reset to '0' by writing a '1' to it.

Bit 2 - OVTPWVDD1 VDD1 regulator overtemperature prewarning interrupt. Set to '1' if the VDD1 regulator junction temperature exceeds the overtemperature prewarning threshold $T_{OT\_PREW\_Set}$ **AND** the OVTPWECE bit is set to '1'. The bit is reset to '0' by writing a '1' to it.

Bit 1 - OVTPWGDU GDU overtemperature prewarning interrupt. Set to '1' if the GDU junction temperature exceeds the overtemperature prewarning threshold $T_{OT\_PREW\_Set}$ **AND** the OVTPWECE bit is set to '1'. The bit is reset to '0' by writing a '1' to it.

Bit 0 - Unimplemented.

Register 25: SIR5 Register – System Interrupt Register 5 (Address 0x17)

Bit	7	6	5	4	3	2	1	0
	VDHOV	**VSUV**	**LOCWU**	**—**	**SPIF**	**PWRON**	**SYSERR**	**OSCF**
Read/Write	R/W	R/W	R/W	U	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	1	0	0

Bit 7 - VDHOV VDH overvoltage interrupt. Set to '1' if a VDH overvoltage occurs **AND** bit VDHOVECE is set to '1'. The bit is reset to '0' by writing a '1' to it.

Bit 6 - VSUV VS undervoltage interrupt. Set to '1' if VS drops below the threshold $V_{VS\_UV\_Set}$ for longer than the fault blanking time **AND** bit VSUVECE is set to '1'. The bit is reset to '0' by writing a '1' to it.

Bit 5 - LOCWU Local wake-up interrupt. Set to '1' if a local wake-up event occurs **AND** the local wake-up detection is enabled. The bit is reset to '0' by writing a '1' to it.

Bit 4 - Unimplemented.

Bit 3 - SPIF SPI failure interrupt. Set to '1' if an SPI failure has been detected **AND** SPIFECE bit is set to '1'. The bit is reset to '0' by writing a '1' to it.

Bit 2 - PWRON Power-on interrupt. Set to '1' if the device is no longer in the Power Off mode. The bit is reset to '0' by writing a '1' to it.

Bit 1 - SYSERR Internal system error status. Will be set to '1' in the following cases:

- The parity check to IC trimming data registers has failed.
- An internal voltage regulator failure has been detected.
- An illegal internal digital state has been detected.

The bit is not latched. It is automatically cleared if the fault is no longer present.

The NIRQ pin is asserted as long as the bit is set to '1'.

Bit 0 - OSCF Internal system clock failure status bit. Set to '1' if the system clock is missing. The bit is not latched and will reset to '0' as soon as the internal system clock recovers. No interrupt at the NIRQ pin will be generated without an internal system clock. The bit can, however, be read via SPI.

Register 26: DSR1 Register – Device Status Register 1 (Address 0x10)

Bit	7	6	5	4	3	2	1	0
	SMTS	**VDD2OTPWS**	**VDD1OTPWS**	**GDUOTPWS**	**—**	**GDUS**	**—**	**—**
Read/Write	R	R	R	R	U	R	U	U
Initial Value	0	0	0	0	0	0	0	0

Bit 7 - SMTS Sleep mode transition status. Set to '0' if the prior transition to Sleep mode was triggered by an SPI command and set to '1' if the prior transition to Sleep mode was forced by a VIO overvoltage event.

Bit 6 - VDD2OTPWS VDD2 regulator overtemperature pre-warning status. Set to '1' if the junction temperature of the VDD2 regulator exceeds the overtemperature pre-warning level ($T_{OT\_PREW\_Set}$). The bit is reset to '0' as soon as the junction temperature drops below the overtemperature pre-warning clear level ($T_{OT\_PREW\_Clear}$).

Bit 5 - VDD1OTPWS VDD1 regulator overtemperature pre-warning status. Set to '1' if the junction temperature of the VDD1 regulator exceeds the overtemperature pre-warning level ($T_{OT\_PREW\_Set}$). The bit is reset to '0' as soon as the junction temperature drops below the overtemperature pre-warning clear level ($T_{OT\_PREW\_Clear}$).

Bit 4 - GDUOTPWS GDU overtemperature pre-warning status. Set to '1' if the junction temperature of the GDU exceeds the overtemperature pre-warning level ($T_{OT\_PREW\_Set}$). The bit is reset to '0' as soon as the junction temperature drops below the overtemperature pre-warning clear level ($T_{OT\_PREW\_Clear}$).

Bit 3 - Unimplemented.

Bit 2 - GDUS GDU status. Set to '1' as soon as the GDU is ready to drive the gate of the external MOSFETs, whereas set to '0' indicates the GDU is not ready yet.

Bits 1:0 - Unimplemented.

Register 27: DSR2 Register – Device Status Register 2 (Address 0x11)

Bit	7	6	5	4	3	2	1	0
	—	**VDD2OVS**	**VDD1OVS**	**VDD2UVS**	**VDD1UVHS**	**VDD1UVLS**	**VGUVS**	**VCPUVS**
Read/Write	U	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

Bit 7 - Unimplemented.

Bit 6 - VDD2OVS VDD2 overvoltage status. Set to '1' if VDD2 overvoltage is detected and set to '0' if the VDD2 voltage is below the overvoltage clear level.

Bit 5 - VDD1OVS VDD1 overvoltage status. Set to '1' if VDD1 overvoltage is detected and set to '0' if the VDD1 voltage is below the overvoltage clear level.

Bit 4 - VDD2UVS VDD2 undervoltage status. Set to '1' if VDD2 undervoltage is detected and set to '0' if the VDD2 voltage is above the undervoltage clear level.

Bit 3 - VDD1UVHS VDD1 undervoltage status ($V_{VDD1} < V_{VDD1\_UV\_Set}$). Set to '1' if VDD1 undervoltage is detected and set to '0' if the VDD1 voltage is above the undervoltage clear level ($V_{VDD1} > V_{VDD1\_UV\_CLR}$).

Bit 2 - VDD1UVLS VDD1 undervoltage status ($V_{VDD1} < V_{VDD1\_IO\_UV\_Set}$). Set to '1' if VDD1 undervoltage is detected and set to '0' if the VDD1 voltage is above the undervoltage clear level ($V_{VDD1} > V_{VDD1\_IO\_UV\_CLR}$).

Bit 1 - VGUVS VG undervoltage status. Set to '1' if VG undervoltage is detected and set to '0' if the VG voltage level is higher than the $V_{VGS\_UV\_Clear\_H}$ threshold.

Bit 0 - VCPUVS VCP undervoltage status. Set to '1' if VCP undervoltage is detected and set to '0' if the VCP voltage is higher than the $V_{VGS\_UV\_Clear\_H}$ threshold.

Register 28: RWPCR Register – Register Write Protection Control Register (Address 0x0F)

Sections of the register address area can be write-protected to prevent unintended modifications.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	**WP0**
Read/Write	U	U	U	U	U	U	U	R/W
Initial Value	0	0	0	0	0	0	0	0

Bits 7:1 - Unimplemented.

Bit 0 - WP0 Write protection. Set to '1' disables register write access to register address areas 0x01 to 0x0E, 0x21 and 0x22. Set to '0' enables write access.

5.13.11 CROSS CONDUCTION PROTECTION (Submit Feedback)

Cross conduction timers at every drive stage prevent switching ON any output driver for a time (t_{CC}) after the counterpart driver in the same phase has been switched OFF. The cross conduction timers are also active in case a short circuit is detected.

The static cross conduction timers can be replaced by adaptive dead-time control. The adaptive dead-time comparators monitor voltages on the gate drive outputs and switch node to determine when to switch the MOSFETs ON and OFF.

To prevent cross conduction when turning ON high side switches, the ATA6847 monitors the low side MOSFETs gate source voltage ($V_{GLx} - V_{GND}$) and prevents turning ON the high side MOSFET in the same branch until the gate source voltage of the low-side switch is lower than V_{LOOFF}.

To prevent cross conduction when switching ON low-side switches, the ATA6847 monitors the voltage on the SHx switching node. Only when the switching node voltage drops below V_{SWTH}, the low-side gate drive can be released. Once the low-side gate drive is released, it is latched until the NIHx signal goes low. This prevents any ringing or oscillations on the switch node, or the SHx pin from turning OFF the GSx driver. If the NIHx pin goes high and the voltage on the SHx pin does not cross the V_{SWTH} threshold, the low-side gate drive is deactivated automatically, after Adaptive Deadtime Force To Switch Delay Time (t_{SWTO}) has passed.

5.14 Limp Home (Submit Feedback)

The Limp Home function is a high-voltage output pin used for signaling unexpected system errors. The LH pin is driven by an open-drain NMOS switch and is activated by the following events:

- A watchdog failure or Reset event. A watchdog timeout event in Sleep mode will not activate LH.
- If the device is in Standby or Normal mode:
  $V_{VDD1} < V_{VDD1\_UV\_Set}$ and RSTLVL bit = '1' (ATA6847-5050) **or**
  $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$ (ATA6847-5050/ATA6847-3333) **or**
  $V_{VDD2} < V_{VDD2\_UV\_IO\_Set}$ (ATA6847-5033)
- $V_{VDD1} < V_{VDD1\_UV\_Set}$ and RSTLVL bit = '1' (ATA6847-5050) **or**
  $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$ (ATA6847-5050 / ATA6847-3333) **or**
  $V_{VDD2} < V_{VDD2\_UV\_IO\_Set}$ (ATA6847-5033) has been detected for longer than t_{Reset} after entering MCU Reset mode, triggered by a wake-up or interrupt event (see cases **e** AND **i** in Device Operating Modes).
- VDDIO overvoltage event has been detected and VDDIOOVSD is enabled (see case **n** in Device Operating Modes).

Releasing the LH pin to high ohmic, after the ATA6847 transitions from MCU Reset mode into Standby mode, requires receiving three valid watchdog trigger values (0x55) via SPI.

6. Electrical Characteristics (Submit Feedback)

6.1 Absolute Maximum Ratings (Submit Feedback)

Parameters	Symbol	Min.	Max.	Unit
Junction Temperature	T_J	-40	170	°C
Storage Temperature	T_S	-55	150	°C
DC Voltage on the VS, VDH, INH, LH pins	V_{VS}, V_{VDH}, V_{INH}, V_{LH}	-0.3	42	V
DC Voltage on the WAKE pin	V_{WAKE}	-1.5	42	V
DC Voltage on the NIRQ, SDO, SDI, NCS, SCK, NIHx, ILx pins	V_X	-0.3	V_{VIO} + 0.3	V
DC Voltage on the NRES pin	V_{NRES}	-0.3	10	V
DC Voltage on the VDD1 pin	V_{VDD1}	-0.3	5.85	V
DC Voltage on the VDD2 pin	V_{VDD2}	-0.3	5.5	V
DC Common Mode Voltage on the OPPx, OPNx pins	V_{OPPX}, V_{OPNX}	-5.5	5.5	V
DC Voltage on the BEMFx, OPOx pins	V_{BEMFX}, V_{OPOX}	-0.3	V_{VIO} + 0.3	V
DC Voltage on the VG, CPN2 pins	V_{VG}, V_{CPN2}	-0.3	15	V
DC Voltage on the GHx to SHx pins	V_{GHX}-V_{SHX}	-0.3	15	V
DC Voltage on the GHx pin	V_{GHX}	V_{SHX} – 0.3	V_{VCP} + 0.3	V
DC Voltage on the SHx pin	V_{SHX}	-5.5	42	V
DC Voltage on the GLx pin	V_{GLX}	V_{GND} – 0.3	V_{VG} + 0.3	V
DC Voltage on the GLx to GND pins	V_{GLX}-V_{GND}	-0.3	15	V
DC Voltage on the GND pin	V_{GND}	-5.5	5.5	V
Differential DC Voltage between GND and GNDEP (exposed die pad)	—	-0.3	0.3	V
DC Voltage on CPN1, CPP1	V_{CPN1}, V_{CPP1}	-0.3	42	V
DC Voltage on CPN2, CPP2, VCP	V_{CPN2}, V_{CPP2}, V_{VCP}	-0.3	55	V
HBM JESD22-A114/AEC-Q100-002 (1.5 kΩ/100 pF) • All pins • Pins VS, VDH, WAKE to GND	—	 -2 -6	 +2 +6	 kV kV
Charge Device Model ESD AEC-Q100-011 - All pins	—	-750	750	V

Attention: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device within these or any other conditions beyond those indicated in the DC/AC Characteristics of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 DC/AC Characteristics (Submit Feedback)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; –40°C ≤ T_J ≤ 125°C; typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
VS, VDH								
Supply Voltage Threshold for Power-On Detection	V_{VS_PWRON}	VS	4.2	—	4.55	V	VS rising	A
Supply Voltage Threshold for Power OFF Detection	V_{VS_PWROFF}	VS	2.8	—	3	V	V_{VS} falling	A
VS Undervoltage Detection Clear	$V_{VS\_UV\_Clear}$	VS	4.6	—	4.9	V	V_{VS} rising	A
VS Undervoltage Detection Set	$V_{VS\_UV\_Set}$	VS	4.2	—	4.55	V	V_{VS} falling	A
VS + VDH Quiescent Current in Deep Sleep Mode	I_{VS_DSLP}	VS	—	10	15	µA	Deep Sleep mode (WAKE wake up only), overvoltage detection OFF, V_{VS} < 25V	A
VS + VDH Current in Sleep Mode	I_{VS_SLP}	VS	—	15	35	µA	Sleep mode, (WAKE wake up), overvoltage detection OFF, T_J < 25°C, V_{VS} < 25V, See Figure 7-9	A
VS Current in Standby Mode	I_{VS_STB}	VS	—	—	80	µA	Standby mode, T_J < 25°C, LDO active, V_{VS} < 25V	A
VDH Current in Normal Mode Without Gate Driving	$I_{VDH\_GDU\_STB}$	VDH	—	—	8.2	mA	Normal mode, GDU Standby mode, 4.2V < V_{VDH} < 12V	A
VDH Overvoltage Detection Set	$V_{VDH\_OV\_Set}$	VDH	32.5	—	34.5	V	V_{VDH} Rising	A
VDH Overvoltage Detection Clear	$V_{VDH\_OV\_Clr}$	VDH	32	—	34	V	V_{VDH} Falling	A
VDH Current in Standby Mode	I_{VDH_STB}	VDH	—	1	—	µA	WAKE wake up, overvoltage detection OFF	A
VDD1 5V: ATA6847-5050, ATA6847-5033								
Output Voltage	$V_{VDD1nom}$	VDD1	4.9	5	5.1	V	V_{VS} > 5.5V (I_{VDD1} = 0 to -100 mA DC)	A
Output Voltage at Low VS	$V_{VDD1low}$	VDD1	V_{VS}-VDx	—	5.1	V	3V < V_{VS} < 5.35V, (I_{VDD1} = 0 to 100 mA)	A
	V_{D1}	VDD1	—	—	100	mV	3V < V_{VS} < 5.35V, I_{VDD1} = 20 mA	A
	V_{D2}	VDD1	—	—	250	mV	3V < V_{VS} < 5.35V, I_{VDD1} = 50 mA	A
	V_{D3}	VDD1	—	—	500	mV	3V < V_{VS} < 5.35V, I_{VDD1} = 100 mA	A
Line Regulation Maximum	$V_{VDD1line}$	VDD1	—	—	0.2	%	5.5V < V_{VS} < 40V, 1mA < I_{VDD1} < 100 mA	A
Load Regulation Maximum	$V_{VDD1load}$	VDD1	—	—	1	%	5.5V < V_{VS} < 40V, 5 mA < I_{VDD1} < 100 mA	A
Power Supply Ripple Reject	PSRR	VDD1	40	60	—	dB	1 V_{PP} @100 Hz, 10 kHz, 100 kHz; I_{VDD1} = 10 mA, 50 mA, 100 mA; V_{VS} = 13.8V	D
Output Current Limitation	$I_{VDD1lim}$	VDD1	100	—	145	mA	V_{VS} = 4.9V	A
Phase Margin	PM	VDD1	35	—	—	Deg.	V_{VS} > 5.5V, I_{VDD1} < 100 mA	D
Load Capacity	C_{VDD1}	VDD1	1.87	2.2	—	µF	MLC capacitor	D

.....continued

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; –40°C ≤ T_J ≤ 125°C; typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Ramp-up Time	$t_{VDD1\_startup}$	VDD1	—	—	0.5	ms	V_{VS} > 5.5V, from enable regulator to V_{VDD1} = 99.5% stable value, C_{VDD1} = 2.7-3.9 µF, I_{VDD1} = 25 mA	C
VDD1 Undervoltage Set Threshold	$V_{VDD1\_UV\_Set}$	VDD1	4.5	—	4.7	V	V_{VDD1} falling	A
VDD1 Undervoltage Clear Threshold	$V_{VDD1\_UV\_Clear}$	VDD1	4.6	—	4.8	V	V_{VDD1} rising	A
VDD1 Undervoltage Hysteresis	$V_{VDD1\_UV\_HYS}$	VDD1	0.08	0.1	0.12	V		C
VDD1 IO Undervoltage Set	$V_{VDD1\_UV\_IO\_Set}$	VDD1	2.4	—	2.7	V	V_{VDD1} falling	A
VDD1 IO Undervoltage Clear	$V_{VDD1\_UV\_IO\_Clear}$	VDD1	2.5	—	2.8	V	V_{VDD1} rising	A
VDD1 IO Undervoltage Hysteresis	$V_{VDD1\_UV\_IO\_HYS}$	VDD1	0.08	0.1	0.12	V		C
Debouncing Time for Detecting VDD1 IO Undervoltage	$t_{VDD1\_UV\_IO\_deb}$	VDD1	6	—	54	µs		A
Output Current Foldback Corner	$I_{VDD1\_fbcorner}$	VDD1	105	—	135	mA	IC in Standby mode	A
Output Current Foldback Short Circuit Current	$I_{VDD1\_fb\_sc}$	VDD1	—	—	30	mA		A
VDD1 Overvoltage Set	$V_{VDD1\_OV\_Set}$	VDD1	5.5	5.68	5.85	V		A
VDD1 Overvoltage Clear	$V_{VDD1\_OV\_Clear}$	VDD1	5.45	5.58	5.75	V		A
Debouncing Time for Detecting VDD1 Overvoltage	$t_{VDD1\_OV\_deb}$	VDD1	6	—	54	µs		A
Debouncing Time for Detecting VDD1 Undervoltage	$t_{VDD1\_uv\_deb}$	VDD1	6	—	54	µs		A
VDD1 5V Output Voltage Load Step	$V_{VDD1loadStep}$	VDD1	-2	—	2	%	I_{VDD1} = 0 to 100 mA, I_{VDD1}= 100 to 0 mA Loadstep transient	C
VDD1 3.3V: ATA6847-3333								
Output Voltage	$V_{VDD1nom}$	VDD1	3.234	3.3	3.366	V	V_{VS} > 3.8V, (I_{VDD1} = 0 to 100 mA)	A A
Output Voltage at Low VS	$V_{VDD1low}$	VDD1	V_{VS}-V_{Dx}	—	3.37	V	3V < V_{VS} < 3.7V, (I_{VDD1} = 0 to 100 mA)	A
	V_{D1}	VDD1	—	—	100	mV	3V < V_{VS} < 3.7V, I_{VDD1} = 20 mA	A
	V_{D2}	VDD1	—	—	250	mV	3V < V_{VS} <3.7V, I_{VDD1} = 50 mA	A
	V_{D3}	VDD1	—	—	500	mV	3V <V_{VS} < 3.7V, I_{VDD1} = 100 mA	A
Line Regulation Maximum	$V_{VDD1line}$	VDD1	—	—	0.2	%	3.8V < V_{VS} < 40V, 1 mA < I_{VDD1} < 100 mA	A
Load Regulation Maximum	$V_{VDD1load}$	VDD1	—	—	1	%	3.8V < V_{VS} < 40V, 5 mA < I_{VDD1} < 100 mA	A
Power Supply Ripple Reject	PSRR	VDD1	40	60	—	dB	1 V_{PP} @100 Hz, 10 kHz, 100 kHz; V_{VS} = 13.8V I_{VDD1} = 10 mA, 50 mA, 100 mA	D
Phase Margin	PM	VDD1	25	—	—	Deg.	V_{VS} > 3.8V, I_{VDD1} < 100 mA	D

.....continued

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; –40°C ≤ T_J ≤ 125°C; typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Load Capacity	C_{VDD1}	VDD1	1.87	2.2	—	µF	MLC capacitor	D
Ramp-up Time	$t_{VDD1\_startup}$	VDD1	—	—	0.5	ms	V_{IN} > 3.8V, from enable regulator to V_{VDD} = 99.5% stable value, C_{VDD1} = 2.2 µF, I_{VDD1} = 25 mA	D
VDD1 IO Undervoltage Set	$V_{VDD1\_UV\_IO\_Set}$	VDD1	2.4	—	2.7	V	V_{VDD1} falling	A
VDD1 IO Undervoltage Clear	$V_{VDD1\_UV\_IO\_Clear}$	VDD1	2.5	—	2.8	V	V_{VDD1} rising	A
VDD1 IO Undervoltage Hysteresis	$V_{VDD1\_UV\_IO\_HYS}$	VDD1	0.08	0.1	0.12	V		C
Debouncing Time for Detecting VDD1 Interface Undervoltage	$t_{VDD1\_UV\_IO\_deb}$	VDD1	6	—	54	µs		A
Output Current Foldback Corner	$I_{VDD1\_fbcorner}$	VDD1	105	—	135	mA	IC in Standby mode	A
Output Current Foldback Short Circuit Current	$I_{VDD1\_fb\_sc}$	VDD1	—	—	30	mA		A
VDD1 Overvoltage Set	$V_{VDD1\_OV\_Set}$	VDD1	3.64	3.75	3.86	V		A
VDD1 Overvoltage Clear	$V_{VDD1\_OV\_Clear}$	VDD1	3.54	3.65	3.76	V		A
Debouncing Time for Detecting VDD1 Overvoltage	$t_{VDD1\_OV\_deb}$	VDD1	6	—	54	µs		A
VDD1 3.3V Output Voltage Load Step	$V_{VDD1loadStep}$	VDD1	-2	—	2	%	I_{VDD1} = 0 to 100 mA, I_{VDD1}= 0 to 100 mA. Load step transient included.	C
VDD2 3.3V: ATA6847-5050, and ATA6847-5033								
Output Voltage	$V_{VDD2nom}$	VDD2	3.234	3.3	3.366	V	V_{VDD1} > 4.5V, (I_{VDD2} = 0 to 70 mA)	A
Output Voltage at Low VDD2	$V_{VDD2low}$	VDD2	V_{VDD1}-V_{Dx}	—	3.37	V	V_{VDD1} < 4.5V, (I_{VDD2} = 0 to 70 mA)	A
Regulator Drop Voltage at Low VDD1	V_{D1}	VDD2	—	—	0.3	V	I_{VDD2} = 20 mA	A
	V_{D2}	VDD2	—	—	0.6	V	I_{VDD2} = 40 mA	A
	V_{D3}	VDD2	—	—	1.05	V	I_{VDD2} = 70mA	A
Line Regulation Maximum	$V_{VDD2line}$	VDD2	—	—	0.2	%	4.5 V < V_{VDD1} < 5.5V, 1 mA < I_{VDD2} < 70 mA	C
Load Regulation Maximum	$V_{VDD2load}$	VDD2	—	—	1.0	%	4.5 V < V_{VDD1} < 5.5V, 5 mA < I_{VDD2} < 70 mA	A
Power Supply Ripple Reject	PSRR	VDD2	40	60	—	dB	1 V_{PP} @100 Hz, 10 kHz, 100 kHz; I_{VDD2} = 10 mA, 50 mA, 70 mA; V_{VDD1} = 5V	D
Phase Margin	PM	VDD1	40	—	—	Deg.	V_{VS} > 4.5V, I_{VDD2} = 70 mA	D
Output Current Limitation	$I_{VDD2lim}$	VDD2	75	—	100	mA		A
Load Capacity	C_{VDD2}	VDD2	1.87	2.2	—	µF	MLC capacitor	D

.....continued

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; –40°C ≤ T_J ≤ 125°C; typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Ramp-up Time	$t_{VDD2\_startup}$	VDD2	—	—	0.5	ms	V_{IN} > 4.5V, from enable regulator to V_{VDD} = 99.5% stable value, C_{VDD2} = 2.7-3.9 µF, I_{VDD2} = 25 mA	C
VDD2 IO Undervoltage Set	$V_{VDD2\_UV\_IO\_Set}$	VDD2	2.4	—	2.7	V	V_{VDD2} falling	A
VDD2 IO Undervoltage Clear	$V_{VDD2\_UV\_IO\_Clear}$	VDD2	2.5	—	2.8	V	V_{VDD2} rising	A
VDD2 IO Undervoltage Hysteresis	$V_{VDD2\_UV\_IO\_HYS}$	VDD2	0.08	0.1	0.12	V		C
Debouncing Time for Detecting VDD2 Interface Undervoltage	$t_{VDD2\_UV\_IO\_deb}$	VDD2	6	—	54	µs		A
VDD2 Overvoltage Set	$V_{VDD2\_OV\_Set}$	VDD2	3.64	3.75	3.86	V		A
VDD2 Overvoltage Clear	$V_{VDD2\_OV\_Clear}$	VDD2	3.54	3.65	3.76	V		A
Debouncing Time for Detecting VDD2 Overvoltage	$t_{VDD2\_OV\_deb}$	VDD2	6	—	54	µs		A
VDD2 3.3V Output Voltage Load Step	$V_{VDD2loadStep}$	VDD2	-2	—	2	%	I_{VDD2} = 0 to 70 mA, I_{VDD2} = 70 to 0 mA. Load step.	C
VG Regulator (regulated charge pump)								
VG Output Voltage	V_{VG}	VG	11.5	12	12.5	V	V_{VDH} > V_{CP_STOP}, I_{VG} < 30 mA	A
VG Output Voltage	V_{VG}	VG	7.8	—	—	V	V_{VDH} > 5.1V, I_{VG} < 21 mA	A
Charge Pump Start	V_{CP_START}	VDH	12.5	—	13.3	V	V_{VDH} falling	A
Charge Pump Stop	V_{CP_STOP}	VDH	13	—	13.8	V	V_{VDH} rising	A
Charge Pump Frequency	f_{CP_VG}	CPN1, CPN2	360	380	400	kHz	V_{VDH} < 13V	A
Output Current Limit	I_{LIM_VG}		35	60	85	mA		A
Line Regulation Maximum	V_{VGline}	VG	—	—	0.2	%	13.8V ≤ V_{VDH} < 36V, 1 mA < I_{VG} < 30 mA	A
Load Regulation Maximum	V_{VGload}	VG	—	—	0.5	%	13.8V ≤ V_{VDH} < 36V, 5 mA < I_{VG} < 30 mA	A
Power Supply Ripple Reject	PSRR	VG	30	60	—	dB	1 V_{PP} @100 Hz, 10 kHz, 100 kHz; I_{VG} = 1 mA, 10 mA, 30 mA; V_{VS} > 13.8V	D
Phase Margin	PM	VG	35	—	—	Deg.	V_{VDH} ≥ 13.8V, I_{VDD1} < 30 mA	D
VCP Charge Pump								A
Charge Pump Output Voltage	V_{VCP}	VCP	12.2	—	—	V	V_{VDH} > 5.1V, V_{VG} > 7.8V, I_{VCP} = 10.6 mA	A
Charge Pump Output Voltage	V_{VCP}	VCP	24	—	—	V	V_{VDH} > 13.8V, V_{VG} > 11.5V, I_{VCP} = 15 mA	A
Gate Drive Unit								
Output Driver Source Resistance	R_{source}	GH/Lx	—	—	27	Ω	I_{GHx}/I_{GLx} = 100 mA	A
Output Driver Sink Resistance	R_{sink}	GH/Lx	—	—	10	Ω	I_{GHx}/I_{GLx} = -100 mA	A

.....continued

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; –40°C ≤ T_J ≤ 125°C; typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Rising Edge Propagation Delay	t_{del_r}	GH/Lx	—	—	240	ns	C_{load} = 0, NIHx 30% to VGHx-VSHx or ILx 70% to V_{GLx} - V_{GND}, reaches 10% of final V_{GS} level (slew rate control disabled)	C
Falling Edge Propagation Delay	t_{del_f}	GH/Lx	—	—	240	ns	C_{load} = 0, NIHx 70% to VGHx - VSHx or ILx 30% to V_{GLx} - V_{GND}, reaches 90% of final V_{GS} level (slew rate control disabled)	C
Propagation Delay Mismatch	t_{del_mis}	GHx, GLx	0	—	100	ns	Absolute high-side edge and low-side edge propagation delay mismatch	C
			0	—	50	ns	Absolute high-side edge and low-side edge propagation delay mismatch in complementary mode	C
Slew Rate Control	SR100	GH/Lx	—	100%	—	full speed	HSSRC/LSSRC = `2'b00`	A
	SR50	GH/Lx	—	50%	—	full speed	HSSRC/LSSRC = `2'b01`	A
	SR25	GH/Lx	—	25%	—	full speed	HSSRC/LSSRC = `2'b10`	A
	SR125	GH/Lx	—	12.50 %	—	full speed	HSSRC/LSSRC = `2'b11`	A
VGS Undervoltage Detection Clear	$V_{VGS\_UV\_Clear\_H}$	GH/Lx	6.1	—	6.55	V	Higher level selected, UVVGSLVL = `1'b1`	A
VGS Undervoltage Detection Clear	$V_{VGS\_UV\_Clear\_L}$	GH/Lx	4.6	—	4.9	V	Lower level selected, UVVGSLVL = `1'b0`	A
VGS Undervoltage Detection Set	$V_{VGS\_UV\_Set\_H}$	GH/Lx	5.6	—	6.0	V	Higher level selected, UVVGSLVL = `1'b1`	A
VGS Undervoltage Detection Set	$V_{VGS\_UV\_Set\_L}$	GH/Lx	4.2	—	4.55	V	Lower level selected, UVVGSLVL = `1'b0`	A
Short Circuit Detection Voltage Threshold Range (Drain-Source Monitoring)	V_{SC_TH}	VDH, SHx, GND	See SCPCR Register			mV	Configurable via SPI	A
Short Circuit Detection Reference Voltage Accuracy (Drain-Source Monitoring)	dV_{SC_TH500}	VDH, SHx, GND	-5%	—	5%	—	V_{SC_TH} ≥ 500 mV	B
	dV_{SC_TH250}		-8%	—	8%	—	V_{SC_TH} = 250 mV	B
	dV_{SC_TH125}		-15%	—	15%	—	V_{SC_TH} = 125 mV	B
VDS Voltage Blanking Time	t_{VDS_Blank}	GH/Lx	See GDUCR2 Register			µs	Configurable via SPI	B
VGS Undervoltage Voltage Detection Blanking Time	$t_{VGS\_UV\_Blank}$	GH/Lx	See GDUCR2 Register			µs	Configurable via SPI	B
VGS Undervoltage Voltage Detection Blanking Time Accuracy	$dt_{VGS\_UV\_Blank}$	GH/Lx	-10%	—	10%	—		B
VGS Undervoltage Voltage Detection Add-on Blanking Time in GDU Standby Mode	$t_{VGS\_UV\_Blank\_ADO}$	GH/Lx	—	2000	—	µs		B

.....continued

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; –40°C ≤ T_J ≤ 125°C; typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Current Limitation Detection Blanking Time	t_{OC_BT}	GH/Lx	See ILIMCR Register			µs	Configurable via SPI	B
Current Limitation Detection Blanking Time Accuracy	dt_{OC_BT}	GH/Lx	-5%	—	5%	—		B
Edge Blanking Time	t_{EG_Blank}	GH/Lx	See GDUCR2 Register			µs	Configurable via SPI	B
Edge Blanking Time Accuracy	dt_{EG_Blank}	GH/Lx	-5%	—	5%	—		B
Cross Conduction Protection Time	t_{CC}	GH/Lx	See GDUCR1 Register			µs	Configurable via SPI	B
Cross Conduction Protection Time Accuracy	dt_{CC}	GH/Lx	-5%	—	5%	—		B
Adaptive Deadtime High-side ON Delay Time Range	t_{HON_DEL}	—	See GDUCR3 Register			ns	Configurable via SPI	A
Adaptive Deadtime High-side ON Delay Time Range Accuracy	dt_{HON_DEL}	—	-5%	—	5%	—		A
Adaptive Deadtime Low-side ON Delay Time Range	t_{LON_DEL}	—	See GDUCR3 Register			ns	Configurable via SPI	A
Adaptive Deadtime Low-side ON Delay Time Range Accuracy	dt_{LON_DEL}	—	-5%	—	5%	—		A
Adaptive Deadtime Force to Switch Delay Time	t_{SWTO}	—	See GDUCR2 Register			ns	Configurable via SPI	A
Adaptive Deadtime Force to Switch Delay Time Accuracy	dt_{SWTO}	—	-5%	—	5%	—		A
Low-side Gate-Source Threshold Voltage for Low-side Gate OFF Detection	V_{LOOFF}	—	1.6	1.8	2	V		C
Low-side Drain-Source Threshold Voltage for High-side Gate OFF Detection	V_{SWTH}	—	1.6	1.8	2	V		C
VDS Short Circuit Detection Delay	t_{VDS_DEL}	—	—	—	130	ns	Analog delay for detection VDS short circuit	D
Low-side Gate Drive Voltage	$V_{LOOUTLO}$	—	7.8	—	—	—	V_{VDH} > 5.1V	B
	$V_{LOOUTTYP}$	—	11.5	—	12.5	V	V_{VDH} > 13.8V	B
High-side Gate Drive Voltage	$V_{HIOUTLO}$	—	7.1	—	—	V	V_{VDH} > 5.1V, V_{VG} > 7.8V	B
	$V_{HIOUTTYP}$	—	10.5	—	—	V	V_{VDH} > 13.8V, V_{VG} > 11.5V	B
DAC								
V_{VIO} = 3.3V: ATA6847-3333, ATA6847-5033								
Resolution	—	—	—	7	—	bits		D
Current Limitation Comparator Reference DAC Output Voltage Range	$V_{DACRANGE}$	—	0.35	—	2.97	V		C
Current Limitation Comparator Reference DAC Output Voltage	V_{DACd0}	—	—	0.35	—	V	DAC = d0	A
	V_{DACd31}	—	—	0.99	—	V	DAC = d31	B
	V_{DACd63}	—	—	1.65	—	V	DAC = d63	B
	$V_{DACd127}$	—	—	2.97	—	V	DAC = d127	A

.....continued

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; –40°C ≤ T_J ≤ 125°C; typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Differential Nonlinearity	DNL	—	-50%	—	+50%	LSB		C
Integral Nonlinearilty	INL	—	-0.5%	—	0.5%	FSR	FSR = Full Scale Range	C
Input to Output Delay	t_{delay}	—	—	—	50	µs		C
V_{VIO} = 5V: ATA6847-5050								
Resolution	—	—	—	7	—	bits		D
Current Limitation Comparator Reference DAC Output Voltage Range	$V_{DACRANGE}$	—	0.53	—	4.5	V		C
Current Limitation Comparator Reference DAC Output Voltage	V_{DACd0}	—	—	0.53	—	V	DAC = d0	A
	V_{DACd31}	—	—	1.5	—	V	DAC = d31	B
	V_{DACd63}	—	—	2.5	—	V	DAC = d63	B
	$V_{DACd127}$	—	—	4.5	—	V	DAC = d127	A
Differential Nonlinearity	DNL	—	-50%	—	+50%	LSB		C
Integral Nonlinearity	INL	—	-0.50 %	—	0.50%	FSR		C
Input to Output Delay	t_{delay}	—	—	—	50	µs		C
Current Sense Amplifier and Comparator								
Input Offset Voltage (Initial)	V_{OFS_INIT}	OPPx, OPNx	-3	0	+3	mV		A
Input Offset Temperature Drift	V_{OFS_DRIFT}	OPPx, OPNx	-1	—	+1	mV	0 < V_{CM} < 2V	C
Common Mode Input Range	V_{IN_CM}	OPPx, OPNx	-0.3	—	+2	V		C
Common Mode Rejection Ratio	CMRR	OPPx, OPNx	—	80	—	dB	20 * log((V_{OUT_diff}/V_{IN_diff}) * (V_{IN_CM} / V_{OUT_CM})), 10 kHz	C
Current Sense Amplifier Input Resistance	R_{IN}	OPPx, OPNx	8.2	—	18	kΩ		A
Output Voltage Range	V_{OPO_CMR}	OPOx	0.15	—	V_{VIO} – 0.15	V	I_{OUT} = ±200 µA	A
Output Voltage Offset	V_{OPO_OFS}	OPOx	—	1/16	—	V_{VIO}	OFFSET = 2'b00 (default)	A
		OPOx	—	1/8	—	V_{VIO}	OFFSET = 2'b01	A
		OPOx	—	1/4	—	V_{VIO}	OFFSET = 2'b10	A
		OPOx	—	1/2	—	V_{VIO}	OFFSET = 2'b11	A
Gain	Av	OPOx	—	8	—	V/V	GAIN = 2'b00, VDIFF = ±180 mV, V_{VIO} = 3.3V	B
		OPOx	—	16	—	V/V	GAIN = 2'b01, VDIFF = ±90 mV, V_{VIO} = 3.3V	B
		OPOx	—	32	—	V/V	GAIN = 2'b10, VDIFF =± 45 mV, V_{VIO} = 3.3V	B
		OPOx	—	64	—	V/V	GAIN = 2'b11, VDIFF = ±22.5 mV, V_{VIO} = 3.3V	B

.....continued

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; –40°C ≤ T_J ≤ 125°C; typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Settling Time	t_{settle}	OPOx	—	—	300	ns	Rise/Fall times for VDIFF = ±1V condition, settling time measured from VDIFF applied from/to 20/80% of the final value be reached, gain = 8	A
Gain Accuracy	dAv	OPOx	-1.5	—	2	%	GAIN = 16, GAIN = 32, GAIN = 64,	C
					4		GAIN = 8	C
Gain Bandwidth Product of CSA OpAmp	GBWP	—	—	40	—	MHz		D
Input Offset Voltage Reference Buffer (Initial)	$V_{OFS\_INIT\_BUF}$	—	-3.2	1	+3.9	mV		D
Input Offset Voltage Temperature Drift of the Reference Buffer	$V_{OFS\_DRIFT\_BUF}$	—	-1	—	+1	mV		D
Current Limitation Detection Comparator Hysteresis	$V_{OV\_COMP\_HYS}$	—	—	10	—	mV		C
Current Limitation Detection Comparator Common Mode Input Range	$V_{OV\_COMP\_CMR}$	—	0.15	—	V_{VIO} – 0.15	V		C
Current Limitation Detection Comparator Input Offset	$V_{OV\_COMP\_OFSET}$	—	-6	—	+6	mV		A
CSA Start-up Time	t_{CSA_START}	—	—	—	20	µs		D
Back EMF								
Input to Output Delay	—	—	—	—	500	ns	V_{SHx} with 500 mV steps	C
BEMFx High-level Output Voltage	V_{BEMFx_H}	BEMFx	V_{VIO} – 0.4	—	V_{VIO}	V	I = -1 mA	A
BEMFx Low-level Output Voltage	V_{BEMFx_L}	BEMFx	-	—	0.4	V	I = 1 mA	A
OFF-state Leakage Current	I_{leak_BEMFx}	BEMFx	-0.5	—	+0.5	µA		A
Back EMF Detection Input Offset Error			-300	—	+300	mV		C
SDI, SCK, NCS, NIHx, ILx (V_{VIO} refers to the selected µC supply)								
High-level Input Voltage	V_{SDI_H}, V_{SCK_H}, V_{NCS_H}, V_{NIHx_H}, V_{ILx_H}	SDI, SCK, NCS, NIHx, ILx	0.7 × V_{VIO}	—	V_{VIO} + 0.3	V		A
Low-level Input Voltage	V_{SDI_L}, V_{SCK_L}, V_{NCS_L}, V_{NIHx_L}, V_{ILx_L}	SDI, SCK, NCS, NIHx, ILx	-0.3	—	0.3 × V_{VIO}	V		A
Input Current	I_{leak_SDI}, I_{leak_SCK}, I_{leak_NCS}, I_{leak_NIHx}, I_{leak_ILx}	SDI, SCK, NCS, NIHx, ILx	-5	—	+5	µA		A

.....continued

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; –40°C ≤ T_J ≤ 125°C; typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Pull-up Resistance on the Pins NCS, NIHx	R_{PU_NCS}, R_{PU_NIHx}	NCS, NIHx	40	60	80	kΩ		A
Pull-down Resistance on the SCK Pin, ILx	R_{PD_SCK}, RP_{D_ILx}	SCK, ILx	40	60	80	kΩ		A
SDO (V_{VIO} refers to the selected µC supply)								
High-level Output Voltage	V_{SDO_H}	SDO	V_{VIO} - 0.4	—	—	V	I = -4 mA	A
Low-level Output Voltage	V_{SDO_L}	SDO	—	—	0.4	V	I = 4 mA	A
Off-state Leakage Current	I_{leak_SDO}	SDO	-5	—	5	µA		A
WAKE								
Input Rising Threshold	$V_{WAKE\_H\_TH}$	WAKE	1	1.6	2.05	V		A
Input Falling Threshold	$V_{WAKE\_L\_TH}$	WAKE	0.75	1.05	1.5	V		A
Input Hysteresis	V_{WAKE_HYS}	WAKE	200	—	600	mV		A
Wake Pull-up Ressistor	—	—	—	1000	—	kΩ		A
Filter Time Delay	t_{local_wu}	—	40	—	180	µs		A
NRES, NIRQ (open drain output pin, V_{VIO} refers to the selected µC supply)								
Low-level Output Voltage	V_{NRESL}, V_{NIRQL}	NRES, NIRQ	—	0.2	0.4	V	I_{NRES} = 2 mA, I_{NIRQ} = 2 mA	A
Watchdog Reset Time	t_{Reset}	NRES	According to the setting in the WDCR2 Register			ms	C_{NRES} = 20 pF	B
Pull-up Resistance	R_{PU}	NRES, NIRQ	6.5	10	13.5	kΩ	Diode in series with pull-up resistance, V_{NRES} < 2V	A
High-level Input Voltage	V_{NRES_H}	NRES	0.7 × V_{VIO}	—	—	V		A
Low-level Input Voltage	V_{NRES_L}	NRES	—	—	0.3 × V_{VIO}	V		A
Input Pulse Length	t_{NRES_input}	NRES	75	—	—	µs		B
Watchdog Long Open Window	t_{LW}	NRES	560	—	700	ms		B
Event Capture Delay Time	$t_{d\_evt\_cap}$	NIRQ	0.9	—	1.1	ms		B
Limp Home								
Low-level Output Voltage	V_{LH}	LH	—	—	0.2	V	V_{VS} > 4.2V, I_{LH} = 4 mA	A
Leakage Current	I_{leak_LH}	LH	—	—	2	µA	V_{LH} < 40V	A
INH								
Output ON Voltage	V_{INH_ON}	INH	V_{VS} – 0.8	—	V_{VS}	V	I_{INH} = -180 µA	A
Leakage Current	I_{leak_INH}	INH	—	—	2	µA	Leakage of grounded INH pin in OFF Mode	A
SPI Timing								
Clock Cycle Time	t_{clk}	SPI	250	—	—	ns	Normal/Standby/Sleep mode	D
SPI Enable Lead Time	t_{ENLEAD}	SPI	50	—	—	ns	Normal/Standby/Sleep mode	D
SPI Enable Lag Time	t_{ENLAG}	SPI	50	—	—	ns	Normal/Standby/Sleep mode	D

.....continued

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; –40°C ≤ T_J ≤ 125°C; typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Clock HIGH Time	t_{clk_H}	SPI	125	—	—	ns	Normal/Standby/Sleep mode	D
Clock LOW Time	t_{clk_L}	SPI	125	—	—	ns	Normal/Standby/Sleep mode	D
Data Input Set-up Time	t_{setup}	SPI	50	—	—	ns	Normal/Standby/Sleep mode	D
Data Input Hold Time	t_{hold}	SPI	50	—	—	ns	Normal/Standby/Sleep mode	D
Data Output Valid Time	t_{dout_v}	SPI	—	—	50	ns	Normal/Standby/Sleep mode	D
Chip Select Pulse Width HIGH	t_{NCS_pw}	SPI	250	—	—	ns	Normal/Standby/Sleep mode, SDO pin; CL = 20 pF	D
VDD- Timings								
Startup Time After Power-on	$t_{startup}$	VS	—	2.8	4.7	ms	From V_{VS} rises above the power-on detection threshold V_{VS_PWRON} until V_{VDD1} > $V_{VDD1\_UV\_Clear}$ or V_{VDD2} > $V_{VDD2\_UV\_Clear}$	C
Temperature Protection								
Overtemperature Protection Shutdown Threshold	T_{OT_sdwn}	—	170	180	190	°C	Junction Temperature	B
Overtemperature Protection Release Threshold	$T_{OT\_release}$	—	155	165	175	°C	Junction Temperature	B
Overtemperature Protection Prewarning Set Threshold	$T_{OT\_PREW\_Set}$	—	150	160	170	°C	Junction Temperature	B
Overtemperature Protection Prewarning Clear Threshold	$T_{OT\_PREW\_Clear}$	—	135	145	155	°C	Junction Temperature	B
Motor Line Diagnostic								
Logic High Detection Threshold	$V_{thSHxHI}$	SHx	—	V_{VDH} – 1.75	—	V	Set MLDCR MLDEN Check MLDRR DIAG_xx	A
Logic Low Detection Threshold	$V_{thSHxLO}$	SHx	—	1.75	—	V	Set MLDCR MLDEN Check MLDRR DIAG_xx	A
Sink Current	$I_{SHxSink}$	SHx	4.4	—	7.2	mA	Set MLDCR SINKx and MLDCR MLDEN V_{SH} > 3V	A
Source Current	$I_{SHxSource}$	SHx	1	—	1.75	mA	Set MLDCR SOURCEx MLDCR MLDEN V_{SH} < V_{DH} – 3V	A

LEGEND: A = 100% Tested, B = 100% Tested through indirect testing or calculation, C = Characterized, not production tested, D = Simulated, not production tested

6.3 Thermal Characteristics (Submit Feedback)

Parameters	Symbol	Min.	Typical	Max.	Unit
Package (no. of pins)					
5.0 mm x 5.0 mm QFN (40L)	R_{thJA}	—	35	—	°C/W
	R_{thJC}	—	10	—	

Note 1: 4-Layer JC51-5 standard board, natural convection.

7. Typical Performance Curves (Submit Feedback)

Figure 7-1. Current Sense Amplifiers Gain Accuracy

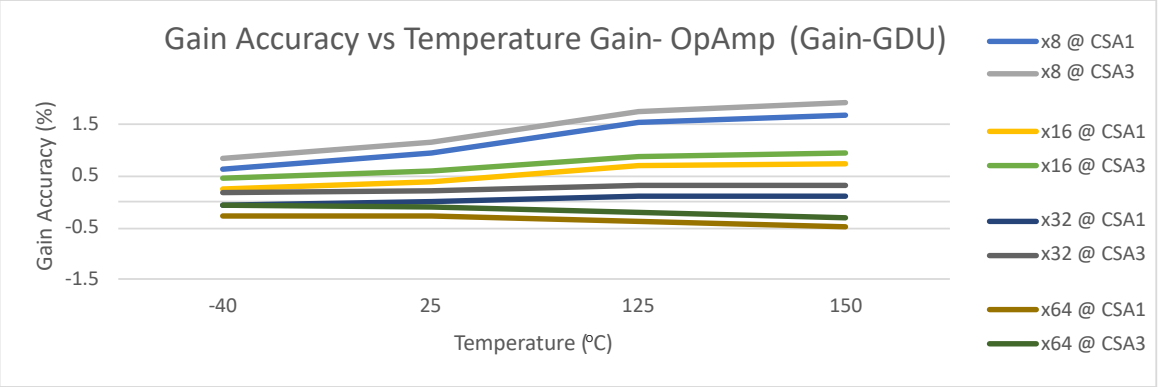


Figure 7-2. Current Sense Amplifiers Gains Mismatch

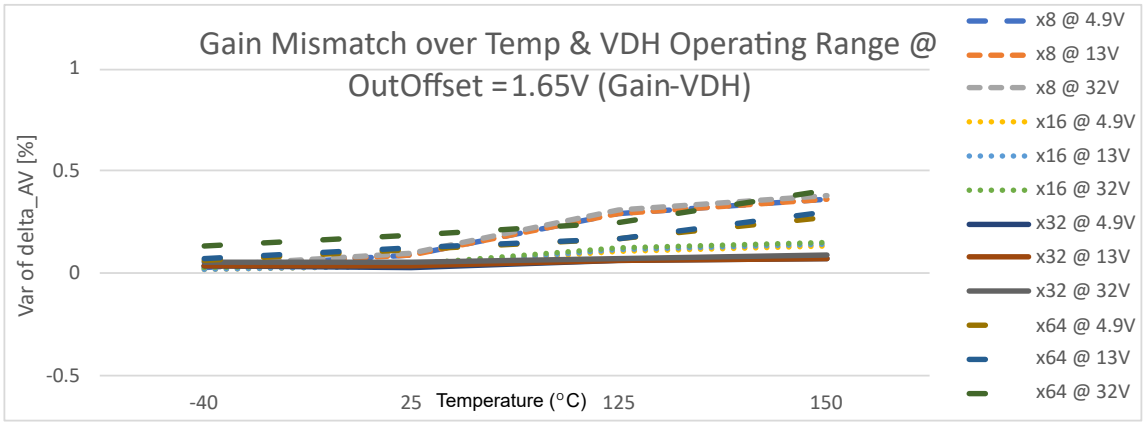


Figure 7-3. Current Sense Amplifiers Output Offset

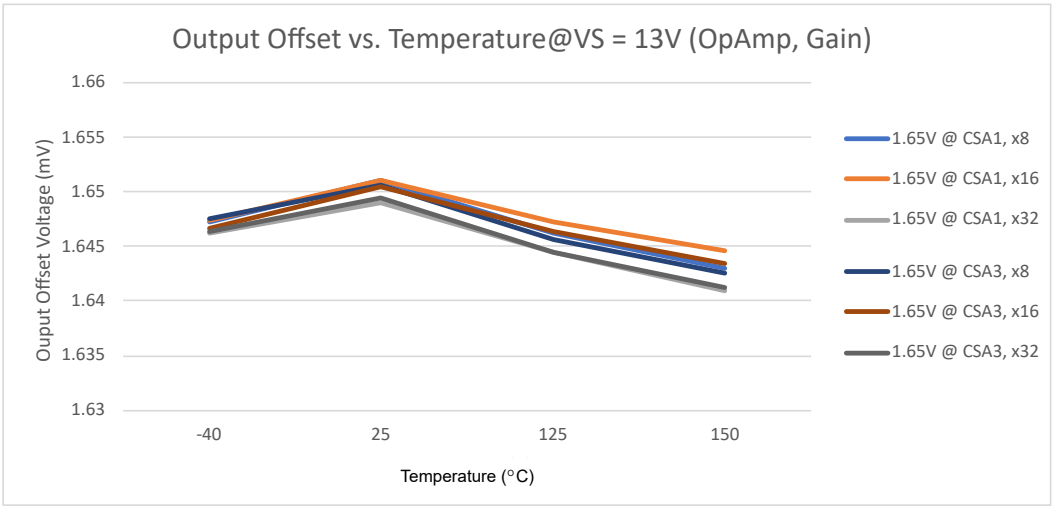


Figure 7-4. Gate Driver Unit Slew Rate Control

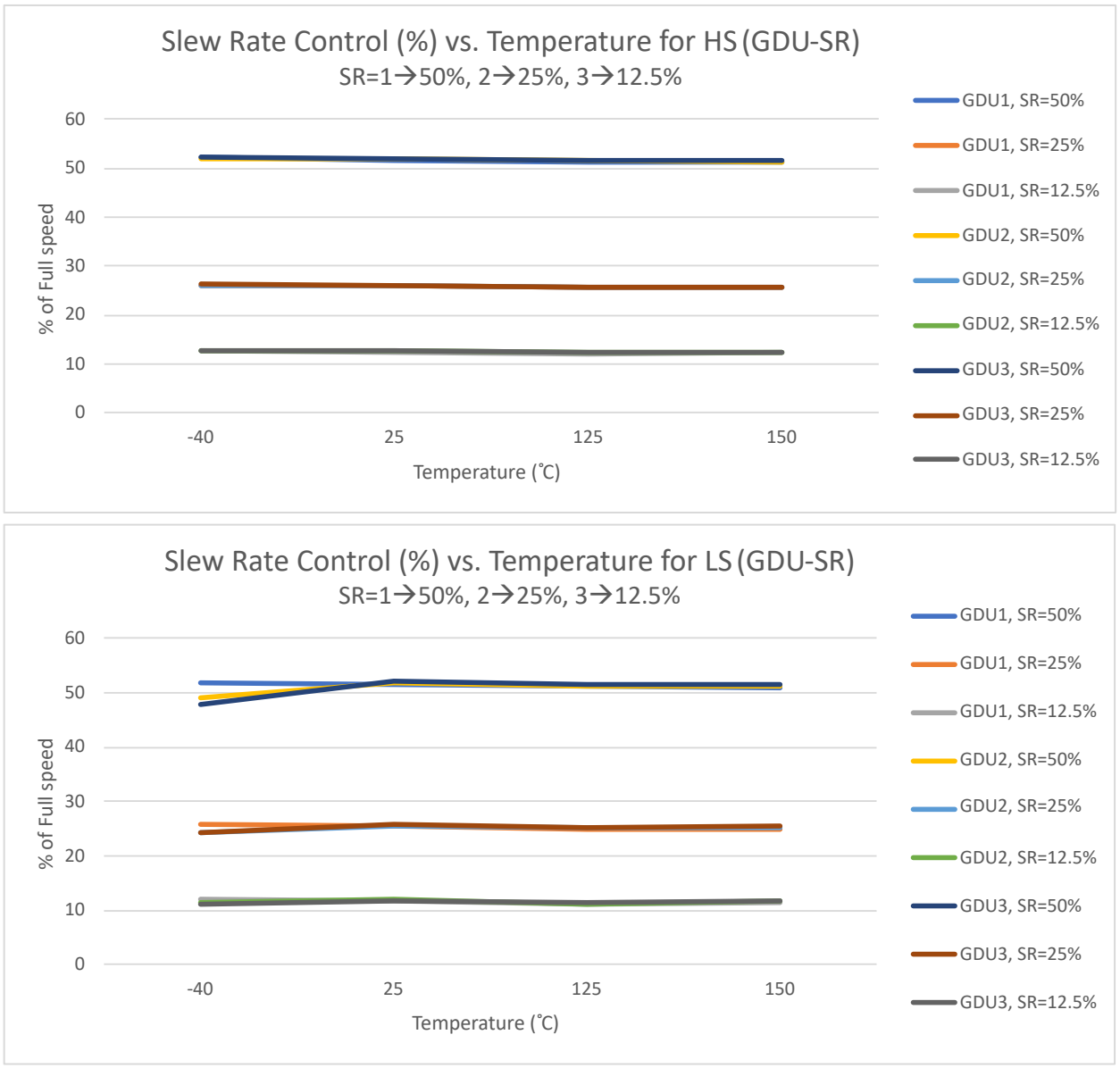
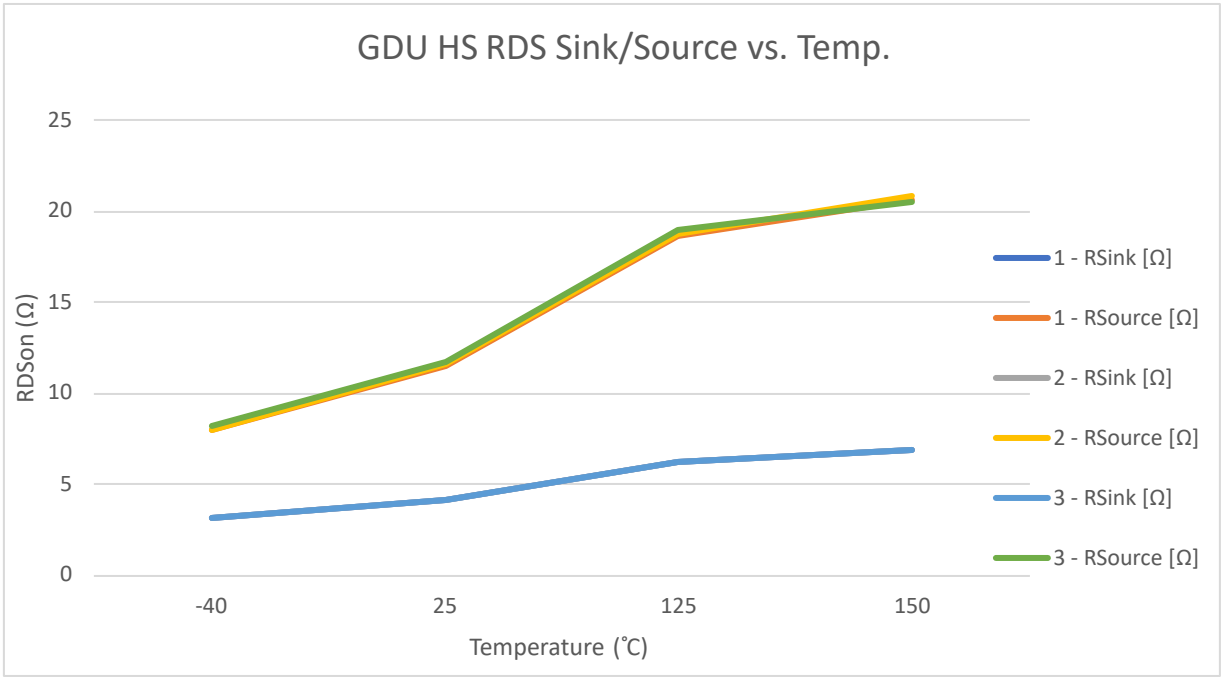


Figure 7-5. Gate Driver Unit Sink/Source ON Resistance vs Temperature



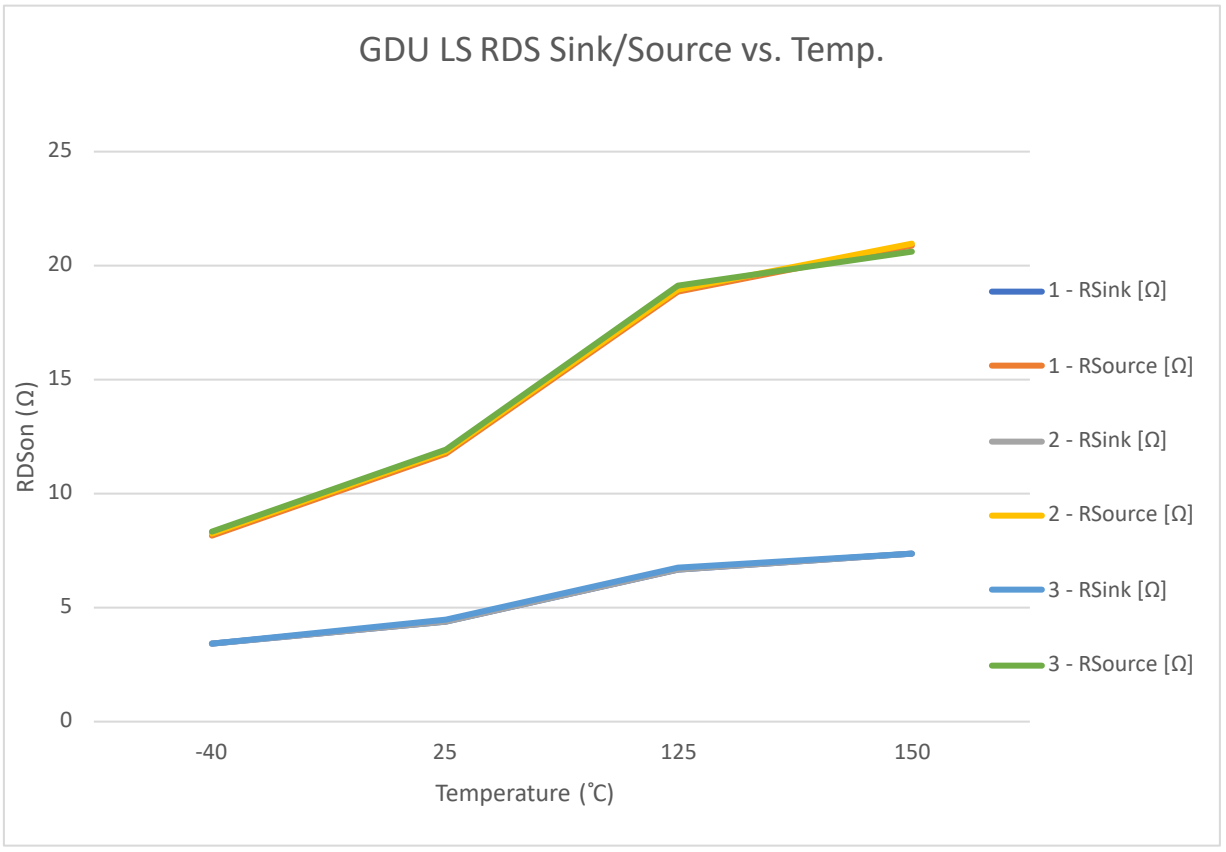
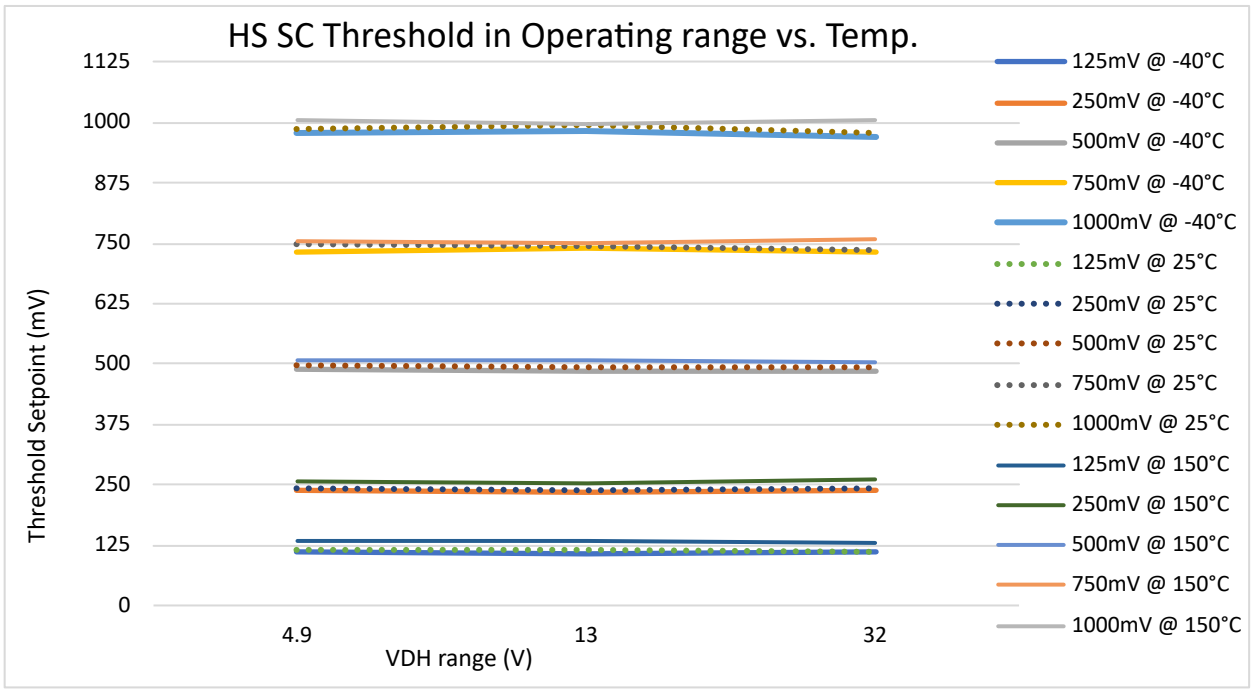


Figure 7-6. Gate Driver Unit Short Circuit Protection Threshold



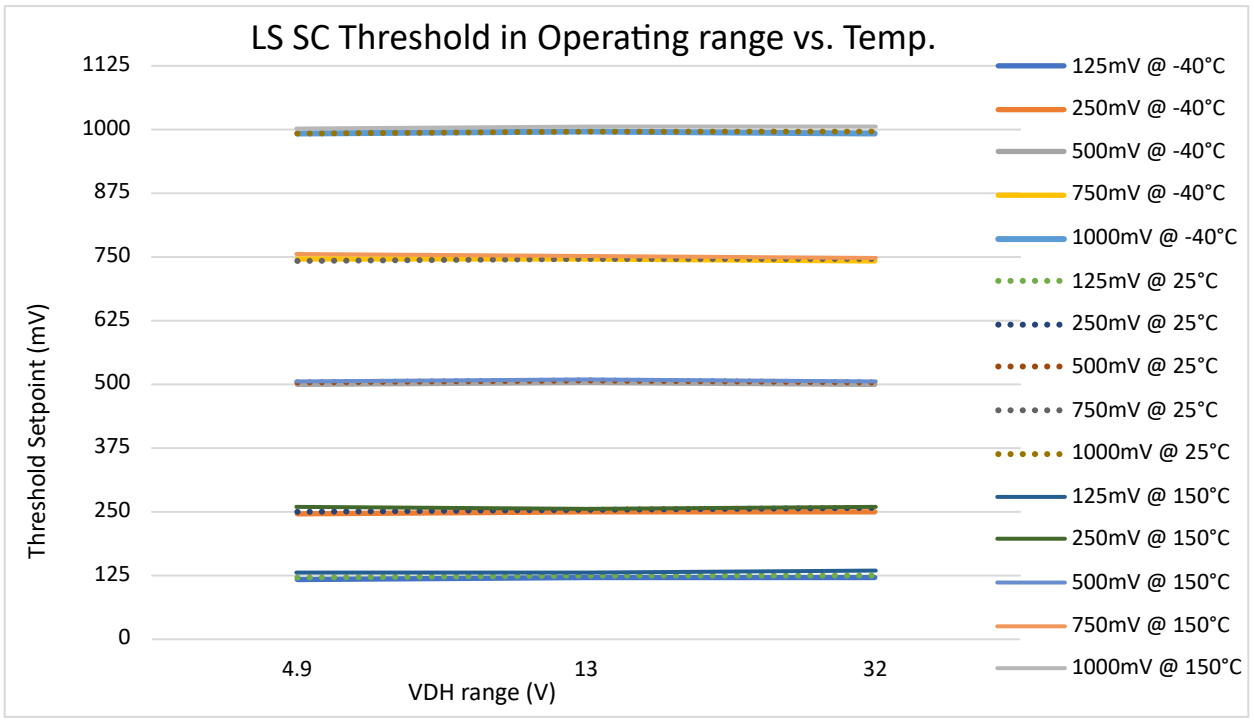


Figure 7-7. Gate Driver Unit Propagation and Mismatch Delay, Rising/Falling Edges

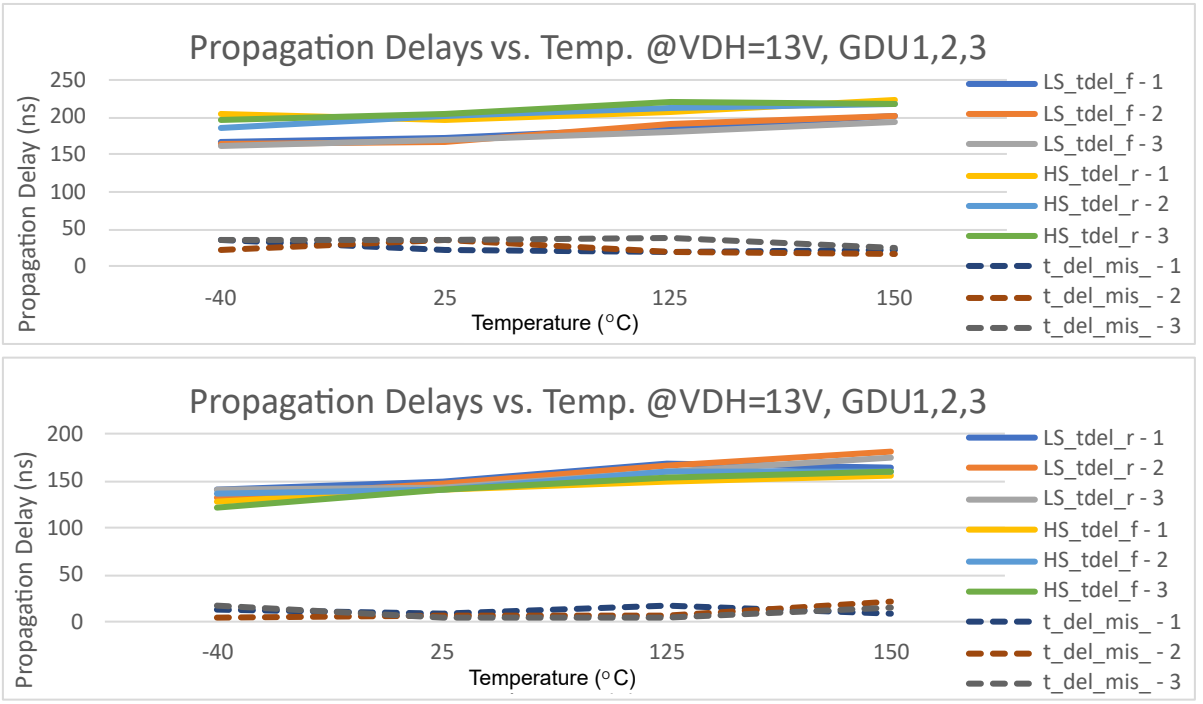
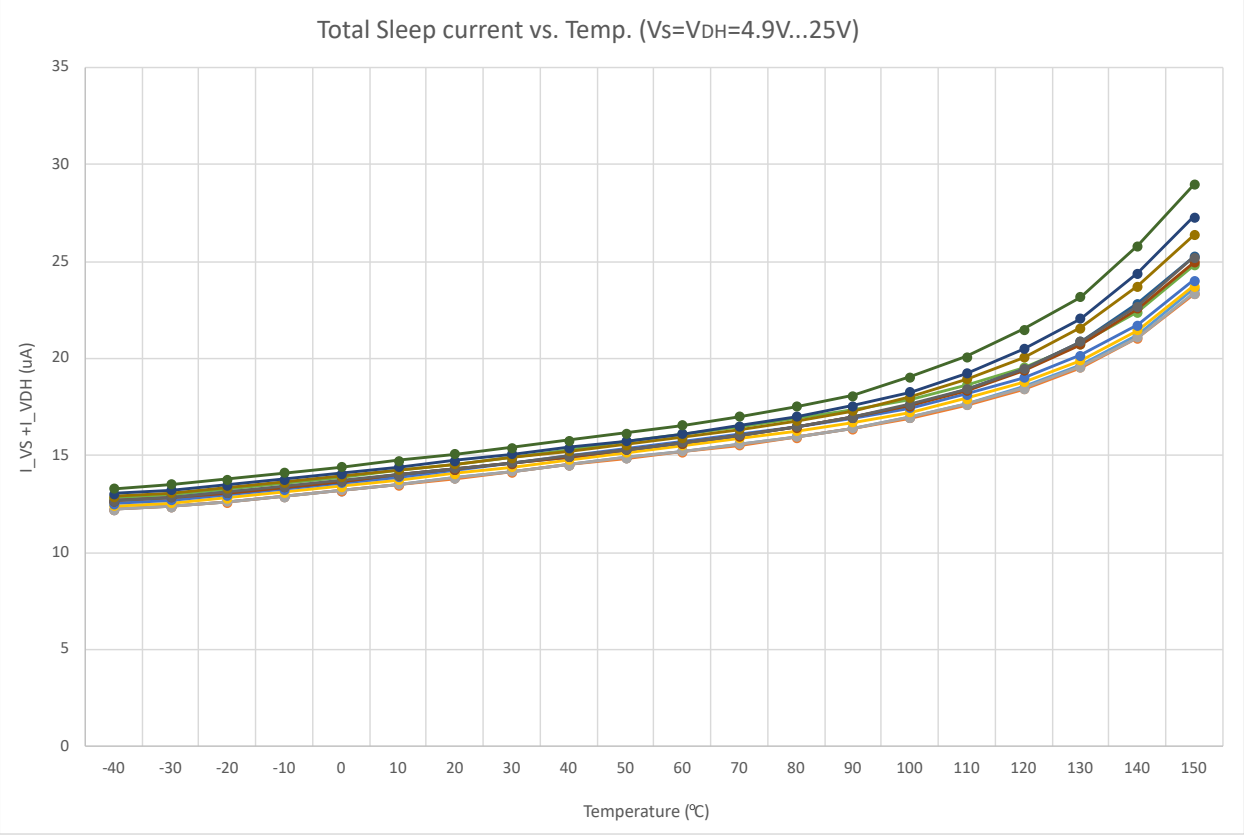


Figure 7-8. Total Sleep Current versus Temperature



8. Application Information (Submit Feedback)

8.1 Startup Initialization (Submit Feedback)

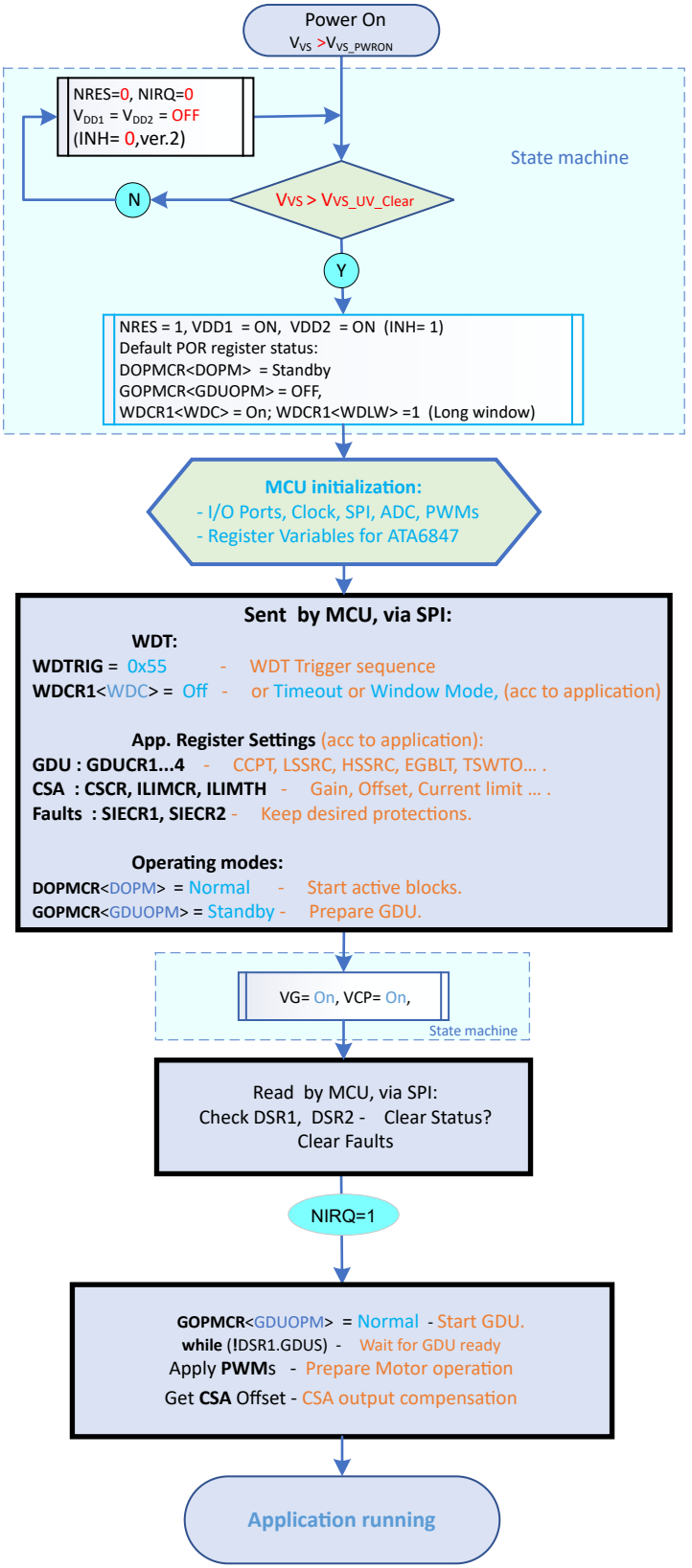
By default, the ATA6847 starts with the watchdog enabled. It is necessary to follow the start-up procedure to enter a normal operation or to reconfigure the watchdog.

As soon as the microcontroller output voltage rises up to the valid operating range, the ATA6847 transitions to Standby mode and deasserts the NRES pin. By default, the WDT starts in Time-out mode. The first microcontroller must trigger the watchdog within the long open window (t_{LW}).

After the first watchdog trigger, the ATA6847 is ready for configuration via SPI. The application should follow the following start-up sequence:

- Once the microcontroller SPI has been initialized, a valid WDT trigger sequence must be sent to the ATA6847 (WDTRIG = `0x55`).
- The watchdog must be configured according to application requirements.
- The remaining ATA6847 configuration registers must be set according to application requirements.

Figure 8-1. ATA6847 Simplified Start-up Procedure



8.2 B-EMF Motor Control Mode (Submit Feedback)

The closed loop of a BLDC motor control is a Phase-Locked Loop (PLL) based on the rotor position. Note that this inner loop does not attempt to modify the position of the rotor; instead, it modifies the commutation times to match whatever position the rotor has. An outer speed loop changes the rotor velocity, and the commutation loop locks to the rotor position to commutate the phases at the correct trigger times.

The back EMF sampler monitors the motor phase voltages. The neutral point Virtual Null simulator calculates the neutral point of the motor, based on the following equation:

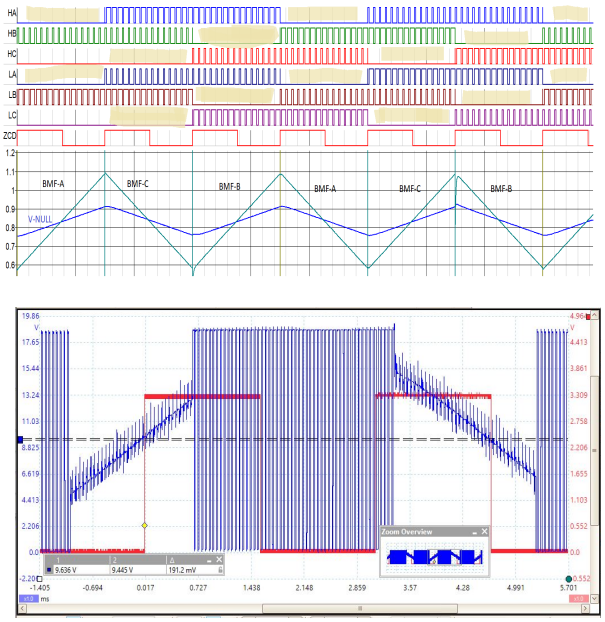
$$VN = (Ph_A + Ph_B + Ph_C)/3$$

The three motor phase voltages are compared with the neutral point. The outputs of the three comparators are available synchronously for estimating the zero-crossing time events accordingly. In '*Star wound*' motor configuration, no extra wire connection is required. For '*Delta wound*' motors, there is no physical neutral point available. The reference point must be estimated anyway.

As the microcontroller knows which motor phase is floating and which two phases are driven to low and high, it is always capable of monitoring the floating phase's comparator output.

When the B-EMF signal crosses the neutral point or Virtual Null (VN), the Zero-Crossing Detector (ZCD) will switch the ZC_X signal. The host controller may use this signal as a '*30 degrees before crossing*' reference point. The host controller must commutate the system after 30 degrees of electrical rotation occurs. See Figure 8-2.

Figure 8-2. Basic Principles



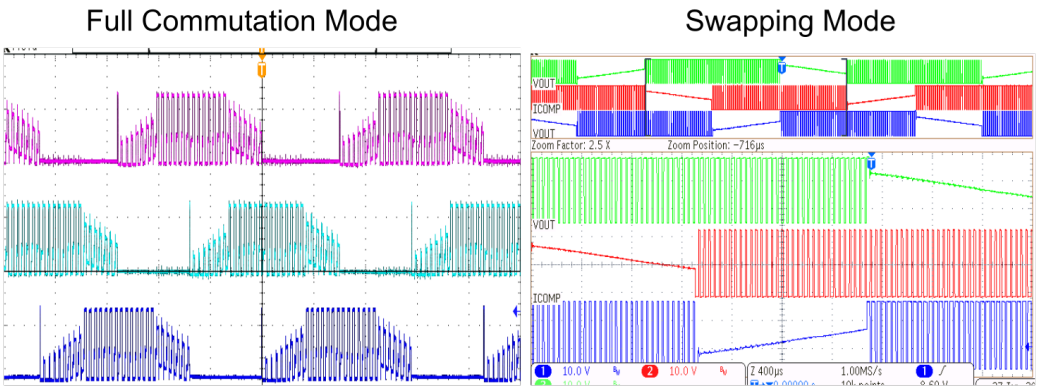
The Zero-Crossing Detection (ZCD) method is typically used in *six-step per electrical revolution* commutation strategies. The motor is driven by energizing two windings at a time. One winding stays unenergized at all times, and the voltage (back EMF or B-EMF) on that unenergized winding can be monitored to determine the rotor position.

For more accuracy in rotor angle estimation, it is recommended to use complementary PWMs for the H/L side MOSFET bridge. The comparative B-EMF waveforms are shown below.

When the motor being driven is at rest, the B-EMF voltage is equal to zero. The motor rotor needs to be initially rotated for the B-EMF sensor to lock onto the rotor position and commutate the motor. It is necessary to bring the rotor from rest up to a speed fast enough to generate sufficient B-EMF voltage (enough to allow the B-EMF sampler to send it).

Depending on the motor construction and the rotor speed, filtering algorithms are required for stable Zero-Crossing Detection (ZCD).

Figure 8-3. Full Commutation and Swapping Modes

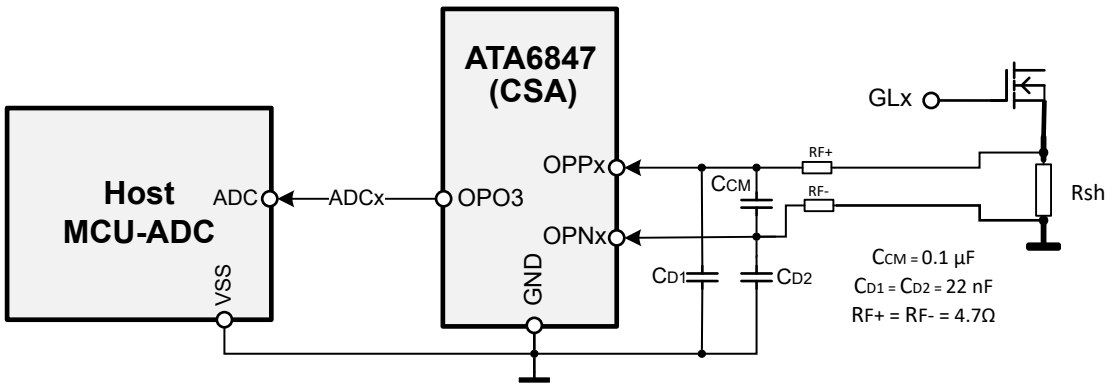


8.3 Current Sense Amplifier Signal Filtering (Submit Feedback)

For high current MC applications, it is required to use a small current sense shunt and a low gain for CSA, in order to match the output signal with the MCU's ADC range.

Due to the CSA's large bandwidth, the sharp parasitic current spikes induced by the external MOSFET bridge commutation can cause the output to be clamped at the rail limits and affect the motor control processing. A filtering method for the signal can be implemented (see CSA Filtering Circuit).

Figure 8-4. CSA Filtering Circuit

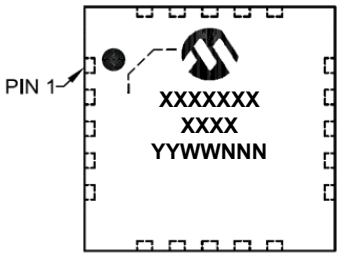


For high efficiency, the filter components should be placed near the CSA inputs. In order to not affect the differential gain and the initial settled offset, the input resistor should stay as low as possible (4.7-10 Ohm).

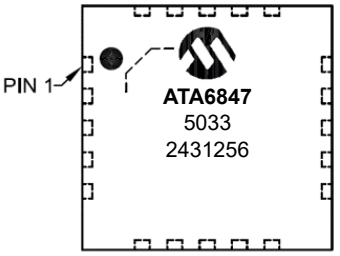
9. Package Information (Submit Feedback)

Package Marking Information

40-VQFN (5x5x0.9 mm^3)



Example:

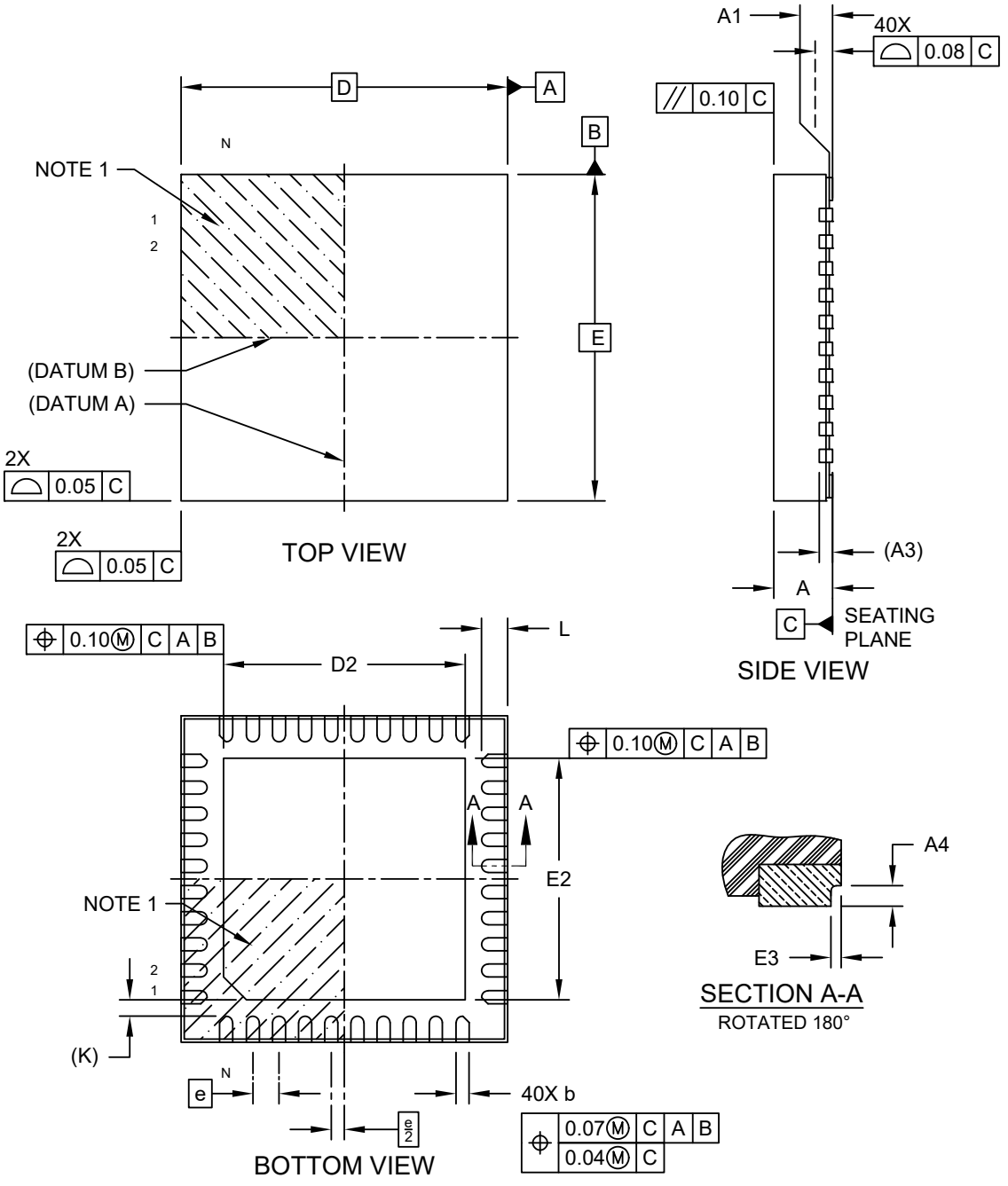


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

40-Lead Very Thin Plastic Quad Flat, No Lead Package (NHX) - 5x5x0.9 mm Body [VQFN] With 3.7x3.7 mm Exposed Pad and Wettable Flanks

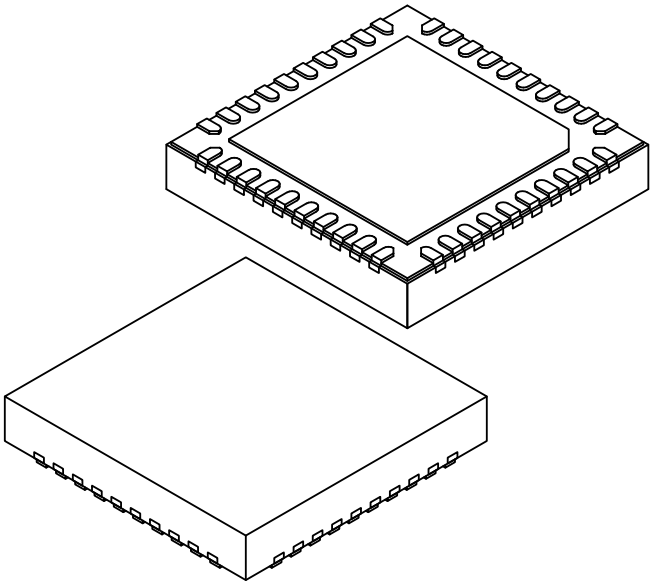
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-425 Rev D Sheet 1 of 2

40-Lead Very Thin Plastic Quad Flat, No Lead Package (NHX) - 5x5x0.9 mm Body [VQFN] With 3.7x3.7 mm Exposed Pad and Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		40	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Wettable Flank Height	A4	0.10	–	0.19
Wettable Flank Width	E3	–	–	0.085
Terminal-to-Exposed-Pad	K		0.25 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

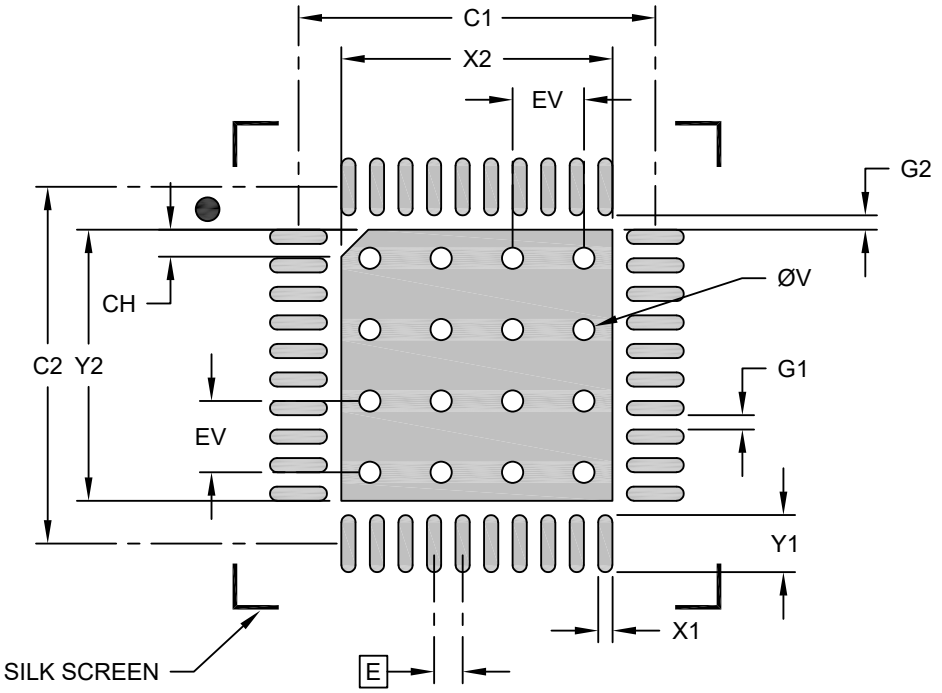
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-425 Rev D Sheet 2 of 2

40-Lead Very Thin Plastic Quad Flat, No Lead Package (NHX) - 5x5x0.9 mm Body [VQFN] With 3.7x3.7 mm Exposed Pad and Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Chamfer	CH		0.38	
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.80
Contact Pad to Pad (X36)	G1	0.20		
Contact Pad to Center Pad (X40)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2425 Rev D

10. Revision History (Submit Feedback)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	10/2024	Initial release of this document.

Microchip Information

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

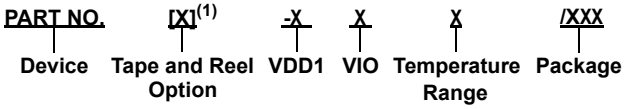
- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Device:	ATA6847: 3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module, Sleep Mode and LIN Transceiver	
Tape and Reel option(1):	T	Tape and Reel (3300/Reel – QFN package)
VDD1:	50	5.0V
	33	3.3V **Note:** INH instead of VDD2 for ATA6847-3333
VIO:	50	VIO = 5.0V
	33	VIO = 3.3V
Temperature:	E	-40°C to +125°C
Package:	NHX	5x5 mm QFN 40L, Very Thin Quad Flatpack No-Leads, Wettable Flanks, copper wire with Exposed Pad.

Examples:

- ATA6847T-5050E/NHX: Tape and Reel, VDD1 = VIO = 5V, 5x5 mm QFN 40L package
- ATA6847T-3333E/NHX: Tape and Reel, VDD1 = VIO = 3.3V, 5x5 mm QFN 40L package
- ATA6847T-5033E/NHX: Tape and Reel, VDD1 = 5V, VIO = 3.3V, 5x5 mm QFN 40L package

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. RoHS compliant, maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (CI) and less than 0.15% (1500) total Bromine (Br) and Chlorine (CI) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.
3. Contact your local Microchip sales office to request automotive qualified variants for other package types.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

Trademarks

ISBN: 978-1-6683-0335-1

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com	**Australia - Sydney** Tel: 61-2-9868-6733	**India - Bangalore** Tel: 91-80-3090-4444	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393
Atlanta Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455	**China - Beijing** Tel: 86-10-8569-7000	**India - New Delhi** Tel: 91-11-4160-8631	**Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829
Austin, TX Tel: 512-257-3370	**China - Chengdu** Tel: 86-28-8665-5511	**India - Pune** Tel: 91-20-4121-0141	**Finland - Espoo** Tel: 358-9-4520-820
Boston Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088	**China - Chongqing** Tel: 86-23-8980-9588	**Japan - Osaka** Tel: 81-6-6152-7160	**France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79
Chicago Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075	**China - Dongguan** Tel: 86-769-8702-9880	**Japan - Tokyo** Tel: 81-3-6880- 3770	**Germany - Garching** Tel: 49-8931-9700
Dallas Addison, TX Tel: 972-818-7423 Fax: 972-818-2924	**China - Guangzhou** Tel: 86-20-8755-8029	**Korea - Daegu** Tel: 82-53-744-4301	**Germany - Haan** Tel: 49-2129-3766400
Detroit Novi, MI Tel: 248-848-4000	**China - Hangzhou** Tel: 86-571-8792-8115	**Korea - Seoul** Tel: 82-2-554-7200	**Germany - Heilbronn** Tel: 49-7131-72400
Houston, TX Tel: 281-894-5983	**China - Hong Kong SAR** Tel: 852-2943-5100	**Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906	**Germany - Karlsruhe** Tel: 49-721-625370
Indianapolis Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380	**China - Nanjing** Tel: 86-25-8473-2460	**Malaysia - Penang** Tel: 60-4-227-8870	**Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44
Los Angeles Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800	**China - Qingdao** Tel: 86-532-8502-7355	**Philippines - Manila** Tel: 63-2-634-9065	**Germany - Rosenheim** Tel: 49-8031-354-560
Raleigh, NC Tel: 919-844-7510	**China - Shanghai** Tel: 86-21-3326-8000	**Singapore** Tel: 65-6334-8870	**Israel - Hod Hasharon** Tel: 972-9-775-5100
New York, NY Tel: 631-435-6000	**China - Shenyang** Tel: 86-24-2334-2829	**Taiwan - Hsin Chu** Tel: 886-3-577-8366	**Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781
San Jose, CA Tel: 408-735-9110 Tel: 408-436-4270	**China - Shenzhen** Tel: 86-755-8864-2200	**Taiwan - Kaohsiung** Tel: 886-7-213-7830	**Italy - Padova** Tel: 39-049-7625286
Canada - Toronto Tel: 905-695-1980 Fax: 905-695-2078	**China - Suzhou** Tel: 86-186-6233-1526	**Taiwan - Taipei** Tel: 886-2-2508-8600	**Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340
	China - Wuhan Tel: 86-27-5980-5300	**Thailand - Bangkok** Tel: 66-2-694-1351	**Norway - Trondheim** Tel: 47-72884388
	China - Xian Tel: 86-29-8833-7252	**Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Poland - Warsaw** Tel: 48-22-3325737
	China - Xiamen Tel: 86-592-2388138		**Romania - Bucharest** Tel: 40-21-407-87-50
	China - Zhuhai Tel: 86-756-3210040		**Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91
			Sweden - Gothenberg Tel: 46-31-704-60-40
			Sweden - Stockholm Tel: 46-8-5090-4654
			UK - Wokingham Tel: 44-118-921-5800 Fax: 44-118-921-5820