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Product Information Notification

PIN

Product Group: SIL/Sunday February 16, 2025/PIN-SIL-000501-2025-REV-0

SiC575A and SiC675A Datasheet Update

For further information, please contact your regional Vishay office.

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Description of Change: Update Pin Configuration and Product Summary to correct previous errors.

Reason for Change: Update and corrected Data Sheet

Expected Influence on Quality/Reliability/Performance: There will be no effect on performance, quality or reliability.

Part Numbers/Series/Families Affected: SIC575ACD-T1-GE3, SIC675ACD-T1-GE3,

Vishay Brand(S): Vishay Siliconix

Time Schedule:

Start Shipment Date: Monday March 17, 2025

Sample Availability: Samples are available now

Product Identification: Lot Number and Country of Origin

Qualification Data: Available upon Request

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PIN-SIL-000501-2025-REV-0

Data Sheet comparison

February 2025

Data Sheet of SIC575A

Updated Datasheet

PIN CONFIGURATION		
PIN NUMBER	NAME	FUNCTION
1	T_{MON}	Temperature monitor output. For multiphase, the T_{MON} pins can be connected together as a common bus; the highest voltage (representing the highest temperature) is sent to the PWM controller. T_{MON} is pulled high (V_{CC_3V3}) to indicate an over-temperature fault. T_{MON} can be turned off or used for other functions via serial digital interface. No more than 470 pF total capacitance can be directly connected across the T_{MON} and GND pins; with a series resistor, a higher capacitance load is
2	$SDIF_{DATA}$	Serial digital interface data input and output; connect 1 kΩ to 3.3 V
3	$SDIF_{CLK}$	Serial digital interface clock input
4	PV_{CC_5V}	+5 V logic and gate drive bias supply; place a high quality low ESR ceramic capacitor (~1 µF/X7R) in close proximity from this pin to A_{GND}
5, 25	GL	No connect (this is a low side gate driver output (GL), optional to monitor for system debugging)
6, 7, 13, 14	P_{GND}	Power ground (source connection of low side MOSFET)
8, 9, 10, 11, 12	SW	Switching junction node between HFET source and LFET drain; connect directly to output inductor
15, 16, 17	V_{IN}	Input of power stage (to drain of high side MOSFET); place at least two ceramic capacitors (10 µF or higher, X5R or X7R) in close proximity across V_{IN} and P_{GND}; for optimal performance, place as many vias as possible in the bottom side V_{IN} paddle
18	PHASE	Return of boot capacitor; internally connected to SW_{node} so no external routing required for SW connection
19	BOOT	Floating bootstrap supply pin for the upper gate drive; place a high quality low ESR ceramic capacitor (0.1 µF/X7R to 0.22 µF/X7R) in close proximity across BOOT and PHASE pins
20	PWM	PWM input of gate driver, compatible with 3.3 V tri-state PWM signal
21	V_{CC_3V3}	+3.3 V logic bias supply; place a high quality low ESR ceramic capacitor (~1 µF/X7R) in close proximity from this pin to GND
22,25	AGND	A_{GND} of driver IC
23	REF_{IN}	Input for external reference voltage for I_{MON} signal; this voltage should be between 0.8 V and 1.3 V; connect REF_{IN} to the appropriate current sense input of the controller; place a high quality low ESR ceramic capacitor (~ 0.1 µF) in close proximity from this pin to A_{GND}
24	I_{MON}	Current monitor output, referenced to REF_{IN}; pulls low to indicate ZCD in DCM mode; connect the I_{MON} output to the appropriate current sense input of the controller; no more than 56 pF capacitance can be directly connected across the I_{MON} and REF_{IN} pins

Previous Datasheet

PIN CONFIGURATION		
PIN NUMBER	NAME	FUNCTION
1	T_{MON}	Temperature monitor output. For multiphase, the T_{MON} pins can be connected together as a common bus; the highest voltage (representing the highest temperature) is sent to the PWM controller. T_{MON} is pulled high (V_{CC_3V3}) to indicate an over-temperature fault. T_{MON} can be turned off or used for other functions via serial digital interface. No more than 470 pF total capacitance can be directly connected across the T_{MON} and GND pins; with a series resistor, a higher capacitance load is
2	SDIFD	Serial digital interface data input and output; connect 1 kΩ to 3.3 V
3	SDIFC	Serial digital interface clock input
4	PV_{CC_5V}	+5 V logic and gate drive bias supply; place a high quality low ESR ceramic capacitor (~1 µF/X7R) in close proximity from this pin to A_{GND}
5, 25	GL	No connect (this is a low side gate driver output (GL), optional to monitor for system debugging)
6, 7, 13, 14	P_{GND}	Power ground (source connection of low side MOSFET)
8, 9, 10, 11, 12	SW	Switching junction node between HFET source and LFET drain; connect directly to output inductor
15, 16, 17	V_{IN}	Input of power stage (to drain of high side MOSFET); place at least two ceramic capacitors (10 µF or higher, X5R or X7R) in close proximity across V_{IN} and P_{GND}; for optimal performance, place as many vias as possible in the bottom side V_{IN} paddle
18	PHASE	Return of boot capacitor; internally connected to SW_{node} so no external routing required for SW connection
19	BOOT	Floating bootstrap supply pin for the upper gate drive; place a high quality low ESR ceramic capacitor (0.1 µF/X7R to 0.22 µF/X7R) in close proximity across BOOT and PHASE pins
20	PWM	PWM input of gate driver, compatible with 3.3 V tri-state PWM signal
21	V_{CC_3V3}	+3.3 V logic bias supply; place a high quality low ESR ceramic capacitor (~1 µF/X7R) in close proximity from this pin to GND
22,26	AGND	A_{GND} of driver IC
23	REF_{IN}	Input for external reference voltage for I_{MON} signal; this voltage should be between 0.8 V and 1.3 V; connect REF_{IN} to the appropriate current sense input of the controller; place a high quality low ESR ceramic capacitor (~ 0.1 µF) in close proximity from this pin to A_{GND}
24	I_{MON}	Current monitor output, referenced to REF_{IN}; pulls low to indicate ZCD in DCM mode; connect the I_{MON} output to the appropriate current sense input of the controller; no more than 56 pF capacitance can be directly connected across the I_{MON} and REF_{IN} pins

Updated Datasheet

PRODUCT SUMMARY	
Part number	SiC575A
Description	40 A smart power stage, 4.5 V_{IN} to 21 V_{IN}, 3.3 V PWM with diode emulation mode
Input voltage min. (V)	4.5
Input voltage max. (V)	21
Current rating (A)	40
Switch frequency max. (kHz)	2000
Enable (yes / no)	No
Monitoring features	I_{MON}, T_{MON}
Protection	UVLO, OCP, OTP
Light load mode	Diode emulation
Pulse-width modulation (V)	3.3
Package type	PowerPAK MLP24-45L
Package size (W, L, H) (mm)	4.0 x 5.0 x 0.75
Status code	1
Product type	VRPower (DrMOS)
Applications	Computer, industrial, networking

Previous Datasheet

PRODUCT SUMMARY	
Part number	SiC575A
Description	60 A smart power stage, 4.5 V_{IN} to 18 V_{IN}, 3.3 V PWM with diode emulation mode
Input voltage min. (V)	4.5
Input voltage max. (V)	18
Continuous current rating max. (A)	40
Switch frequency max. (kHz)	2000
Enable (yes / no)	No
Monitoring features	I_{MON}, T_{MON}
Protection	UVLO, OCP, OTP, HS-short
Light load mode	Diode emulation
Pulse-width modulation (V)	3.3
Package type	PowerPAK MLP24-45L
Package size (W, L, H) (mm)	4.0 x 5.0 x 0.60
Status code	2
Product type	VRPower (DrMOS)
Applications	Computer, industrial, networking

Data Sheet of SIC675A

Updated Datasheet

PIN CONFIGURATION		
PIN NUMBER	NAME	FUNCTION
1	SDIF_DATA	Serial digital interface data input and output. Connect 1 kΩ to 3.3 V
2	SDIF_CLK	Serial digital interface clock input
3	PV_{CC}	+5 V logic and gate drive bias supply. Place a high quality low ESR ceramic capacitor (~1 µF/X7R) in close proximity from this pin to A_{GND}
4, 17, 18, 19, 33	P_{GND}	Power ground (source connection of low side MOSFET)
5, 32	GL	This is a low side gate driver output (GL)
6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16	SW	No connect (this is a low side gate driver output (GL), optional to monitor for system debugging)
20, 21, 25, 34	V_{IN}	Input of power stage (to drain of High side MOSFET). Place at least 2 ceramic capacitors (10 µF or higher, X5R or X7R) in close proximity across V_{IN} and P_{GND}. For optimal performance, place as many vias as possible in the bottom side V_{IN} paddle
22	PHASE	Return of boot capacitor. Internally connected to SW node so no external routing required for SW connection
23	BOOT	Floating bootstrap supply pin for the upper gate drive. Place a high quality low ESR ceramic capacitor (0.1 µF/X7R to 0.22 µF/X7R) in close proximity across BOOT and PHASE pins
24	PWM	PWM input of gate driver, compatible with 3.3 V tri-state PWM signal
26	V_{CC}_3 V 3	+3.3 V logic bias supply. Place a high quality low ESR ceramic capacitor (~1µF/X7R) in close proximity from this pin to GND
27, 31	A_{GND}	A_{GND} of driver IC
28	REF_{IN}	Input for external reference voltage for I_{MON} signal. This voltage should be between 0.8 V and 1.3 V. Connect REF_{IN} to the appropriate current sense input of the controller. Place a high quality low ESR ceramic capacitor (~ 0.1 µF) in close proximity from this pin to A_{GND}
29	I_{MON}	Current monitor output, referenced to REF_{IN}. Pulls low to indicate ZCD in DCM mode. Connect the I_{MON} output to the appropriate current sense input of the controller. No more than 56pF capacitance can be directly connected across the I_{MON} and REF_{IN} pins.
30	T_{MON}	Temperature monitor output. For multiphase, the T_{MON} pins can be connected together as a common bus; the highest voltage (representing the highest temperature) will be sent to the PWM controller. T_{MON} will be pulled high (to 2.5 V) to indicate an over-temperature fault. No more than 250 pF total capacitance can be directly connected across T_{MON} and GND pins; with a series resistor, a higher capacitance load is allowed, such as 1 kΩ for 100 nF load

Previous Datasheet

PIN CONFIGURATION		
PIN NUMBER	NAME	FUNCTION
1	SDIFD	Serial digital interface data input and output. Connect 1 kΩ to 3.3 V
2	SDIFC	Serial digital interface clock input
3	PV_{CC}_5 V	+5 V logic and gate drive bias supply. Place a high quality low ESR ceramic capacitor (~1 µF/X7R) in close proximity from this pin to A_{GND}
4, 17, 18, 31, 33	P_{GND}	Power ground (source connection of low side MOSFET)
5, 32	GL	This is a low side gate driver output (GL)
6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16	SW	No connect (this is a low side gate driver output (GL), optional to monitor for system debugging)
20, 21, 34	V_{IN}	Input of power stage (to drain of High side MOSFET). Place at least 2 ceramic capacitors (10 µF or higher, X5R or X7R) in close proximity across V_{IN} and P_{GND}. For optimal performance, place as many vias as possible in the bottom side V_{IN} paddle
22	PHASE	Return of boot capacitor. Internally connected to SW node so no external routing required for SW connection
23	BOOT	Floating bootstrap supply pin for the upper gate drive. Place a high quality low ESR ceramic capacitor (0.1 µF/X7R to 0.22 µF/X7R) in close proximity across BOOT and PHASE pins
24	PWM	PWM input of gate driver, compatible with 3.3 V tri-state PWM signal
26	V_{CC}_3 V 3	+3.3 V logic bias supply. Place a high quality low ESR ceramic capacitor (~1µF/X7R) in close proximity from this pin to GND
27	A_{GND}	A_{GND} of driver IC
28	REF_{IN}	Input for external reference voltage for I_{MON} signal. This voltage should be between 0.8 V and 1.3 V. Connect REF_{IN} to the appropriate current sense input of the controller. Place a high quality low ESR ceramic capacitor (~ 0.1 µF) in close proximity from this pin to A_{GND}
29	I_{MON}	Current monitor output, referenced to REF_{IN}. Pulls low to indicate ZCD in DCM mode. Connect the I_{MON} output to the appropriate current sense input of the controller. No more than 56pF capacitance can be directly connected across the I_{MON} and REF_{IN} pins.
30	T_{MON}	Temperature monitor output. For multiphase, the T_{MON} pins can be connected together as a common bus; the highest voltage (representing the highest temperature) will be sent to the PWM controller. T_{MON} will be pulled high (to 2.5 V) to indicate an over-temperature fault. No more than 250 pF total capacitance can be directly connected across T_{MON} and GND pins; with a series resistor, a higher capacitance load is allowed, such as 1 kΩ for 100 nF load

Updated Datasheet

Added product summary table in the updated datasheet

PRODUCT SUMMARY	
Part number	SiC675A
Description	60 A smart power stage, 4.5 V_{IN} to 21 V_{IN}, 3.3 V PWM with diode emulation mode
Input voltage min. (V)	4.5
Input voltage max. (V)	21
Current rating (A)	60
Switch frequency max. (kHz)	2000
Enable (yes / no)	No
Monitoring features	I_{MON}, T_{MON}
Protection	UVLO, OCP, OTP
Light load mode	Diode emulation
Pulse-width modulation (V)	3.3
Package type	PowerPAK® MLP30-55L
Package size (W, L, H) (mm)	5.0 x 5.0 x 0.75
Status code	1
Product type	VRPower (DrMOS)
Applications	Computer, industrial, networking

Previous Datasheet

No product summary table in the previous datasheet.