EVAL_PMG1_S3_DUALDRP Evaluation Kit user guide

About this document

Scope and purpose

The EVAL_PMG1_S3_DUALDRP is an evaluation kit for the EZ-PD™ PMG1-S3 USB Power Delivery (PD) microcontroller (MCU). The kit features two high-voltage USB PD ports with dual-role power (DRP) functionality. The EVAL_PMG1_S3_DUALDRP kit is used to design products that use two USB PD ports with DRP and need an MCU to implement different functionalities. Power Delivery Microcontroller Gen1 (PMG1) is a family of high-voltage PD microcontrollers that include a CPU core, USB PD controller, and configurable integrated analog and digital peripherals. PMG1 is targeted at embedded systems that consume power from or provide power to high-voltage USB-C ports and require an MCU to control the actions and features of a product.

Intended audience

This document is intended for users of the EVAL_PMG1_S3_DUALDRP Evaluation Kit (EVK).

Reference Kit

Product(s) embedded on a PCB, with focus on specific applications and defined use cases that can include software. PCB and auxiliary circuits are optimized for the requirements of the target application.

Note: Boards do not necessarily meet safety, EMI, quality standards (for example UL, CE) requirements.

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Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

	**Caution:** *The EVAL_PMG1_S3_DUALDRP kit is intended for use as an evaluation platform for hardware or software in a laboratory environment. The board is an open-system design, which does not include a shielded enclosure. Due to this reason, the board may cause interference to other electrical or electronic devices in close proximity. In such cases, take adequate preventive measures. Also, do not use this board near any medical equipment or RF devices.*
	**Caution:** *Attaching additional wiring to EVAL_PMG1_S3_DUALDRP kit or modifying the product operation from the factory default may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures must be taken.*
	**Caution:** *The components and device surfaces of the EVAL_PMG1_S3_DUALDRP kit may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *EVAL_PMG1_S3_DUALDRP kit contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing, or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The EVAL_PMG1_S3_DUALDRP kit is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*
	**Caution:** *Maximum current that can be consumed by an external load connected to the EVAL_PMG1_S3_DUALDRP kit board cannot exceed 5A.*

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1 Introduction

The EVAL_PMG1_S3_DUALDRP Evaluation Kit (EVK) is based on the EZ-PD™ PMG1-S3 MCU, which is a part of the PMG1 product family of Infineon's USB Type-C and Power Delivery controllers. This EVK is an evaluation vehicle for customers who want to use PMG1-S3 for embedded systems that provide or consume power from a high-voltage USB Type-C port and need a microcontroller to control the actions and features of a product.

A USB-C port configured as DRP can operate either as a power provider or power consumer or can alternate between these two states. Initially when operating as a power provider, the port takes the data role of a downward facing port (DFP) and, when operating as a sink, the port takes the data role of an upward facing port (UFP). However, the port's power role can be dynamically changed using the USB PD message (power role swap).

EVAL_PMG1_S3_DUALDRP EVK provides customers a complete single solution evaluation platform to quickly develop, test, and kick-start the dual-port DRP EPR (extended power range) application designs using the EZ-PD™ PMG1-S3 MCU.

1.1 Key features

The EVAL_PMG1_S3_DUALDRP kit supports the following key features:

- Support for dual-port USB PD 3.1 sink role, source role, or DRP role
- Dual power operation: USB bus-powered and externally powered (24 V + 10%, 10 A)
- Compatible with the example projects implemented in ModusToolbox™ software
- Onboard KitProg3 programming and debugging module
- 100 W (20 V, 5 A) power handling capability as source
- 140 W (28 V, 5 A) power handling capability as sink
- Snap-away design to separate KitProg3 and EZ-PD™ PMG1 microcontroller board
- Onboard 5 V and 3. 3 V regulator
- Optional 10-pin standard SWD interface for MiniProg4 or third-party programmer/debugger module
- Two firmware-controlled user LEDs and a user switch
- Two self-capacitance-based CAPSENSE™ buttons and one 5-segment CAPSENSE™ slider
- Debug I/O headers

1.2 Kit contents

EVAL_PMG1_S3_DUALDRP kit contains the following:

- EVAL_PMG1_S3_DUALDRP kit board
- Quick start guide

1.2.1 Hardware not included with the kit

The EVAL_PMG1_S3_DUALDRP kit requires the following items to perform the demonstrations mentioned in Kit operation.

- A USB Type-C power adapter that supplies power over the Type-C port
- USB-C cable for connecting the USB Type-C power adapter to the Type-C receptacle on the EVK
- A 24 V/10 A DC power supply/adapter for Source mode operation (2.50 mm ID, 5.50 mm OD)
- USB Type-C load

- Multimeter and other measurement equipment
- CY4500 EZ-PD™ Protocol Analyzer
- Optional PD3.1 EPR capable USB-C cable to connect the 140 W EPR power adapter to the Type-C receptacle on the EVK

1.3 Getting started

For Instructions on how to run a quick demonstration and observe the kit functionality, see the Kit operation section. Download the documents and the hardware design files for the EVK from the kit webpage. The documents include a quick start guide, kit user guide (this document), and release notes. The hardware design files include the kit board schematics, BOM, and layout files.

For a summary of the different MCUs available in the EZ-PD™ PMG1 product line, visit the PMG1 webpage.

The EZ-PD™ PMG1 MCU-based projects are developed using the ModusToolbox™ software development tool [5].

2 Board details

Figure 1 and Figure 2 show the front and back views of the board with critical components highlighted for the EVAL_PMG1_S3_DUALDRP EVK, which are essential to demonstration kit functionality.

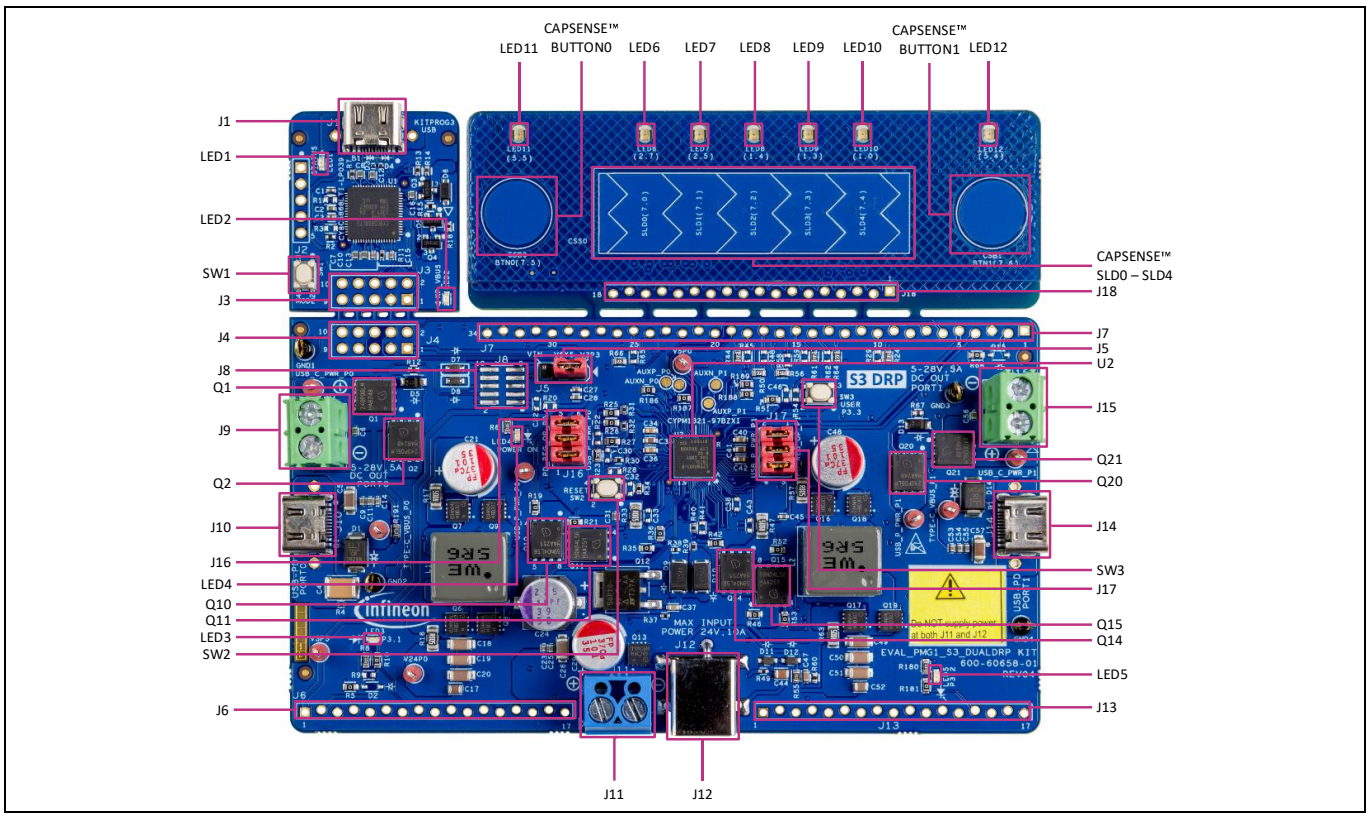

Figure 1 Board (front view) details

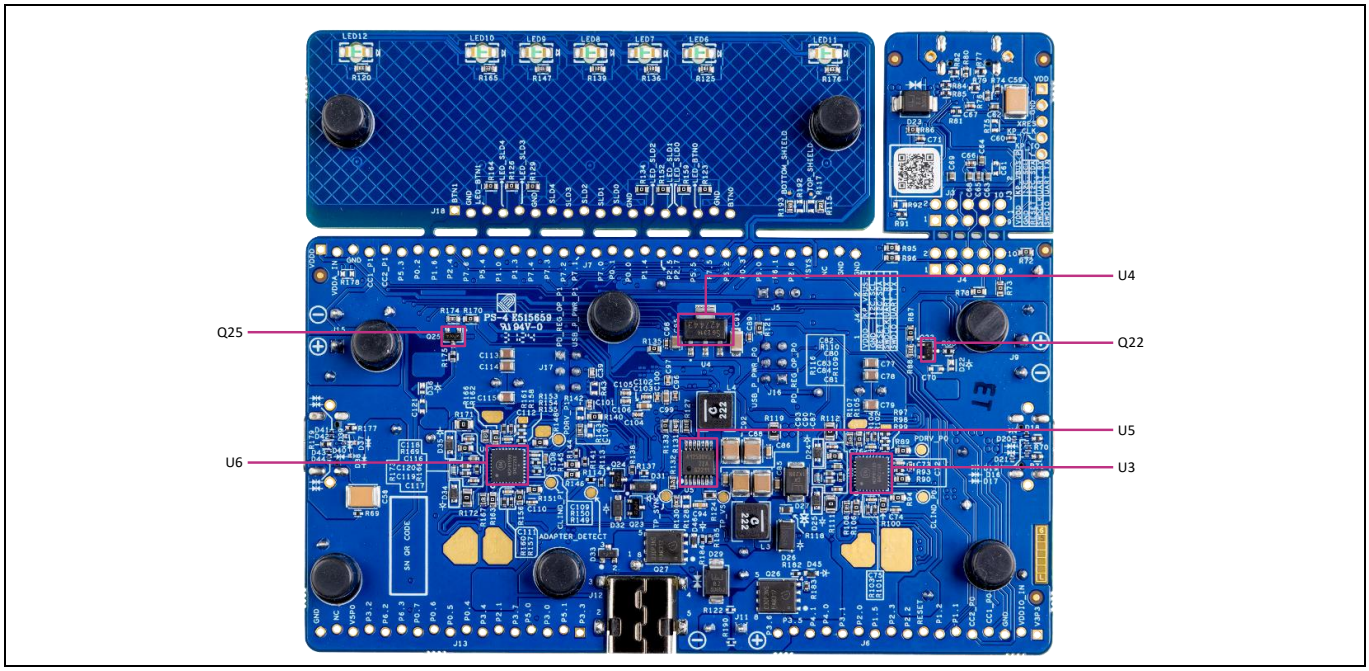

Figure 2 Board (back view) details

Board details

The following tables list the major components of the EVK. A detailed bill of materials (BOM) list is available in the design files on the kit webpage.

Table 2 Jumper settings

REFDES	Component	Default position	Description
J5	Power selection jumper	1 - 2 (V3P3)	3-pin header to select the EZ-PD™ PMG1-S3 MCU power source (see Power selection jumper)
J16	Port 0 PD regulator power	1 – 2 3 – 4 5 – 6	6-pin header to connect the PD regulator Port 0 output to the power input of the provider path of Port 0
J17	Port 0 PD regulator power	1 – 2 3 – 4 5 – 6	6-pin header to connect the PD regulator Port 1 output to the power input of the provider path of Port 1

Table 3 EVK components

REFDES	Component	Description
U2	EZ-PD™ PMG1-S3 controller (CYPM1322-97BZXI)	EZ-PD™ PMG1-S3 dual-port USB Type-C PD high-voltage MCU
Q10, Q11, Q14, Q15	Provider FETs (BSC059N04LS6ATMA1)	MOSFET N-CH 40 V, 17 A, TDSON
Q1, Q2, Q20, Q21	Consumer FETs (ISC240P06LM)	MOSFET P-CH 60 V, 59 A, TDSON
Q22, Q25	Consumer FET CTRLs (2N70002LT1G)	MOSFET N-CH 60 V, 115 MA, SOT23-3
U3, U6	Buck-boost converter (NCP81599MNTXG)	5-20 V DC-DC buck-boost regulator for USB PD source operation
U5	5 V buck converter (TLS4125D0EPV50XUMA1)	5 V buck switching regulator for system power
U4	3.3 V LDO (TLE42744GSV33HTMA1)	3.3 V Linear Voltage Regulator

Table 4 EVK LEDs

REFDES	LED	Color	Description
LED1	KitProg3 status LED	Amber	Indicates the Programming mode and status. The LED functions only when the KitProg3 Type-C port is connected to a PC. See the KitProg3 user guide for details.
LED2	KitProg3 power LED	Amber	Turns ON when the kit is powered through KitProg3 Type-C port and indicates that the PSoC™ 5LP MCU device is powered.
LED3, LED5	User LED	Green	Firmware-driven LED. The kit must be powered to use this LED.
LED4	Power LED	Green	Indicates that the PMG1-S3 MCU is powered. The LED is powered via VDDIO.

Board details

REFDES	LED	Color	Description
LED11, LED12	CAPSENSE™ button LEDs	Green	Indicator LEDs for CAPSENSE™ buttons, BTN0 and BTN1. Firmware-driven LEDs to indicate the state of CAPSENSE™ buttons. LED11 – BTN0 LED12 – BTN1
LED6, LED7, LED8, LED9, LED10	CAPSENSE™ slider LEDs	Green	Indicator LEDs for CAPSENSE™ slider. Firmware-driven LEDs indicate the state of each sensor in a 5-sensor CAPSENSE™ slider. LED6 – SLD0 LED7 – SLD1 LED8 – SLD2 LED9 – SLD3 LED10 – SLD4

Table 5 EVK switches

REFDES	Button	Description
SW1	KitProg3 mode	The mode button is used to put the KitProg3 into Bootloader mode. See the KitProg3 user guide for details.
SW2	Reset switch	This button is used to reset the EZ-PD™ PMG1-S3 MCU. It connects the EZ-PD™ PMG1-S3 MCU reset (XRES) pin to the ground.
SW3	User switch	This button can be used to provide input to the EZ-PD™ PMG1-S3 MCU. This button pulls the pin to the ground, by default.

Table 6 Connectors and terminal blocks

REFDES	Connector name	Description
J1	KitProg3 USB	USB Type-C connector to connect the kit with a PC for EVK programming and debugging
J3	KitProg3 debug header KitProg3 side	10-pin header for connections between KitProg3 and EZ-PD™ PMG1-S3 MCU
J4	KitProg3 debug header EZ-PD™ PMG1-S3 side	10-pin header for connections between KitProg3 and EZ-PD™ PMG1-S3 MCU
J6, J13	I/O header 17x1	Observing and measuring various signals and connecting external modules for development if required
J7	I/O header 34x1	Observing and measuring various signals and connecting external modules for development if required
J8	EZ-PD™ PMG1-S3 SWD/JTAG header	10-pin SWD/JTAG header to program the EZ-PD™ PMG1-S3 MCU using MiniProg4 or third-party SWD debuggers/programmers.
J9, J15	2-pin OUTPUT load terminal	2-pin header to connect DC load up-to 28 V, 5 A in sink operation
J10, J14	Type-C connector	Type-C receptacle connector for interfacing with Type-C PD source or sink device

Board details

REFDES	Connector name	Description
J11	2-pin INPUT DC terminal	2-pin header to connect 24 V, 10 A input power to the kit for source operation. WARNING: Max input should not exceed 24 + 10% V.
J12	Barrel jack	Barrel jack connector (2.50 mm ID, 5.50 mm OD) to connect 24 V, 10-A input power to the kit for source operation. **WARNING: Maximum input should not exceed 24 + 10% V. Do not power J11 and J12 at the same time.**

3 EVAL_PMG1_S3_DUALDRP kit system design

This section details the complete system overview and description of the critical circuit blocks of the EVK board design. For more details, see the schematics of the EVAL_PMG1_S3_DUALDRP kit board on the kit webpage.

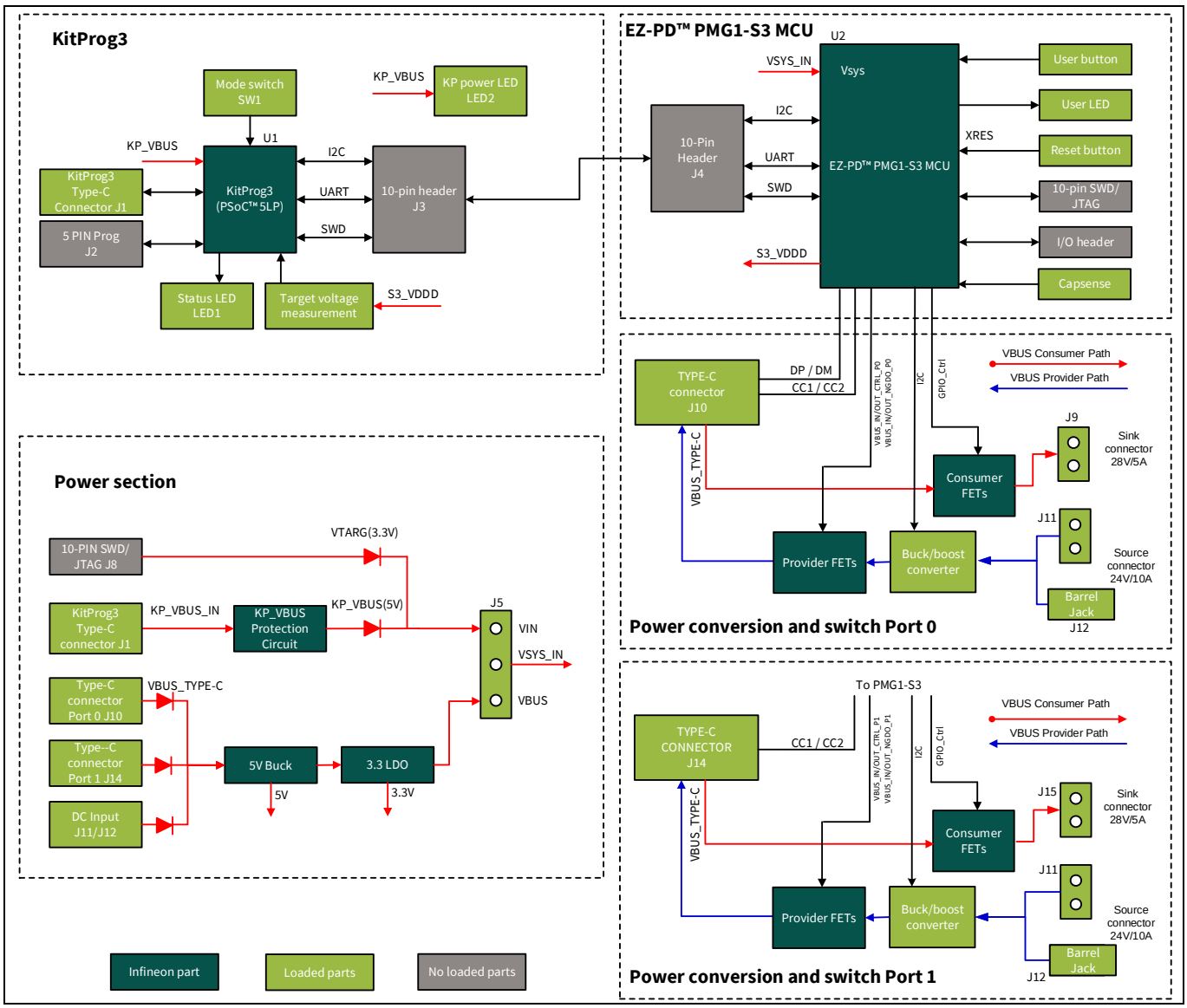

Figure 3 EVAL_PMG1_S3_DUALDRP kit block diagram

The PMG1-S3 MCU controls the functionality of the two USB Type-C ports on the kit by controlling the consumer FETs and provider FETs. Each USB Type-C port has a buck-boost converter that is controlled by the PMG1-S3 MCU to set the output voltage when the respective USB Type-C port is in source operation. Each of the ports, Port 0, and Port 1 can be either in source or sink operation independent of each other's role. Table 7 lists the possible port combinations when both USB Type-C ports are in Operational mode.

Table 7 USB Type-C ports combinations

Port	Port 0	Port 1
Role	Sink	Sink
	Sink	Source
	Source	Sink
	Source	Source

3.1 System power supply design

The EVK consists of two step-down regulators to generate the 5 V and 3.3 V outputs to provide for VCONN, board peripherals, and EZ-PD™ PMG1-S3 MCU system power. The 5 V DC-DC converter generates 5 V from the DC input power supply when the EVK is in the Source mode or, when the EVK is in Sink mode, the regulator generates 5 V from the Type-C port that is sinking power. This regulator output also supplies the VCONN for both Type-C ports.

The onboard 3.3 V LDO generates 3.3 V from the output of the 5 V regulator and is available as the power input for MCU. This 3.3 V regulated output is also available on an I/O header and can be used as a power rail for external components and modules. The onboard 3.3 V LDO can source a maximum current of 400 mA.

To power the USB Type-C VBUS in Source mode, the EVK uses two NCP81599 buck-boost DC-DC converters as the variable output VBUS source for both the ports. The voltage output of the regulators is controlled using the I2C interface from the EZ-PD™ PMG1-S3 MCU.

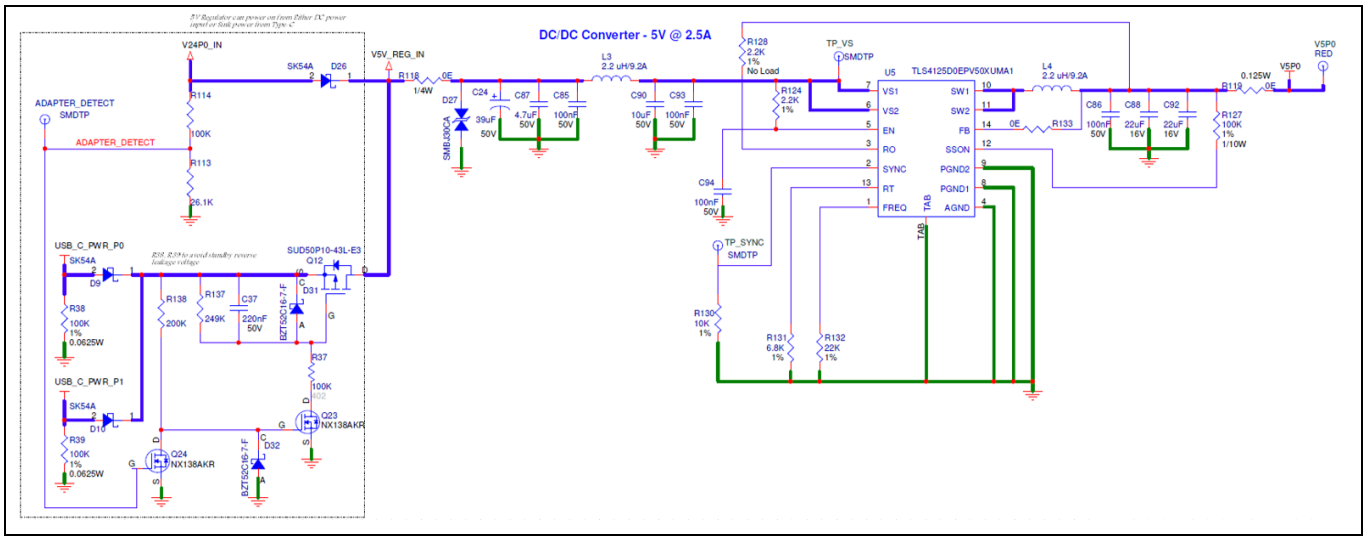

Figure 4 5 V regulator

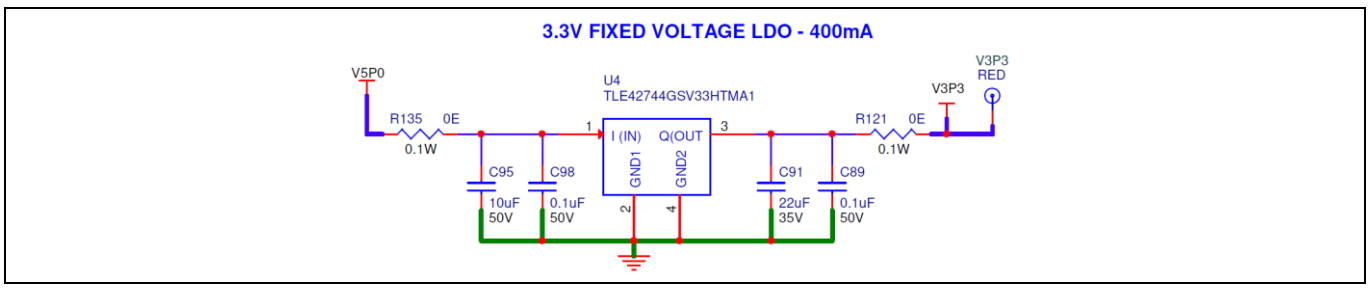

Figure 5 3.3 V LDO

3.1.1 Power selection jumper

The EZ-PD™ PMG1-S3 MCU on the EVK can operate with two possible external supply voltages, VBUS, or VSYS. The VDDIO supply powers the device I/Os. VDDD generates 3.3 V from an internal regulator, and this can be shorted to VDDIO. VCCD is the output voltage from the core regulator and this pin is intended to connect only a decoupling capacitor. The VCCD pin cannot be used as a voltage source. The EZ-PD™ PMG1-S3 MCU has power supply inputs at the VCONN pin to provide power to EMCA cables through the integrated VCONN FETs.

The onboard EZ-PD™ PMG1-S3 MCU supports two types of powering modes:

- **Programming mode:** For programming using the onboard KitProg3, the kit gets powered through the KitProg3 USB Type-C port (J1) or the SWD header (J8), whichever is available. When the Programming mode setting is selected, power from the programming connector (J4 or J8) is connected to the VSYS pin of the EZ-PD™ PMG1-S3 MCU.
- **Operational mode:** For normal operation, the prototyping kit gets powered through 24 V power input at J11 and J12 in Source mode operation or Type-C adapter port in Sink mode operation. The input power is fed to the 5 V regulator and 3.3 LDO network to generate the system power, which powers the EZ-PD™ PMG1-S3 MCU.

The position of the power selection jumper(J5) decides the power input connected to the MCU and selects between the programming and operation power supply. Short pins 1–2 (V3P3) for Operational mode and short 2–3 (VIN) for Programming mode.

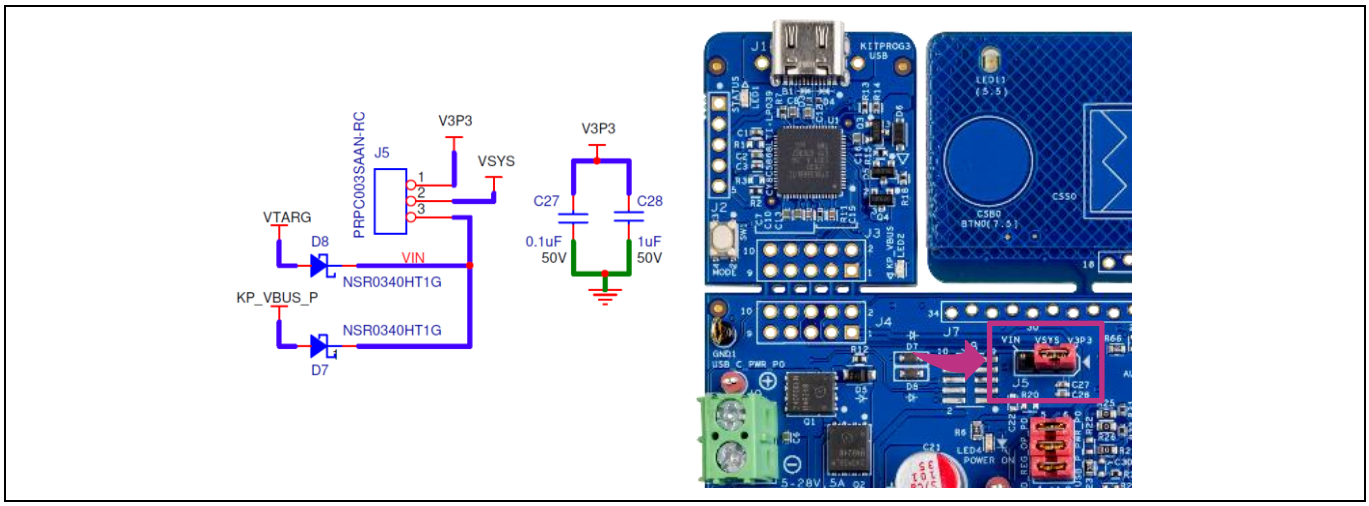

Figure 6 Power selection jumper

Note: The EZ-PD™ PMG1-S3 MCU can be powered via VBUS_C_P0 & VBUS_C_P1 pins also. So, in the Sink mode the prototyping kit can get power directly from the Type-C_VBUS and can function without the jumper connection.

3.2 Provider and consumer switch

The EVK provides two USB Type-C ports that are capable of DRP operation. For each port, there are two paths that VBUS power can travel through:

- Provider path (sourcing of power)
- Consumer path (sinking of power)

3.2.1 Provider and consumer path Port 0

EZ-PD™ PMG1-S3 has two integrated NFET gate drivers: VBUS_IN_CTRL _P0 and VBUS_OUT_CTRL _P0 to control the VBUS provider path connecting the USB Type-C Port 0 VBUS to the power Type-C load on Port 0. PMG1-S3 uses a GPIO to control the VBUS consumer path connecting the USB Type-C Port 0 VBUS to the Port 0 DC load terminal.

While in Source mode, the power is supplied from the 24 V buck-boost regulator to the Type-C port 0 (J10) using NFETs, Q10, and Q11. These NFETs are controlled via the VBUS_IN_CTRL _P0 and the VBUS_OUT_CTRL _P0 pins of the EZ-PD™ PMG1-S3 MCU.

In the provider path, a shunt resistance (R33) is connected in series to measure the current flowing to the Type-C port. The PMG1-S3 MCU uses this current measure to implement OCP/SCP/RCP on Type-C VBUS. PMG1-S3 also supports VBUS discharge and OVP/UVP features. This is done by monitoring the voltages on the VBUS_C_P0 pin of the PMG1-S3 MCU and providing a discharge path on it.

While in Sink mode, the power is supplied to the DC load terminal Port 0(J9) from the Type-C Port 0 connector (J10) using PFETs Q1 and Q2. These PFETs are controlled via a GPIO pin of the EZ-PD™ PMG1-S3 MCU.

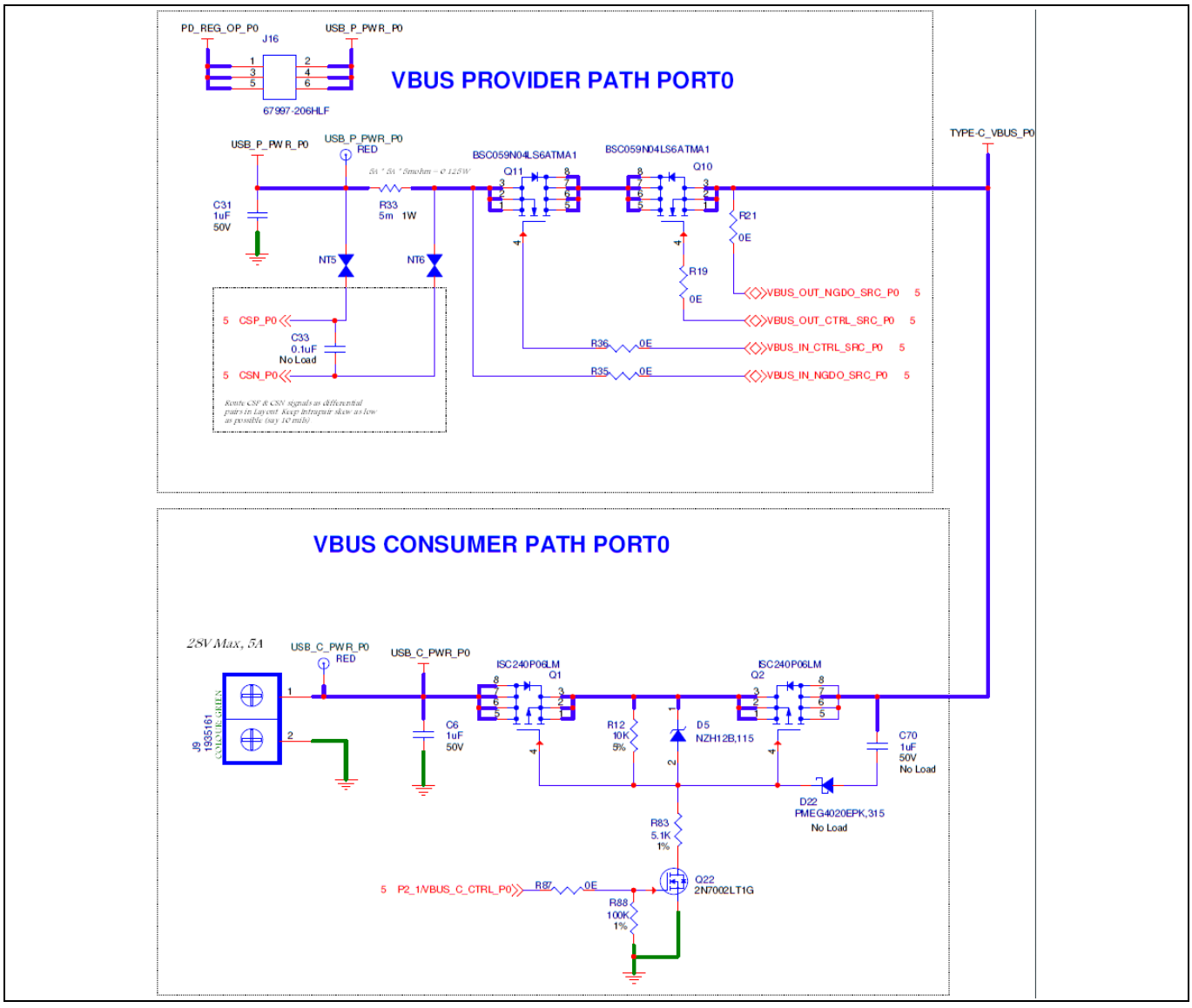

Figure 7 VBUS provider and consumer path Port 0

3.2.2 Provider and consumer path Port 1

Similar to Port 0, EZ-PD™ PMG1-S3 has two integrated NFET gate drivers: VBUS_IN_CTRL _P1 and VBUS_OUT_CTRL _P1 to control the VBUS provider path connecting the USB Type-C Port 1 VBUS to the power Type-C load on Port 1. PMG1-S3 uses a GPIO to control the VBUS consumer path connecting the USB Type-C Port 1 VBUS to the Port 1 DC load terminal.

While in Source mode, the power is supplied from the 24 V buck-boost regulator to the Type-C port 1 (J14) using NFETs, Q14, and Q15. These NFETs are controlled via the VBUS_IN_CTRL _P1 and VBUS_OUT_CTRL _P1 pins of the EZ-PD™ PMG1-S3 MCU.

In the provider path, a shunt resistance (R47) is connected in series to measure the current flowing to the Type-C port. The PMG1-S3 MCU uses this current measure to implement OCP/SCP/RCP on Type-C VBUS. PMG1-S3 also supports VBUS discharge and OVP/UVP features. This is done by monitoring the voltages on the VBUS_C_P1 pin of the PMG1-S3 MCU and providing a discharge path on it.

While in Sink mode, the power is supplied to the DC load terminal Port 1 (J15) from the Type-C Port 0 connector (J14) using PFETs Q20 and Q21. These PFETs are controlled via a GPIO pin of the EZ-PD™ PMG1-S3 MCU.

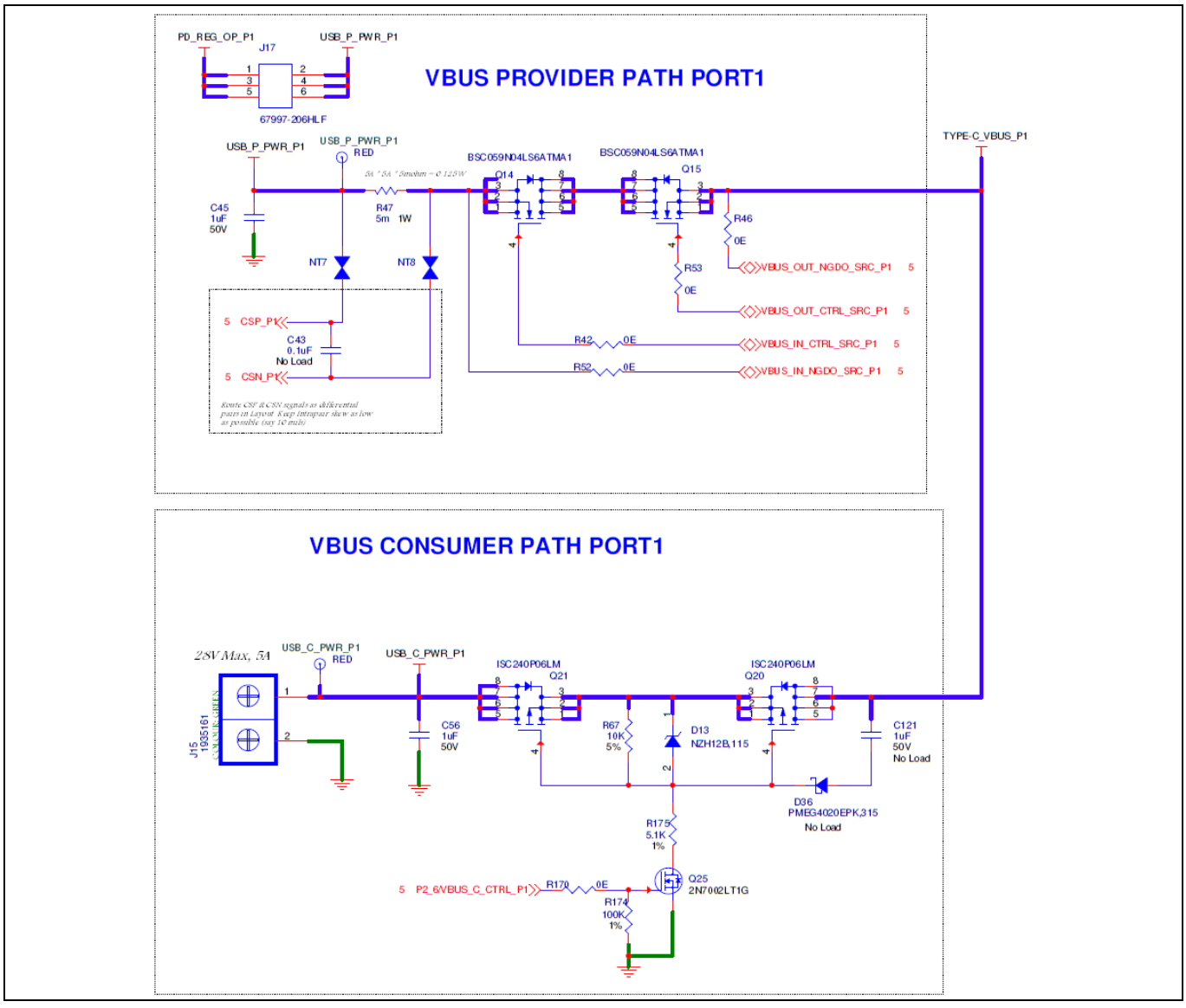

Figure 8 VBUS provider and consumer path Port 1

Bypassing the onboard 24 V PD regulator Port 0

The J16 jumper provides pinouts to bypass the onboard 24 V PD regulator as an input to the VBUS provider path. The input USB_P_PWR_P0 of the provider path can be connected to an external PD regulator by connecting Pins 2, 4, and 6 of J16 to the output of the external PD regulator (see Table 10). Use this feature to connect an external PD regulator that outputs EPR power (28 V, 5 A) to the provider path.

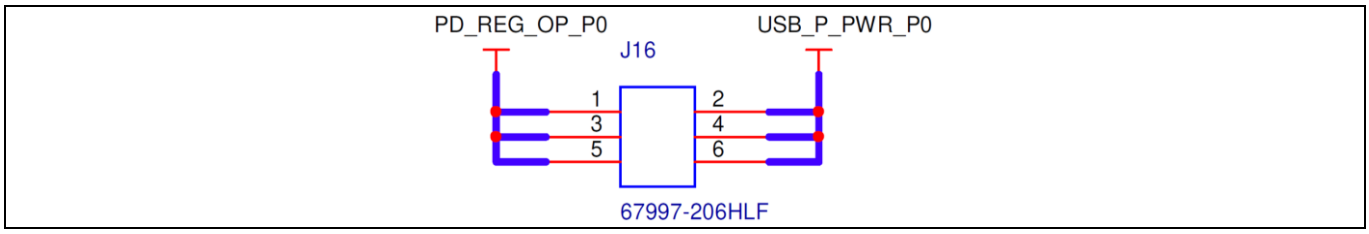

Figure 9 Jumper J16 to bypass onboard PD regulator Port 0

Bypassing the onboard 24 V PD Regulator Port 1

The J17 jumper provides pinouts to bypass the onboard 24 V PD regulator as an input to the VBUS provider path. The input USB_P_PWR _P1 of the provider path can be connected to an external PD regulator by connecting Pins 2, 4, and 6 of J17 to the output of the external PD regulator (see Table 2). Use this feature to connect an external PD regulator that outputs EPR power (28 V, 5 A) to the provider path.

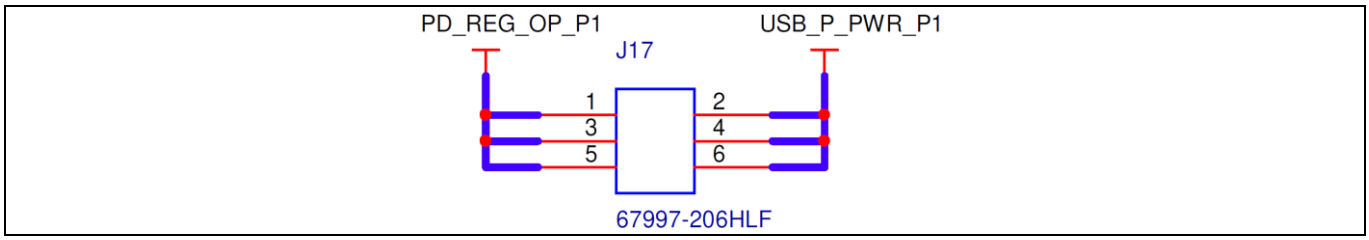

Figure 10 Jumper J17 to bypass onboard PD regulator Port 1

3.3 I/O headers

The EVK has four I/O headers; all GPIOs, PD-specific function signals, regulator output, and other power signals are routed to these headers.

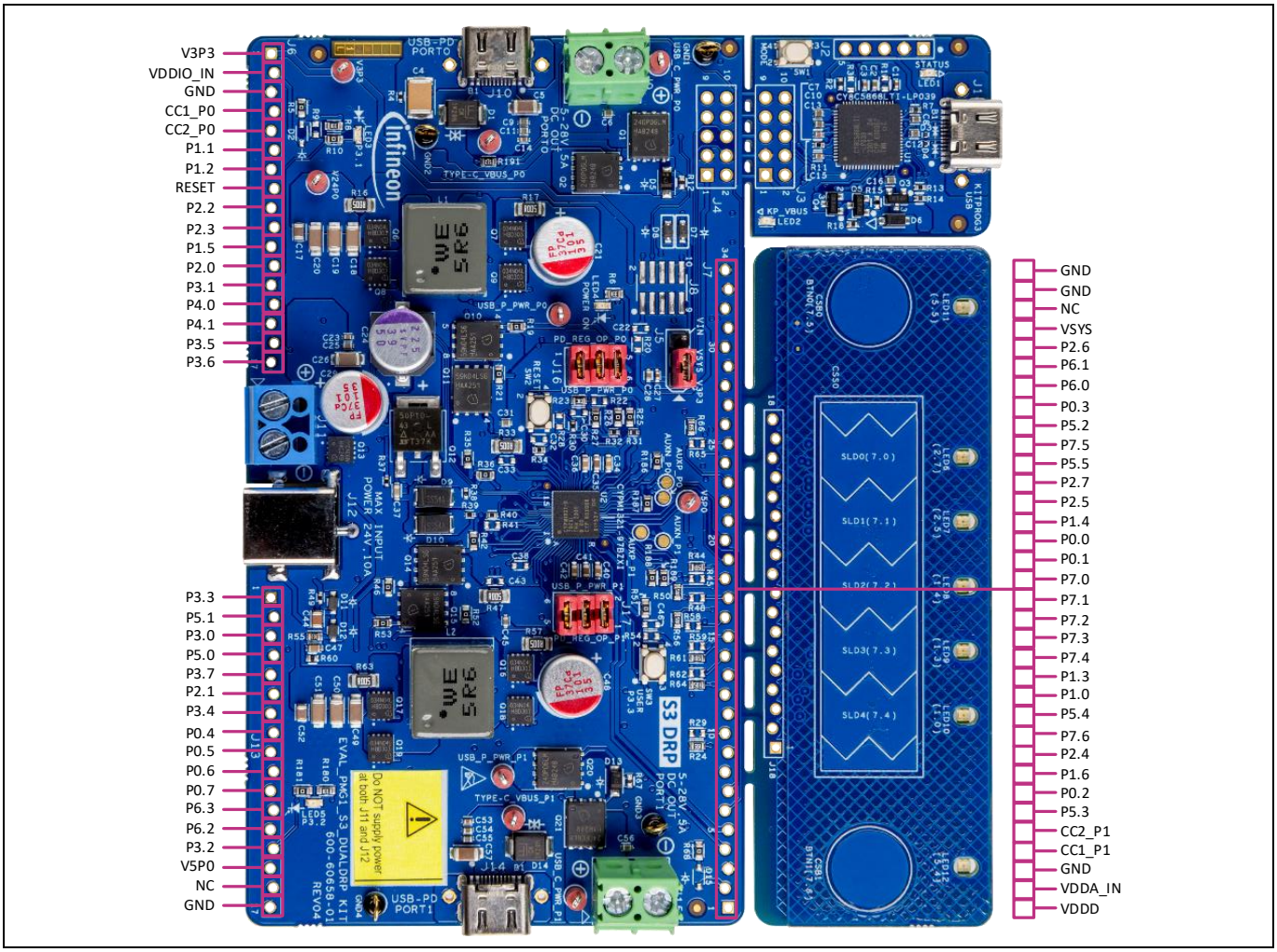

Figure 11 EVK I/O headers

Table 8 I/O header pinout at J6

EVK pin J6	EVK pin name	PMG1-S3 MCU pin	Primary function	Secondary function	Connection details
1	V3P3	-	3.3 V regulator output	External 3.3 V regulator input to board	Connected to power and CAPSENSE™ LEDs
2	VDDIO_IN	-	VDDIO external input	-	Connected through the non-populated resistor/diode
3	GND	-	-	-	Connected to ground
4	CC1_P0	N14, N15	Port 0 CC1 signal	-	Connected to Type-C Port 0 CC1 channel
5	CC2_P0	J14, J15	Port 0 CC2 signal	-	Connected to Type-C Port 0 CC2 channel
6	P1.1/SWD_CLK	P3	SWD clock	P1.1 (GPIO)	Connected to KitProg3

EVK pin J6	EVK pin name	PMG1-S3 MCU pin	Primary function	Secondary function	Connection details
7	P1.2/SWD_IO	R3	SWD data	P1.2 (GPIO)	Connected to KitProg3
8	RESET	E14	Reset signal	-	Connected to SW2 and KitProg3 Reset
9	P2.2/REG_I2C_SDA	A3	PD regulator I2C data line	P2.2 (GPIO)	Connected to PD regulator I2C data line
10	P2.3/REG_I2C_SCL	B5	PD regulator I2C clock line	P2.3 (GPIO)	Connected to PD regulator I2C clock line
11	P1.5/REG_EN_P0	M12	Port 0 PD regulator enable signal	P1.5 (GPIO)	Connected to Port 0 PD regulator enable pin
12	P2.0/REG_INT_P0	A2	Port 0 PD regulator interrupt signal	P2.0 (GPIO)	Connected to Port 0 PD regulator interrupt pin
13	P3.1	B3	User LED 1	P3.1 (GPIO)	Connected to LED3
14	P4.0/I2C_SCL	E15	I2C clock signal	P4.0 (GPIO)	Connected to KitProg3 for USB to I2C bridge
15	P4.1/I2C_SDA	D12	I2C data signal	P4.1 (GPIO)	Connected to KitProg3 for USB to I2C bridge
16	P3.5/UART_RX	F4	UART RX	P3.5 (GPIO)	Connected to KitProg3 UART by default
17	P3.6/UART_TX	E2	UART TX	P3.6 (GPIO)	Connected to KitProg3 UART by default

Table 9 I/O header pinout at J13

EVK pin J13	EVK pin name	PMG1-S3 MCU pin	Primary function	Secondary function	Connection details
1	P3.3	B1	User switch signal	P3.3 (GPIO)	Connected to SW3
2	P5.1/CMOD	E1	CAPSENSE™ capacitor	P5.1 (GPIO)	Connected to CAPSENSE™ capacitor
3	P3.0	A1	P3.0 (GPIO)	-	Connected to VREF bypass capacitor for 12-bit SAR ADC
4	P5.0/CTANK	G2	CAPSENSE™ capacitor output	P5.0 (GPIO)	CTANK capacitor connected through no-load resistor
5	P3.7	C1	P3.7 (GPIO)	-	-
6	P2.1/ VBUS_C_CTRL_P0	B2	Port 0 VBUS consumer FET control signal	P2.1 (GPIO)	Connected to Port 0 consumer path NFET gate
7	P3.4	D4	P3.4 (GPIO)	-	-
8	P0.4/DBG2_P0	P8	-	P0.4 (GPIO)	-
9	P0.5/DBG1_P0	M8	-	P0.5 (GPIO)	-
10	P0.6/LSTX_P0	R9	-	P0.6 (GPIO)	-

EVK pin J13	EVK pin name	PMG1-S3 MCU pin	Primary function	Secondary function	Connection details
11	P0.7/LSRX_P0	R11	-	P0.7 (GPIO)	-
12	P6.3/SBU1_P0	R13	Type-C Port 0 SBU1 signal	P6.3 (GPIO)	Connected to Port 0 Type-C SBU1 channel
13	P6.2/SBU2_P0	P13	Type-C Port 0 SBU2 signal	P6.2 (GPIO)	Connected to Port 0 Type-C SBU2 channel
14	P3.2	C2	User LED 2	P3.2 (GPIO)	Connected to user LED 2
15	V5P0	-	5 V supply for VCONN	Input to 3.3 V fixed voltage LDO	Connected to 5 V DC/DC converter output
16	-	-	-	-	-
17	GND	-	-	-	Connected to ground

Table 10 I/O header pinout at J7

EVK pin J7	EVK pin name	PMG1-S3 MCU pin	Primary function	Secondary function	Connection details
1	VDDD	D8	EZ-PD™ PMG1-S3 MCU Internal LDO output when VSYS is not prioritized	-	VDDD, VDDA, and VDDIO are shorted in the design with 0-ohm resistors in between
2	VDDA_IN	-	External supply to VDDA	-	Connected to VDDA through no load resistor/diode
3	GND	-	-	-	Connected to ground
4	CC1_P1	N1, N2	Port 1 CC1 signal	-	Connected to Type-C Port 1 CC1 channel
5	CC2_P1	J1, J2	Port 1 CC2 signal	-	Connected to Type-C Port 1 CC2 channel
6	P5.3	H1	P5.3 (GPIO)	AFC pull-down resistor	-
7	P0.2/DBG1_P1	P7	-	P0.2 (GPIO)	-
8	P1.6/REG_EN_P1	K12	Port 1 PD regulator enable signal	P1.6 (GPIO)	Connected to Port 1 PD regulator enable pin
9	P2.4/REG_INT_P1	A7	Port 1 PD regulator interrupt signal	P2.4 (GPIO)	Connected to Port 1 PD regulator interrupt pin
10	P7.6	B9	CAPSENSE™ BUTTON1 input	P7.6 (GPIO)	Connected to BUTTON1 through 560-ohm resistor

EVAL_PMG1_S3_DUALDRP kit system design

EVK pin J7	EVK pin name	PMG1-S3 MCU pin	Primary function	Secondary function	Connection details
11	P5.4	G1	CAPSENSE™ BUTTON1 LED output	P5.4 (GPIO)	Connected to LED_BTN1 through a 0-ohm resistor
12	P1.0	H2	CAPSENSE™ SLIDER4 LED output	P1.0 (GPIO)	Connected to LED_SLD4 through a 0-ohm resistor
13	P1.3	K4	CAPSENSE™ SLIDER3 LED output	P1.3 (GPIO)	Connected to LED_SLD3 through a 0-ohm resistor
14	P7.4	B11	CAPSENSE™ SLIDER4 input	P7.4 (GPIO)	Connected to SLIDER4 through a 560-ohm resistor
15	P7.3	B13	CAPSENSE™ SLIDER3 input	P7.3 (GPIO)	Connected to SLIDER3 through a 560-ohm resistor
16	P7.2	A14	CAPSENSE™ SLIDER2 input	P7.2 (GPIO)	Connected to SLIDER2 through a 560-ohm resistor
17	P7.1	G14	CAPSENSE™ SLIDER1 input	P7.1 (GPIO)	Connected to SLIDER1 through a 560-ohm resistor
18	P7.0	G15	CAPSENSE™ SLIDER0 input	P7.0 (GPIO)	Connected to SLIDER0 through a 560-ohm resistor
19	P0.1/LSTX_P1	R7	-	P0.1 (GPIO)	-
20	P0.0/LSRX_P1	R8	-	P0.0 (GPIO)	-
21	P1.4	M10	CAPSENSE™ SLIDER2 LED output	P1.4 (GPIO)	Connected to LED_SLD2 through a 0-ohm resistor
22	P2.5	A5	CAPSENSE™ SLIDER1 LED output	P2.5 (GPIO)	Connected to LED_SLD1 through a 0-ohm resistor
23	P2.7	A8	CAPSENSE™ SLIDER0 LED output	P2.7 (GPIO)	Connected to LED_SLD0 through a 0-ohm resistor
24	P5.5	H4	CAPSENSE™ BUTTON0 LED output	P5.5 (GPIO)	Connected to LED_BTN0 through 0-ohm resistor
25	P7.5	A9	CAPSENSE™ BUTTON1 input	P7.5 (GPIO)	Connected to BUTTON0 through 560-ohm resistor
26	P5.2/SHIELD	H6	CAPSENSE™ shield ground	P5.2 (GPIO)	Connected to CAPSENSE™ shield through a no load 560-ohm resistor
27	P0.3/DBG2_P1	K6	-	P0.3 (GPIO)	-
28	P6.0/SBU1_P1	R5	Type-C Port 1 SBU1 signal	P6.0 (GPIO)	Connected to Port 1 Type-C SBU1 channel
29	P6.1/SBU2_P1	P5	Type-C Port 1 SBU2 signal	P6.1 (GPIO)	Connected to Port 1 Type-C SBU2 channel

EVK pin J7	EVK pin name	PMG1-S3 MCU pin	Primary function	Secondary function	Connection details
30	P2.6/ VBUS_C_CTRL_P1	B7	Port 1 VBUS consumer FET control signal	P2.6 (GPIO)	Connected to Port 1 consumer path NFET gate
31	VSYS	B14	VSYS power to MCU	-	Connection determined by J5 jumper setting
32	-	-	-	-	-
33	GND	-	-	-	Connected to ground
34	GND	-	-	-	Connected to ground

Table 11 I/O header pinout at J18

EVK pin J18	EVK pin name	PMG1-S3 MCU pin	Primary function	Secondary function	Connection details
1	BUTTON1	-	CAPSENSE™ button 1 input	P7.6 (GPIO)	Connected to P7.6 through a 560-ohm resistor
2	GND	-	-	-	Connected to GND
3	LED_BTN1	-	CAPSENSE™ button 1 LED output	P5.4 (GPIO)	Connected to LED_BTN1 through a 330-ohm resistor and to P5.4 through a 0-ohm resistor
4	LED_SLD4	-	CAPSENSE™ button 4 LED output	P1.0 (GPIO)	Connected to LED_SLD4 through a 330-ohm resistor and to P1.0 through a 0-ohm resistor
5	LED_SLD3	-	CAPSENSE™ button 3 LED output	P1.3 (GPIO)	Connected to LED_SLD3 through a 330-ohm resistor and to P1.3 through a 0-ohm resistor
6	GND	-	-	-	Connected to GND
7	SLIDER4	-	CAPSENSE™ sensor 4 output	P7.4 (GPIO)	Connected to P7.4 through a 560-ohm resistor
8	SLIDER3	-	CAPSENSE™ sensor 3 output	P7.3 (GPIO)	Connected to P7.3 through a 560-ohm resistor
9	SLIDER2	-	CAPSENSE™ sensor 2 output	P7.2 (GPIO)	Connected to P7.2 through a 560-ohm resistor
10	SLIDER1	-	CAPSENSE™ sensor 1 output	P7.1 (GPIO)	Connected to P7.1 through a 560-ohm resistor
11	SLIDER0	-	CAPSENSE™ sensor 0 output	P7.0 (GPIO)	Connected to P7.0 through a 560-ohm resistor
12	GND	-	-	-	Connected to GND
13	LED_SLD2	-	CAPSENSE™ button 2 LED output	P1.4 (GPIO)	Connected to LED_SLD2 through a 330-ohm resistor and to P1.4 through a 0-ohm resistor

EVK pin J18	EVK pin name	PMG1-S3 MCU pin	Primary function	Secondary function	Connection details
14	LED_SLD1	-	CAPSENSE™ button 1 LED output	P2.5 (GPIO)	Connected to LED_SLD1 through a 330-ohm resistor and to P2.5 through a 0-ohm resistor
15	LED_SLD0	-	CAPSENSE™ button 0 LED output	P2.7 (GPIO)	Connected to LED_SLD5 through a 330-ohm resistor and to P2.7 through a 0-ohm resistor
16	LED_BTN0	-	CAPSENSE™ button 0 LED output	P5.5 (GPIO)	Connected to LED_BTN0 through a 330-ohm resistor and to P5.5 through a 0-ohm resistor
17	GND	-	-	-	Connected to GND
18	BUTTON0	-	CAPSENSE™ button 0 input	P7.5 (GPIO)	Connected to P7.5 through a 560-ohm resistor

3.4 Programming and debugging

The EVAL_PMG1_S3_DUALDRP EVK includes a PSoC™ 5LP-based KitProg3 module to enable programming and debugging of the kit without additional hardware/programmer module and interface the KitProg3 module through a USB programming connector (Type-C). The PCB design enables breaking apart the KitProg3 section of the board if required. The portion of the board, which contains the EZ-PD™ PMG1-S3 MCU, can operate independently even after the KitProg3 section is detached.

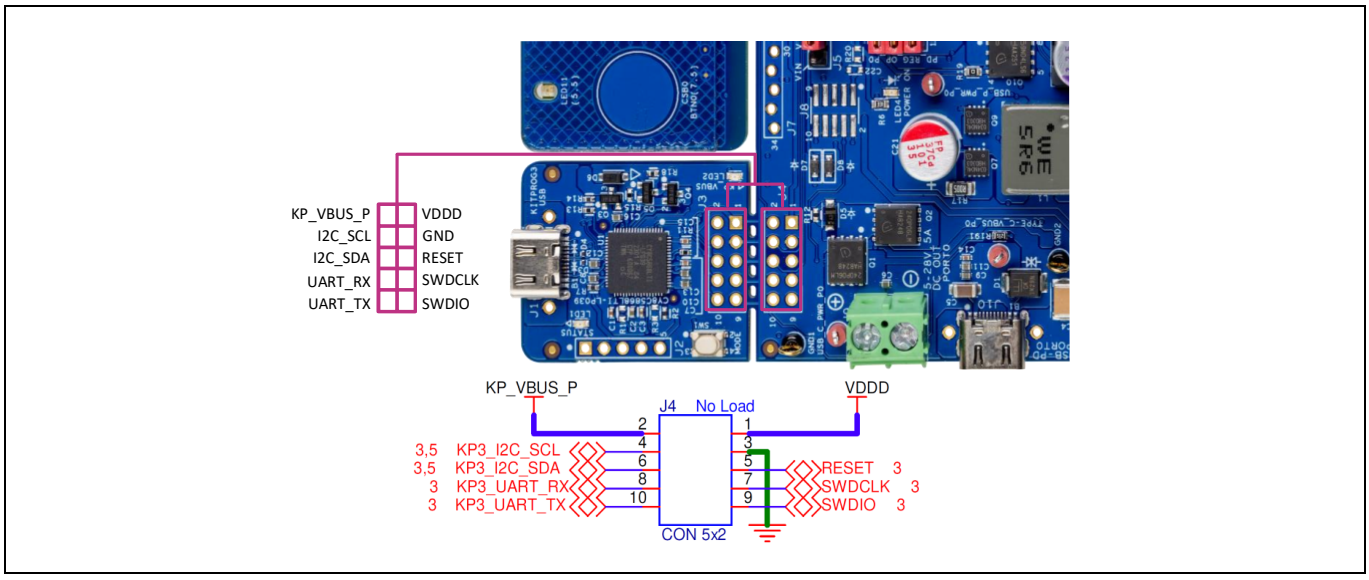

Figure 12 KitProg3 header

Table 12 KitProg3 header (J3 and J4) pinout

Pin#	Pin name	Description
1	VDDD	Target (EZ-PD™ PMG1-S3 MCU) internal regulator output
2	KP_VBUS_P	KitProg3 VBUS/programming VBUS

Pin#	Pin name	Description
3	GND	Ground
4	I2C_SCL	I2C SCL signal between KitProg3 and EZ-PD™ PMG1-S3 MCU
5	RESET	Reset signal for programming EZ-PD™ PMG1-S3 MCU
6	I2C_SDA	I2C SDA signal
7	SWDCLK	SWD clock
8	UART_RX	UART Rx
9	SWDIO	SWD data
10	UART_TX	UART Tx

The EVK also has a 10-pin SWD/JTAG header (J8) for programming and debugging. The header is pin-compatible with all the standard 10-pin SWD/JTAG interfaces and supports Infineon's MiniProg4 program and debug kit.

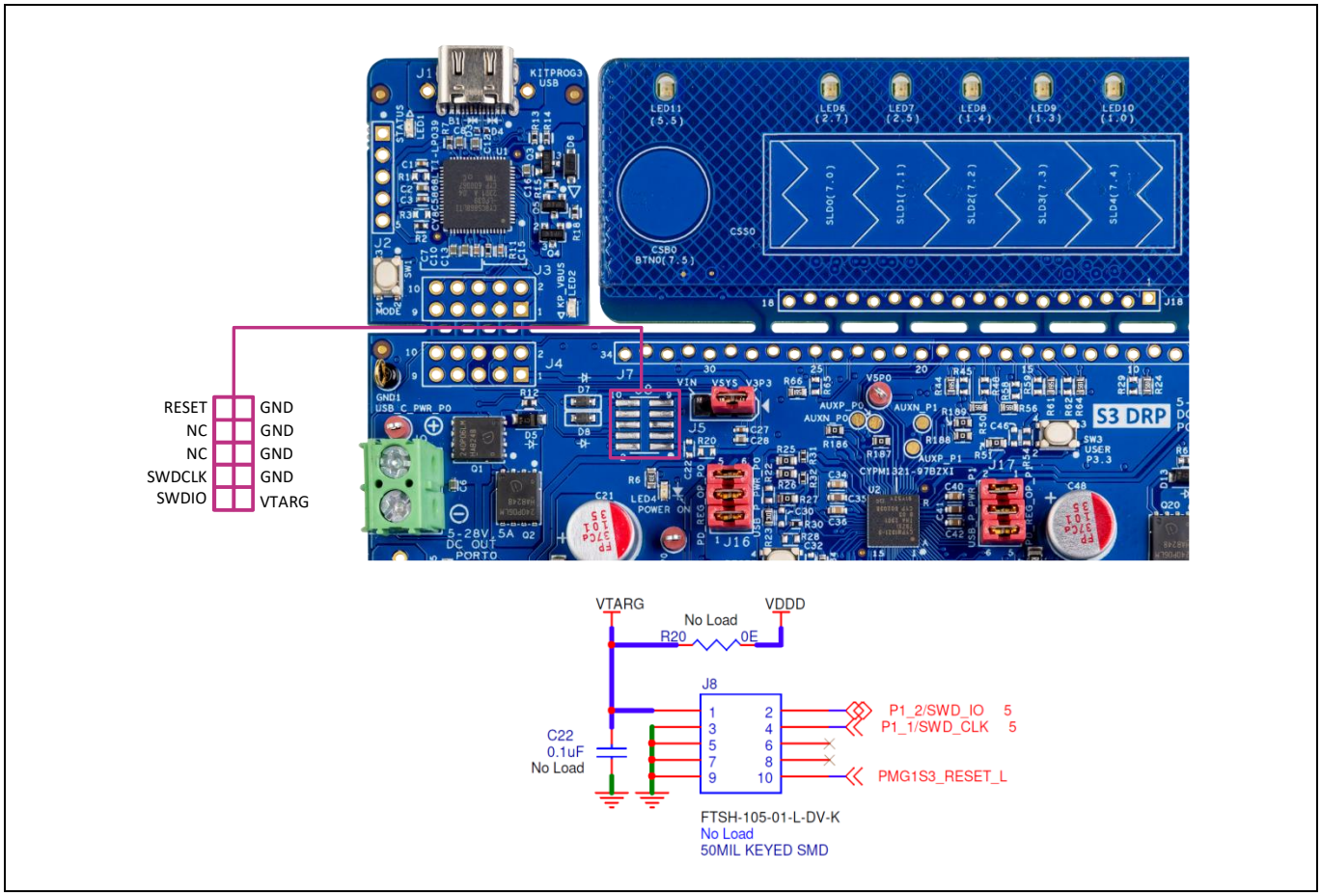

Figure 13 SWD/JTAG header

Table 13 SWD header (J8) pinout

Pin#	Pin name	Description
1	VTARG	Target (EZ-PD™ PMG1-S3 MCU) internal regulator output
2	SWDIO	SWD data
3	GND	Ground
4	SWDCLK	SWD clock

Pin#	Pin name	Description
5	GND	Ground
6	-	-
7	GND	Ground
8	-	-
9	GND	Ground
10	RESET	Reset signal for programming EZ-PD™ PMG1-S3 MCU

3.5 User LEDs and switch

The EVK has two user LEDs and one user switch connected to the EZ-PD™ PMG1-S3 MCU GPIOs. The user LEDs (green) are connected to the P3.1 and P3.2, and their functionality can be configured via the firmware. The GPIOs needs to be driven LOW to turn ON the user LEDs.

The user switch (SW3) is a tactile push-button switch on the EVK whose functionality can be configured via the firmware. When the switch is pressed, the GPIO (P3.3) connected to the button is pulled down to the ground.

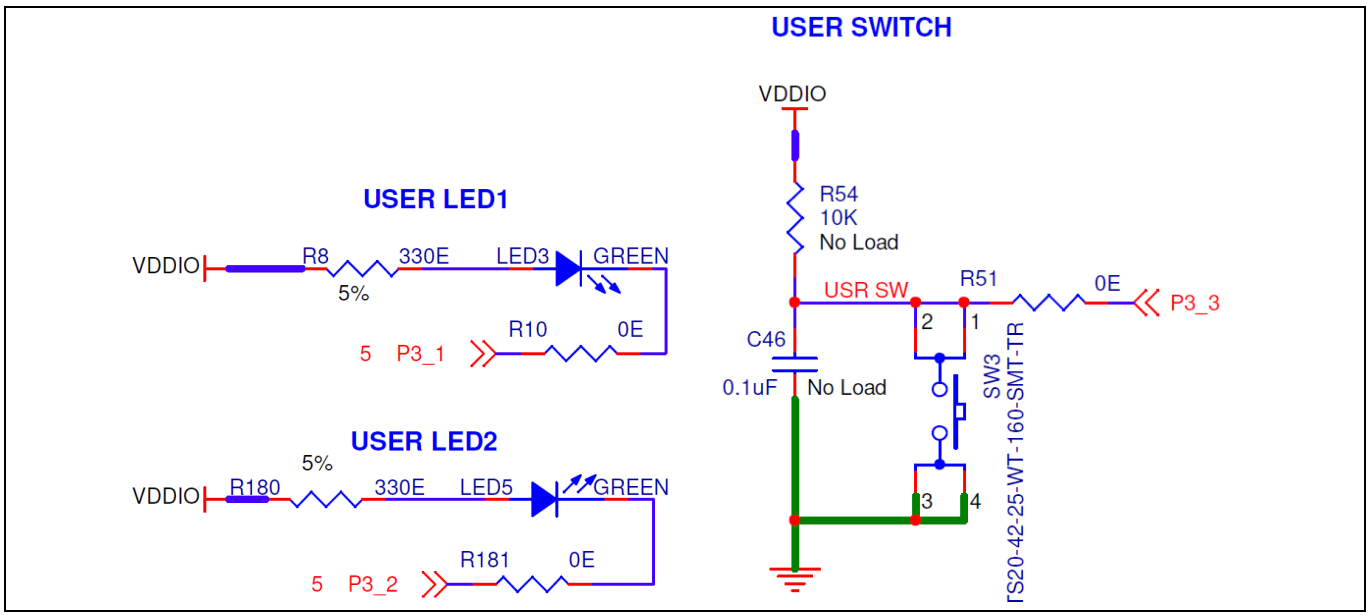

Figure 14 User LEDs and switch

3.6 Reset button

The EVK has a reset button (SW2) to manually reset the device. When the reset button is pressed, the XRES pin on the device is pulled down to the ground and resets the device.

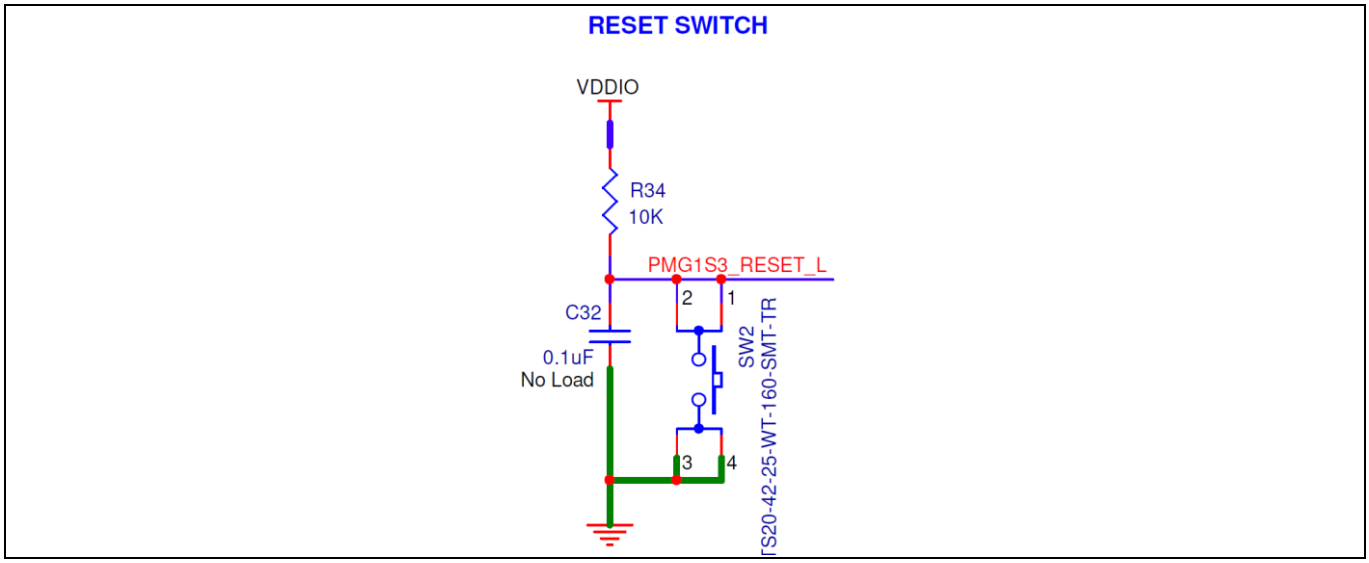

Figure 15 Reset button

3.7 CAPSENSE™ buttons and slider

The EZ-PD™ PMG1-S3 MCU supports Infineon's capacitive touch sensing called CAPSENSE™. The EVAL_PMG1_S3_DUALDRP kit has two touch buttons and one 5-sensor slider implemented using the CAPSENSE™ touch sensing feature. CAPSENSE™ buttons BUTTON0 and BUTTON1 are designed to exercise a self-capacitance-based touch button implementation. The CAPSENSE™ slider is implemented using five sensors and uses self-capacitance sensing.

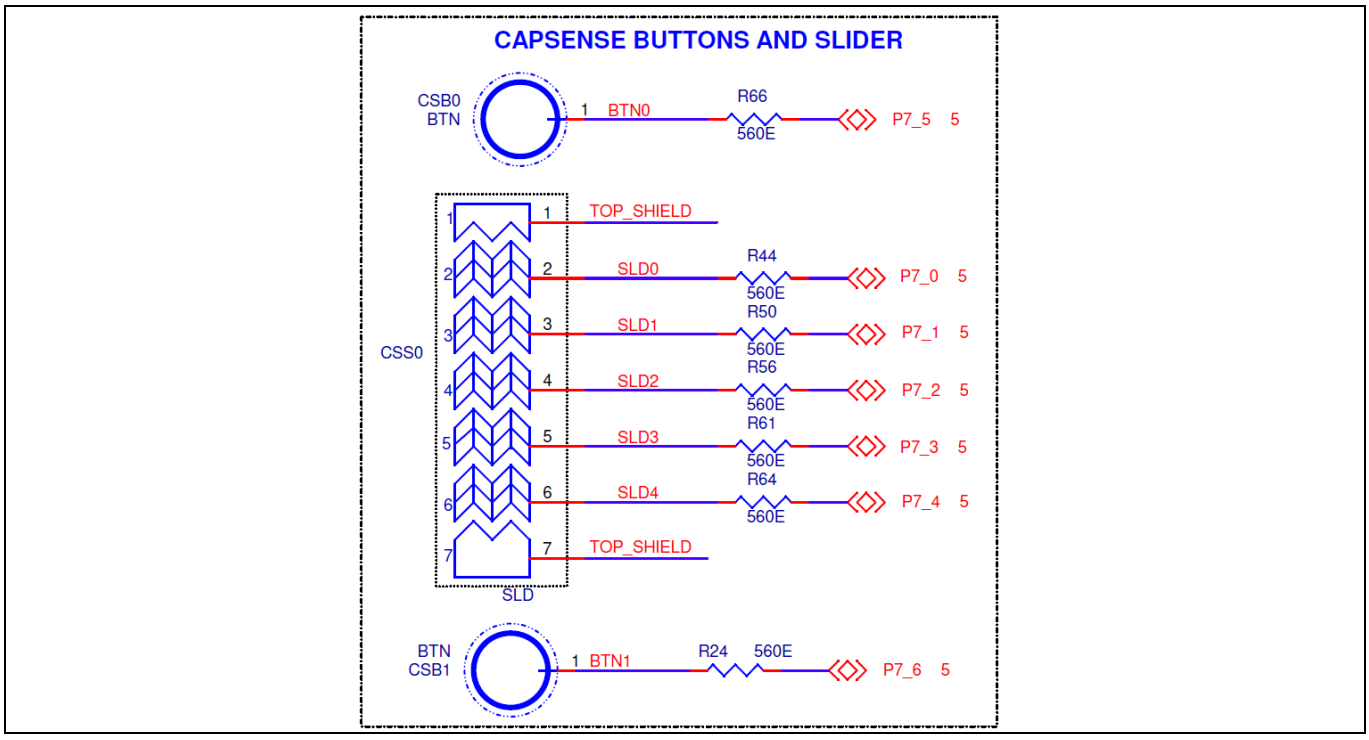

Figure 16 CAPSENSE™ buttons and slider

See the Getting started with CAPSENSE™ for a detailed introduction to CAPSENSE™ and see the PSoC™ 4 and PSoC™ 6 MCU CAPSENSE™ design guide for CAPSENSE™ design guidelines.

Each CAPSENSE™ sensor has an associated LED to indicate the status of the sensor. For the CAPSENSE™ button, the LED corresponding to the button turns ON when the button detects a touch. In the CAPSENSE™ slider, the LED corresponding to the sensor on which a finger is placed during a sliding action turns ON. The following table lists the CAPSENSE™ button, LEDs, and corresponding GPIOs.

Table 14 CAPSENSE™ buttons and slider

CAPSENSE™ widget	CAPSENSE™ sensor	Sensor GPIO	LED	LED GPIO
CAPSENSE™ button	CSB0	P7.5	LED11	P5.4
	CSB1	P7.6	LED12	P5.5
CAPSENSE™ slider	SLD0	P7.0	LED6	P1.0
	SLD1	P7.1	LED7	P1.3
	SLD2	P7.2	LED8	P1.4
	SLD3	P7.3	LED9	P2.5
	SLD4	P7.4	LED10	P2.7

CAPSENSE™ also requires an external capacitor, CMOD for self-capacitance sensing. CAPSENSE™ sensor pads are connected to the EZ-PD™ PMG1-S3 MCU through 560 Ω series resistors placed close to the MCU GPIOs that are configured as CAPSENSE™ sensor pins. The CAPSENSE™ sensors on the kit are covered with a transparent overlay (insulator material) which serves as the touch surface for the sensor below it. The sensor pads are surrounded by shield electrodes and provide optional provisions for active driven shields or ground shields to provide liquid tolerance and proximity sensing support. By default, both top and bottom shields are active driven. The shields can be connected to ground by populating the ground resistors and removing the shield connections. It is recommended to connect the CTANK capacitor for enabling the drive-in-shield feature.

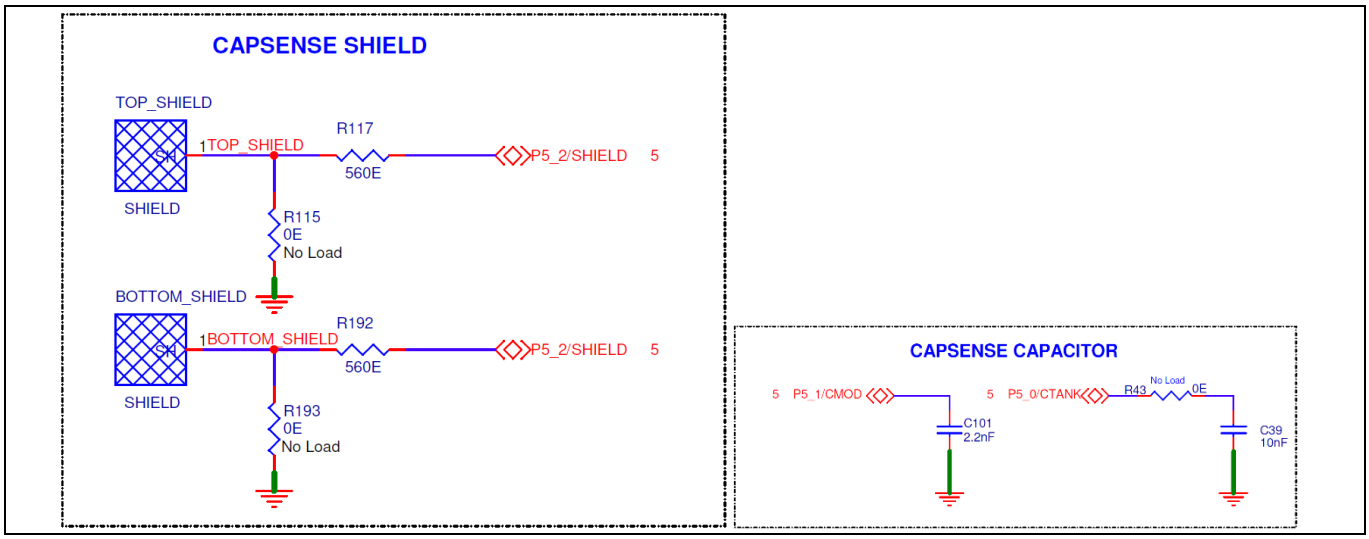

Figure 17 CAPSENSE™ shield, mod, and tank capacitor

Table 15 Components and associated features

Component	Associated feature	GPIO	LED GPIO
CTANK	Driven shield, liquid tolerance, and proximity sensing	P5.0	10-nF capacitor connected to CTANK pin through “no load” component. Populate R43 to enable CTANK
CMOD	Self-capacitance sensing	P5.1	2.2-nF capacitor connected to CMOD pin
TOP_SHIELD	Driven shield, liquid tolerance, and proximity sensing	P5.2	Shield is connected to the PMG1-S3 through resistors (R117). Remove PMG1-S3 connection and populate series resistor (R115) to enable ground shield
BOTTOM_SHIELD	Driven shield, liquid tolerance, and proximity sensing	P5.2	Shield is connected to the PMG1-S3 through resistors (R192). Remove PMG1-S3 connection and populate series resistor (R193) to enable ground shield

3.8 Vref bypass capacitor for 12-bit SAR ADC

To use 12-bit SAR ADC for sampling rates above 100 ksps (at 12 bit) in the EZ-PD™ PMG1-S3 MCU, it is recommended to use an external Vref bypass capacitor. EVAL_PMG1_S3_DUALDRP has a provision to mount the Vref capacitor (C38). By default, the capacitor is not loaded.

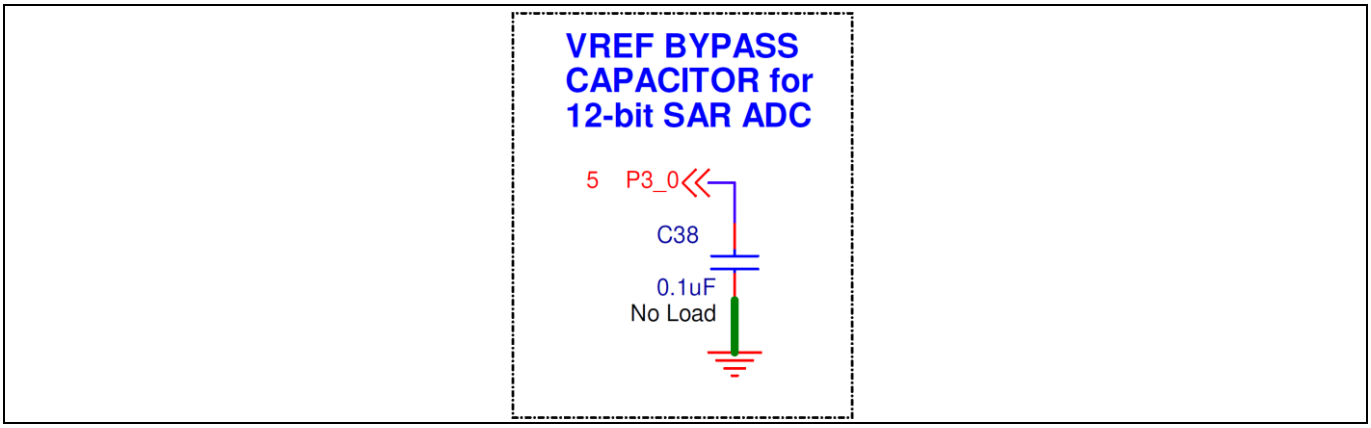

Figure 18 Vref capacitor for 12-bit SAR ADC

4 Kit operation

This section explains the operation, programming, and debugging modes of the kit. It also describes the procedure for programming and debugging the application firmware on the kit in detail.

The EVK is designed to work as a USB PD DRP and the firmware associated with the USB PD dual-role power (DRP) CAPSENSE™ code example supported in ModusToolbox™ software is downloaded in the factory on the kit.

4.1 USB PD sink operation

The EVK supports up to a maximum contract of 28 V, 5 A (140 W) in the Sink mode. The Type-C port (J10 or J14) on the EVK automatically switches to the Sink mode when a Type-C adapter is connected to it.

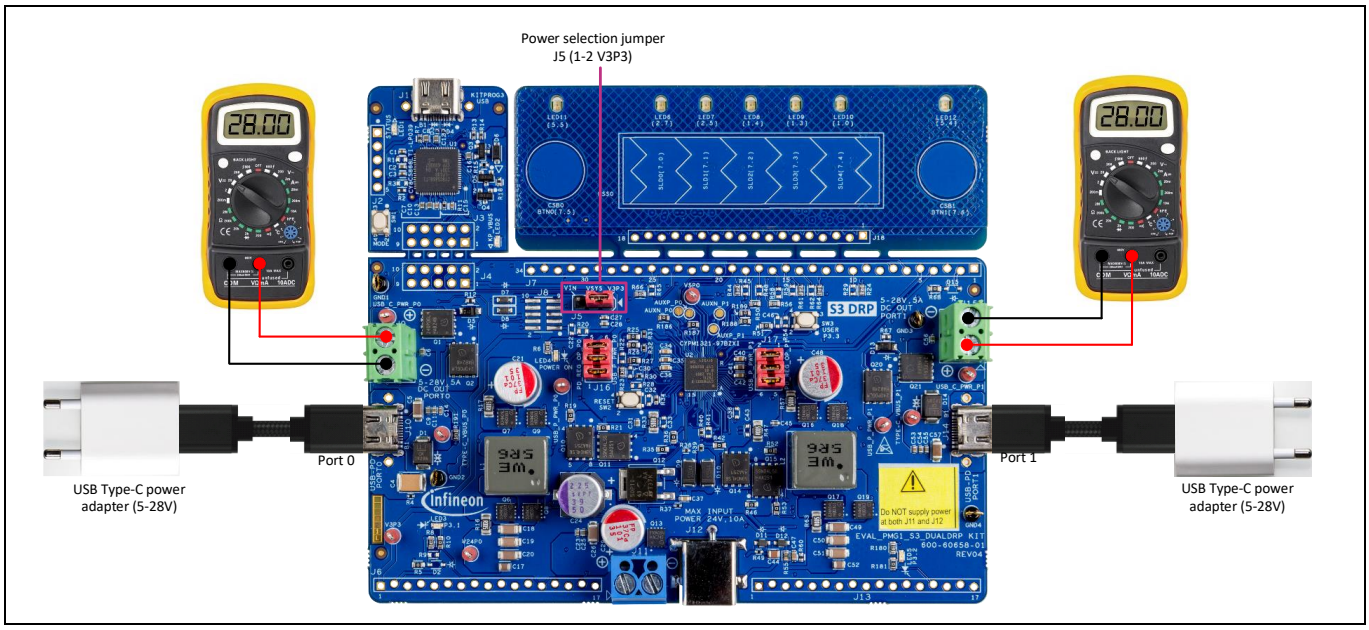

Figure 19 Test setup in Sink mode

Follow these steps to operate the EVK in the USB PD Sink mode:

1. Set the kit in Operational mode by placing a jumper shunt on the power selection jumper (J5) at position 1-2 to select the 3.3 V LDO (powered by the USB-C power adapter) as the power source for the EVK.
2. Connect the USB PD Type-C port (J10 or J14) of the board to the USB-C power adapter using the USB Type-C cable.
3. Confirm that the power LED (LED4) glows green and the user LED (LED3 for J10 and LED5 for J14) blinks green at a rate of 1 Hz.
4. Measure the DC_OUT voltage by connecting a multimeter to the terminal block (J9 for Port 0 and J15 for Port 1). Confirm that the DC_OUT voltage value is within the 4.75 V–29.4 V range. The actual value is determined by the maximum voltage, which the USB-C power adapter can supply. Only power adapters that support USB PD EPR can provide PD contract voltages greater than 20 V.
5. If Port 0 is connected to the power adapter, the CAPSENSE™ buttons and sliders can be used to renegotiate the PD contract at different voltage levels based on the connected USB-C power adapter capability. Touch CAPSENSE™ Button 0 to negotiate up 20 V at 900 mA SPR PD contract or touch CAPSENSE™ Button 1 to negotiate up to 28 V at 5 A EPR PD contract. Touch CAPSENSE™ slider 0, 1, 2, 3, or 4 to negotiate PD contracts up to 5 V, 9 V, 12 V, 15 V, or 20 V respectively at 900 mA.

6. Remove the multimeter and connect an external load to the terminal block (J9 for Port 0 and J15 for Port 1) to sink the power output.

Attention: ***The maximum current that can be consumed by an external load is limited to 5 A by the USB PD specification. If the load exceeds 5 A, the USB-C power adapter may trigger overcurrent protection (OCP) and cut off the power supply to the kit. This behavior is dependent on the implementation of the USB-C power adapter.***

4.2 USB PD source operation

The EVK switches to Source mode if powered via an external power supply at the DC input terminal (J11) or the DC input barrel jack (J12). The EVK supports up to a maximum contract of 20 V and 5 A (100 W) in the Source mode. When a Type-C device is connected to any of the USB PD Type-C ports (J10 for Port and J14 for Port 1) of the EVK, the EVK offers the PDOs of 5 V, 9 V, 12 V, 15 V, and 20 V on the connected port. The connected Type-C device should be compatible with one of these PDOs to test the source operation successfully.

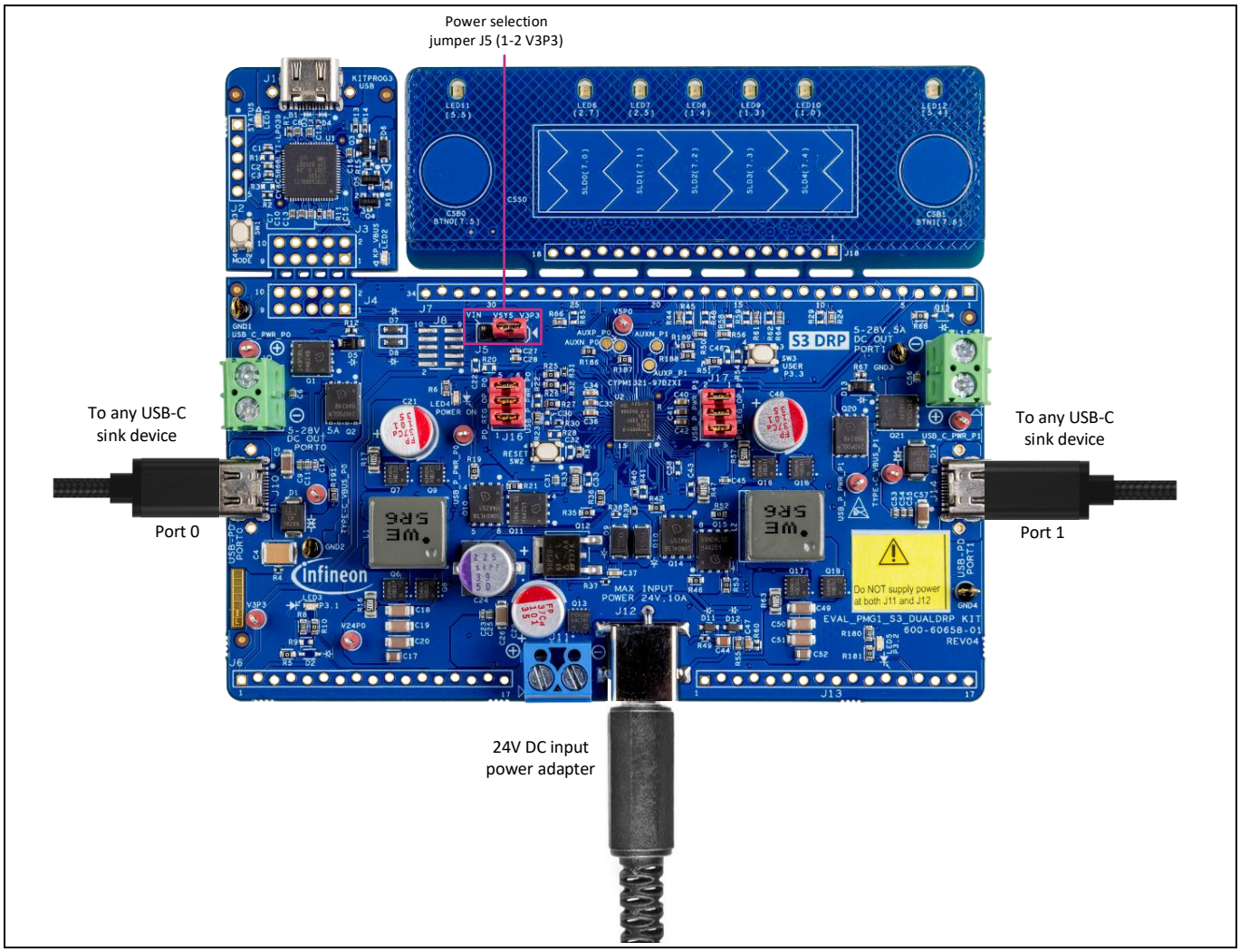

Figure 20 Test setup in Source mode

Follow these steps to operate the EVK in the USB PD Source mode:

1. Set the kit in Operational mode by placing a jumper shunt on the power selection jumper (J5) at position 1-2 to select the 3.3 V LDO (powered by the DC input) as the power source for the EVK.

2. Power up the kit using a 24 V power adapter (J12) or using an external 24 V DC power supply (J11). Do not connect both power sources together, see the Attention section.
3. Confirm that the power LED (LED4) glows continuously.
4. Connect a Type-C USB PD sink device at the USB PD Type-C port (J10 for Port 0 and J14 for Port 1) of the EVK.
5. Confirm that the user LED (LED3 for J10 and LED5 for J14) glows continuously.
6. Check if the Type-C device is drawing the power (if the load is a mobile device, it starts charging).
7. If Port 0 is connected to the Type-C device, the CAPSENSE™ sliders can be used to renegotiate the PD contract at different voltage levels. Touch CAPSENSE™ slider 0, 1, 2, 3, or 4 to negotiate PD contracts up to 5 V, 9 V, 12 V, 15 V, or 20 V, respectively, at 900 mA.

Two ports operation:

To test simultaneous source and sink operation, connect one Type-C device to the one USB PD Type-C port of the EVK (as mentioned in steps 4-7) and test the other port for load sinking by repeating the steps 2-5 from the USB PD sink operation.

Optionally, test the different combinations in Table 7 to see the EVK's USB PD Type-C ports in different power roles independent of each other.

Attention: ***Verify that only one of J11 or J12 is powered during EVK operation, as both supplies are shorted together at board level and may damage the board/supplies if powered together.***

Attention: ***The kit should be powered on using a compatible power adapter only. The voltage output of the power adapter/DC supply connected at J12/J11 should be 24 V ± 10%.***

Attention: ***The components and device surfaces of the EVAL_PMG1_S3_DUALDRP kit may become hot if higher power is being sourced from the USB PD Type-C port of the EVK. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.***

5 Application development on EVK using ModusToolbox™ and ModusToolbox™ Programmer

The EZ-PD™ PMG1 MCU-based projects are developed using the ModusToolbox™ software development tool. ModusToolbox™ software is a set of multi-platform development tools and a comprehensive suite of GitHub-hosted firmware libraries.

If you are new to the ModusToolbox™ software, see the documentation on the ModusToolbox™ software environment home page.

The prototyping kit can be programmed and debugged through any of the following interfaces:

- KitProg3 USB Type-C port
- 10-pin SWD header
- I/O header pins

The kit supports programming and debugging via the KitProg3 interface by default.

5.1 Programming through the KitProg3 interface

5.1.1 Using ModusToolbox™ software

KitProg3 is a PSoC™ 5LP MCU-based onboard programming and debugging solution integrated with the EZ-PD™ PMG1 MCU prototyping kits. You can program and debug the kit without using any separate programming and debug module. Connect the kit to the PC using the programming connecter as shown in Figure 21.

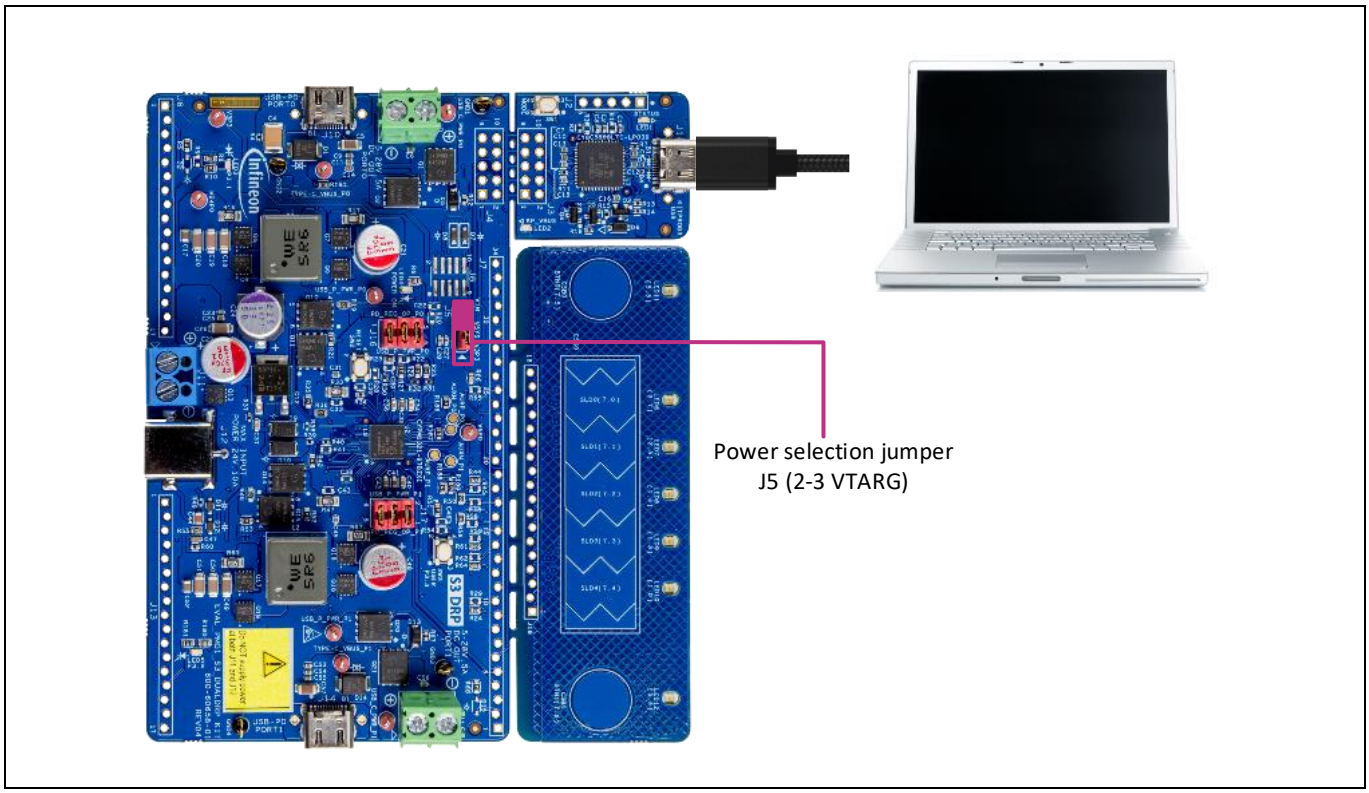

Figure 21 Programming through the KitProg3 interface

Application development on EVK using ModusToolbox™ and ModusToolbox™ Programmer

Follow these steps to program the prototyping kit using the KitProg3 interface from the ModusToolbox™ software:

1. Open the Eclipse IDE for ModusToolbox™ software and select the PMG1 project on the host PC. For details, see the Eclipse IDE for ModusToolbox™ user guide.
2. Connect the power section jumper (J5) to position 2-3 (VIN).
3. Connect the kit to the host PC through the KitProg3 USB Type-C port (J11).
4. Ensure that LED1 and LED2 glow amber.
   - LED2 (KitProg3 power LED) indicates that the KitProg3 module and target MCU are powered
   - LED1 (status LED) indicates the Programming mode and status, and is ON when KitProg3 is powered
5. In the Project Explorer, select the intended project as the current active project as shown in the following figure.

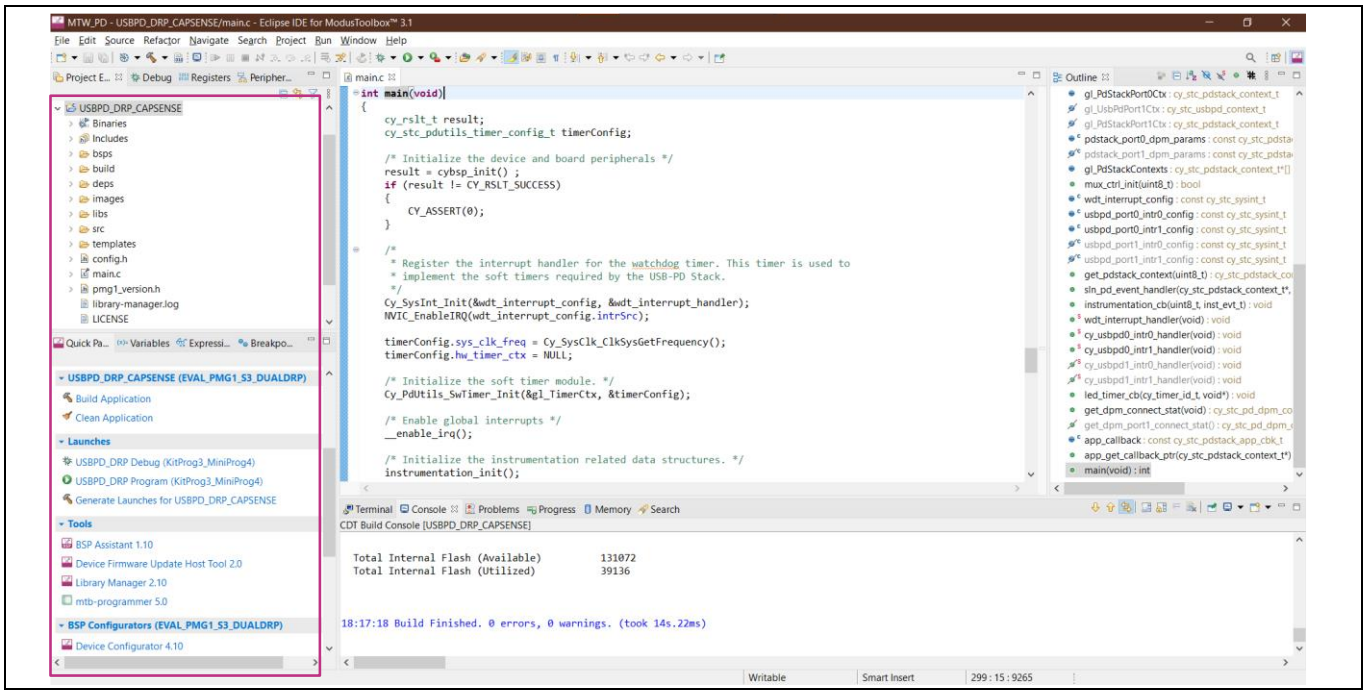

Figure 22 Eclipse IDE for ModusToolbox™ software

6. On the **Quick Panel**, click **<Application name> Program (KitProg3_MiniProg4)** from the **Launches** section as shown in Figure 23.

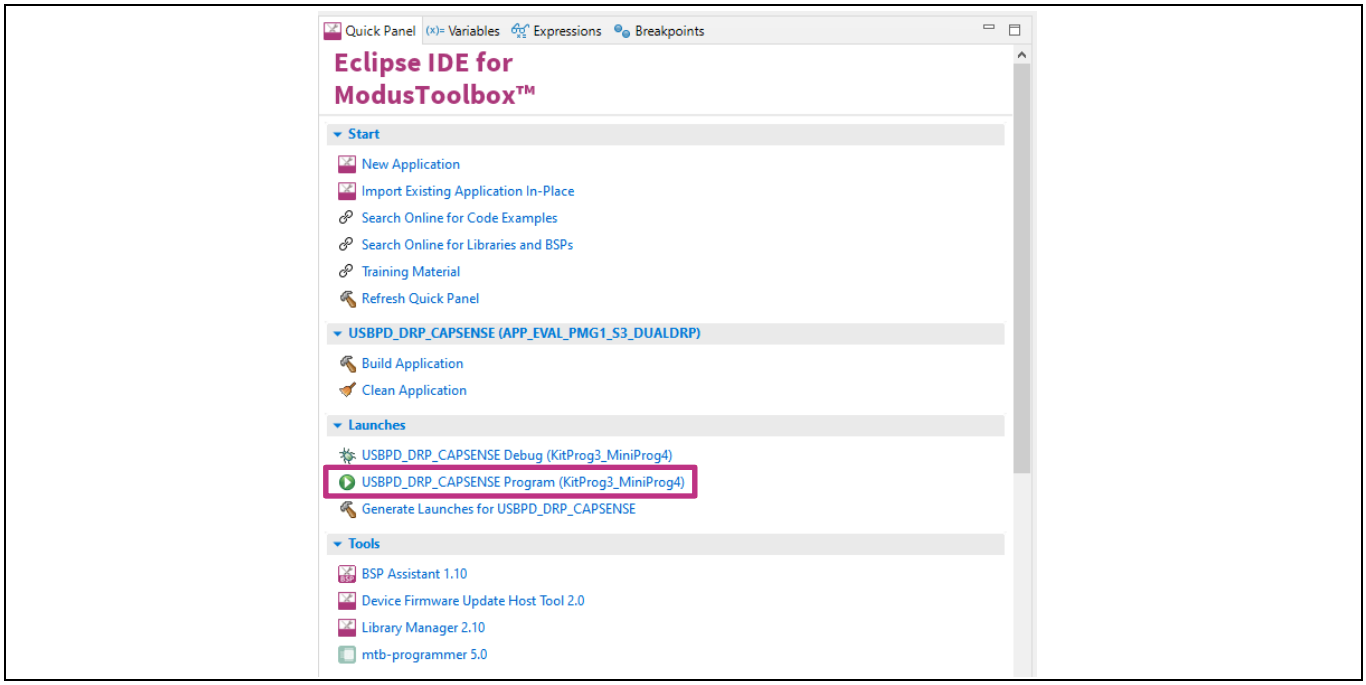

Figure 23 Quick Panel and programming options

7. The **Console** tab displays the progress of the build/program. You can check the **Problems** tab for any errors and warnings. On successful program completion, the success message is displayed on the **Console** tab.

5.1.2 Using ModusToolbox™ Programmer

ModusToolbox™ Programmer is a stand-alone, cross-platform, flash programmer tool. It provides a GUI to program, erase, verify, and read the flash of the target MCU. Also, it supports the HEX, SREC, ELF, and BIN programming file formats.

Download and install ModusToolbox™ Programmer through Infineon Developer Center and do the following to program the EVAL_PMG1_S3_DUALDRP kit.

1. Connect the power section jumper (J5) to position 2–3 (VIN).
2. Connect the kit to the host PC through the KitProg3 connector. See Figure 21 for the setup.
3. Launch ModusToolbox™ Programmer.
4. From the **Probe/Kit** dropdown list, select **EVAL_PMG1_S3_DUALDRP**. Based on the selection, the **Platform** displays PMG1 and the **Log** panel displays the selected device/kit/probe name.

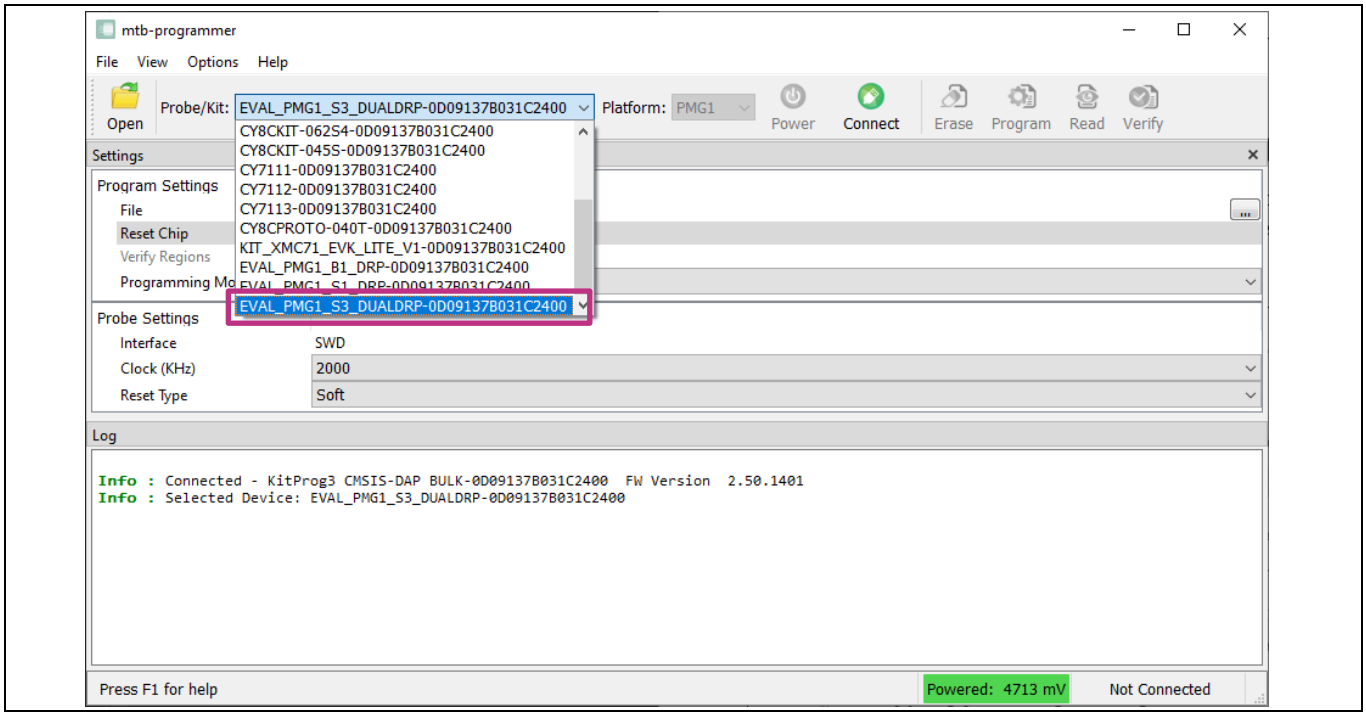

Figure 24 Selecting the probe/kits

5. Click **Open** to load the programming file. In the **Open programming file** dialog, browse to the location of the HEX, SREC, ELF, or BIN file to be loaded. Select the file and click **Open**.

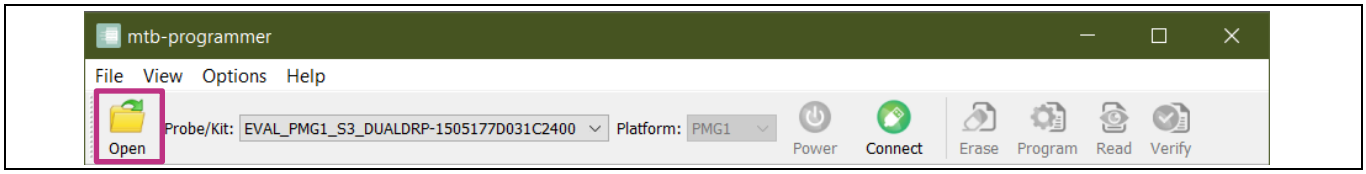

Figure 25 Loading the programming file

6. Click **Connect**. ModusToolbox™ Programmer connects to the target board and the **Erase**, **Program**, **Read**, and **Verify** options appear.

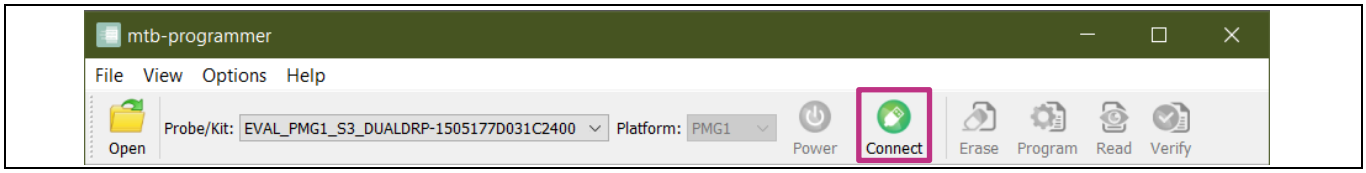

Figure 26 Establishing a connection with MCU

7. Click **Program** to initiate the firmware update. On successful program completion, the message “Device programmed successfully” appears on the bottom left as shown in Figure 27.

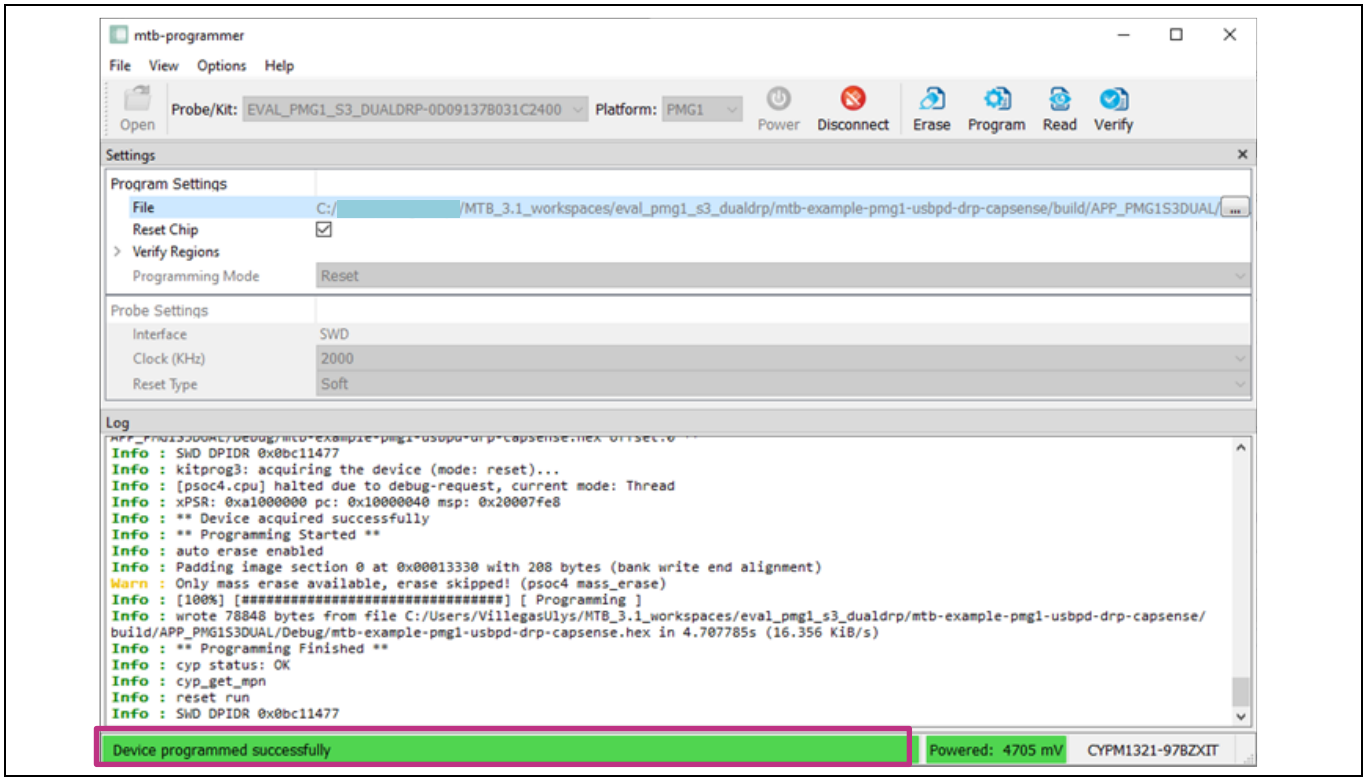

Figure 27 Programming through ModusToolbox™ Programmer

5.2 Debug mode using KitProg3 interface and ModusToolbox™

The kit power selection jumper(J5) needs to be configured in Operational mode for the debugging.

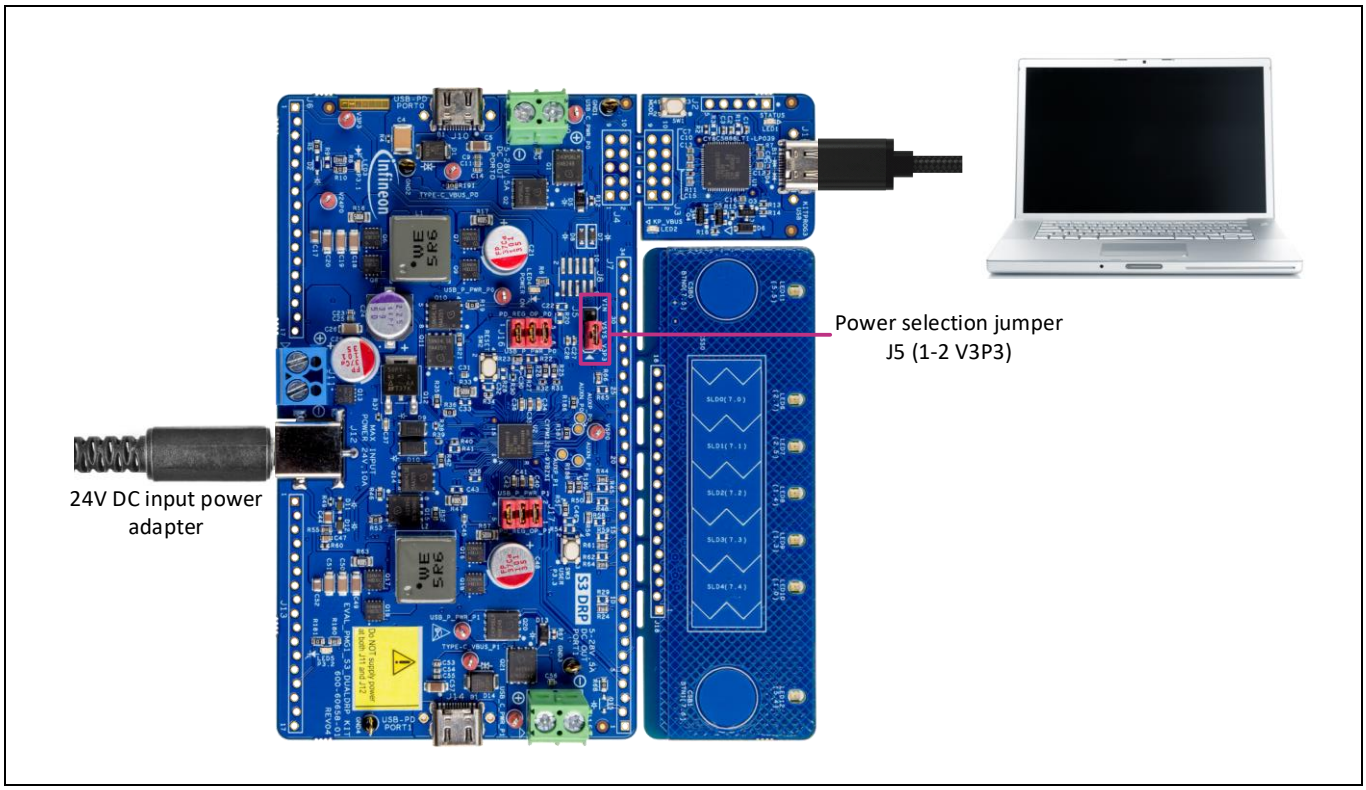

Figure 28 Debugging through KitProg3

Application development on EVK using ModusToolbox™ and ModusToolbox™ Programmer

Follow these steps to enter the Debug mode from the KitProg3 interface using the Eclipse IDE for ModusToolbox™ software.

1. Open the Eclipse IDE for ModusToolbox™ software and select the PMG1 project on the host PC. For details, see the Eclipse IDE for ModusToolbox™ software user guide.
2. Place the jumper shunt on pins 1–2 of the power section jumper (J5) to configure the kit in Operational mode.
3. Connect the external power to the kit using the power adapter (J12) or the DC power supply (J11).
4. Connect the kit to the host PC through the programming KitProg3 USB Type-C port. Ensure that LED1 and LED2 glow amber.
5. On the **Quick Panel**, click the **USBPD_DRP_CAPSENSE Debug (KitProg3_MiniProg4)** option from the **Launches** section.
6. The IDE switches to the debug mode and halts at the first line of the `main()` function, indicating that the application is ready for debugging.

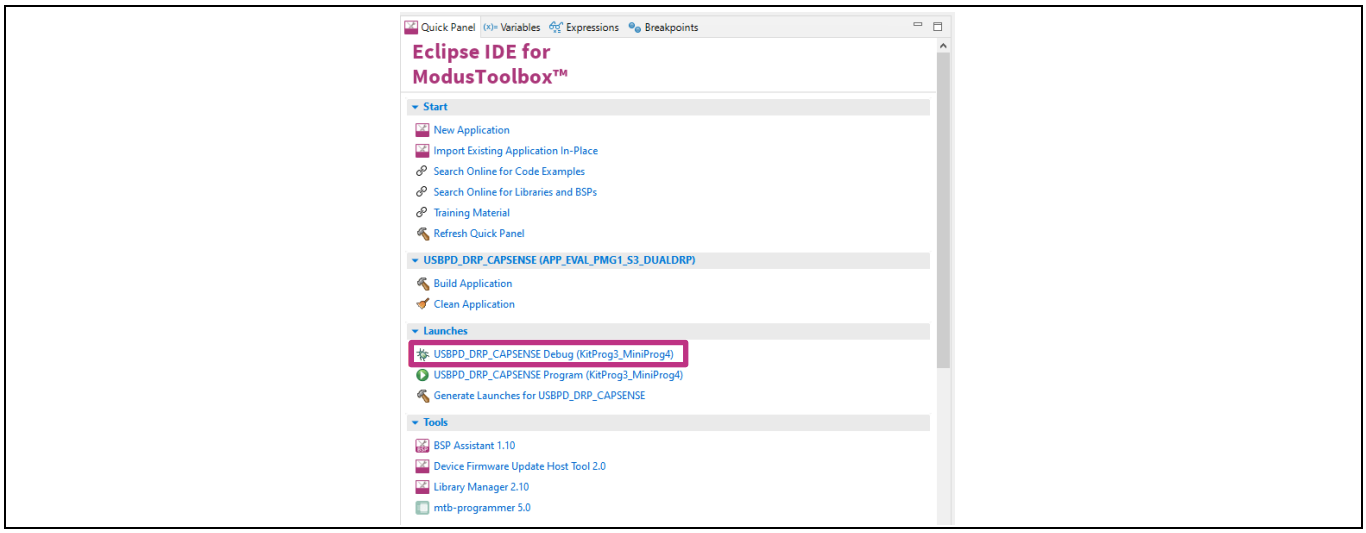

Figure 29 Quick Panel and programming options

5.3 Programming and debugging using J-Link debug probes

The EZ-PD™ PMG1 family MCUs are supported by the Segger J-Link software. Download and install the latest version (v7.92 or above) of J-Link software from the J-Link/J-Trace download page.

The EVAL_PMG1_S3_DUALDRP kit supports programming and debugging using the Segger J-Link in-circuit debugger through the 10-pin SWD connector (J8).

The J-Link debugger probes have a 19-pin (2.54 mm) connector to interface with target boards. For interfacing J-Link Debugger probes to the EVK through the onboard 10-pin SWD connector, use a 9-pin Cortex®-M Adapter from Segger.

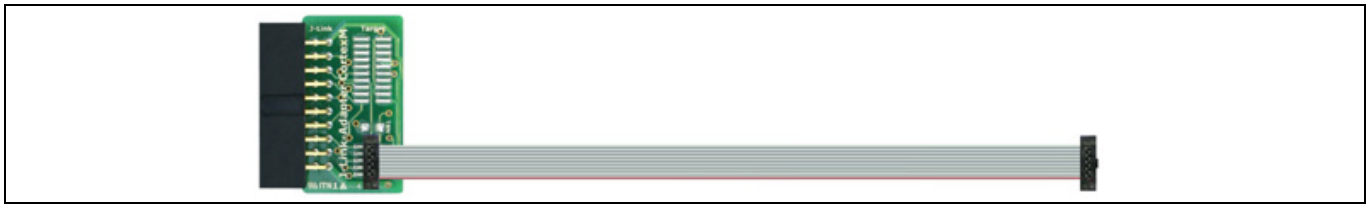

Figure 30 9-Pin Cortex®-M adapter

Application development on EVK using ModusToolbox™ and ModusToolbox™ Programmer

The J-Link debugger measures the target MCU's voltage through the VTARG pin to detect and establish the connection. The reverse voltage protection diode (D8) between the VTARG pin (of J8) and VSYS (J5.3) prevents the measurement of the target MCU voltage on the VTARG pin. Do the following changes in hardware before using J-Link.

1. Solder on a standard mini SWD 0.05-inch-pitch connector. FTSH-105-01-L-DV-K-P-TR from Samtech is the recommended connector.
2. Populate the 0 ohm series resistor (R20) between VTARG (J8.1) and VDDD (MCU).

Do the following to program or debug the EVAL_PMG1_S3_DUALDRP kit using the J-Link probe from ModusToolbox™ software:

1. Open the Eclipse IDE for ModusToolbox™ software on the host PC and select the PMG1 project. For details, see the Eclipse IDE for ModusToolbox™ software user guide.
2. Place the jumper shunt on pins 1-2 of the power section jumper (J5) to configure the kit in Operational mode.
3. Connect the USB PD sink port (J10 or J14) to the USB PD source to activate the onboard LDO, load switch, and user LED. Ensure that the LED4 (power LED) glows green.
4. Connect the J-Link debugger to the EVK through a 10-pin SWD connector and use a 9-pin Cortex®-M adapter.

Do the following on the Quick Panel to program and debug the application:

- To program the MCU, click **<Application name> Program (J-Link)** from the **Launches** section
- To debug the application, click **<Application name> Debug (J-Link)** from the **Launches** section. The IDE switches to Debugging mode and halts at the first line of the `main()` function. This indicates that the application is ready for debugging.

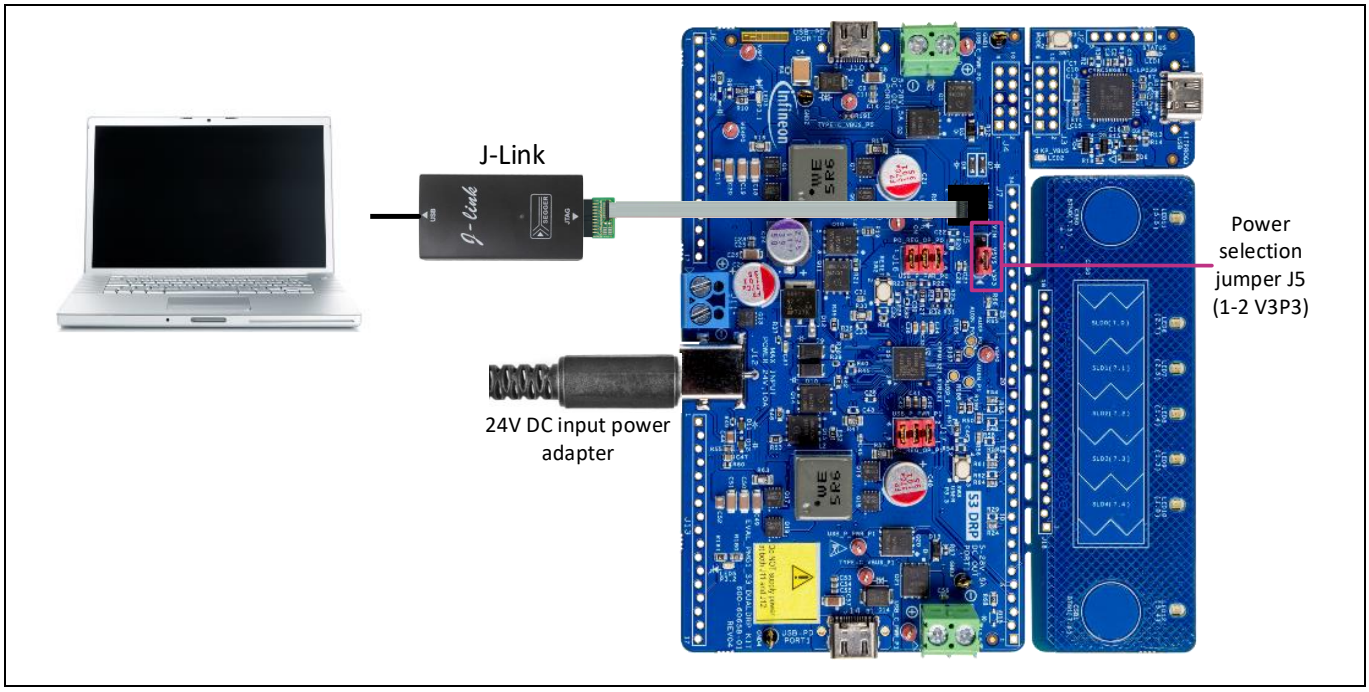

Figure 31 Program/debug using J-Link debugger probes

6 Troubleshooting

6.1 Common problems and troubleshooting

Table 16 lists common problems and troubleshooting methods that may be encountered during operation in the Kit operation section.

Table 16 Common issues, causes, and solutions

S. No.	Issue	Possible cause	Possible solution(s)
1	The EVK USB PD Type-C port does not enter PD contract	The power selection jumper may not be set to the correct setting.	Set the power selection jumper to Operational mode (1-2).
2	Connection to PMG1-S3 is unsuccessful using KitProg3	PMG1-S3 may not be powered.	If the power selection jumper is in Operational mode (1-2), verify that the kit is powered externally via J11 or J12 or alternatively set the power selection jumper to Programming mode (2-3)
3	The USB PD Type-C port only makes a 5 V contract.	The Type-C device connected to the port only supports 5 V contract.	Connect a Type-C device that supports PDOs greater than 5 V.
4	An EPR Type-C power adapter is connected to the USB PD Type-C port of the EVK, but does not enter a PD contract greater than 100 W.	The Type-C cable used does not support EPR.	Connect a Type-C cable that supports extended power range (EPR – up to 140 W).
5	The EVK is in Operational mode and power is connected to the DC input, but the PD port does not supply power.	The jumper (J16/J17) that connects the on-board PD regulator output to the Type-C VBUS is incorrectly set.	Set the jumper position to the default jumper settings (1-2, 3-4, 5-6).

7 Appendices

7.1 Appendix A

7.1.1 KitProg3

An onboard PSoC™ 5LP MCU (CY8C5868LTI-LP039)-based KitProg3 module is used to program and debug the EZ-PD™ PMG1 microcontroller.

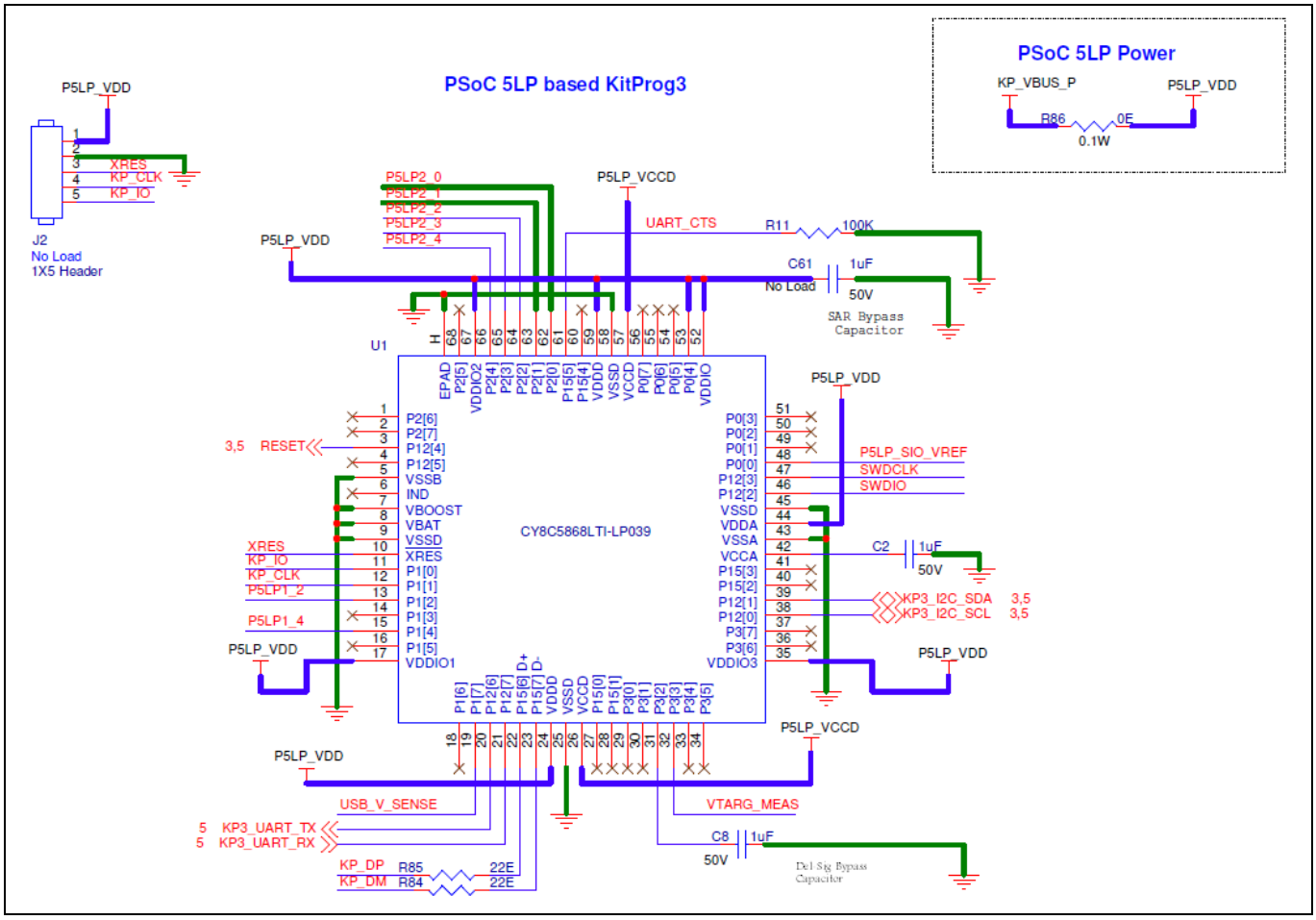

Figure 32 PSoC™ 5LP MCU device

The PSoC™ 5LP MCU device interfaces with a PC through a Type-C USB connector (J1), and functions as a bridge between the PC and EZ-PD™ PMG1-S3 MCU over SWD, I2C, and UART interfaces. The KitProg3 module is powered through the J1 port and receives and transmits data between the host PC through D+ and D-signals. The programming/debugging module can access the EZ-PD™ PMG1-S3 MCU in Programming or Debugging mode via the SWD header. In addition to being an onboard programmer, the KitProg3 functions as an interface for the USB-I2C and USB-UART bridges.

The USB-serial pins of the PSoC™ 5LP MCU are hard-wired to the I2C pins of the EZ-PD™ PMG1-S3 MCU, and these pins are also available on the KitProg3 headers (J3 and J4). The USB-UART bridge functionality is enabled by default by hard-wired connections of the UART lines between KitProg3 and EZ-PD™ PMG1-S3 MCU.

7.1.1.1 Mode button

The KitProg3 mode button on the EVK enables the KitProg3 module to enter Bootloader mode. The Bootloader mode is required to update the KitProg3 firmware on PSoC™ 5LP MCU when the existing firmware is corrupted or a newer version is available.

7.1.1.2 KitProg3 power and status LEDs

The KitProg3 power LED (LED2, amber) turns ON when the KitProg3 module is powered. The LED will always be ON in a fault-free condition when the kit is powered through the programming connector.

The status LED (LED1, amber) indicates the KitProg3 USB connection and programming status. See the KitProg3 user guide for details.

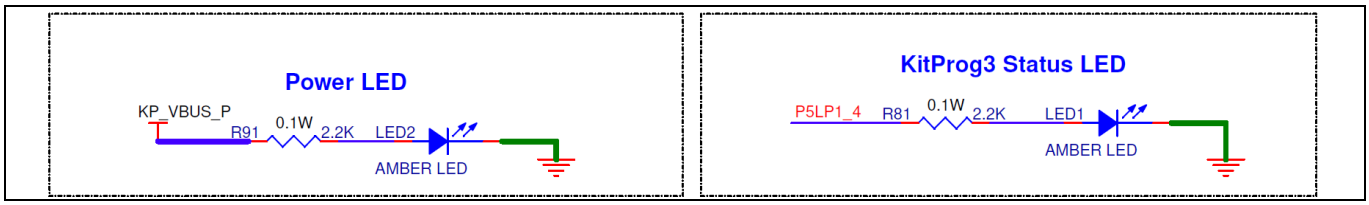

Figure 33 KitProg3 Power and status LED

7.1.1.3 KitProg3 overvoltage protection circuit

A MOSFET and a Zener diode-based protection circuit is implemented to protect the KitProg3 (PSoC™ 5LP MCU) from damage due to overvoltage and reverse voltage fault on the programming Port (J1). The maximum rating for the PSoC™ 5LP MCU device is 5.8 V; the circuit shuts down the power supply if the voltage exceeds 5.8 V.

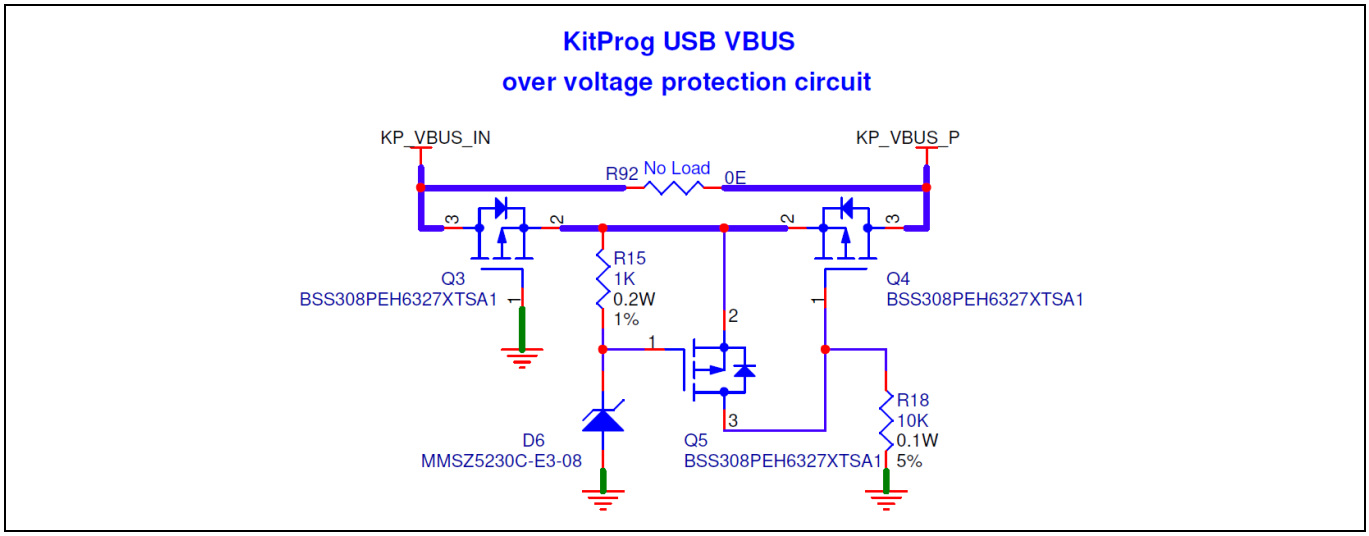

Figure 34 Overvoltage protection circuit for KitProg3

7.1.1.4 Target voltage measurement

The KitProg3 module is required to monitor the voltage at which the target MCU is working. The measured target voltage is used as the reference to configure the logic level for communication between the KitProg3 and the EZ-PD™ PMG1-S3 MCU.

7.2 Appendix B

7.2.1 EVAL_PMG1_S3_DUALDRP schematics

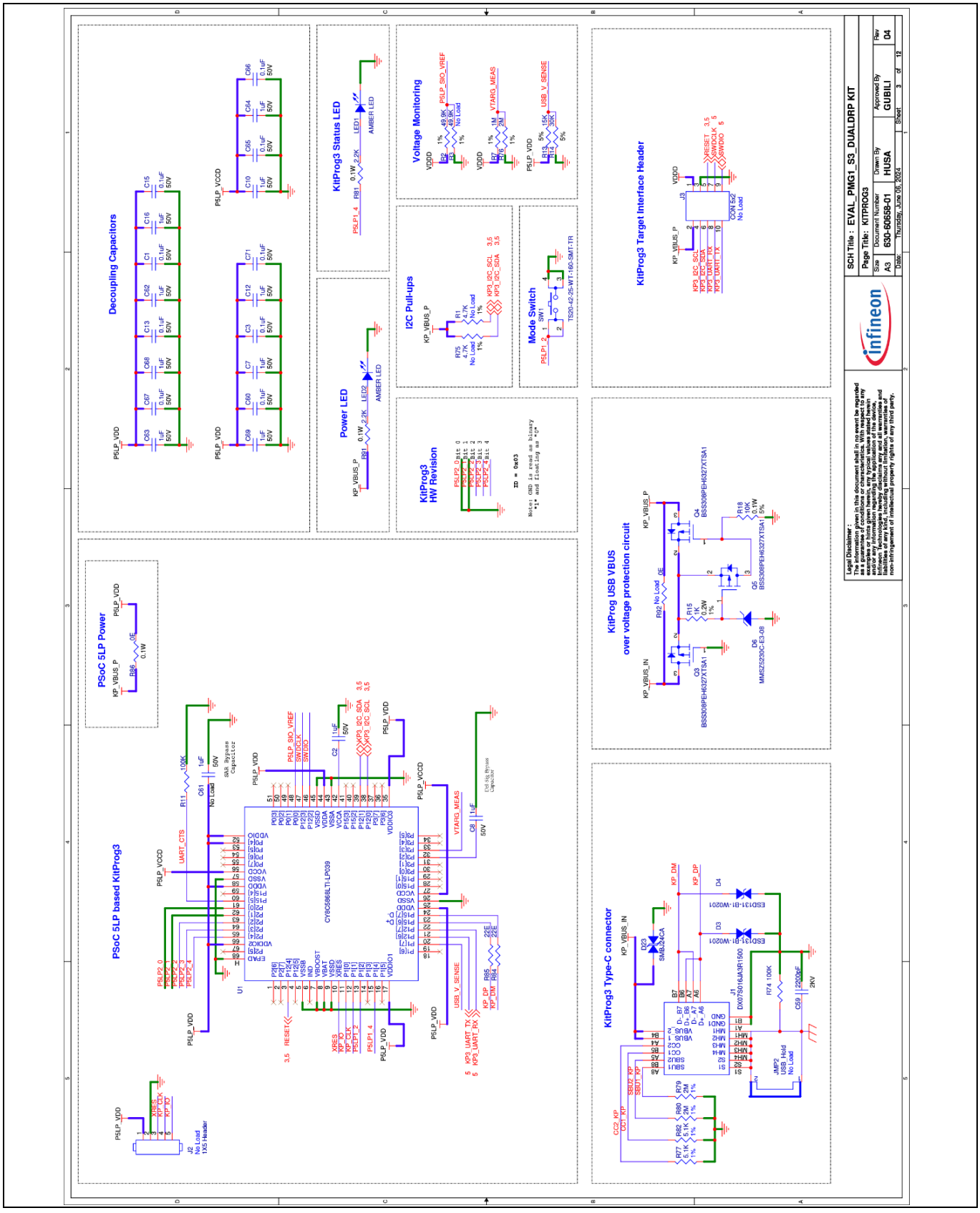

Figure 35 KitProg schematics

Appendices

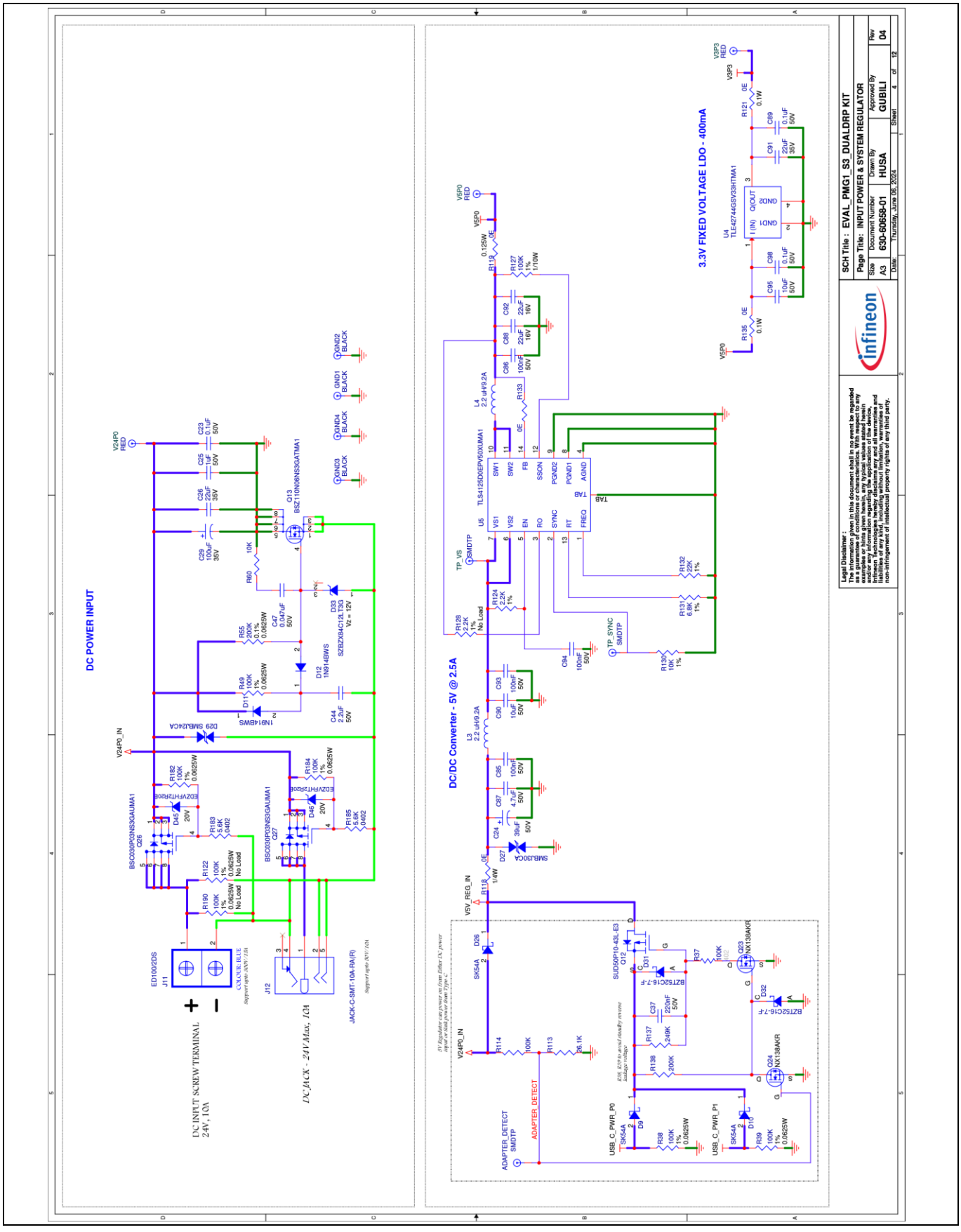

Figure 36 DC input power and system regulator schematics

Appendices

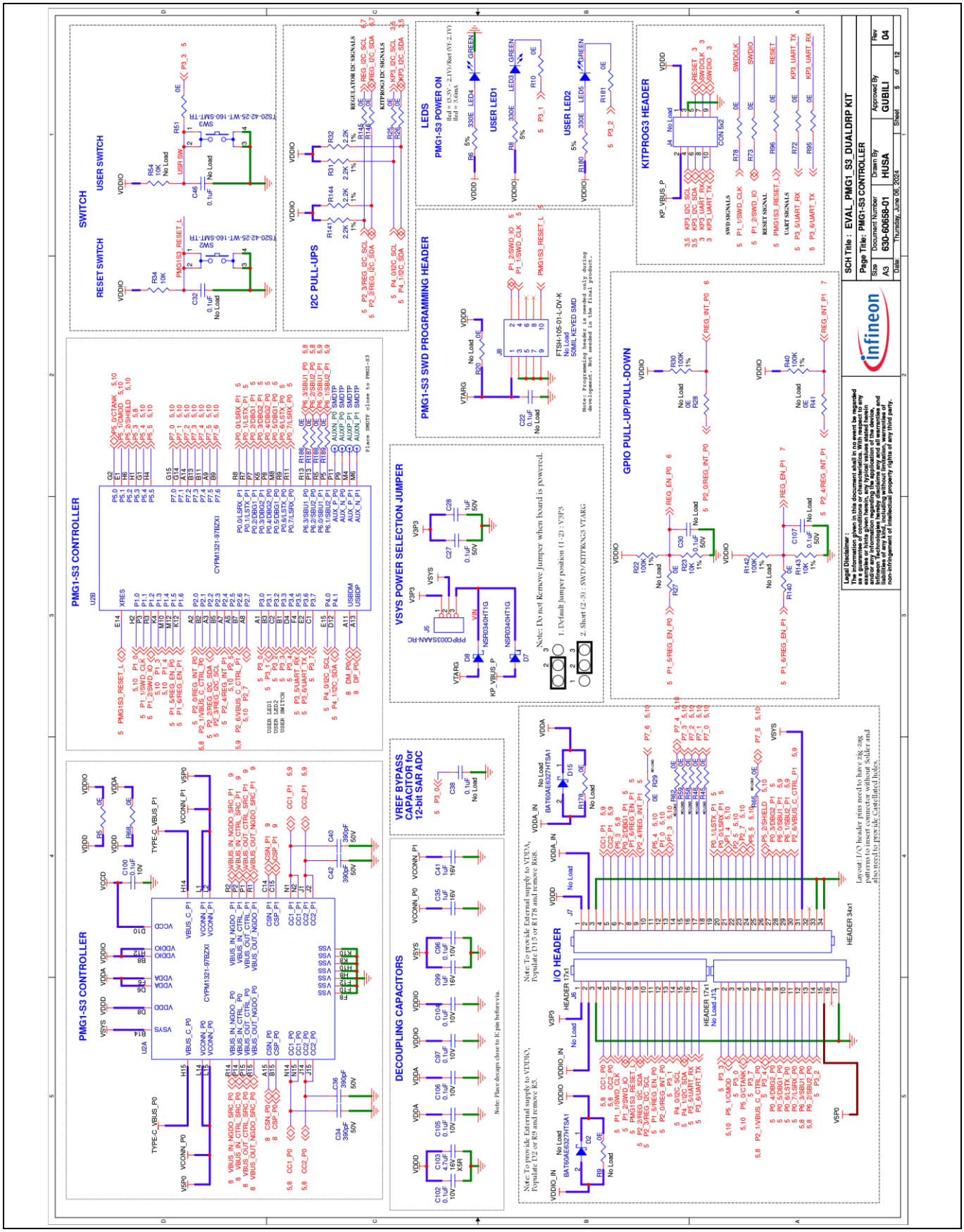

Figure 37 PMG1 S3 MCU schematics

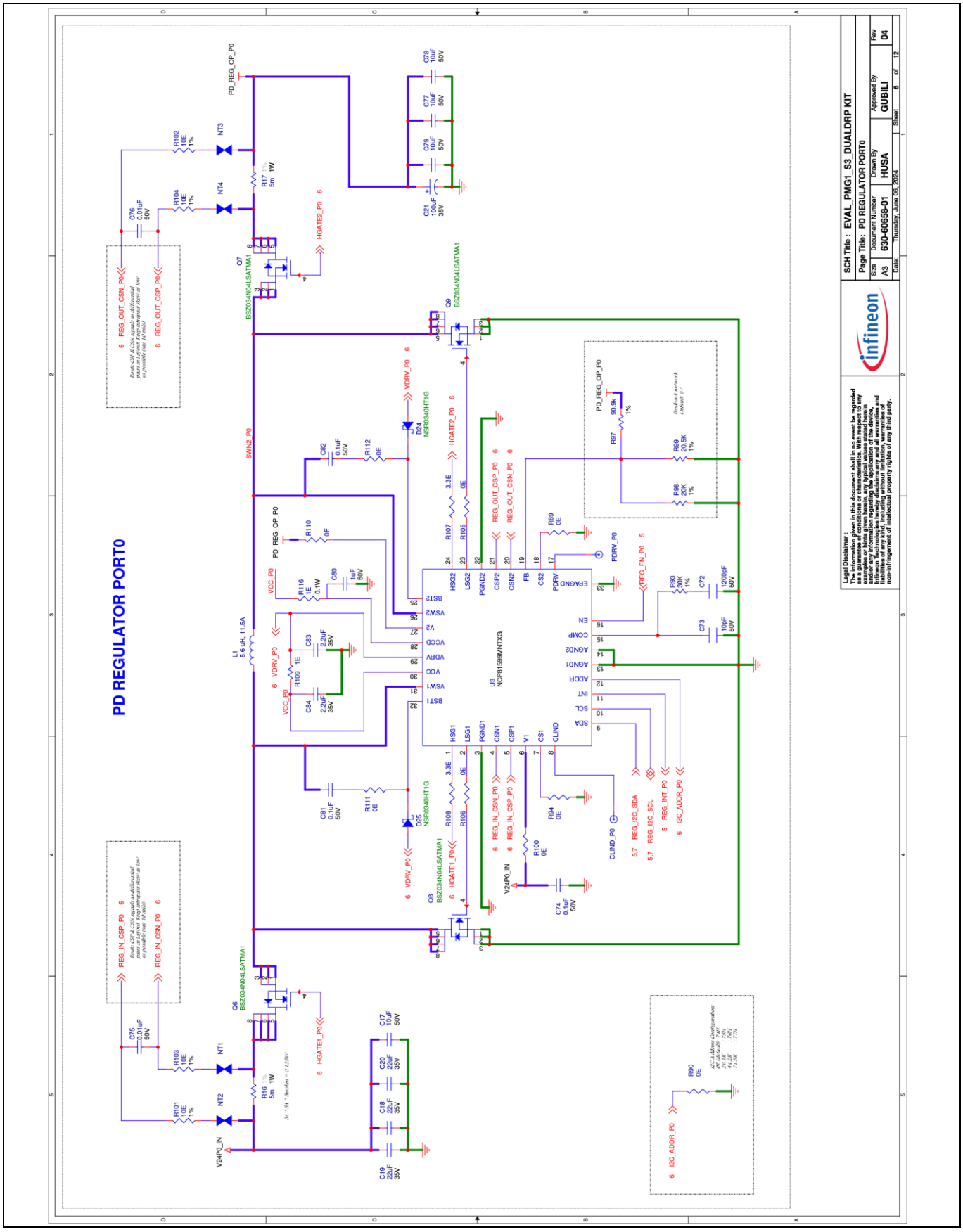

Figure 38 USB PD source buck-boost regulator Port 0 schematics

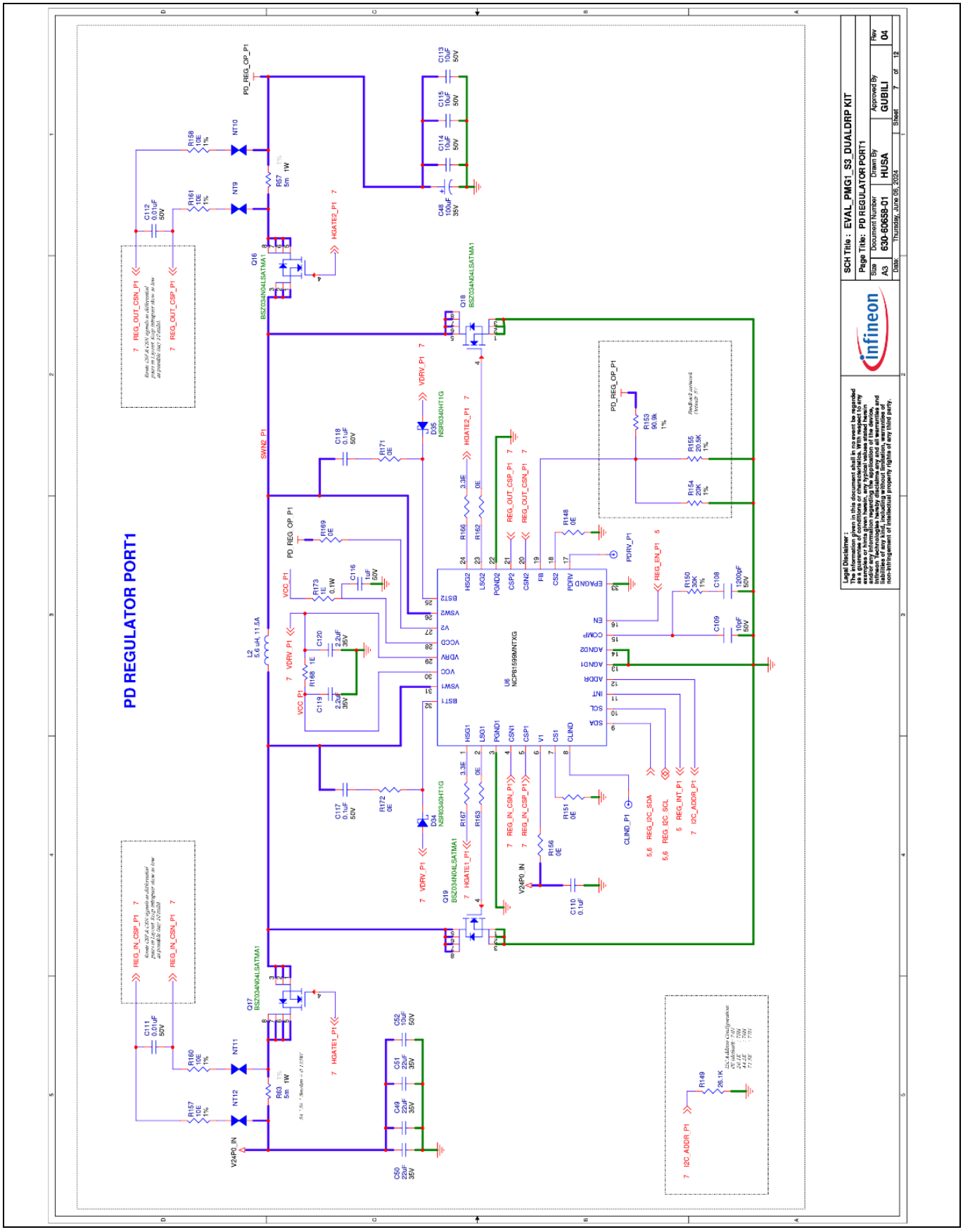

Figure 39 USB PD source buck-boost regulator Port 1 schematics

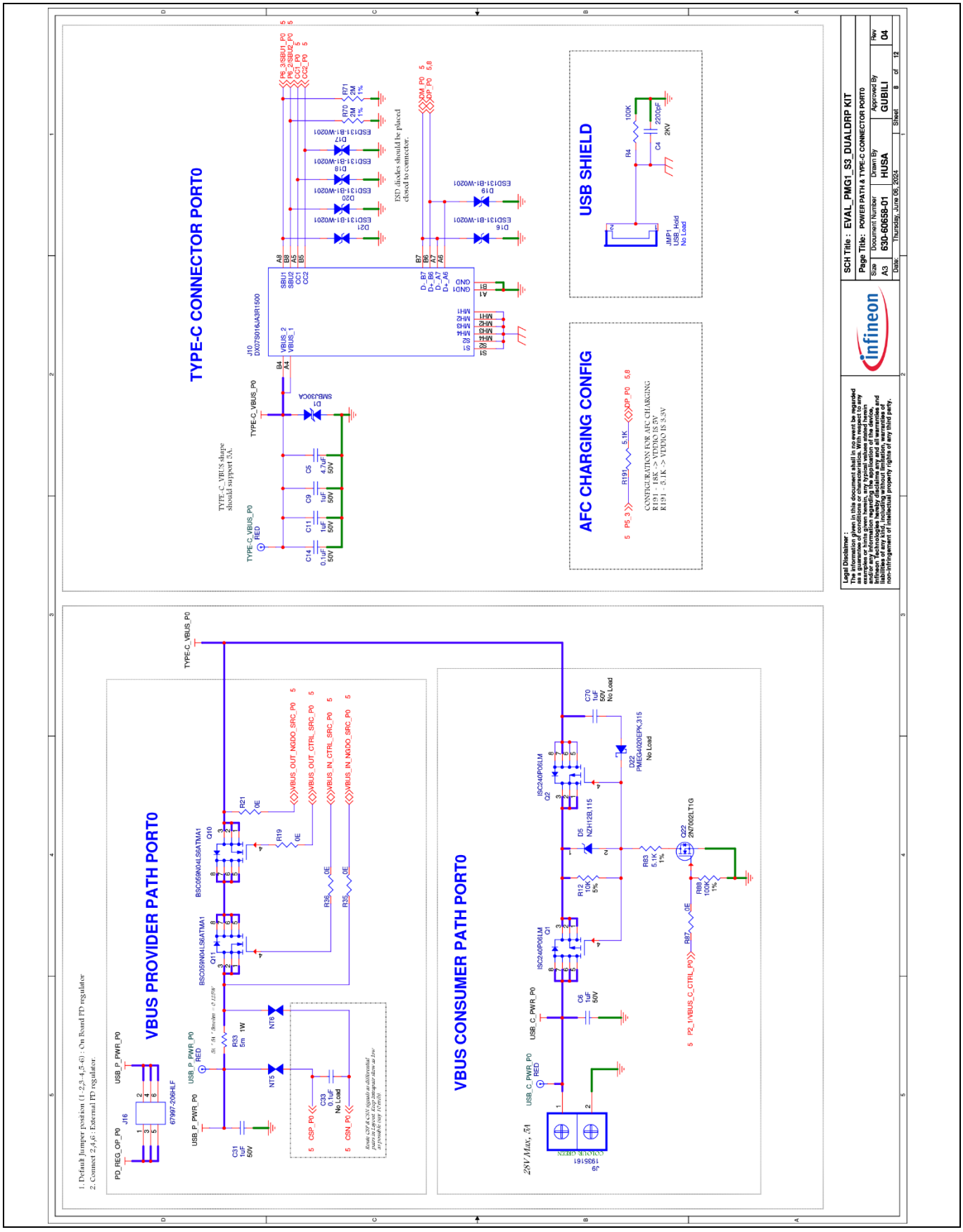

Figure 40 Port 0 provider and consumer switch schematics

Appendices

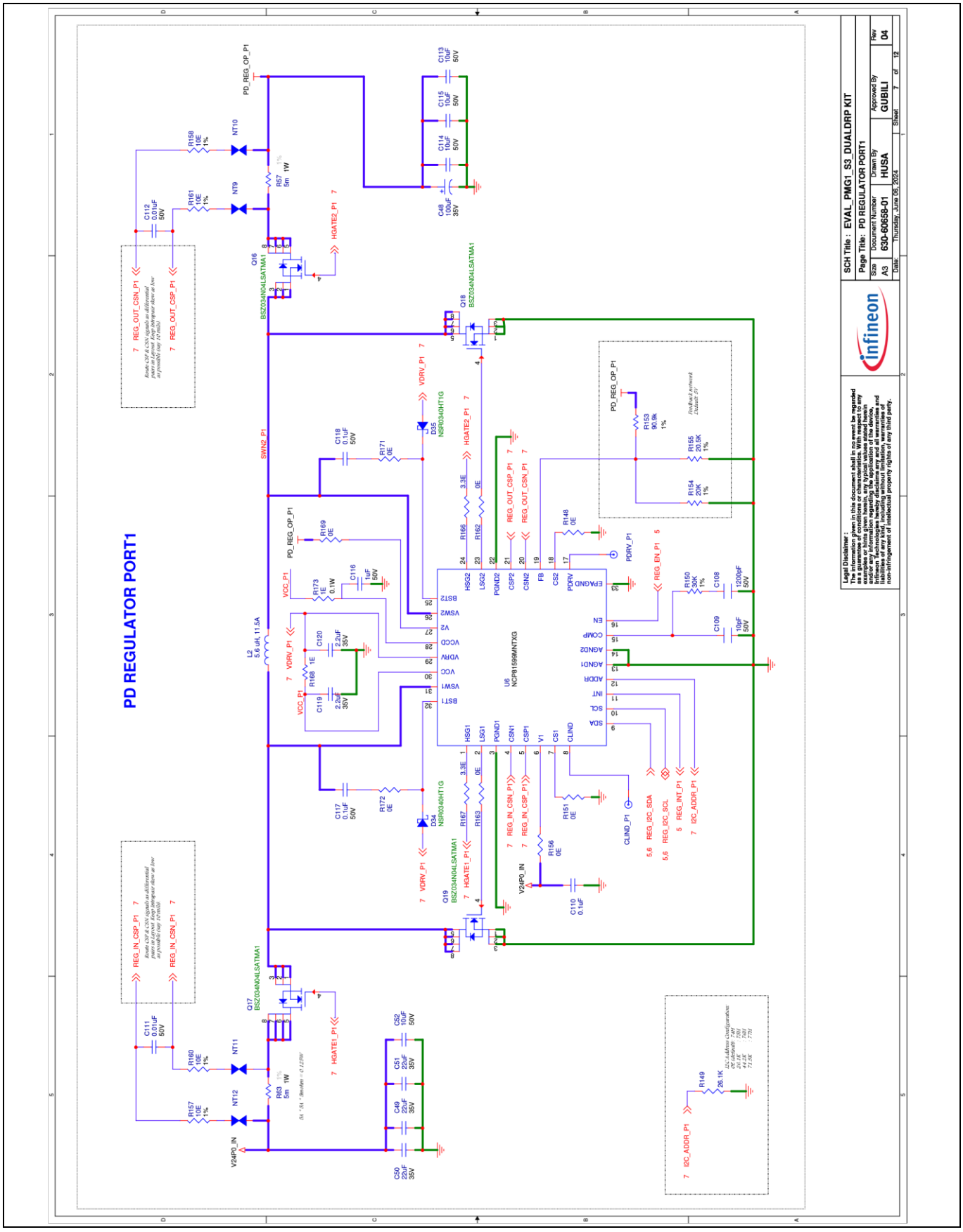

Figure 41 Port 1 provider and consumer switch schematics

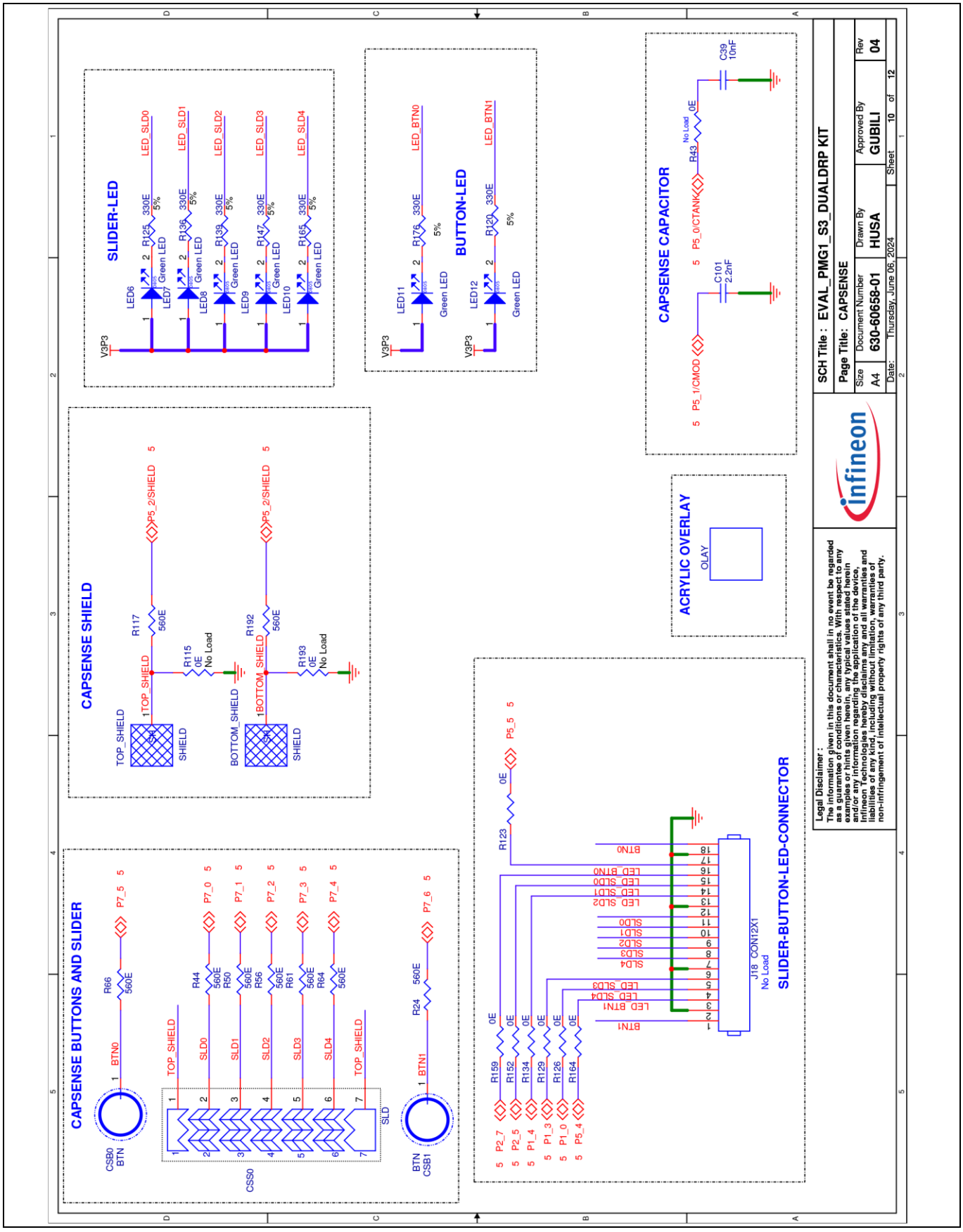

Figure 42 CAPSENSE™ schematics

References

[1] Infineon Technologies AG: *EVAL_PMG1_S3_DUALDRP kit page*; Available online

[2] Infineon Technologies AG: *EZ-PD™ PMG1-S3 webpage*; Available online

[3] Infineon Technologies AG: *AN232553 - Getting started with EZ-PD™ PMG1 MCU on ModusToolbox™ software*; Available online

[4] Infineon Technologies AG: *PMG1 code examples on GitHub*; Available online

[5] Infineon Technologies AG: *ModusToolbox™ software*; Available online

Glossary

AFC
adaptive fast charging

BC
Battery Charging

DFP
downstream facing port

DNP
Do Not Populate

DRP

dual-role power

EMCA
Electronically Marked Cable Assembly

ERP
extended power range

ESD
electrostatic discharge

EVK
Evaluation Kit

FET
Field-Effect Transistor

GPIO
general-purpose input/ output

IC
integrated circuit

LED
light-emitting diode

NA
not applicable

OVP
overvoltage protection

PA
power adapter

PD
Power Delivery

PDO
Power Data Object

Glossary

PFET
P-channel Field Effect Transistor

PSoC™
programmable system on chip

SoC
system on chip

UFP
upstream facing port

USB
Universal Serial Bus

USB PD
Universal Serial Bus Power Delivery

UVP
undervoltage protection

Revision history

Document revision	Date	Description of changes
**	2023-12-07	Initial release.
*A	2024-03-15	-Restructured section 2 and 3. -Updated Safety precautions table. -Added Figure 11. -Corrected GPIO pin number in I/O pinout table, CAPSENSE™ gpio header, buttons, and slider table as per rev03 schematics Updated Table 8, Table 9, Table 10, Table 11, Table 14 -Corrected J21 to J13 and J20 to J18 -Removed note for kit revision -Updated Table 2. -Added notes for power-on via Type-C VBUS -Merged KP3 overvoltage, voltage measurement, and KP3 section into Appendices section. -Added section 3.4. -Removed Onsemi buck boost circuit images from system design section. -Added vref for 12-bit SAR ADC section. -Updated section 3.1.1. -Added a note for heat dissipation in source mode. -Updated images in section 4 with multimeter and adapters. -Updated programming and debugging section images with adapters and tools.
*B	2024-09-23	- Updated EVK images to rev 04 board - Updated schematics to rev 04 board - Minor fixes throughout the document

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