PXIe-5114 Features

2025-04-10

Contents

PXIe-5114

NI 5114 high-speed digitizers feature deep onboard acquisition memory and SDTV, EDTV, and HDTV triggering. This digitizer meets the needs of test systems that make automated time-domain measurements.

Features

The NI 5114 has the following features:

- 2 channels
- 8-bit vertical resolution
- 250 MS/s real-time sampling rate
- 5.0 GS/s random interleaved sampling (RIS) rate
- 125 MHz bandwidth
- 8, 64, or 256 MB of memory per channel
- 1 MΩ or 50 Ω selectable input impedance
- AC/DC/GND coupling
- Analog, digital, SDTV/EDTV/HDTV video triggering
- NI-TClk synchronization

Related concepts:

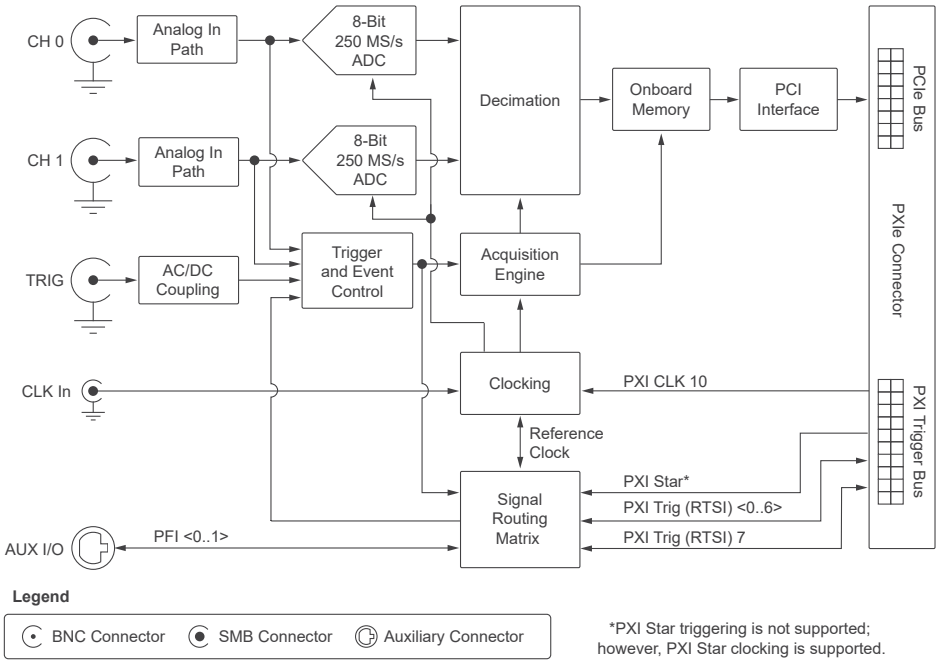
- SMC-Based Device Synchronization

Related information:

- Features Supported by Device

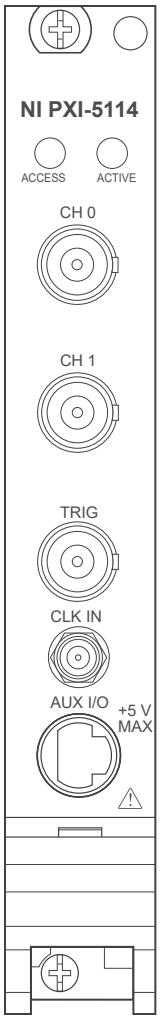
NI PXIe-5114 Block Diagram

The following figure shows a detailed block diagram of the NI PXIe-5114.



NI PXIe-5114 Front Panel

The following figure shows the front panel of the NI PXIe-5114. Descriptions of the LEDs and connectors are shown below.



LEDs

The NI PXIe-5114 has two LEDs to indicate status: Access and Active.

Access LED

The Access LED indicates basic hardware status, as listed in the following table.

Color	Indications
Off	Module is not yet functional, or the module has detected a problem with a power rail.
Amber	The module is being accessed.
Green	The module is ready to be programmed by NI-SCOPE.

Active LED

The Active LED indicates the module state, as listed in the following table.

Color	Indications
Off	Module is not armed, triggered, or acquiring a waveform.
Amber	The module is armed and waiting for a Trigger.
Green	The module has received a Reference (Stop) Trigger. Also indicates that the module is acquiring a waveform.
Red	The module has detected an error. NI-SCOPE must access the module to determine the cause of the error. The LED remains red until the error condition is removed. Example errors include the following: • **PLL unlocked**—The module has detected an unlocked condition on a previously locked PLL. A PLL that is unlocked while in reset does not show an error. • **External sample clock error**—The module is unable to detect the external sample clock. • **Overvoltage error**—The module has detected a 50 Ω overvoltage error. **Note** Certain driver interactions may cause the Active LED to flash red. An error condition does not exist unless the Active LED remains red.

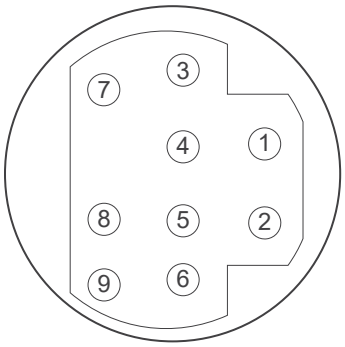
Connectors

The NI 5114 has the following six connectors on the front panel.

Connector	Description	Function
CH 0, CH 1	Standard BNC connector	Analog input connection; digitizes data and triggers acquisitions
TRIG	Standard BNC connector	External analog trigger connection; signals on the TRIG connector cannot be digitized
CLK IN	SMB jack	Imports an external reference or sample clock to the digitizer
AUX I/O	9-pin mini-circular DIN connector	Provides access to the external digital trigger lines, PFI 0 and PFI 1 (with optional cable)

AUX I/O Connector Pin Assignments

Figure 1. 9-Pin DIN Connector

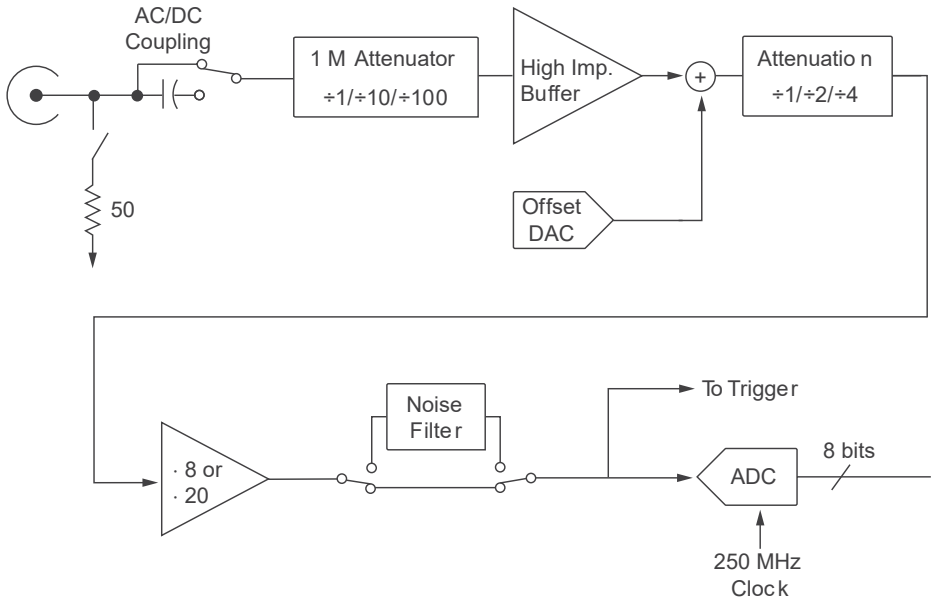


1. 5 V (Fused)
2. GND
3. Reserved
4. Reserved
5. Reserved
6. PFI 1
7. Reserved
8. Reserved
9. PFI 0

Note Be sure to use an NI adapter cable or a cable that has the same pinout shown in the previous figure.

NI 5114 Input Signal Conditioning

The NI 5114 provides two independent digitizer input channel signal conditioning paths. Each path provides you with a choice of 50 Ω input impedance or 1 MΩ input impedance, as shown in the following diagram.



Note The ground on the device inputs is connected to the chassis ground.

NI 5114 Input Ranges

As shown in the following table, the 1 MΩ path supports up to 40 V_{pk-pk} whereas the 50 Ω path supports up to 10 V_{pk-pk}.

50 Ω Input Path	1 MΩ Input Path
0.04 V_{pk-pk}	0.04 V_{pk-pk}
0.1 V_{pk-pk}	0.1 V_{pk-pk}
0.2 V_{pk-pk}	0.2 V_{pk-pk}
0.4 V_{pk-pk}	0.4 V_{pk-pk}
1 V_{pk-pk}	1 V_{pk-pk}
2 V_{pk-pk}	2 V_{pk-pk}
4 V_{pk-pk}	4 V_{pk-pk}
10 V_{pk-pk}	10 V_{pk-pk}
—	20 V_{pk-pk}

50 Ω Input Path	1 MΩ Input Path
—	40 V_{pk-pk}

NI 5114 Input Impedance

You can set the NI 5114 analog input impedance to either 50 Ω or 1 MΩ. The 1 MΩ path is required in applications that require minimal loading or that require using a standard 10:1 oscilloscope probe.

Protection

The 50 Ω inputs of the NI 5114 are protected by a thermal disconnect circuit. If an overvoltage event is large and sudden enough, however, the protection circuits might not have enough time to react before permanent damage occurs. It is therefore important to observe the maximum signal input, especially when the inputs are set for 50 Ω.

NI 5114/5122/5124/5142 AC/DC/GND Coupling

You can select AC, DC, or GND input coupling for the 1 MΩ input path, and DC or GND input coupling for the 50 Ω input path. Select AC-coupling if the input signal has a DC component that you want to reject, provided that you are not concerned about low-frequency flatness. A DC input offset adjustment is available if the signal you want to measure is below this limit, or if you are using the 50 Ω path.

Ground coupling disconnects the input channel from the signal connected and internally connects the channel to ground to provide a ground reference.

Related information:

- Input Coupling

NI 5114 Vertical Offset

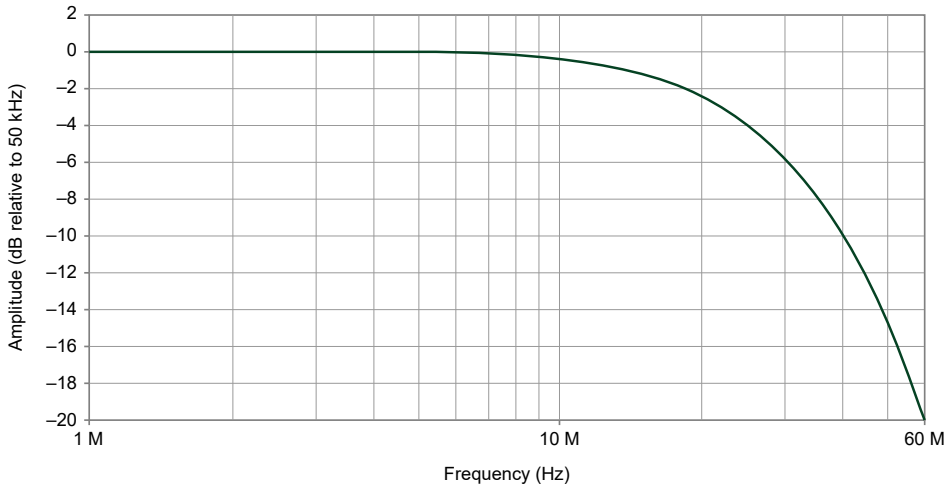
The following table shows the valid vertical offset for each range on the NI 5114.

Range	50 Ω Vertical Offset	1 MΩVertical Offset
0.04 V_{pk-pk}	±0.8 V	±0.8 V
0.1 V_{pk-pk}	±0.8 V	±0.8 V
0.2 V_{pk-pk}	±0.8 V	±0.8 V
0.4 V_{pk-pk}	±0.8 V	±0.8 V
1 V_{pk-pk}	±6.5 V	±8 V
2 V_{pk-pk}	±6 V	±8 V
4 V_{pk-pk}	±5 V	±8 V
10 V_{pk-pk}	±2 V	±30 V
20 V_{pk-pk}	N/A	±25 V
40 V_{pk-pk}	N/A	±15 V

Note The maximum allowable DC voltage is 7 V in the 50 Ω path and 35 V in the 1 MΩ path. The vertical offsets were chosen to stay within these voltage limits.

NI 5114 Noise Filter

The NI 5114 has a 20 MHz noise filter that limits the bandwidth of the signal path through both the 1 MΩ and 50 Ω signal paths. This filter is intended to reduce noise when the signal content is 20 MHz or less. A typical frequency response of the noise filter is shown in the following figure.



The noise filter provides over 20 dB of attenuation at 100 MHz, which is useful for rejecting out of band or background noise in lower frequency applications. An example application would be characterization of video waveforms in the presence of IF noise. Because most of the signal content is below the 8 MHz range, the 20 MHz noise filter is ideal. Many standard noise tests specify a 20 MHz noise bandwidth.

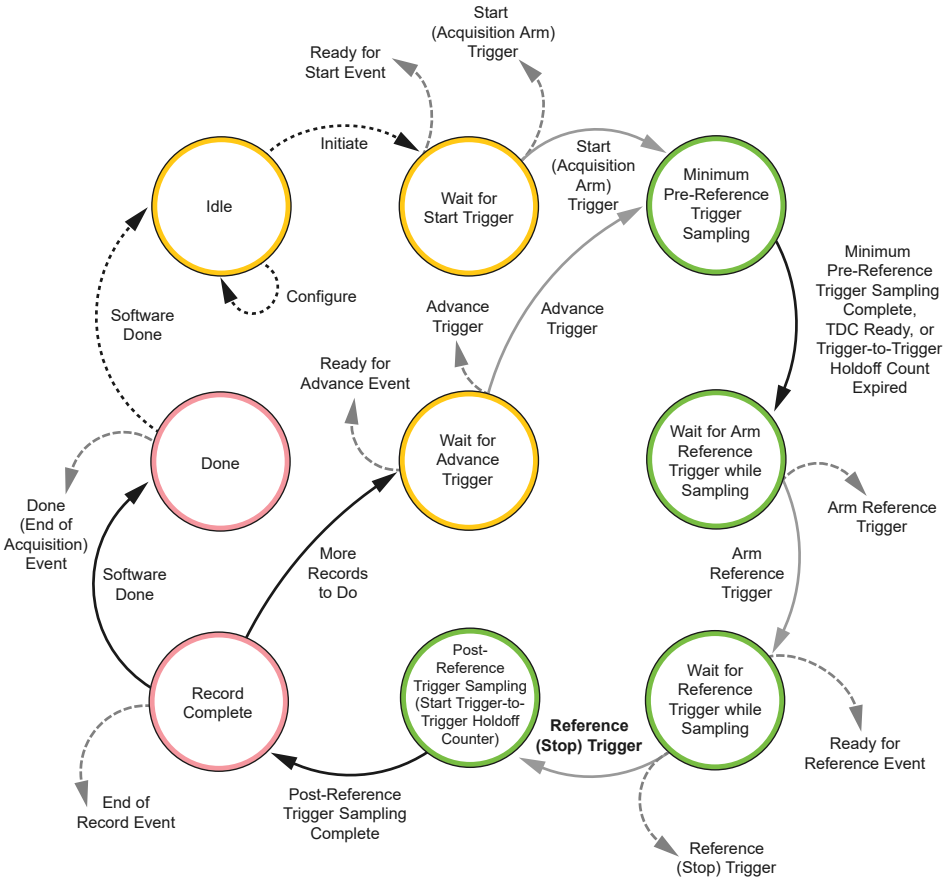
Note To enable/disable the noise filter, call the niScope Configure Chan Characteristics VI or the `niScope_ConfigureChanCharacteristics` function and set the **Max Input Frequency** parameter to the appropriate value.

Related information:

- niScope Configure Chan Characteristics
- niScope_ConfigureChanCharacteristics

SMC-Based Digitizers Acquisition Engine State Diagram

The following figure shows the acquisition engine state diagram for SMC-Based digitizers.



Note The **Reference (Stop) Trigger** is the same as the trigger level input of any traditional benchtop oscilloscope. To configure a digitizer to behave as a traditional benchtop oscilloscope, configure only this trigger using the **niScope Configure Trigger** function.

Arrow Color	Indication
Blue	State transitions always caused by software
Black	State transitions caused by the internal state machine of the device
Red	Output signals
Orange	User-configurable state transitions caused by software or hardware

NI SMC-based digitizers can be in any of the following basic states during the course of operation.

Idle—The module is not sampling a waveform. All the session attributes can be programmed in this state. In this state, the attributes have not necessarily been applied to hardware yet, so the hardware configuration of the module may not match the session attribute values. Also, the module remains configured as it was the last time a session was committed. When initiate is called on the module, all the attributes are programmed to the hardware. If the computer has just been reset, or `niScope_ResetDevice` has just been called, the module is in the Idle state.

Wait for Start Trigger—On initiating an acquisition, the module transitions to this state. If the Start (Acquisition Arm) Trigger Source is configured to Immediate, the module immediately transitions out of this state and generates a Start Trigger Event. If the Start Trigger Source has been configured for software or hardware trigger from one of the available sources, the module remains in this state until the configured trigger occurs. When the module recognizes a trigger condition, it transitions out of this state on the next clock cycle and generates a Start Trigger Event. The default Start Trigger Source is Immediate.

Minimum Pre-Reference Trigger Sampling—The module can transition into this state two ways: receiving the Start (Acquisition Arm) Trigger from the Start (Acquisition Arm) Trigger Source or receiving the Advance Trigger from the Advance Trigger Source. Transitioning into this state depends on the previous state of the module. While in this state, the module samples according to the session attributes configured. The module remains in this state until three conditions are satisfied: the minimum Pre-Reference Trigger sampling completes, the TDC is ready, and the trigger-to-trigger holdoff count has expired. The minimum Pre-Reference Trigger sampling is at least the user-configured Minimum Record Length multiplied by the user-configured Reference Position. The first time through this state, the trigger-to-trigger holdoff does not have an effect. When the three conditions have been satisfied, the module transitions out of this state on the next clock cycle.

Wait for Arm Reference Trigger while Sampling—After the module finishes the Minimum Pre-Reference Trigger Sampling state, the module transitions into this state. While in this state, the module continues to acquire Pre-Reference Trigger samples according to the session attributes configured. If the Arm Reference Trigger Source is configured to Immediate, the module transitions out of this state on the next clock edge. If the Arm Reference Trigger Source has been configured for a software trigger or a hardware trigger from one of the available sources, the module remains in this state until the configured trigger occurs. When the module recognizes a trigger condition,

the module transitions out of this state. The default Arm Reference Trigger Source is Immediate.

Wait for Reference Trigger while Sampling—After the module receives Arm Reference Trigger from the Arm Reference Trigger Source, the module transitions into this state. If the Reference Trigger Source has been configured for a software or hardware trigger from one of the available sources, the module remains in this state until the configured trigger occurs. When the module recognizes a trigger condition, the module transitions out of this state. The default Reference Trigger Source is Immediate.

Post-Reference Trigger Sampling—After the module receives the Reference (Stop) Trigger, the module transitions into this state. At the beginning of this state, the module starts a trigger-to-trigger holdoff counter. This holdoff counter corresponds to the user-configurable **Trigger Holdoff** attribute and is used in the Minimum Pre-Reference Trigger Sampling State. You can use the **Trigger Holdoff** attribute to delay the module from looking for a Reference Trigger between records. At the same time, the trigger-to-trigger holdoff counter is started, the module begins sampling Post-Reference Trigger samples according to the session attributes configured. When the Post-Reference Trigger sampling is completed, the module transitions out of this state.

Record Complete—After the module completes Post-Reference Trigger sampling, the module transitions into this state. The module leaves this state after the current record has been stored in the onboard memory. Upon leaving this state, the module outputs an End of Record Event.

Wait for Advance Trigger—After the module has completed a record and determines that there are still more records to complete, the module transitions into this state. If the Advance Trigger Source is configured to immediate, the module transitions out of this state on the next clock edge. If the Advance Trigger Source has been configured for software or hardware trigger from one of the available sources, the module remains in this state until the configured trigger occurs. Upon the module recognizing a trigger condition, the module transitions out of this state. The default Advance Trigger Source is Immediate.

Done—After the module completes a record and determines that all the records are done, it transitions into this state. Upon entering this state, the module outputs the End of Acquisition Event, which is a temporary state. The software transitions the module out of this state and back to the Idle state when you call either Fetch or Check

Status.

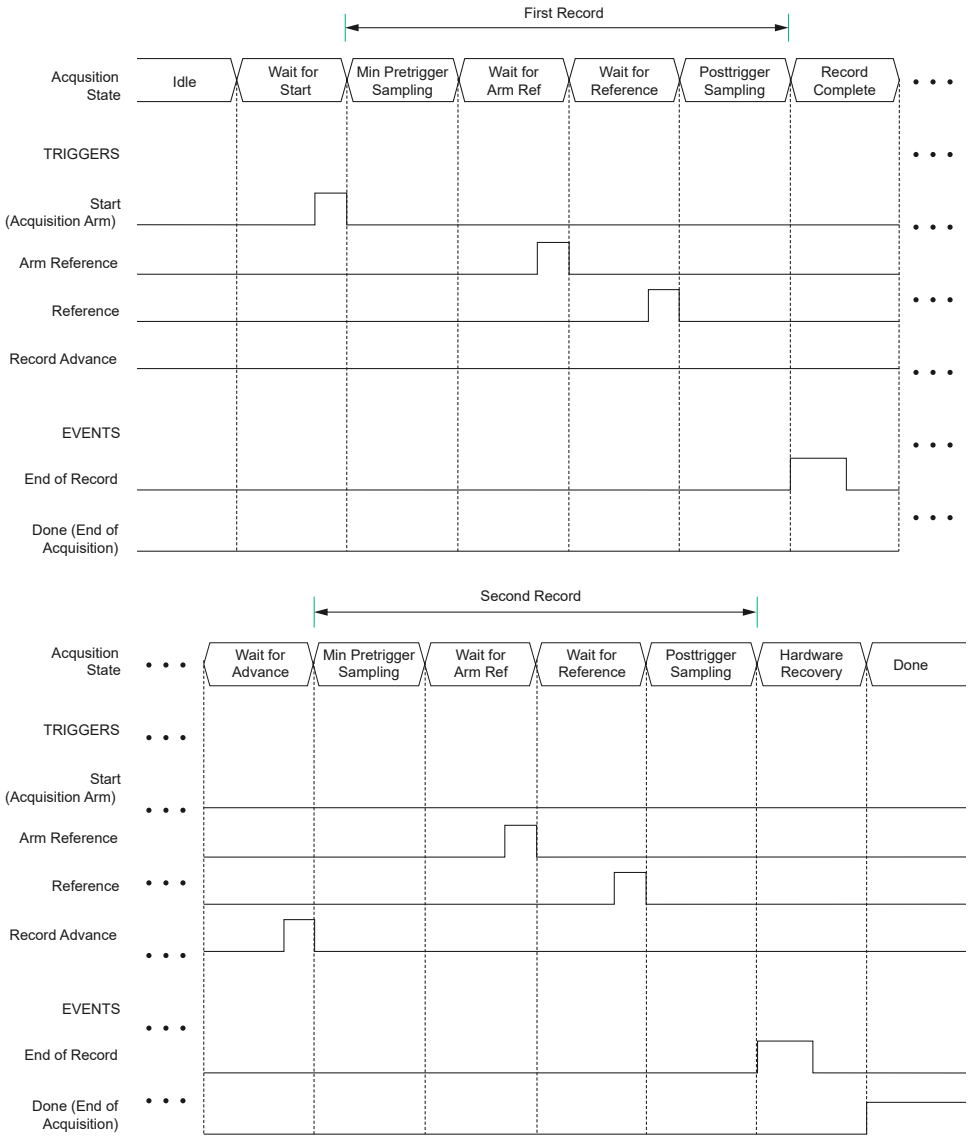
Related information:

- Triggering
- Trigger Types
- niScope Configure Trigger (poly)

SMC-Based Digitizers Timing Diagram

SMC-Based digitizers (NI 5105/5114/5122/5124/5142/5152/5153/5154/5160/5162/5622/5922) support multirecord acquisitions, which allow the capture of multiple triggered waveforms without software intervention. In this mode, the digitizer automatically begins storing a new record to onboard memory a short time after finishing the previous record. The number of records and record size are both configurable.

The following timing diagram illustrates how SMC-based digitizers react to the user-configurable input triggers during a multirecord acquisition.



Each state prefixed by Wait for is a state in which an input trigger can be configured. This trigger tells the digitizer when to transition out of that particular state. The hardware is only sensitive to a particular trigger when in that trigger's appropriate Wait for state. For example, the hardware is not sensitive to a high level on the Advance Trigger until it enters the Wait for the Advance trigger state.

Note The trigger signals in the timing diagram assume active high level triggers.

The exportable events are also shown in the timing diagram. The End of Record Event is generated once per record when the digitizer has acquired all of its pre- and post-

Reference Trigger samples. This signal can be used for handshaking between devices in a system. The Done Event asserts when all of the records have been completed, but it does not assert if the acquisition is aborted or times out.

NI PXIe-5114 Routing Matrix

The following table shows the signals available for export from the NI PXIe-5114 and the lines to which they can be routed.

Source	Destination	
	PXI_Trig <0..6>(PXI Bus)	PFI <0..1>(AUX I/O)
Exported Clocks		
Reference Clock (External)	√	√
Triggers		
Acquisition Arm (Start) Trigger	√	√
Reference (Stop) Trigger	√	√
Events		
End of Record Event	√	√
End of Acquisition Event	√	√
Ready for Start Event	√	√
Ready for Reference Event	√	√
Ready for Advance Event	√	√

NI 5114/5122/5124/5142 Analog Trigger Types

The NI 5114/5122/5124/5142 supports the following analog trigger types: edge, hysteresis, window, and video triggers.

Related concepts:

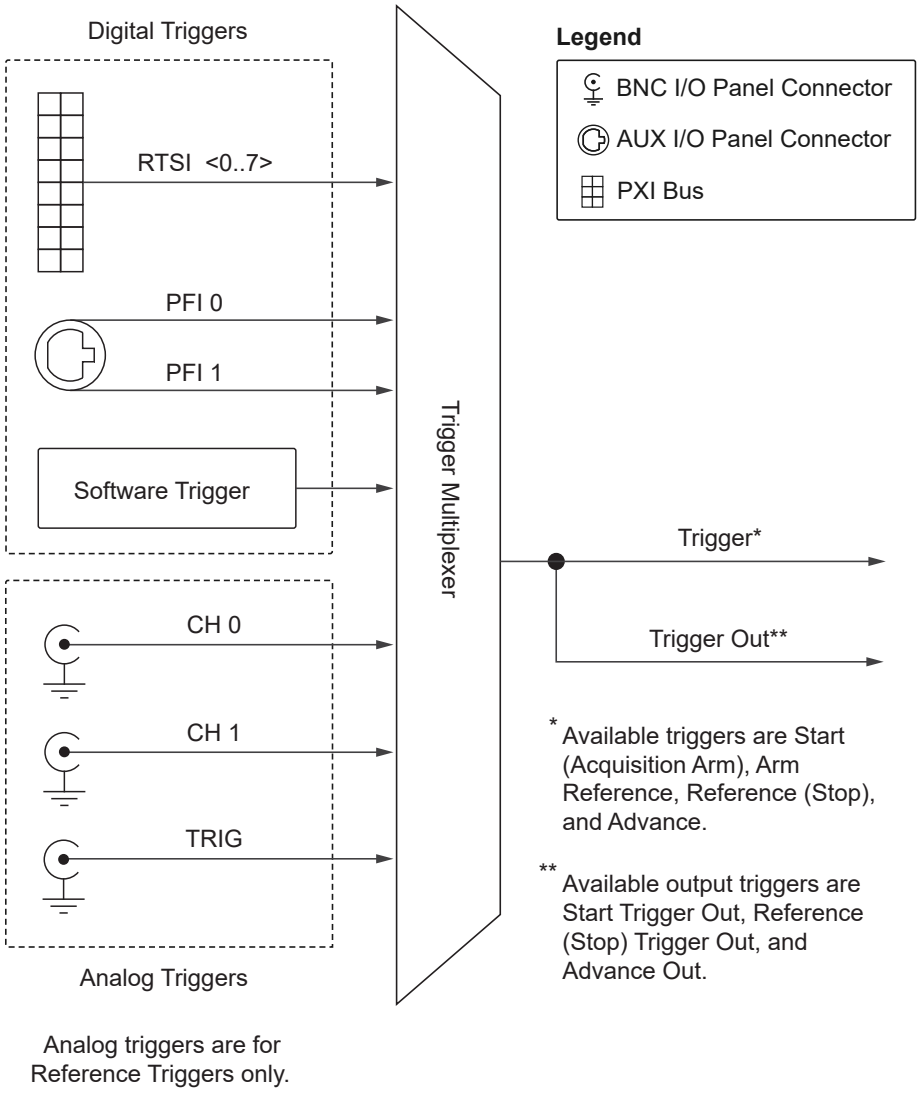
- NI 5114/5122/5124/5142 Video Triggering

Related information:

- Edge Triggers
- Hysteresis Triggers
- Window Triggers

NI PXIe-5114/5122/5124 Trigger Sources

The following figure shows the trigger sources for the NI PXIe-5114/5122/5124.



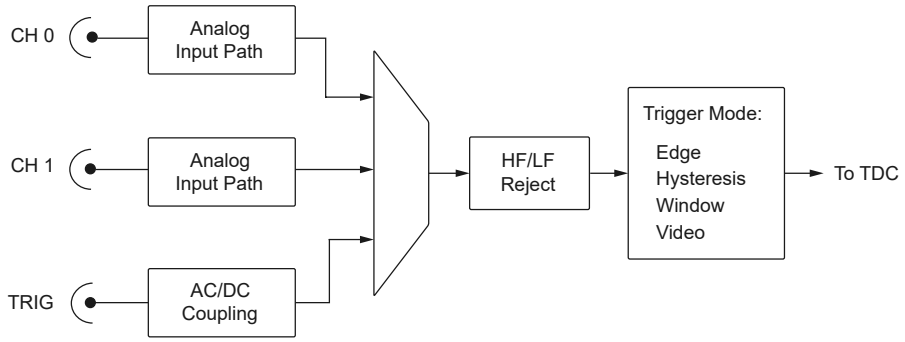
NI 5114/5122/5124/5142 Analog Trigger Paths

With high-speed digitizers, triggering capability is as important as input signal conditioning. The NI 5114/5122/5124/5142 provides flexible, high-precision, low-jitter triggering features.

The NI 5114/5122/5124/5142 has three fundamental analog trigger paths:

- Channel 0 input (CH 0)
- Channel 1 input (CH 1)
- External trigger input (TRIG)

The following figure shows the analog trigger paths for the NI 5114/5122/5124/5142.



External Trigger Channel (TRIG)

Unlike the input channels (CH 0 and CH 1), the external trigger channel uses a fixed input range and impedance to give a higher bandwidth for triggering the digitizer. Signals that travel through the external trigger channel are not digitized.

NI 5114/5122/5124/5142/5152/5153/5154 Trigger Filters

LF and HF Reject Filters

The NI 5114/5122/5124/5142/5152/5153/5154 has two filter selections, LF Reject and HF Reject, available for all analog trigger sources. These are defined as trigger coupling options. Both are single pole filters, with the cutoff frequency set to 50 kHz.

LF Reject Example

An example application for the LF Reject is in triggering on a 455 kHz IF signal in the presence of line cycle noise. If the 50 or 60 Hz line signal has sufficient magnitude, it causes triggering and timing errors versus the desired 455 kHz signal. This can be a challenging signal to use as a trigger. Using the 50 kHz highpass filter, the 50 or 60 Hz component is attenuated by nearly 60 dB, greatly improving the trigger stability and jitter performance of the acquisition.

HF Reject Example

An example application for the HF Reject is triggering on a 1 kHz Sigma-Delta integrator output in the presence of high-frequency signal content, including overshoot and ringing on the transitions. When this high frequency content crosses over the trigger threshold, false triggers occur. Using the 50 kHz lowpass filter, you can reject the high-frequency content, noise, and overshoot to obtain a clean trigger source.

NI 5114/5122/5124/5142 Video Triggering

The NI 5114/5122/5124/5142 includes a mode for triggering on certain video signals. You can trigger on any line, a specific line number, or a specific field. For more information on video signals, refer to Video Fundamentals.

The NI 5114/5122/5124/5142 supports negative polarity in video mode for certain video signal formats. Negative trigger polarity means that the synchronization pulses must go to a negative voltage with respect to the back porch level. The following tables show the video formats supported by each digitizer model, and whether negative trigger polarity is supported in video mode.

Note Using a vertical range that is too high may cause the digitizer to not lock correctly to the video signal.

NI 5114

Video Signal Format	FormatSupported	Negative PolaritySupported
Standard (SDTV)		
M-NTSC	√	√
B/G-PAL	√	√
SECAM	√	√
M-PAL	√	√
Enhanced Definition (EDTV)		
480i/59.94 fps	√	√
480i/60 fps	√	√
480p/59.94 fps	√	√
480p/60 Fps	√	√
576i/50 fps	√	√
576p/50 Fps	√	√
High Definition (HDTV)		
720p/50 Fps	√	N/A
720p/59.94 Fps	√	N/A
720p/60 Fps	√	N/A
1080i/50 fps	√	N/A
1080i/59.94 fps	√	N/A
1080i/60 fps	√	N/A
1080p/24 Fps	√	N/A

NI 5122/5124/5142

Note The NI 5122/5124/5142 does not support EDTV and HDTV video formats.

Video Signal Format	FormatSupported	Negative PolaritySupported
Standard (SDTV)		
M-NTSC	√	√
B/G-PAL	√	√
SECAM	√	√
M-PAL	√	√

Video Signal DC Restoration

The NI 5114/5122/5124/5142 supports DC restoration, which adjusts the back porch level of the video signal to 0 V. DC restore is performed on the digital data, rather than with an analog clamping circuit. When using DC restore, set the input voltage range to approximately twice the expected signal amplitude to prevent signal clipping as the amplitude and offset of the video signal change. DC restore measures the voltage of the back porch during the interval between the end of the colorburst and before the start of the active line, then subtracts this value from the signal for the remainder of the active video line. Excess noise on the back porch portion of the video signal may cause inconsistent level restoration between lines.

Signal Conditioning

To provide proper termination to the video signal, use a 75 Ω terminator on the input of the digitizer in 1 MΩ input mode.

Copy Protection System Implications

Many video signal sources, particularly DVD players, produce a copy protection signal. DVDs can be encoded to enable this function, which inhibits copying the signal by injecting pulses that violate video signal standards, and disrupts input circuitry on VCRs. These signals often include false synchronization pulses and signals that exceed the voltage range of a standard signal. Any false pulses may cause erroneous line triggering on the digitizer. To avoid this error in your application, try one of the following solutions:

- Deactivate or remove the copy protection signal from the signal source.

- Recover triggering information in software by taking an untriggered waveform with the NI 5114/5122/5124/5142 and searching for legal trigger points in the waveform.

Related information:

- Video Fundamentals
- Active Image

NI 5114/5122/5124/5142/5152/5153/5154 Trigger Holdoff

For NI 5114/5122/5124/5142/5152/5153/5154 devices, the holdoff timer is started by the Reference Trigger. When the current record finishes and the minimum number of pretrigger samples for the next record have been acquired, the holdoff timer is evaluated. If the timer has expired, the digitizer arms its Reference Trigger circuit. If the timer has not expired, the digitizer continues pretrigger sampling until the timer expires, and then arms its Reference Trigger circuit. Holdoff is applied for each Reference Trigger during a multirecord acquisition.

TDC On

When the time-to-digital converter (TDC) is enabled on the digitizer, the minimum holdoff you can set is 10 µs (for the NI 5114/5122/5124/5142) or 8 µs (for the NI 5152/5153/5154). This minimum holdoff time between Reference Triggers is required for the TDC to settle; any holdoff value below these values is coerced up.

TDC Off

When the TDC is disabled, the minimum holdoff value you can set is decreased to 2 µs (for the NI 5114/5122/5124/5142) or 1 µs (for the NI 5152/5153/5154) when using the internal sample clock. For minimum trigger holdoff when using an external sample clock, refer to the specifications document for your digitizer.

Related information:

- Trigger Holdoff
- TDC

NI 5114/5152/5153/5154 Trigger Delay

Trigger delay, which is specified in seconds, is achieved on the NI 5114/5152/5153/5154 by adding the appropriate number of posttrigger samples to the record while keeping the allocated onboard memory equal to the record size you request. NI-SCOPE then corrects the trigger time by the delay you specify. To determine the maximum delay for a particular actual sample rate, use the following formula:

Max trigger delay in seconds = $[(2^{35} - 1) - \text{requested posttrigger samples}] \times (1/\text{actual sample rate})$

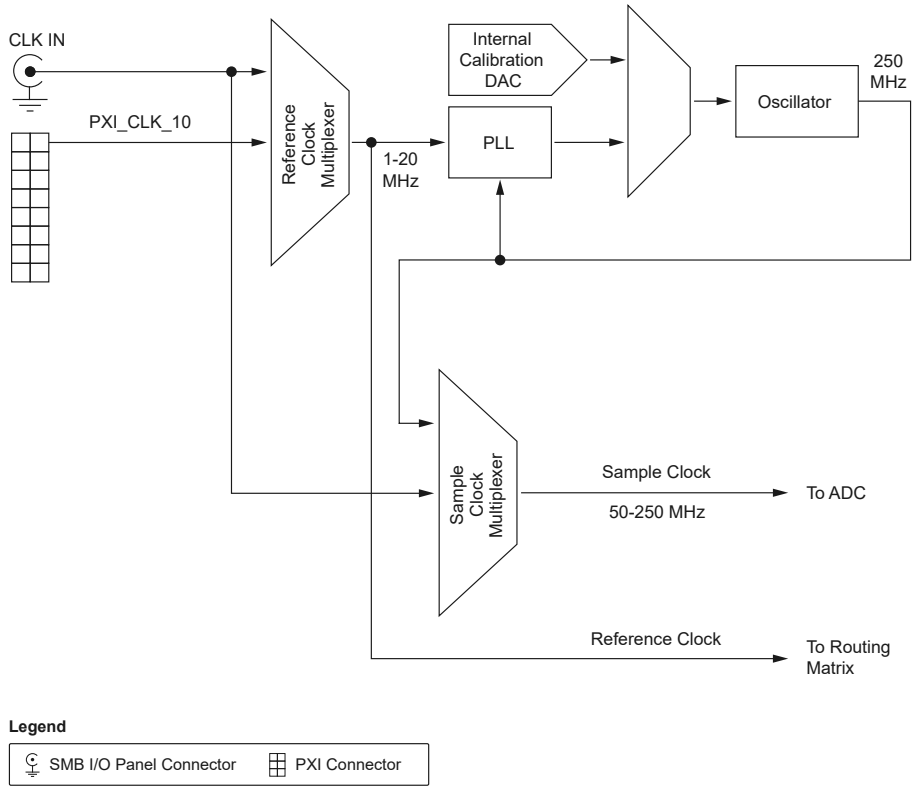
Note The maximum trigger delay changes when you use an external sample clock, and when you sample at rates other than full rate while using the internal sample clock.

Related information:

- Trigger Delay

NI PXIe-5114 Clocking

The clock circuitry on the NI PXIe-5114 offers versatile clocking options with its ability to use either the internal 250 MHz sample clock or to accept an external sample clock that you provide. You can also use the phase-locked loop (PLL) circuit on the NI PXIe-5114 to phase lock the internal 250 MHz sample clock with the PXI 10 MHz reference or with an external reference clock that you provide. The following diagram shows the clocking options of the NI PXIe-5114.



Sample Clock

The sample clock is sent to the ADC of each channel and to the input timing engine. The NI PXIe-5114 can decimate its sample clock (internal or external) by an integer divisor. When using an external clock, you can use decimation to achieve rates below the external clock frequency.

Internal Sample Clock

The NI PXIe-5114 has an onboard voltage controlled crystal oscillator (VCXO) running at 250 MHz. When using the onboard 250 MHz oscillator, you can choose either free-run mode or PLL mode. In free-run mode, the sample clock is the calibrated 250 MHz frequency of the VCXO. In PLL mode, the NI PXIe-5114 phase locks its 250 MHz sample clock to the supplied reference clock. The PLL mode is useful when synchronizing the NI PXIe-5114 with other devices in a measurement system.

External Sample Clock

Some applications may require sampling at specific intervals that cannot be achieved by using the internal 250 MHz clock. In these cases the NI PXIe-5114 can accept an external sample clock. External clocking also provides a method to synchronize the NI PXIe-5114 to other devices in a measurement system by distributing a common clock to multiple devices. An external sample clock can be supplied to the NI PXIe-5114 from the front panel connector or by routing the signal on the PXI backplane over the PXI star trigger line. Refer to the NI PXI/PXIe/PCI-5114 Specifications document that shipped with the device for external sample clock requirements.

Note When you use an external sample clock, the TDC is disabled. Refer to the NI PXI/PXIe/PCI-5114 Specifications for information on how this affects trigger holdoff and trigger resolution.

Reference Clock

The reference clock is used in the NI PXIe-5114 phase-locked loop (PLL) circuit to synchronize the sample clock to the reference clock. The NI PXIe-5114 can accept a reference clock from its front panel (CLK IN) as well as from PXI_CLK10. This reference clock can be any frequency from 5 MHz to 20 MHz (in 1 MHz increments) if it is provided to CLK IN. The PXI_CLK10 is always a 10 MHz clock. The frequency stability of the sample clock matches that of the PLL reference clock when the two are phase locked. In turn, phase locking synchronizes clocks of multiple devices that are phase locked to the same reference clock. The default setting for the NI PXIe-5114 reference clock is `None`, or no reference clock is used.

Note Locking to a reference clock is not valid when using an external sample clock.

Exporting Reference Clock

If you are using an external reference clock to phase lock the internal sample clock, you can export the reference clock for use with other instruments. For more information on exporting the reference clock, refer to the NI PXIe-5114 Routing Matrix.

Related concepts:

- NI PXIe-5114 Routing Matrix

Related information:

- Reference Clock/Phase-Lock Loop
- PXI Star Trigger Line
- TDC

NI 5114 Onboard Memory

The NI 5114 allocates at least 256 bytes of onboard memory for each record in a single multirecord acquisition. Samples are stored in this buffer before transfer to the host computer. Thus the minimum size for a buffer in the onboard memory is 256 8-bit samples. Software allows you to specify buffers of less than these minimum buffer sizes, but only the specified number of points are transferred from onboard memory into the host computer memory.

The total number of samples that can be stored depends on the size of the acquisition memory size option. The maximum number of records in a single multirecord acquisition is equal to the size of the memory option divided by 256 samples. The available memory options are 8 MS, 64 MS, and 256 MS per channel.

Triggering and Memory Usage

During an acquisition, samples are stored in a circular buffer that is continually rewritten until a trigger is received. After the trigger is received, the NI 5114 continues to acquire posttrigger samples if you have specified a posttrigger sample count. The acquired samples are placed into onboard memory. The number of posttrigger or pretrigger samples is only limited by the amount of onboard memory.

SMC-Based Device Synchronization

SMC-based digitizers are built on the National Instruments Synchronization and Memory Core (SMC) technology and therefore support TClk synchronization. Refer to

the NI-TClk Synchronization Help for more information.

Related information:

- National Instruments Synchronization and Memory Core (SMC)
- NI-TClk Synchronization Help
- Features Supported by NI-SCOPE Instruments

SMC-Based Digitizers Multiple-Record Acquisition

SMC-based digitizers support multiple-record acquisition, which allows the capture of multiple triggered waveforms without software intervention. In this mode, the digitizer automatically begins a new acquisition in a new memory record soon after finishing the previous record. Multiple-record acquisitions can quickly acquire numerous triggered waveforms because they allow hardware rearming of the digitizer. Between each record, there is a dead time during which no triggers are accepted. During this time, the device sets up for the next record, as it transitions through the subsequent states of the SMC-Based Digitizers Acquisition Engine State Diagram. There is also a holdoff between the last trigger in a record and the trigger of a new record. This means that the minimum time between triggers is the greater of either:

- The between-record dead time plus the time per record, or
- The user-specified holdoff time (by default, the holdoff time = 0 s).

To increase the minimum time between triggers, use the trigger holdoff feature. For more information, refer to the SMC-Based Digitizers Acquisition Engine State Diagram.

Some digitizers specify a minimum rearm time. Minimum rearm time is the minimum time between reference triggers as the record length approaches a minimum (for example, record length = 1 sample).

The number of records that can be acquired varies depending on the memory option of the device. Depending on the digitizer, NI-SCOPE limits to approximately 100,000 records that can be configured without fetching during the acquisition. However, if an application allows for fetching records while they are being acquired, NI-SCOPE allows more records to be configured. Refer to Acquiring More Records Than Fit in Digitizer Memory for more information.

Related concepts:

- SMC-Based Digitizers Acquisition Engine State Diagram

Related information:

- Acquiring More Records Than Fit in Digitizer Memory
- Features Supported by NI-SCOPE Instruments
- Making Multiple-Record Acquisitions

NI 5114 Calibration

Every measurement instrument performs within its specifications over some finite temperature range and time period. If the temperature changes and time exceed those specified, and your application requires tight specifications, calibration is required.

For example, if the accuracy of a digitizer is specified as ±(1% of input + 10 mV), and you apply 5 V to the input, the error is:

1% of 5 V + 10 mV = 60 mV for temperature range 18-28 °C

This example demonstrates the traditional method of specifying accuracy. The problem with the traditional method is that in a system environment, temperature is not easily controlled. When a system is composed of multiple instrument integrated together, the system is subject to temperature rise caused by inherent compromises in air circulation and other factors. Self-heating from surrounding equipment, uncontrolled manufacturing floor environment, and dirty fan filters are among these factors.

If the ambient temperature is outside of the 18-28 °C range, you may need to know exactly what the measurement accuracy is to compensate for this temperature variation. With the traditional method, the only way to achieve the specified accuracy outside of the 18-28 °C range is to externally calibrate the system at the desired temperature. However, an external calibration is time-consuming and expensive and is infrequently done, so the specified accuracy is rarely obtained. You can learn more about external calibration at ni.com/calibration. In the example, if the ambient temperature of the digitizer is 48 °C, assuming the Tempco (TC), error is specified as

TC = (0.1% of input +1 mV)/ °C (a typical number is 10% of accuracy/ °C)

the additional error is

20 °C x TC = ±(2% of input + 20 mV) or 120 mV

The total error is three times the specified error (180 mV in the example above, versus 60 mV if temperature effect is ignored) due to the 48 °C ambient temperature.

Self-Calibration

To eliminate errors caused by changing temperatures, NI-SCOPE provides a highly repeatable self-calibration function.

For the NI 5114, this self-calibration capability yields the following benefits:

- Corrects for DC gain and offset errors within the digitizer by comparison to a precision, high-stability internal voltage reference. This is done for all ranges, both input impedance paths (50 Ω and 1 MΩ), and all filter paths (enabled/disabled).
- Calibrates trigger level offset and gain.
- Calibrates trigger timing, as well as the time-to-digital conversion (TDC) circuitry to ensure accurate trigger timing and time-stamping.
- Compensates 1 MΩ input frequency flatness.
- Takes approximately 1 minute to complete.

When to Self-Calibrate

For optimum performance, use self-calibration when the digitizer is placed in a new system, any time the temperature changes more than 5 °C from the previous self-calibration, or 90 days after the previous self-calibration. The result is a product that yields full performance over its operating temperature range and two-year calibration cycle for DC accuracy, AC response, and trigger level/timing. When the two-year calibration interval expires, an external calibration is required.

The NI 5114 has a temperature sensor that monitors temperature variations. The previous self-calibration time and date can also be read. Unless temperature variations are a serious problem, self-calibration is not recommended more than once per day.

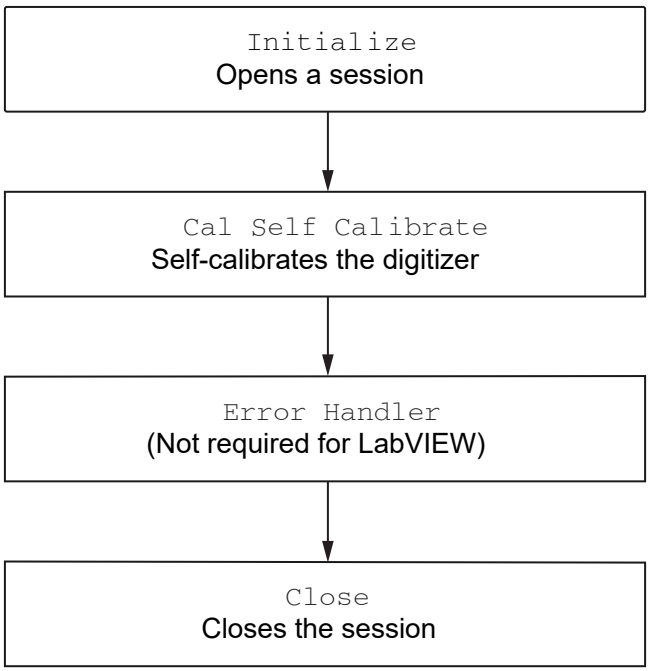
Input Connections During Self-Calibration

The NI 5114 internal circuitry is automatically isolated from the input during self-calibration. However, problems may occur if high-voltage, high-frequency signals (in excess of 500 V/µs slew rate) are present during self-calibration.

When in doubt, disconnect the inputs as directed. If you are absolutely certain that the maximum slew rate of the input signal is below 500 V/µs, then it is acceptable to leave the input signal connected during self-calibration.

Programming Flow

The following diagram shows the typical programming flow for self-calibration.



NI-SCOPE provides the `Calibrate` example, which you can find by using the shortcut at **Start»All Programs»National Instruments»NI-SCOPE»Examples**.

Summary of Calibration Options

A summary of the calibration options available and when to use them is shown in the

following table.

Calibration	Impact	When	Notes
External calibration	Calibrate time drift of onboard reference	Every 2 years	Calibrates and verifies to full specifications
Self-calibration	Offset and gain Trigger level Trigger timing AC flatness Input capacitance	90 days, or when temperature changes >5 °C	Ensures range to range matching Ensures trigger accuracy Optimizes performance with external 10:1 probes
No calibration	None, within 2 year calibration cycle or if temperature stays within ±5 C	High accuracy not required outside of 5 °C	If self-calibration is not used, derate the accuracy using the specified Tempco

Related information:

- Calibration