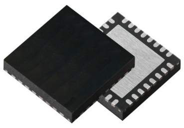
STM32WL30xx

Datasheet

Multiprotocol LPWAN 32-bit MCU Arm® Cortex®-M0+ 2(G)FSK, 4(G)FSK, ASK, D-BPSK, up to 128 KB flash, 16 KB SRAM



VFQFPN32 (5 x 5 mm)

Product summary	
Reference	**Part number**
STM32WL30xx	STM32WL30KB
	STM32WL30K8

Features

- Includes ST state-of-the-art patented technology
- Ultra-low power sub-1GHz wireless system-on-chip
- Programmable MCU
  - Core: Arm® Cortex®-M0+ 32-bit, running up to 64 MHz
  - Program memory: 64-Kbyte / 128-Kbyte flash memory
  - Data memory: 8-Kbyte / 16-Kbyte SRAM (full retention)
  - Additional storage: 1-Kbyte OTP (user data)
- Radio
  - Frequency bands: 413-479 MHz, 826-958 MHz
  - Air data rate from 0.1 to 600 kbit/s
  - Programmable TX power up to +20dBm
  - RX sensitivity @ 1% BER:
    - -132 dBm @300 bit/s 433 MHz OOK
    - -128 dBm @300 bit/s 868 MHz 2(G)FSK
    - -112 dBm @38.4 bit/s 868 MHz 2(G)FSK
  - Modulation schemes:
    - 2(G)FSK, 2(G)MSK, 4(G)FSK
    - OOK, ASK
    - D-BPSK
    - DSSS (direct sequence spread spectrum)
    - I/Q channels data access
    - Compatible with proprietary and standardized wireless protocols (W-MBUS, Sigfox, Mioty, KNX-RF, IEEE 802.15.4g, others)
  - Suitable for worldwide certifications:
    - Europe: ETSI EN 300 220, category 1 compliant, ETSI EN 303 131
    - US: FCC part 15 and part 90
    - Japan: ARIB STD T67, T108
  - Fully-configurable hardware sequencer for autonomous radio operations (Sniff mode, Frequency hopping, Low Duty Cycle mode, Listen before talk)
- Ultra-low power architecture
  - Dynamic current consumption: 21 µA/MHz
  - 14 nA in Shutdown mode
  - 960 nA in Deepstop mode
  - Radio only consumption:
    - 4 mA in RX
    - 8 mA in TX @ +10 dBm
    - 78 mA in TX @ +20 dBm
  - Consumption: 1.3 mA current in WFI conditions (direct HSE mode)
  - Wakeup capability from both Deepstop and Shutdown modes

- Peripherals and analog front-end
  - Battery voltage monitoring with low-level detection
- Communication interfaces
  - Up to 17 GPIOs (VFQFPN32), all with retention capability
  - 1x USART. Supports of LIN, Smartcard Protocol, IrDA, SIR ENDEC specifications, and modem operations (CTS/RTS)
  - 1x LPUART (available also in low-power mode), with wakeup capability
  - 1x SPI
  - 1x DMA 8 channels controller, supporting SPIs, USART, LPUART, timers, AES
- Clock sources and timers
  - Flexible clocking scheme, featuring:
    - 64 MHz (HSI or PLL)
    - Fail-safe 48 MHz crystal oscillator (HSE), with integrated trimming capacitors
    - 32 kHz crystal oscillator (LSE)
    - Integrated low-power 32 kHz RC (LSI)
  - 1x 16-bits, four channels general purpose timer
  - 1x 16-bits, two channels general purpose timer
  - 1x RTC
  - 1x independent watchdog
  - Radio timer with wakeup capability
- Security
  - Secure bootloader with SWD disabling
  - AES-128 co-processor and 16-bit TRNG
  - Embedded UART bootloader with selectable write and read-out protection
- Operating range and reset
  - Ultra-low-power power-on-reset (POR) and power-down-reset (PDR)
  - Programmable voltage detector (PVD)
  - Supply voltage: from 1.7 to 3.6 V
  - Temperature range: -40 °C to 105 °C
- All packages are ECOPACK2 compliant

Applications

- Asset tracking
- Wireless sensors
- Industrial monitoring and control
- Home energy management systems
- Smart home and alarm systems
- Building automation
- Heat cost allocator
- Remote metering

1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32WL30xx microcontrollers, based on Arm® core.

This document must be read in conjunction with the STM32WL30xx reference manual (RM0511).

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32WL30xx errata sheet (ES0653).

For information on the Arm® Cortex®-M0+ core, refer to the Cortex®-M0+ technical reference manual, available from the www.arm.com website.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 Glossary

Table 1. Definition of terms

Acronym	Description
AES	Advanced encryption standard hardware accelerator
AHB	Advanced high-performance bus
APB	Advanced peripheral bus
BOR	Brown out reset
CHF	Channel filter
CRC	Cyclic redundancy check
DMAMUX	Direct memory access multiplexer
ETSI	European telecommunications standards institute
GFSK	Gaussian frequency shift keying
HSE	High speed external clock oscillator
HSI	High speed Internal clock oscillator
IRQ	Interrupt request
LDO	Low drop output
LPWAN	Low-power wide-area network
LSE	Low-speed external clock oscillator
LSI	Low-speed internal clock oscillator
OTP	One time programmable
PDR	Power down reset
POR	Power on reset
PVD	Programmable voltage detector
PWR	Power controller
SMPS	Switch mode power supply
SPI	Serial peripheral interface (communication standard)
SWD	Single wire debug
SYSCFG	System configuration
TIM	Timer
VREF	Voltage reference
WFI	Wait for instruction (Arm instruction entering low power mode)
WDG	Watchdog

2 Description

The STM32WL30xx is a high performance ultra-low power wireless application processor, intended for RF wireless applications in the sub-1 GHz band. It is designed to operate in both the license-free ISM and SRD frequency bands such as 433, 868, and 915 MHz.

It adopts a single-core architecture embedding an Arm® 32-bit Cortex®-M0+ CPU that can operate up to 64 MHz. It integrates high-speed and flexible memory types: up to 128 Kbyte flash memory, and up to 16 Kbyte RAM, one-time programmable (OTP) memory area of 1 Kbyte.

The STM32WL30xx embeds a wide set of peripherals, RTC, IWDG, general purpose timers, AES-128, RNG, CRC, communication interfaces such as USART, and SPI. Moreover, the security features enable secure boot with USART/SWD block (write protection) and sensitive information storage in flash (read-out protection).

Direct data transfer between memory and peripherals and from memory-to-memory is supported by seven DMA channels with fully-flexible channel mapping by the DMAMUX peripheral.

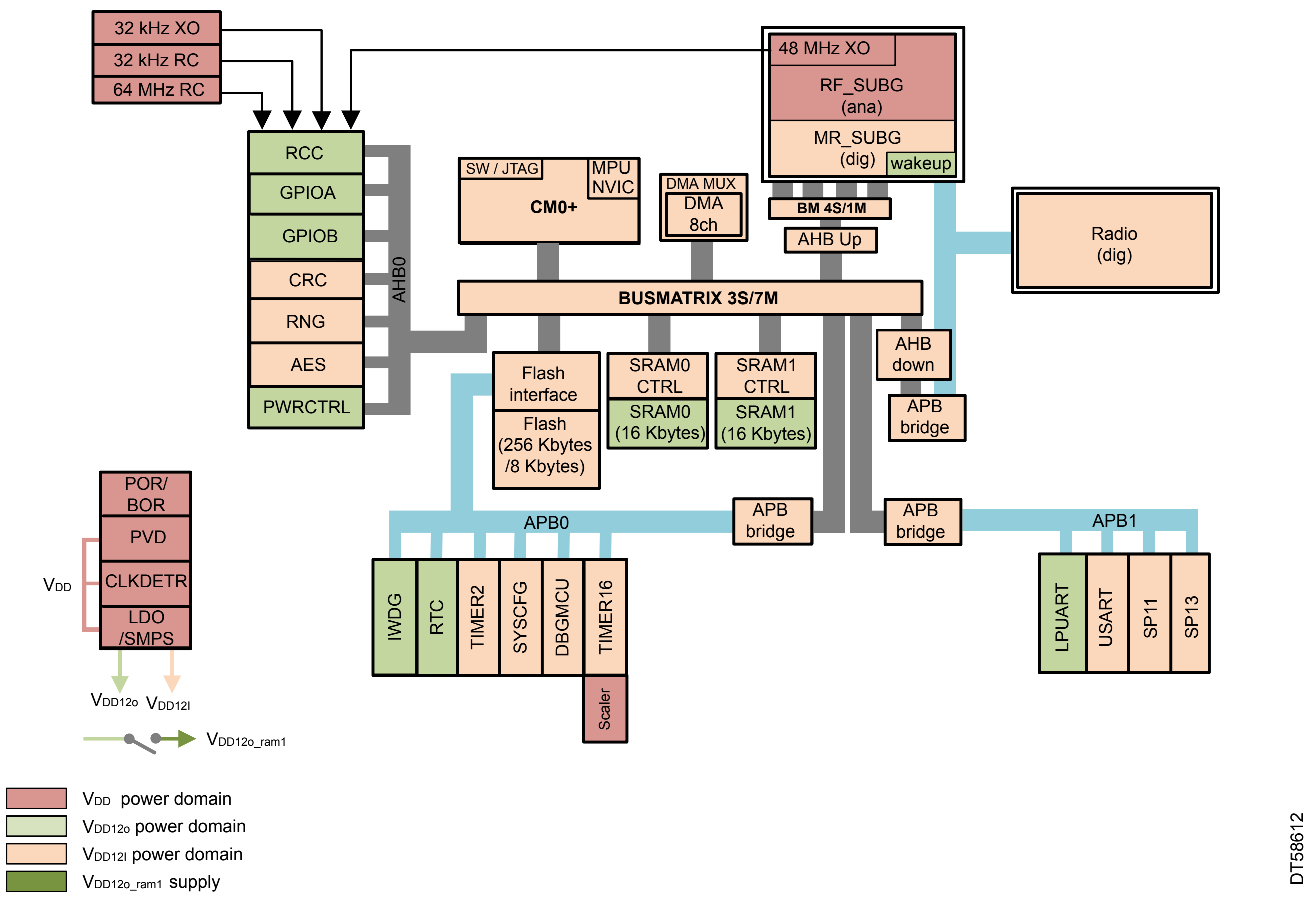
It can be configured to support standalone or network processor applications. In the first configuration, the STM32WL30xx operates as single device in the application for managing both the application code and proprietary sub-1 GHz protocol stacks.

It operates in the -40 to +105 °C temperature range from a 1.7 V to 3.6 V power supply. A comprehensive set of power-saving modes enables the design of low-power applications.

The integrated highly efficient SMPS step-down converter together with the state transition speed between low-power and active states minimize in every condition the average current consumption enabling the STM32WL30xx to be the wireless application processor most suited for battery-operated applications.

The STM32WL30xx comes in a VFQFPN32 package supporting up to 17 I/Os.

Figure 1. Block diagram



3 Functional overview

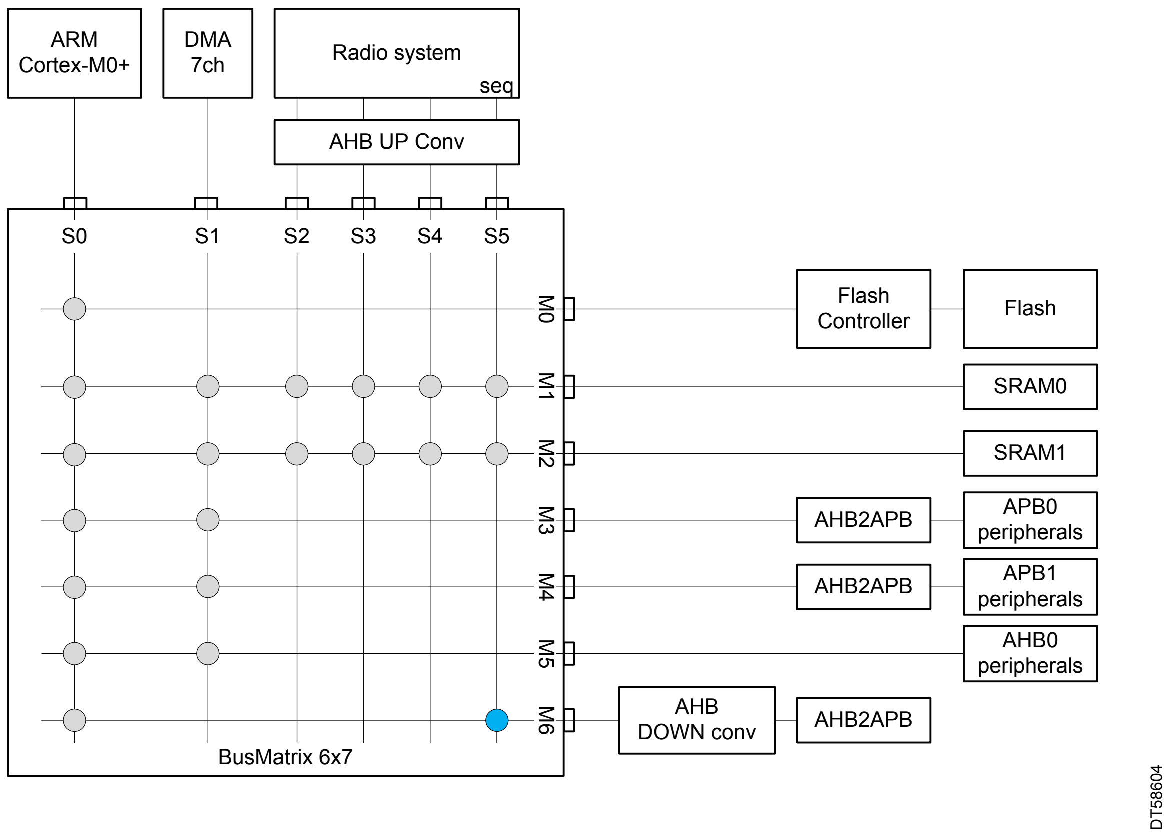
3.1 Architecture

The devices embed a sub-GHz RF subsystem that interfaces with a generic microcontroller subsystem using an Arm Cortex®-M0+ core. The main system consists of a 32-bit multilayer AHB bus-matrix interconnect:

- Three masters:
  - CPU (Cortex -M0+) core S-bus
  - DMA1
  - Sub-1 GHz radio subsystem
- Seven slaves:
  - Internal flash memory on CPU (Cortex®-M0+) S bus
  - Internal SRAM0 (16 Kbytes)
  - Internal SRAM1 (16 Kbytes)
  - APB0 peripherals (through an AHB to APB bridge)
  - APB1 peripherals (through an AHB to APB bridge)
  - AHB0 peripherals
  - AHBRF including AHB to APB bridge and Radio peripherals (connected to APB2)

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously. This architecture is shown in Figure 2.

Figure 2. STM32WL30xx system architecture



The system consists of a Cortex®-M0+ “Radio protocol and application” processor with its radio sub-system. There is a single flash memory to be used by the CPU for both sub-1 GHz protocols and application management. The peripherals are located on the different system buses (AHB, APB0, APB1, APB2 for the radio system). There are 2 SRAM banks, a SRAM0 always power supplied and SRAM1 that can be programmed to be always on or switchable.

3.2 Arm Cortex-M0+ core with MPU

The STM32WL30xx contains an Arm Cortex-M0+ microcontroller core. The Cortex-M0+ provides a low-cost platform that meets the needs of CPU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts. The Cortex-M0+ can run from 1 MHz up to 64 MHz. The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier. The interrupts are handled by the Cortex-M0+ nested vector interrupt controller (NVIC). The NVIC controls specific Cortex-M0+ interrupts as well as the STM32WL30xx peripheral interrupts. With its embedded Arm core, the STM32WL30xx family is compatible with all Arm tools and software.

3.3 Memories

3.3.1 Embedded flash memory

The flash controller implements the erase and program flash memory operation. The flash controller also implements the read and write protection.

The flash memory features are:

- Memory organization:
  - 1 bank of 128 Kbytes
  - Page size: 2 Kbytes
- 32-bit wide data read/write
- Page erase (2 Kbytes) and mass erase

Flash controller features:

- flash memory read operations
- flash memory write operations: single data write, or 4x32-bits burst write
- flash memory erase operations
- page write protection mechanism (by 4 segments of variable sizes from 1 to 127 pages)

Option-byte loader hardware mechanism reserved for ST analog trimming bits.

3.3.2 Embedded SRAM

The STM32WL30xx integrates a total of 16 Kbytes of embedded SRAM in the STM32WL30KB, and 8 Kbytes in the STM32WL30K8.

3.3.3 Embedded OTP

The one-time-programmable (OTP) is a memory of 1 Kbyte dedicated for user data. The user can protect the OTP data area by writing the last word at address 0x1000 1BFC and by performing a system reset. This operation freezes the OTP memory from further unwanted write operations.

3.3.4 Memory protection unit (MPU)

The MPU is used to manage accesses to memory to prevent one task from accidentally corrupting the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas. The MPU is especially helpful for applications where critical or certified code must be protected against the behavior of other tasks.

3.4 RF subsystem

The STM32WL30xx embeds an ultra-low-power radio supporting Sub-1GHz operation.

It integrates a high performance ultra-low power Sub-1GHz transceiver supporting different modulation schemes: 2(G)FSK, 4(G)FSK, OOK and ASK and air data rate programmable from 0.1 to 300 kbit/s for 2-GFSK and up to 600 kbit/s for 4-GFSK.

The STM32WL30xx RF output power can be programmed to deliver up to +20 dBm, in TX+TXHP mode, enabling long communication ranges. Up to +16 dBm in TXHP mode or up to +10 dBm in TX modes, exploiting the extremely optimized architecture for ultra-low-current consumption and battery-operated system.

The STM32WL30xx receiver offers best in class sensitivity performance together with extremely low current consumption. Moreover, it is compliant with ETSI CAT1 adjacent channel selectivity specification and very high blocker rejection, resulting in receiver robustness and in the capability to demodulate packets even in the presence of high interferer signals in very crowed frequency channel.

The IQ data access in receiver mode, coupled with polar mode control of the transmitter, enables the implementation of custom modulation schemes using the embedded microcontroller or using an external DSP.

3.4.1 RF front-end

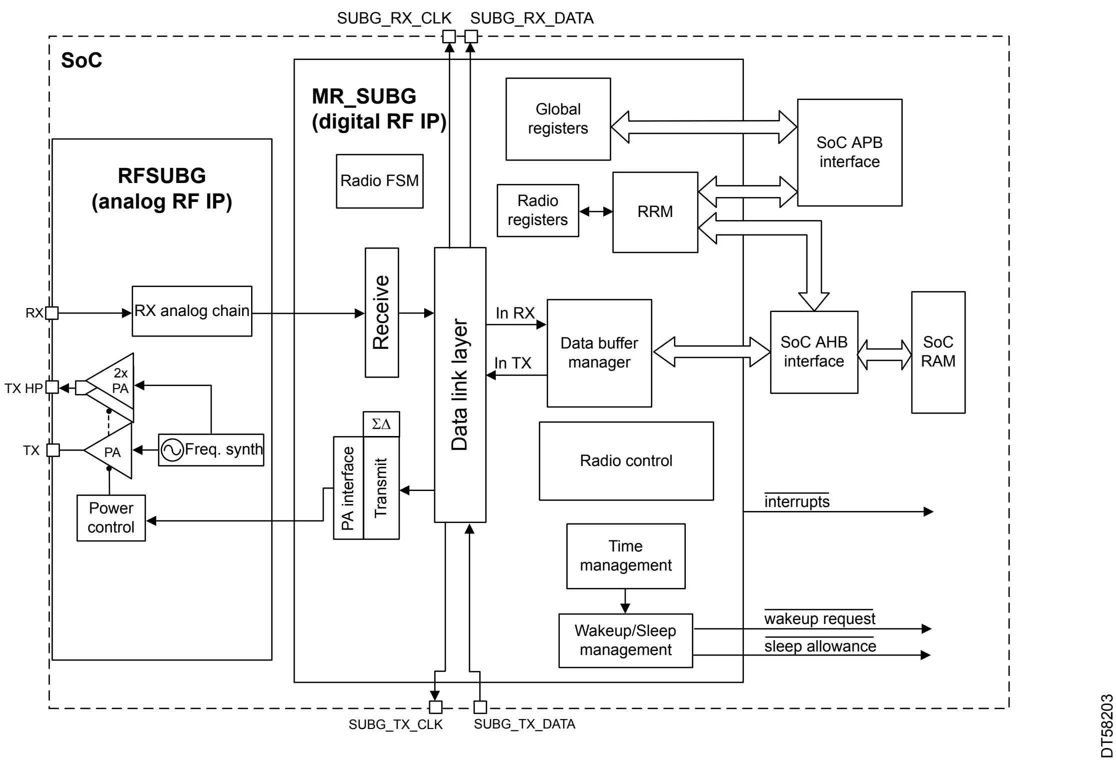
The RF front-end is based on a direct modulation of the carrier in TX and used a low IF architecture in RX mode.

In transmit mode, three different topologies, with dedicated BOM configuration on the board, address operations in different output power range according to the selection of TX and TX_HP.

Moreover, the output power is user selectable through the dedicated programmable register. A linearized, smoothed analog control offers a clean power ramp-up.

In receive mode, the automatic gain control (AGC) can reduce the chain gain at both RF and IF locations, for optimized interferer rejections. Thanks to the use of complex filtering and highly accurate I/Q architecture, high sensitivity and excellent linearity can be achieved.

Figure 3. Sub-1GHz IP block diagram



3.4.2 TX and RX event alert

The STM32WL30xx is provided with the TX_SEQUENCE and RX_SEQUENCE signals which alert, respectively, transmission and reception activities.

A signal can be enabled for TX and RX on two pins, through alternate functions:

- TX_SEQUENCE is available on PA10 (AF2) or PB14 (AF2)
- RX_SEQUENCE is available on PA8 (AF2) or PA11 (AF2)

The signal is high when radio is in TX (or RX), low otherwise.

The signals can be used to control external antenna switching and support coexistence with other wireless technologies.

Note: The RF_ACTIVITY signal is used to notify if there is an ongoing RF operation (either TX or RX). It is a logical OR between the RX_SEQUENCE and TX_SEQUENCE.

3.5 Power supply management

3.5.1 SMPS step-down converter

The device integrates a step-down converter to improve low power performance when the V_{DD} (also referred to as V_{DDIO}) voltage is high enough.

The SMPS output voltage can be programmed from 1.2 V to 2.4 V with a granularity of 100 mV. The SMPS output voltage can be controlled by the PWRC_CR5.SMPSLVL[3:0] register.

The relation between the SMPSLVL and the V_{out} of the SMPS is given by Table 2:

Table 2. SMPS output voltage

SMPSLV	V_{out}	Min. V_{DD}
0	1.2 V	1.95 V
1	1.2 V	1.95 V
2	1.2 V	1.95 V
3	1.3 V	1.95 V
4	1.4 V	2.0 V
5	1.5 V	2.0 V
6	1.6 V	2.15 V
7	1.7 V	2.2 V
8	1.8 V	2.3 V
9	1.9 V	2.45 V
10	2.0 V	2.6 V
11	2.1 V	2.7 V
12	2.2 V	2.8 V
13	2.3 V	2.8 V
14	2.4 V	2.9 V
15	2.4 V	2.9 V

It is internally clocked at 4 MHz or 8 MHz. It can be clocked at a frequency in-between 4 MHz and 8 MHz by means of the KRM feature. In this case the SMPS can be clocked at system clock divided by 8 to 16 by unitary steps. This feature is useful to avoid that the channel to be received is at a frequency that is an integer multiple of the SMPS clock.

The device can operate without the internal SMPS either by using a dedicated hardware setting, or by using the bypass-on-the-fly (BOF) feature. The bypass-on-the-fly permits internal connection of the SMPS output to the battery via a current-limited switch (Static mode), or bypass of the SMPS by the use of an internal regulator (dynamic). In both modes the SMPS is off while the bypass-on-the-fly is operating, and a programmable current limitation is provided. The Static mode connects the SMPS output to the battery after the first start-up of the STM32WL30xx, and the connection is maintained until a reset occurs. In this case, the transmission is limited to +14 dBm. The dynamic mode bypasses the SMPS with a regulator. For instance, this can be done dynamically to use the SMPS during transmission and to bypass the SMPS via a regulator during reception.

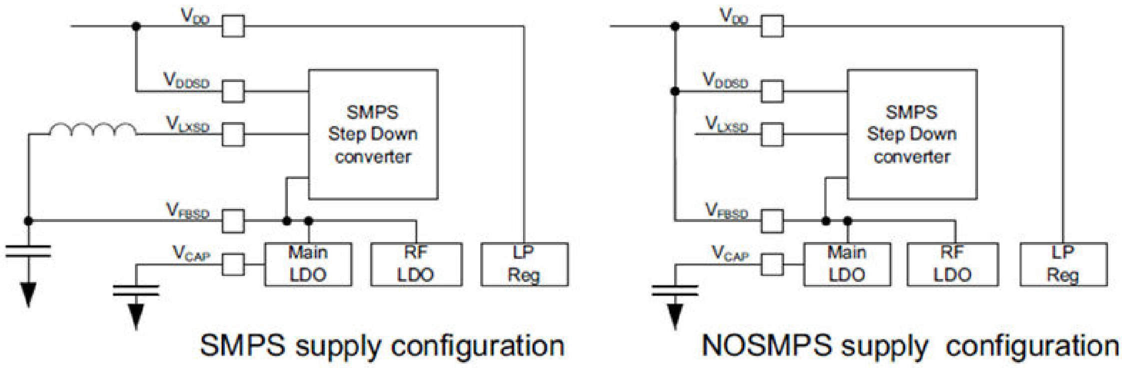
The SMPS has the following possible configurations:

- SMPS_ON
  - the VFBSD pin of the SMPS outputs a regulated voltage (from 1.2 V to 2.4 V)
  - the SMPS needs a clock.
- No SMPS
  - VFBSD pin must be connected or to an external supply or to VDD
  - VLXSD pin must be floating
  - the SMPS does not need a clock

- STATIC BYPASS ON THE FLY
  - the VFBSD pin is internally connected to VDDSD via a switch, with a maximum current of 40 mA
  - the SMPS does not need a clock and is disabled
- DYNAMIC BYPASS ON THE FLY
  - the VFBSD pin internally connected to the output of a programmable voltage regulator, with a maximum current of 40 mA.
  - the SMPS doesn't need a clock and is disabled

Except for the configuration SMPS OFF, an L/C BOM must be present on the board and connected to the VFBSD pad.

Figure 4. Power supply configuration



3.5.2 SMPS bypass on-the-fly (BOF)

Bypass on-the-fly (BOF) is a feature that allows the SMPS to be bypassed. This can be done directly with a power switch (static bypass mode), or via an LDO (dynamic bypass mode).

In case extra radio sensitivity is needed, the user can switch to dynamic bypass mode before entering radio receiver mode. In this way the SPSM is OFF. When BOF is done in static bypass mode, the SMPS is disabled and the SMPS output is connected to the battery via an internal switch. In this case both Deepstop and Run mode operations can be chosen.

When BOF is done in dynamic bypass mode, the SMPS is disabled and the LDO is enabled. The LDO is connected between the battery and the VFBSD pin and its output voltage is programmable like the SMPS.

A current limitation is implemented in both static and dynamic bypass modes.

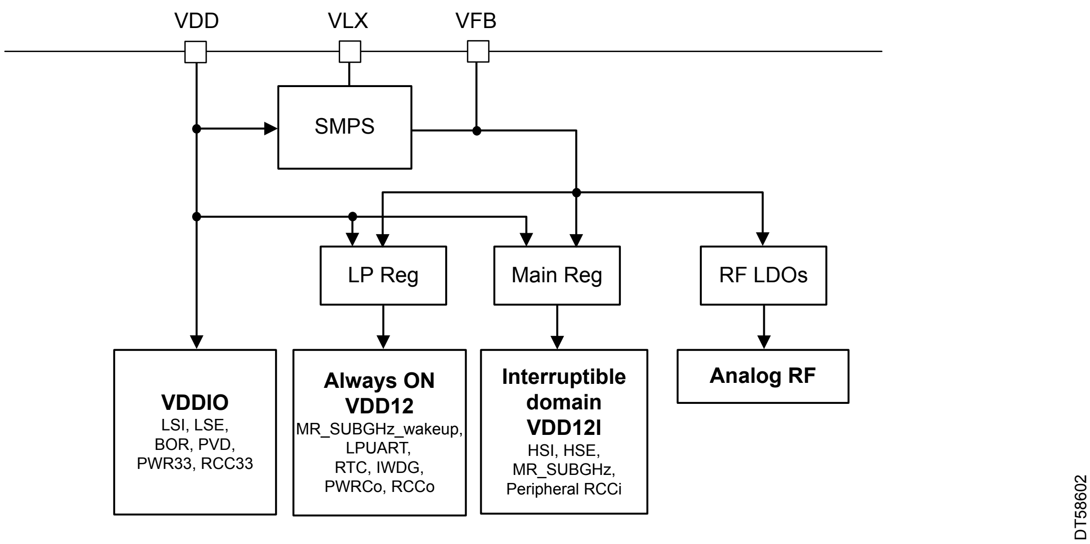
3.5.3 Linear voltage regulators

The digital power supplies are provided by different regulators:

- main LDO (MLDO):
  - provides 1.2 V from a 1.4 to 3.6 V input voltage
  - supplies both VDD12i and VDD12o when the device is active
  - is disabled during the low power mode (Deepstop)
- Low power LDO (LPREG):
  - stays enabled during both active and low power phases
  - provides 1.0 V or 1.2 V voltage selectable by software
  - not connected to the digital domain when the device is active
  - connected to the VDD12o domain during low power mode (Deepstop)
- Dedicated LDO (RFLDO) to provide a 1.2 V to the analog RF block

The embedded SMPS step-down converter is inserted between the external power and the LDOs.

Figure 5. Power-supply domains overview



3.5.4 Power voltage supervisor

The STM32WL30xx device embeds several power voltage monitoring:

- Power On reset (POR) / Power Down reset (PDR) / Brown-Out reset (BOR)
- BORH monitoring
- Power voltage detector (PVD)

3.6 Operating modes

The STM32WL30xx supports three main operating modes:

- Run mode
- Deepstop mode
- Shutdown mode

The transition from one mode to another one is managed through a PMU state machine.

3.6.1 Run mode

In Run mode, the STM32WL30xx is fully operational.

In Run mode:

- both regulators (MLDO and LPREG) are enabled
- the MLDO provides the power supply for both VDD12i and VDD12o
- the system clock and the bus clock are running
- the CPU core and the radio can be used
- the power consumption may be reduced by gating the clock of the unused peripherals

3.6.2 Deepstop mode

Deepstop is the only low power mode of the STM32WL30xx allowing the restart from a saved context environment and the application at wake-up to go on running.

The conditions to enter Deepstop mode are:

- The radio (MR_SUBG) is sleeping (no radio activity)
- The CPU is sleeping (WFI with SLEEPDEEP bit activated)
- No unmasked wake-up sources are active (including those from a previous wakeup sequence for which the software did not clear the associated flag after wakeup) the PWRC_CR1.LPMS bit is equal to 0.
- The system is clocked on RC64MPLL (HSI or PLL locked mode)
- Reset PWRC_CR5.GPIORET bit when PWRC_DBGR.DEEPSTOP2 bit is set, otherwise set PWRC_CR5.GPIORET bit
- If SMPS clock variable rate multiplier is enabled RCC_KRMR.KRMEN=1, in order to guarantee a good SMPS startup at next wakeup, its mandatory to put RCC_CFGR.SMPSDIV=0.

In Deepstop mode:

- The system and the bus clocks are stopped as the RC64MPLL block is OFF
- the VDD12i power domain is switched off
- the VDDI2o power domain is ON and supplied by the LPREG which regulated voltage is:
  - 1.2 V if the bit PWRC_CR2.LPREG_FORCE_VH=1
  - 1.0 V in all the other cases

The current regulation status of the LPREG is reported by the PWRC_CR2.LPREG_VH_STATUS bit:

- the RAM0 bank is kept in retention
- the other RAM banks are in retention or not, depending on software choice in PWRC_CR2 register
- the slow clock can be running or stopped, depending on the software configuration present before Deepstop entry:
  - ON or OFF
  - LSE or LSI source
- The RTC, IWDOG, and LPUART stay active (if enabled and one slow clock source is ON).
- The MR_SUBG wakeup block including its timer stay active (if enabled and one slow clock source is ON).
- The configurations of all the I/Os are latched before entering Deepstop mode:
  - AF configuration is latched only for the I/Os on which at least one pin of a peripheral that can be active in Deepstop mode (RTC, IWDOG, and LPUART) is mapped
  - I/O analog switch configurations are retained for the I/Os on which at least one analog pin of a peripheral that can be active in Deepstop mode is mapped
  - All the I/Os that can be outputs driving either a static low or high level, and also some IOs with the slow clock information, LCO, or RTC_OUT.

A version of the Deepstop mode called DEEPSTOP2 has been implemented to emulate the Deepstop mode without losing the debugger connection and breakpoints nor watchpoints.

- This variant can be selected by setting the PWRC_DBGR.DEEPSTOP2 bit.
- In this case, the Deepstop mode sequence (entry and exit) is done without shutting down the VDD12i power domain.

Possible wake-up sources are:

- The radio block is able to generate two events to wake up the system through its embedded wake-up timer running on low speed clock:
  - SUBG RFIP wakeup time is reached
- the RTC is able to generate a wakeup event
- the LPUART is able to generate a wakeup event

- the IWDG is able to generate a reset event
- all I/Os are able to wake up the system.

At wakeup, the hardware resources located in the VDD12i power domain are reset, the CPU reboots. The reason for wakeup is visible in a PWRC register.

3.6.3 Shutdown mode

The Shutdown mode is the least power consuming mode. The conditions to enter Shutdown mode are the same conditions needed to enter Deepstop mode except that the PWRC_CR1.LPMS bit must be equal to 1. (PWRC_DBGR.DEEPSTOP2 bit must be maintained equal to 0).

In Shutdown mode, the STM32WL30xx is in ultra-low power consumption: all voltage regulators, clocks and the RF interface are not powered. The STM32WL30xx can enter shutdown mode by internal software sequence. There are two ways to exit shutdown mode: by asserting and de-asserting the RSTN pin or by configurable pulse polarity on GPIO PB0.

In Shutdown mode:

- The system is powered down as both the regulators are OFF
- The V_{DDIO} power domain is ON
- All the clocks are OFF, LSI and LSE are OFF
- The I/O pull-ups and pull-downs can be controlled during Shutdown mode, depending on the software configuration
- Two wake-up sources are available: a low pulse on the RSTN pin or a configurable pulse polarity on GPIO PB0.

The exit from Shutdown is like a POR start up. The BOR feature can be enabled or disabled during Shutdown.

3.7 Reset management

The STM32WL30xx offers two resets:

- PORESETn: this reset is provided by the APMU analog power management unit block and corresponds to a POR or BOR root cause. It is linked to power voltage ramp-up or ramp-down. This reset impacts all resources of the STM32WL30xx device.
  Exit from Shutdown mode is equivalent to a POR/BOR and thus generates a PORESETn.
- The PADRESETn (system reset): this reset is built through several sources:
  - PORESETn
  - Reset due to the watchdog The STM32WL30xx embeds a watchdog timer, which may be used to recover from software crashes.
  - Reset due to CPU lockup. The Cortex-M0+ generates a lockup to indicate the core is in the lock-up state resulting from an unrecoverable exception. The lock-up reset is masked if a debugger is connected to the Cortex-M0+.
  - Software system reset. The system reset request is generated by the debug circuitry of the Cortex-M0+. The debugger sets the SYSRESETREQ bit of the application interrupt and reset control register (AIRCR). This system reset request through the AIRCR can also be done by the embedded software (into the hardfault handler for instance).
  - Reset from the NRSTn external pin The NRSTn pin toggles to inform that a reset has occurred.

The PADRESETn resets all resources of the STM32WL30xx, except:

- debug features
- flash controller key management
- RTC timer
- power controller unit
- part of the RCC registers

The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In case of reset from the RSTN external pad, the reset pulse is generated when the pad is asserted low.

3.8 Clock management

Three different clock sources may be used to drive the system clock (CLK_SYS) of the STM32WL30xx (see Figure 6. Fast clock tree generation):

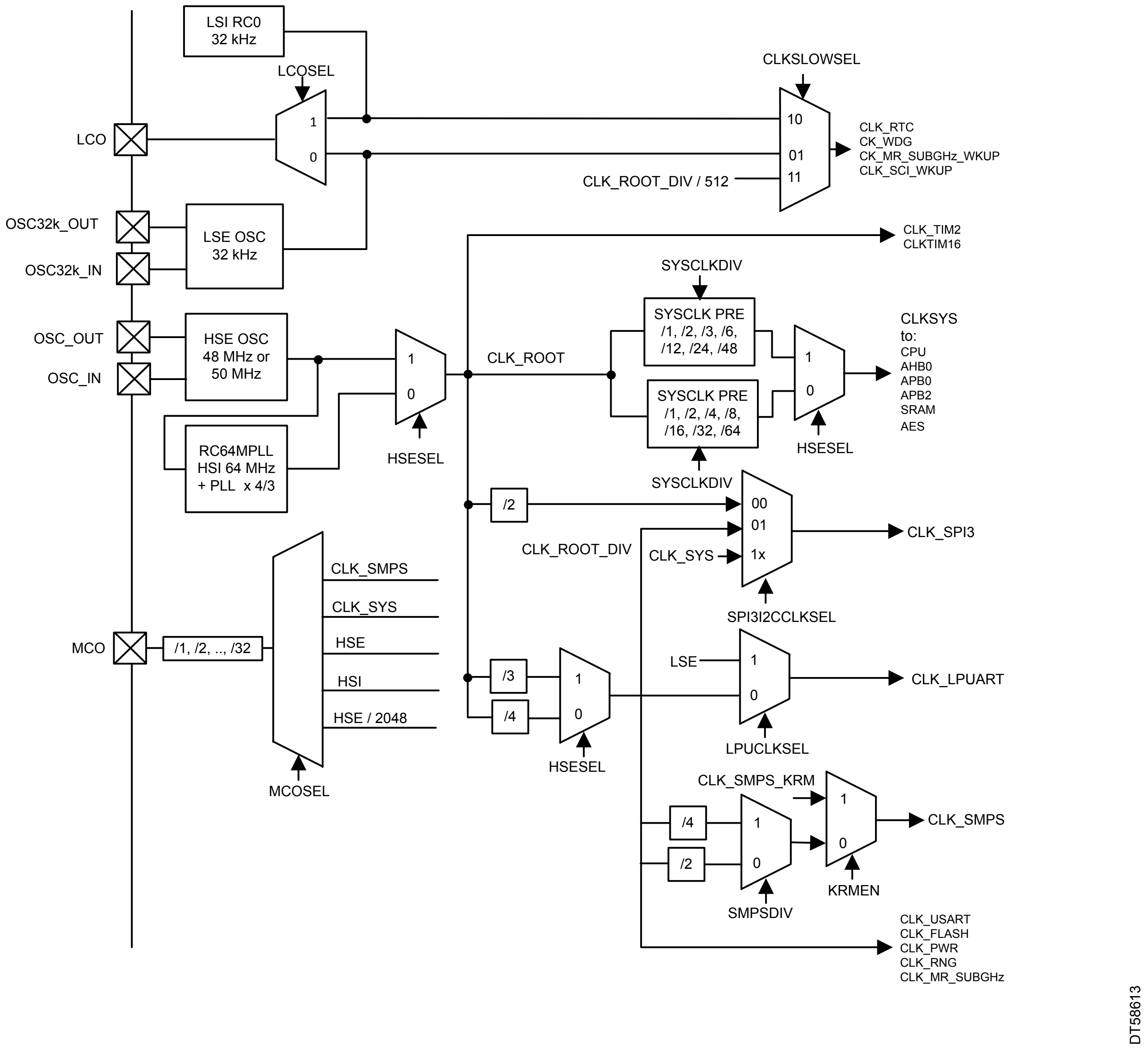
- HSI: high speed internal 64 MHz RC oscillator
- PLL64M: 64 MHz PLL clock based on HSE 48 MHz
- HSE (High Speed External):
  – high speed 48 MHz external crystal
    or
  – provided by a single ended 48 MHz input instead of a crystal

The STM32WL30xx has also a slow frequency clock tree used by some peripherals (RTC, watchdog, LPUART, and MR_SUBG radio timer). Three different clock sources can be used for this slow clock tree:

- LSI: low speed low drift internal RC with a fixed frequency between 24 kHz and 49 kHz depending on the sample. It is called the 32 kHz clock within this document for simplicity.
- LSE:
  – 32.768 kHz low speed external crystal.
    or
  – provided by a single-ended 32.768 kHz input instead of a crystal
- The CLOCK_ROOT_DIV/512 (see Figure 6): In this case, the slow clock is not available in Deepstop mode and it must not be used for peripherals working in Deepstop mode.

Figure 6 provides an overview of the fast clock tree in the STM32WL30xx.

Figure 6. Fast clock tree generation



3.8.1 System clock details

The HSI and the PLL64M clocks are provided by the same analog block which can synthesize:

- a non-accurate clock (target is 1% typical) when no external XO provides an input clock to this block
- an accurate clock when the external XO provides the 48 MHz and once its internal PLL is locked.

The use of PLL64M or HSE as clock source is mandatory for sub-1 GHz radio operations (because a high accuracy clock is needed).

This fast clock source is used to generate all the fast clocks of the device through dividers as shown in Figure 6. After reset, the CLK_SYS is divided by four to provide a 16 MHz to the whole system (CPU, DMA, memories, and peripherals). Then the software can program another system clock frequency (CLK_SYS) in the following way using the RCC_CFGR.CLKSYSDIV bits:

- 000: CLK_SYS is CLK_ROOT
- 001: CLK_SYS is CLK_ROOT/2
- 010: CLK_SYS is CLK_ROOT/4 (HSESEL = 0) or CLK_ROOT/3 (HSESEL = 1)
- 011: CLK_SYS is CLK_ROOT/8 (HSESEL = 0) or CLK_ROOT/6 (HSESEL = 1) (forbidden when radio is in use)
- 100: CLK_SYS is CLK_ROOT/16 (HSESEL = 0) or CLK_ROOT/12 (HSESEL = 1) (forbidden when radio is in use)
- 101: CLK_SYS is CLK_ROOT/32 (HSESEL = 0) or CLK_ROOT/24 (HSESEL = 1) (forbidden when radio is in use)
- 110: CLK_SYS is CLK_ROOT/64 (HSESEL = 0) or CLK_ROOT/48 (HSESEL = 1) (forbidden when radio is in use)

Forbidden configuration means that the “in use” feature cannot work if the system clock runs at this frequency.

Special care must be taken when programming the CLK_SYS as some constraints need to be respected:

CLK_SYS frequency must be greater or equal to CLK_MR_SUBGHz.

3.9 Boot mode

Following CPU boot, the application software can modify the memory map at address 0x0000 0000. This modification is performed by programming the REMAP bit in the flash controller. The following memory can be remapped:

- main flash memory SRAM0 memory

The STM32WL30xx SOC has a pre-programmed bootloader supporting USART protocol with automatic baud rate detection. The main features of the embedded bootloader are:

- auto baud rate detection up to 1 Mbps
- flash mass erase, section erase
- flash programming
- flash readout protection enable/disable

The pre-programmed bootloader is an application, which is stored in the STM32WL30xx internal ROM at manufacturing time by STMicroelectronics. This application allows upgrading the device flash memory with a user application using a serial communication channel (USART).

The bootloader is activated by hardware by forcing PA10 high during hardware reset, otherwise, application residing in flash memory is launched.

STMicroelectronics provides a boot loader executed after each CPU reboot. This boot loader has its own documentation.

3.10 General purpose inputs/outputs (GPIO)

Each general-purpose I/O port has four 32-bit configuration registers, two 32-bit data registers, and a 32-bit set/reset register. In addition, all GPIOs have a 32-bit locking register and two 32-bit alternate function selection registers.

Each of the GPIO pins can be configured by software:

- Output states: push-pull or open drain with pull-up/down
- Output data from output data register or peripheral (alternate function output)
- Speed selection for each I/O
- Input states: floating, pull-up/down, analog
- Input data to input data register or peripheral (alternate function input)
- Bit set and reset register for bitwise write access
- Locking mechanism provided to freeze the I/O port configurations
- Analog function
- Alternate function selection registers
- Fast toggle capable of changing every clock cycle
- Highly flexible pin multiplexing allows the use of I/O pins as GPIOs or as one of several peripheral functions.

3.11 Direct memory access (DMA)

Direct memory access (DMA) provides high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations. The implemented DMA has an arbiter for handling the priority between DMA requests. The DMA main features are as follows:

- Eight independently configurable channels (requests)
- Each of the eight channels is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software
- Priorities between requests from channels of the DMA are software programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, and so on.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size
- Support for circular buffer management
- event flags (DMA Half Transfer, DMA Transfer Complete and DMA Transfer Error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer (SRAM0/SRAM1)
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to SRAMs, APB0 and APB1 peripherals as source and destination
- Programmable number of data to be transferred: up to 65536

3.12 Nested vectored interrupt controller (NVIC)

The interrupts are handled by the Cortex-M0+ Nested Vector Interrupt Controller (NVIC). The NVIC controls specific Cortex-M0+ interrupts (address 0x00 to 0x3C) as well as 32 user interrupts (address 0x40 to 0xBC). In the STM32WL30xx device, the user interrupts have been connected to the interrupt signals of the different peripherals (GPIO, flash controller, timer, USART, and so on). These interrupts can be controlled using the ISER, ICER, ISPR and ICOR registers (see “Cortex-M0+ Devices Generic User Guide”).

3.13 Advanced encryption standard hardware accelerator (AES)

The AES hardware accelerator can be used to both encrypt and decrypt data using the AES algorithm. It is a fully compliant implementation of the advanced encryption standard (AES) as defined by Federal Information Processing Standards Publication (FIPS PUB 197, 2001 November 26). Multiple key sizes and chaining modes are supported: ECB, CBC, CTR for key sizes of 128 bits The AES is a 32-bit AHB peripheral. It supports DMA single transfers for incoming and outgoing data (two DMA channels required). The AES IP provides hardware acceleration to AES crypto algorithm packaged in STM32WL30xx crypto library (excluding key length of 192-bit).

The main features of the AES are:

- NIST FIPS publication 197, Advanced Encryption Standard (AES) compliant implementation
- 128-bit data block processing
- Support for cipher keys length of 128-bit
- Encryption and decryption with multiple chaining modes: – Electronic Code Book (ECB) – Cipher Block Chaining (CBC) – Counter Mode (CTR)
- 51 clock cycles for processing one 128-bit block of data with a 128-bit key in ECB mode
- Integrated key scheduler with its key derivation stage (ECB or CBC decryption only)
- 32-bit AHB interface for register accesses, supporting complete 32- bit word access only. (AHB sequential accesses are not supported).
- 128-bit registers for storing initialization vectors (4× 32-bit)
- 1x32-bit INPUT buffer and 1x32-bit OUTPUT buffer
- Automatic data flow control with support of direct memory access (DMA) using two channels (one for incoming data, one for processed data). Single transfers only.
- Data swapping logic to support 1-bit, 8-bit, 16-bit or 32-bit data
- Possibility for software to suspend a message if the IP needs to process another message with a higher priority (context swapping)

3.14 True random number generator (RNG)

The RNG is a random number generator based on a continuous analog noise that provides a 16-bit value to the host when read.

3.15 Cyclic redundancy check (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size. Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the flash memory integrity. The CRC calculation unit helps to compute a signature of the software during runtime, which can later be compared with a reference signature generated at link-time, and which can be stored at a given memory location.

3.16 General purpose timers

The STM32WL30xx embeds one general purpose timer (TIM2) supporting up to 4 independent channels, one general purpose timer (TIM16) supporting one single channel and one complementary.

3.16.1 General Purpose timer (TIM2)

The general purpose 16-bit timer (TIM2) consists of a 16-bit auto-reload counter driven by a programmable prescaler.

It may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare, PWM). Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler on the timer input clock which is at 32MHz.

The TIM2 main features are:

- 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing division (also “on the fly”) the counter clock frequency either by any factor between 1 and 65536
- Up to 4 independent channels for:
  - input capture
  - output compare
  - PWM generation (edge and center-aligned mode)
  - one-pulse mode output
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Repetition counter to update the timer registers only after a given number of cycles of the counter
- Interrupt/DMA generation on the following events:
  - update: counter overflow/underflow, counter initialization (by software or internal/external trigger)
  - input capture
  - output comparison
  - trigger event (counter start, stop, initialization or count by internal/external trigger)
- Supports incremental (quadrature) encoder for positioning purposes
- Trigger input for external clock or cycle-by-cycle current management
- The counter can be frozen in debug mode

3.16.2 General purpose timer (TIM16)

The TIM16 timer consists of a 16-bit auto-reload counter driven by a programmable prescaler. It may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescaler.

The main TIM16 features are:

- 16-bit auto-reload upcounter
- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
- One channel for:
  - input capture
  - output comparison
  - PWM generation (edge-aligned mode)
  - one-pulse mode output
  - trigger event (counter start, stop, initialization or count by internal/external trigger)
- Complementary output with programmable dead-time
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Repetition counter to update the timer registers only after a given number of cycles of the counter
- Break input to put the timer’s output signals in the reset state or a known state

- Interrupt/DMA generation on the following events:
  - update: counter overflow
  - input capture
  - output comparison
  - break input (interrupt request)
- The counter can be frozen in debug mode.

3.17 Independent watchdog (IWDG)

The STM32WL30xx integrates an embedded watchdog peripheral which offers a combination of high safety level, timing accuracy and flexibility of use. The independent watchdog peripheral serves to detect and resolve malfunctions due to software failure, and to trigger system reset when the counter reaches a given timeout value.

The independent watchdog (IWDG) is clocked by its own dedicated low-speed clock (LSI) and thus stays active even if the main clock fails.

The IWDG is best suited to applications which require the watchdog to run as a totally independent process outside the main application but have lower timing accuracy constraints. The counter can be frozen in debug mode.

3.18 Real-time clock (RTC)

The STM32WL30xx integrates a real-time clock (RTC). It is an independent BCD timer/counter. The RTC provides a time of day/clock/calendar with programmable alarm interrupt. RTC includes also a periodic programmable wake-up flag with interrupt capability. The RTC provides an automatic wake-up to manage all low power modes.

Two 32-bit registers contain seconds, minutes, hours (12- or 24-hour format), day (day of week), date (day of month), month, and year, expressed in binary coded decimal format (BCD). The sub-second value is also available in binary format. Compensations for 28-, 29- (leap year), 30-, and 31-day months are performed automatically. Daylight saving time compensation can also be performed. Additional 32-bit registers contain the programmable alarm sub seconds, seconds, minutes, hours, day, and date.

One anti-tamper detection pin with programmable filter is available. A timestamp feature can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, by a tamper event, or by a switch to Deepstop mode.

A digital calibration circuit is available to compensate for quartz crystal inaccuracy. After power-on reset, all RTC registers are protected against possible parasitic write accesses. As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low power mode or under system reset).

The RTC contains 5 backup registers which are supplied through a switch that takes power either from the VDD12I supply (when present) or from the VDD12O pin.

The backup registers are 32-bit registers used to store 20 bytes of user application data when VDD12I power is not present. They are not reset by a system or power reset, or when the device wakes up from Deepstop mode.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes. The counter can be frozen in debug mode.

3.19 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32WL30xx embeds a universal synchronous asynchronous receiver transmitter (USART) that offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The USART offers a very wide range of baud rates using a fractional baud rate generator.

It supports synchronous one-way communication and half-duplex single wire communication. It also supports the local interconnection network (LIN), SmartCard Protocol and IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). It also supports multiprocessor communications.

High speed data communication is possible by using the DMA (direct memory access) for multibuffer configuration.

The USART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to give flexibility between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data, that can be enabled/disabled by software. FIFOs come with status flags for FIFOs states.
- A common programmable transmit and receive baud rate of up to 2 Mbit/s with the clock frequency at 16 MHz and oversampling is by 8.
- Dual clock domain with a dedicated kernel clock allowing baud rate programming independent from the PCLK reprogramming.
- Auto baud rate detection
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous master/slave mode and clock output/input for synchronous communications
- SPI slave transmission underrun error flag Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications
- Wake up from mute mode (by idle line detection or address mark detection)

3.20 Low power universal asynchronous receiver transmitter (LPUART)

The low power universal asynchronous receiver transmitted (LPUART) is an UART which allows bidirectional UART communications with a limited power consumption. Only 32.768 kHz LSE clock is required to allow UART communications up to 9600 baud/s. Higher baud rates can be reached when the LPUART is clocked by clock sources different from the LSE clock.

Even when the microcontroller is in stop mode, the LPUART can wait for an incoming UART frame while having an extremely low energy consumption. The LPUART includes all necessary hardware support to make asynchronous serial communications possible with minimum power consumption.

It supports half-duplex single wire communications and modem operations (CTS/RTS). It also supports multiprocessor communications.

DMA (direct memory access) can be used for data transmission/reception.

The main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 baud/s to 9600 baud/s using a 32.768 kHz clock source
- Higher baud rates can be achieved by suing a higher frequency clock source
- Two internal FIFOs for transmit and receive data, that can be enabled/disabled by software. FIFOs come with status flags for FIFOs states.
- Dual clock domain allowing:
  - UART functionality and wakeup from stop mode
  - convenient baud rate programming independent from the PCLK reprogramming
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - receive buffer full
  - transmit buffer empty
  - busy and end-of-transmission flags
- Parity control:
  - transmits parity bit
  - checks parity of received data byte
- Four error detection flags:
  - overrun error
  - noise detection
  - frame error
  - parity error
- Interrupt sources with flags
- Multiprocessor communications: the LPUART enters mute mode if the address does not match
- Wakeup from mute mode (by idle line detection or address mark detection)

3.21 Serial peripheral interface (SPI)

The STM32WL30xx embeds two serial peripheral interfaces (SPIs), SPI1 and SPI3.

SPI Motorola mode is selected by default after a device reset.

The SPI interfaces allow communication at up to 32 Mbit/s in both master and slave modes.

The serial peripheral interface (SPI) protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices. The interface can be configured as master, and in this case it provides the communication clock (SCK) to the external slave device. The interface is also capable of operating in multimaster configuration.

The main SPI features are:

- Master or slave operation
- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- 4-bit to 16-bit data size selection
- Multimaster mode capability
- 8 master mode baud rate prescalers up to fPCLK/2
- Slave mode frequency up to fPCLK/2
- NSS management by hardware or software for both master and slave: dynamic change of master/slave operations
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- SPI Motorola support
- Hardware CRC feature for reliable communication:
  - CRC value can be transmitted as last byte in Tx mode
  - automatic CRC error checking for last received byte
- Master mode fault, overrun flags with interrupt capability
- CRC error flag
- Two 32-bit embedded Rx and Tx FIFOs with DMA capability
- SPI TI mode support
- DMA capability for transmission and reception (16-bit wide)

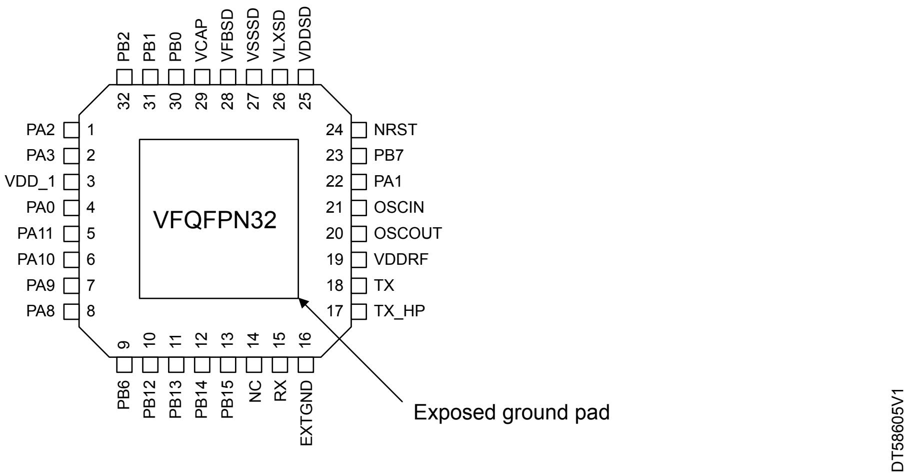
3.22 Debug support (DBG)

The STM32WL30xx embeds an Arm serial wire debug (SWD) interface that enables interactive debugging and programming of the device. The interface is composed of only two pins: SWDIO and SWCLK. The enhanced debugging features for developers allow up to 4 breakpoints and up to 2 watchpoints.

4 Pinouts and pin description

The STM32WL30xx comes in a VQFPN32 package offering 17 GPIOs.

Figure 7. Pinout top view (QFN32 package - 5 mm x 5 mm)



Note: All PAx and PBx type pins can wake up the circuit.

Table 3. Pin description

Pin number VFQFPN32	Pin Name (function after reset)	Pin type	Alternate functions	Additional functions
1	PA2	I/O	SWDIO, USART1_CK, TIM16_CH1, TIM2_CH1	-
2	PA3	I/O	SWCLK, USART1_RTS_DE, TIM16_CH1N, SPI3_SCK, TIM2_CH2	-
3	VDD_1	S	-	1.7 to 3.6 V battery voltage input
4	PA0	I/O	USART_CTS, TIM2_CH3	-
5	PA11	I/O	MCO, RX_SEQUENCE, SPI3_MOSI, SUBG_TX_CLOCK	-
6	PA10	I/O	LPUART1_CTS, TX_SEQUENCE, SUBG_TX_DATA	LCO
7	PA9	I/O	USART1_TX, RTC_OUT, SPI3_NSS, TIM2_CH4	-
8	PA8	I/O	RTC_OUT/RTC_TAMP1/RTC_TS, USART1_RX, RX_SEQUENCE, SPI3_MISO, TIM2_CH3	-
9	PB6	I/O	LPUART1_TX, SPI3_SCK, TIM2_CH3	-
10	PB12	I/O	USART1_RTS_DE, LPUART1_CTS, LCO, TIM2_CH3	SXTALO
11	PB13	I/O	TIM2_CH4	SXTALI
12	PB14	I/O	USART1_RX, TX_SEQUENCE, MCO, TIM2_ETR	PVD_VIN
13	PB15	I/O	USART1_TX	-
14	NC	-	-	Not connected
15	RX	I/RF	-	RF RX port
16	EXTGND	S	-	-
17	TX_HP	O/RF	-	RF TX port
18	TX	O/RF	-	RF TX port
19	VDDRF	S	-	1.7 to 3.6 V battery voltage input
20	OSCOUT	I/O	-	48 MHz crystal
21	OSCIN	I/O	-	48 MHz crystal
22	PA1	I/O	USART1_TX, TIM16_BRK, TIM2_CH4	-
23	PB7	I/O	LPUART1_RX, RF_ACTIVITY, SPI3_MOSI, TIM2_ETR	-
24	NRST	RSTS	-	Reset pin
25	VDDSD	S	-	1.7 to 3.6 V battery voltage input SMPS input
26	VLXSD	S	-	SMPS LX pin
27	VSSSD	S	-	SMPS Ground
28	VFBSD	S	-	SMPS output
29	VCAP	S	-	1.2 V digital core

Pin number VFQFPN32	Pin Name (function after reset)	Pin type	Alternate functions	Additional functions
30	PB0	I/O	USART1_RX, LPUART1_RTS_DE, TIM16_CH1, ANTENNA_SWITCH	-
31	PB1	I/O	USART1_CK, SWDIO, TIM16_CH1N, SUBG_RX_DATA	-
32	PB2	I/O	USART1_RTS_DE, SWCLK, TIM16_BRK, SUBG_RX_CLK	-
Exposed pad	GND	S	-	Ground

Table 4. **Alternate function port A**

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF/RTC/ USART	SYS_AF/ USART/ LPUART	SYS_AF/ TIM2	SYS_AF/ SPI3	SYS_AF/ TIM2	SYS_AF/ Single-wire debug
Port A	PA0	-	USART1_CTS	-	-	TIM2_CH3	-
	PA1	-	USART1_TX	TIM16_BRK	-	TIM2_CH4	-
	PA2	SWDIO	USART1_CK	TIM16_CH1	-	TIM2_CH1	SWDIO
	PA3	SWCLK	USART1_RTS_DE	TIM16_CH1N	SPI3_SCK/	TIM2_CH2	SWCLK
	PA8	RTC_OUT/ RTC_TAMP1/ RTC_TS	USART1_RX	RX_SEQUENCE	SPI3_MISO	TIM2_CH3	-
	PA9	-	USART1_TX	RTC_OUT	SPI3_NSS	TIM2_CH4	-
	PA10	-	LPUART1_CTS	TX_SEQUENCE	-	SUBG_TX_DATA	-
	PA11	MCO		RX_SEQUENCE	SPI3_MOSI	SUBG_TX_CLOCK	-

Table 5. Alternate function port B

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF/RTC/ USART	SYS_AF/ USART/ LPUART	SYS_AF/ TIM16	SYS_AF/ SPI1/SPI3	SYS_AF/ TIM2	SYS_AF/
Port B	PB0	USART1_RX	LPUART1_RTS_DE	TIM16_CH1	-	ANTENNA_SWITCH	-
	PB1	USART1_CK	SWDIO	TIM16_CH1N	-	SUBG_RX_DATA	-
	PB2	USART1_RTS_DE	SWCLK	TIM16_BRK	-	SUBG_RX_CLOCK	-
	PB6	-	LPUART1_TX	-	SPI3_SCK	TIM2_CH3	-
	PB7	-	LPUART1_RX	RF_ACTIVITY	SPI3_MOSI	TIM2_ETR	-
	PB12	USART1_RTS_DE	LPUART1_CTS	LCO	-	TIM2_CH3	-
	PB13	-	-	-	-	TIM2_CH4	-
	PB14	-	USART1_RX	TX_SEQUENCE	MCO	TIM2_ETR	-
	PB15	-	USART1_TX	-	-	-	-

5 Application circuits

The schematics below are purely indicative.

Figure 8. STM32WL30xx application circuit without SMPS, VFQFPN32 package

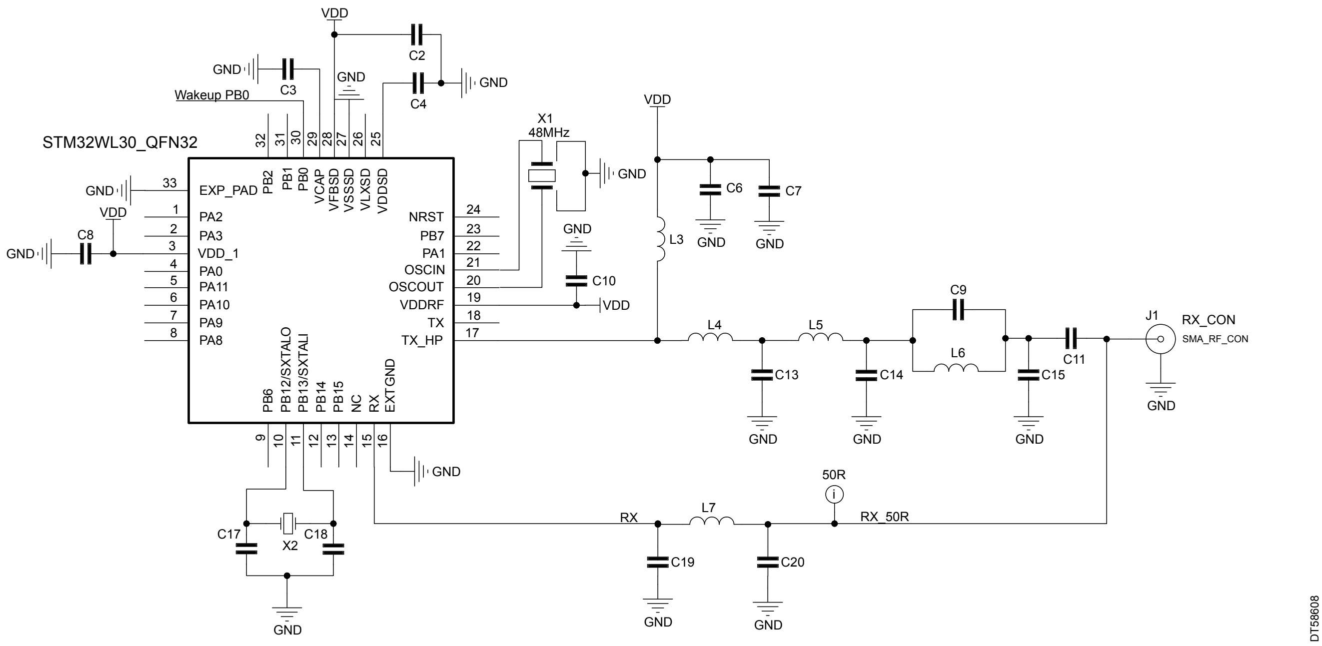


Figure 9. STM32WL30xx application circuit with SMPS, VFQFPN32 package

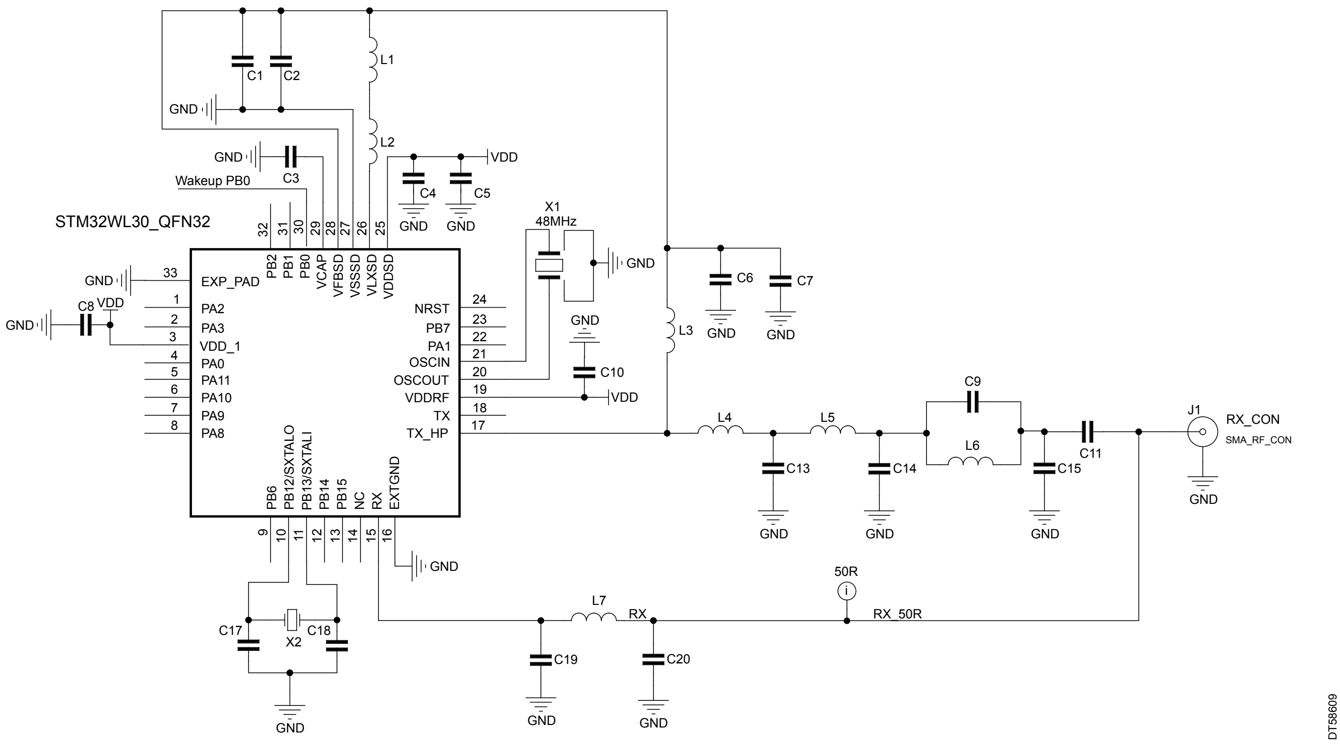


Table 6. Application circuit external components

Components	Description
C6, C7	Decoupling capacitor for PA VDD pin
C8	Decoupling capacitor for VDD_1
C10	Decoupling capacitor for VDDRF
C3	Decoupling capacitor for VCAP
C4, C5	Decoupling capacitor for VDDSD. Input capacitors for internal DCDC converter
C1, C2	Output capacitors for internal DCDC converter
L1	Power inductor for DCDC converter.
L2	SMPS noise filter
C17, C18	32.768 kHz crystal loading capacitors
L3	RF choke inductor
L7, C19, C20	Filter/matching for RX path
L4, C13, L5, C14	Filter/matching for TX path
C9, L6, C15	Notch filter and low pass filter
C11	DC blocking capacitors
X1	48 MHz crystal

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to ground (GND).

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the following standard conditions:

- Ambient temperature is T_A = 25 °C
- Supply voltage is V_{DD}: 3.3 V
- System clock frequency is 64 MHz (clock source HSI)
- SMPS clock frequency is 4 MHz, if not specified otherwise

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V. They are given only as design guidelines and are not tested. Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2σ).

6.2 Absolute maximum ratings

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages refer to GND.

Table 7. Absolute maximum ratings

Pin name	Comment	Min.	Max.	Unit
VDD_1, VDD_2, VDDRF, VDDSD	DC-DC converter supply voltage input and output	-0.3	+3.9	V
VCAP	DC voltage on linear voltage regulator	0.3	+1.4	
OSCOUT, OSCIN	DC Voltage on HSE	0.3	+1.32	
PAx and PBx	DC voltage on digital input/output pins	0.3	+3.9	
VLXSD, VFBSD	DC voltage on analog pins	0.3	+3.9	
XTAL0/PB12, XTAL1/PB13	DC voltage on XTAL pins	0.3	+3.9	
RX	DC voltage on RF pin	0.3	+1.4	
TX	DC voltage on RF pin	0.3	+3.9	
TX_HP	DC voltage on RF pin	0.3	+3.9	
|ΔVDD|	Variations between different supplies: VDD_x and VDDRF, VDD_x and VDDSD[1]	-	50	mV

1. *VDD_1 and VDD_2 to be shorted on PCB.*

Table 8. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source)	130	mA
ΣI_{VGND}	Total current out of sum of all ground lines (sink)	130	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)	100	
$I_{VGND(PIN)}$	Maximum current out of each ground pin (sink)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins	100	
	Total output current sourced by sum of all I/Os and control pins	100	
$\Sigma \lvert I_{INJ(PIN)} \rvert$	Total injected current (sum of all I/Os and control pins)	-50	

Table 9. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-40 to +125	°C
T_J	Maximum junction temperature	125	

6.3 Operating conditions

6.3.1 Operating range

Table 10. Operating range

Parameter	Min.	Typ.	Max.	Unit
Operating battery supply voltage (V_{BAT})	1.7	3.3	3.6	V
Operating ambient temperature range	-40	25	+105	°C

6.3.2 Thermal properties

The maximum chip junction temperature ($T_{Jmax.}$) must never exceed the values in general operating conditions.

The maximum chip-junction temperature, T_J max., in degrees Celsius, can be calculated using the equation:

$$T_J\text{max.} = T_A\text{max.} + (PD\text{max} \times \theta JA) \quad (1)$$

where:

- T_A max. is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W
- PD max. is the sum of PINT max. and PI/O max. (PD max. = PINT max. + PI/O max.)
- PINT max. is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power

PI/O max represents the maximum power dissipation on output pins:

- PI/O max. = Σ (V_{OL} × I_{OL}) + Σ ((V_{DD} – V_{OH}) × I_{OH})

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the applications.

Table 11. Thermal data

Symbol	Parameter	Value	Unit
Q_{JA}	Thermal resistance junction-ambient VFQFPN32 - 5 mm x 5 mm	26.9	°C/W

6.3.3 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is put under the following conditions:

- all I/O pins are in pull-up or pull-down configuration
- all peripherals are disabled except when explicitly mentioned
- the flash memory access time is adjusted with the minimum number of wait states.

Table 12. Shutdown and Reset current

Symbol	Parameter	Test condition	Typ. V_{DD} = 3.3 V	Unit
I_{CORE}	Shutdown	-	14	nA
	Current under Reset condition	-	955	µA

Table 13. Current consumption in Deepstop mode

Symbol	Parameter	Test condition	Typ. V_{DD} = 3.3 V	Unit
I_{CORE}	Deepstop current[2]	No timer, only wake-up GPIO enabled, RAM0 retained	910	nA
		No timer, only wake-up GPIO enabled, all RAM retained	980	nA
		(32 kHz LSI), RAM0 retained	1460	nA
		(32 kHz LSI), all RAM retained	1540	nA
		(32 kHz LSE), RAM0 retained	1163	nA
		(32 kHz LSE), all RAM retained	1240	nA
		Timer source LSI RTC ON	1710	nA
		Timer source LSI IWDG ON	1558	nA
		Timer source LSI, RTC and IWDG ON	1748	nA
		Timer source LSE RTC ON	1430	nA
		Timer source LSE IWDG ON	1273	nA
		Timer source LSE LPUART ON	1370	nA
		Timer source LSE RTC, LPUART and IWDG ON	1670	nA

1. The current consumption in Deepstop mode is measured considering that the entire SRAM is retained.

Table 14. Current consumption in Run and WFI mode with SMPS ON (SMPS frequency 4 MHz, SMPS V_{out} =1.4 V)

Symbol	Parameter	Test condition	Typ. V_{DD} = 3.3 V	Unit
I_{CORE}	Supply current	CPU in Run (16 MHz). Dhrystone, clock source PLL64	2172	µA
		CPU in Run (32 MHz). Dhrystone, clock source PLL64	2532	µA
		CPU in Run (64 MHz). Dhrystone, clock source PLL64	3210	µA
		CPU in WFI (16 MHz), all peripherals off, clock source PLL64	1899	µA
		CPU in WFI (32 MHz), all peripherals off, clock source PLL64	1984	µA
		CPU in WFI (64 MHz), all peripherals off, clock source PLL64	2143	µA
$I_{DYNAMIC}$	Dynamic current	Computed value: (CPU 64 MHz Dhrystone - CPU 32 MHz Dhrystone) / 32	21.18	µA/MHz

Table 15. Current consumption in Run and WFI mode with SMPS bypassed

Symbol	Parameter	Test condition	Typ. V_{DD} = 3.3 V	Unit
I_{CORE}	Supply current in Run mode	CPU in Run (16 MHz). Dhrystone, clock source PLL64	2422	µA
		CPU in Run (32 MHz). Dhrystone, clock source PLL64	3245	µA
		CPU in Run (64 MHz). Dhrystone, clock source PLL64	4771	µA
		CPU in WFI (16 MHz), all peripherals off, clock source PLL64	1788	µA
		CPU in WFI (32 MHz), all peripherals off, clock source PLL64	1989	µA
		CPU in WFI (64 MHz), all peripherals off, clock source PLL64	2368	µA
$I_{DYNAMIC}$	Dynamic current	Computed value: (CPU 64 MHz Dhrystone - CPU 32 MHz Dhrystone) / 32	47.68	µA/MHz

Table 16. Peripheral current consumption at V_{DD}=3.3V, T=25°C System clock 32 MHz, SMPS ON

Peripheral	Typical value	Unit
GPIOA	1	µA
GPIOB	1	
DMA	38	
AES	32	
RNG	103	
CRC	6	
SYSCFG	34	
RTC	18	
WDG	11	
USART	77	
LPUART	56	
SPI3	38	
TIM2	152	
TIM16	94	
PVD	0	
MRSUBG	68	
DBGMCU	1	
SYSTICK	10	

6.3.4 RF general characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

Two reference test conditions are used in the RX measurements: high performance mode (HPM), where the priority is given to the performances, and low power mode (LPM) where the priority is given to the low consumption.

High performance mode (HPM) conditions: V_{DD} = 3.3 V, T_A = 25 °C, SMPS ON, SMPS frequency 4 MHz (unless otherwise stated), SMPS V_{out} = 1.4 V,16 MHz system clock, HSIPLL mode, HSE GMC setting 0x0A and PA_LEVEL7 = 81.

Low power mode (LPM) conditions: SMPS ON (unless otherwise stated), SMPS frequency 4 MHz (unless otherwise stated), SMPS V_{out} =1.2 V, LDO RF bypassed, 16 MHz system clock, HSE direct mode, HSE GMC setting 0x0A.

For RX current consumption, the global SOC consumption is reported as well as the computed contribution due to the sub-1 GHz radio alone (difference between the global consumption and the SOC consumption in WFI mode).

Transmission measurements are performed for V_{DD} = 3.3 V, T_A = 25 °C, SMPS ON, high performance mode (HPM).

Table 17. Current consumption in reception, fc = 915 MHz

Parameter	Test condition	HPM	LPM	Unit
STM32WL30xx supply current	As detailed above	7.0	5.7	mA
CPU current	CPU in WFI state	1.8	1.3	
Radio supply current contribution	Computed value	5.2	4.4	

Table 18. Current consumption in reception, fc = 868 MHz (SMPS clock frequency = 4.27 MHz)

Parameter	Test condition	HPM	LPM	Unit
STM32WL30xx supply current	As detailed above	6.8	5.6	mA
CPU current	CPU in WFI state	1.8	1.3	
Radio supply current contribution	Computed value	5.0	4.3	

Table 19. Current consumption in reception, fc = 433 MHz

Parameter	Test condition	HPM	LPM	Unit
STM32WL30xx supply current	As detailed above	6.7	5.5	mA
CPU current	CPU in WFI state	1.8	1.3	
Radio supply current contribution	Computed value	4.9	4.2	

Table 20. Current consumption in transmission, fc = 433 MHz

Parameter	Test condition	HPM	Unit
Supply current	Measurements TX @ CW 10 dBm TX pin connected, TX Mode	12.5	mA
	Measurements TX @ CW 14 dBm TXHP pin connected, TXHP mode	25	mA
	Measurements TX @ CW 16 dBm TXHP pin connected, TXHP mode PA_DEGEN_ON VSMPS = 1.6 V	31	mA

Table 21. Current consumption in transmission mode, fc = 868 MHz

Parameter	Test condition	HPM	Unit
Supply current	Measurements TX @ CW 10 dBm TX pin connected, TX Mode PA_LEVEL7 = 78	10	mA
	Measurements TX @ CW 14 dBm TXHP pin connected, TXHP mode	22	mA
	Measurements TX @ CW 16 dBm TXHP pin connected, TXHP mode, VSMPS = 1.5 V, PA_DEGEN_ON	30.5	mA
	Measurements TX @ CW 20 dBm TX + TXHP pins connected VSMPS = 2 V, PA_DEGEN_ON	80	mA

Table 22. Current consumption in transmission mode, fc = 915 MHz

Parameter	Test condition	HPM	Unit
Supply current	Measurements TX @ CW 10 dBm TX pin connected, TX Mode	10.5	mA
	Measurements TX @ CW 14 dBm TXHP pin connected, TXHP mode	22	mA
	Measurements TX @ CW 16 dBm TXHP pin connected, TXHP mode, VSMPS = 1.5 V PA_DEGEN_ON	30.5	mA
	Measurements TX @ CW 20 dBm TX+TXHP pin connected, TX+TXHP mode, VSMPS = 2.2 V PA_DEGEN_ON	80	mA

Table 23. RF state transition times

Parameter	Test condition	Typ.	Unit
RADIO ENABLE to TX time	Including PLL calibration	111	µs
RADIO ENABLE to RX time	Including PLL calibration	101	µs
RX to TX	Including PLL calibration	87	µs
TX to RX	Including PLL calibration	102	µs

Table 24. General characteristics

Parameter		Typ.	Unit
Frequency range		413-479	MHz
		826-958	MHz
Symbol rate	2-(G)FSK	0.1-300	ks/s
	4-(G)FSK	0.1-300	ks/s
	OOK/ASK	0.1-125	ks/s
Symbol rate accuracy		±100	ppm
Frequency deviation FDEV		0.15 - 500	kHz

If "Manchester" or "3-out-of-6" or FEC coding options are enabled the actual bit rate is affected as follows:

Table 25. Data rate with different coding options

Coding option	2GFSK[kbit/s]	4GFSK[kbit/s]
NRZ	300	600
FEC	150	300
Manchester	150	Not supported
3-out-of-6	200	Not supported

6.3.5 RF receiver

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to 25°C temperature, VBAT = 3.3 V, no frequency offset in the RX signal.

All performance figures are referred to the reference designs optimized for each different configuration. The reference designs associated with each configuration are listed below:

- 433 MHz: STDES-WL3C4SML
- 868 MHz: STDES-WL3C4SMH
- 915 MHz: STDES-WL3C4SHH

Two reference test conditions are used in the RX measurements: High performance mode (HPM), where the priority is given to the performances, Low power mode (LPM) where the priority is given to the low consumption.

- High performance mode (HPM) conditions: V_{DD} = 3.3V, T_A = 25^o C, SMPS ON, SMPS frequency 4 MHz (unless otherwise stated), SMPS V_{out} =1.4V, 16 MHz system clock, HSIPLL mode, HSE GMC setting 0x0A.
- Low power mode (LPM) conditions: SMPS ON, SMPS frequency 4MHz (unless otherwise stated), SMPS V_{out} =1.2V, LDO RF bypassed, 16 MHz system clock, HSE direct mode, HSE GMC setting 0x0A.

RX blocking and selectivity tests are performed in ETSI conditions: the wanted signal is 3 dB higher than the ETSI sensitivity, given by the following formula:

$$ETSI\_sensitivity = 10 \log CHF_{kHz} - 117\ dBm$$

Table 26. RF receiver characteristics

Parameter	Description		Typical value	Unit
Receiver channel bandwidth range	-		1.8-1100	kHz
Rx maximum power	RF input power in RX operation mode		10	dBm
Input third order intercept point	Interferers are continuous wave @ 6 MHz and 12 MHz offset from carrier	433 MHz	-19	dBm
		868 MHz	-19	
Input impedance at LNA	Max. RX gain R // C	433 MHz	151-j103	Ω
		868 MHz	51-j107	

Table 27. Sensitivity at 433 MHz (SMPS clock frequency= 4 MHz)

Parameter	Test condition	SMPS OFF		HPM/LPM SMPS ON		Unit
		0.1% BER	1% BER	0.1% BER	1% BER	
Sensitivity BER @ 2-GFSK, BT = 0.5	DR = 0.3 kbit/s, FDEV = 0.25 kHz, CHF = 1.7 kHz AFC ON	-128	-130	-128	-130	dBm
	DR = 1.2 kbit/s, FDEV = 1.2 kHz, CHF = 4 kHz	-124	-126	-124	-126	
	DR = 38.4 kbit/s, FDEV = 20 kHz, CHF = 74.8 kHz	-112	-114	-112	-114	
	DR = 38.4 kbit/s, FDEV = 20 kHz, CHF = 100 kHz (TX pin mode and 10 dBm BOM)	-111.5	-113.5	-111.5	-113.5	
	DR = 38.4 kbit/s, FDEV = 20 kHz, CHF = 100 kHz (TXHP mode and 16 dBm BOM)	-111	-113	-111	-113	
	DR = 300 kbit/s, FDEV = 150 kHz, CHF = 780 kHz	-102	-104	-102	-104	
Sensitivity BER @ 4-GFSK, BT = 0.5	DR = 4.8 ks/s, DEV = 2.4 kHz, CHF = 10 kHz	-112	-115	-112	-115	dBm
	DR = 9.6 ks/s, DEV = 4.8 kHz, CHF = 20 kHz	-109	-112	-109	-112	
	DR = 19.2 ks/s, DEV = 9.6 kHz, CHF = 40 kHz	-106	-109	-106	-109	
	DR = 300 ks/s, DEV = 300 kHz, CHF = 900 kHz	-97	-100	-97	-100	
Sensitivity BER @ OOK	DR = 0.3 kbit/s, CHF = 1.7 kHz	-129	-132	-129	-132	dBm
	DR = 1.2 kbit/s, CHF = 4 kHz	-124	-127	-124	-127	
	DR = 38.4 kbit/s, CHF = 120 kHz	-109	-112	-109	-112	
	DR = 125 kbit/s, CHF = 400 kHz	-103	-106	-103	-106	

Table 28. Blocking, selectivity and saturation at 433 MHz (SMPS clock frequency= 4 MHz)

Parameter	Test condition	HPM	LPM	Unit
Selectivity and blocking 0.1% BER @ 2-GFSK, BT = 0.5, FDEV=1.2 kHz, DR = 1.2 kbit/s, CHF = 4 kHz. Wanted signal = ETSI sensitivity + 3 dB = -108 dBm. Not modulated interferer signal.	+12.5 kHz (adjacent channel)	-40	-42	dBm
	-12.5 kHz (adjacent channel)	-41	-43	
	+25 kHz (alternate channel)	-40	-43	
	-25 kHz (alternate channel)	-40	-43	
	Image rejection	-47	-47	
	+2 MHz	-24	-24	
	-2 MHz	-29	-29	
	±10 MHz	-17	-18	
	±15 MHz	-16	-16	
Selectivity and blocking 0.1% BER @ 2-GFSK, BT = 0.5, FDEV = 20 kHz , DR = 38.4 kbit/s, CHF = 100 kHz. Wanted signal = ETSI sensitivity + 3 dB = -94 dBm. Not modulated interferer signal.	+100 kHz (adjacent channel)	-38	-42	dBm
	-100 kHz (adjacent channel)	-38	-42	
	+200 kHz (alternate channel)	-38	-41	
	-200 kHz (alternate channel)	-44	-44	
	Image rejection Offset = -600 kHz	-38	-39	

Parameter	Test condition	HPM	LPM	Unit
Selectivity and blocking 0.1% BER @ 2-GFSK, BT = 0.5, FDEV = 20 kHz , DR = 38.4 kbit/s, CHF = 100 kHz. Wanted signal = ETSI sensitivity + 3 dB = -94 dBm. Not modulated interferer signal.	±2 MHz	-23	-23	dBm
	±10 MHz	-16	-17	
	±15 MHz	-16	-16	
ETSI saturation at adjacent channel 0.1% BER @ 2-GFSK, BT = 0.5, FDEV = 1.2 kHz, DR = 1.2 kbit/s, CHF = 4 kHz.	Wanted signal = -68 dBm Offset = ±25 kHz (adjacent channel)	-3	-6	dBm
ETSI saturation at adjacent channel 0.1%. BER @ 2-GFSK, BT = 0.5, FDEV = 20 kHz , DR = 38.4 kbit/s, CHF = 100 kHz.	Wanted signal = - 54 dBm Offset = ±100 kHz (adjacent channel)	-3	-6	dBm

Table 29. Sensitivity at 868.5 MHz (SMPS clock frequency = 4.27 MHz)

Parameter	Test condition(1)	SMPS OFF		HPM/LPM SMPS ON		Unit
		0.1% BER	1% BER	0.1% BER	1% BER	
Sensitivity BER @ 2-GFSK, BT = 0.5	DR = 0.3 kbit/s, FDEV = 0.25 kHz, CHF = 1.7 kHz	-126	-128	-126	-128	dBm
	DR = 1.2 kbit/s, FDEV = 1.2 kHz, CHF = 4 kHz	-122	-124	-122	-124	
	DR = 38.4 kbit/s, FDEV = 20 kHz, CHF = 74.8 kHz	-110	-112	-110	-112	
	DR = 38.4 kbit/s, FDEV = 20 kHz, CHF = 100 kHz (TX pin connected 10 dBm BOM)	-110	-112	-110	-112	
	DR = 38.4 kbit/s, FDEV = 20 kHz, CHF = 100 kHz (TXHP pin connected and 16 dBm BOM)	-109	-111	-109	-111	
	DR = 300 kbit/s, FDEV = 150 kHz, CHF = 780 kHz	-101	-103	-101	-103	
Sensitivity BER @ 4-GFSK, BT = 0.5	DR = 4.8 ks/s, DEV = 2.4 kHz, CHF = 10 kHz	-111	-114	-111	-114	
	DR = 9.6 ks/s, DEV = 4.8 kHz, CHF = 20 kHz	-108	-111	-108	-111	
	DR = 19.2 ks/s, DEV = 9.6 kHz, CHF = 40 kHz	-105	-108	-105	-108	
	DR = 300 ks/s, DEV = 300 kHz, CHF = 900 kHz	-96	-99	-96	-99	
Sensitivity BER @ OOK	DR = 0.3 kbit/s, CHF = 1.7 kHz	-128	-131	-128	-131	
	DR = 1.2 kbit/s, CHF = 4 kHz	-122	-125	-122	-125	
	DR = 38.4 kbit/s, CHF = 120 kHz	-107	-110	-107	-110	
	DR = 125 kbit/s, CHF = 400 kHz	-102	-105	-102	-105	

1. *For optimal results in 868 MHz sensitivity tests, the KRM feature needs to be used.*

Table 30. **Blocking, selectivity and saturation at 868 MHz (SMPS clock frequency = 4.27 MHz)**

<table>
<tr><th>Parameter</th><th>Test condition</th><th>HPM</th><th>LPM</th><th>Unit</th></tr>
<tr><td rowspan="9">Selectivity and blocking 0.1% BER @ 2-GFSK, BT = 0.5, DR = 1.2 kbit/s, FDEV = 1.2 kHz, CHF = 4 kHz.
Wanted signal = ETSI sensitivity + 3 dB = -108 dBm
Not modulated interferer signal.</td><td>+12.5 kHz (adjacent channel)</td><td>-44</td><td>-46</td><td rowspan="9">dBm</td></tr>
<tr><td>-12.5 kHz (adjacent channel)</td><td>-44</td><td>-47</td></tr>
<tr><td>+25 kHz (alternate channel)</td><td>-43</td><td>-48</td></tr>
<tr><td>-25 kHz (alternate channel)</td><td>-44</td><td>-48</td></tr>
<tr><td>Image rejection
Offset = -600 kHz</td><td>-46</td><td>-46</td></tr>
<tr><td>+2 MHz</td><td>-26</td><td>-25</td></tr>
<tr><td>-2 MHz</td><td>-29</td><td>-30</td></tr>
<tr><td>±10 MHz</td><td>-22</td><td>-24</td></tr>
<tr><td>±15 MHz</td><td>-17</td><td>-17</td></tr>
<tr><td rowspan="8">Selectivity and blocking 0.1%.
BER @ 2-GFSK, BT = 0.5, FDEV = 20 kHz, DR = 38.4 kbit/s, CHF = 100 kHz, channel separation 100 kHz.
Wanted signal = ETSI sensitivity + 3 dB = -94 dBm,
Not modulated interferer signal.</td><td>+100 kHz (adjacent channel)</td><td>-43</td><td>-48</td><td rowspan="8">dBm</td></tr>
<tr><td>-100 kHz (adjacent channel)</td><td>-43</td><td>-48</td></tr>
<tr><td>+200 kHz (alternate channel)</td><td>-43</td><td>-46</td></tr>
<tr><td>-200 kHz (alternate channel)</td><td>-44</td><td>-45</td></tr>
<tr><td>Image rejection
Offset = -600 kHz</td><td>-41</td><td>-41</td></tr>
<tr><td>±2 MHz</td><td>-26</td><td>-27</td></tr>
<tr><td>±10 MHz</td><td>-19</td><td>-21</td></tr>
<tr><td>±15 MHz</td><td>-16</td><td>-17</td></tr>
<tr><td>ETSI saturation at adjacent channel 0.1% BER @ 2-GFSK, BT = 0.5, FDEV = 1.2 kHz, DR = 1.2 kbit/s, CHF = 4 kHz.</td><td>Wanted signal = -68 dBm
Offset = ±25 kHz (adjacent channel)</td><td>-5</td><td>-9</td><td>dBm</td></tr>
<tr><td>ETSI saturation at adjacent channel 0.1% BER @ 2-GFSK, BT = 0.5 20 kHz FDEV, DR = 38.4 kbit/s, CHF = 100 kHz.</td><td>Wanted signal = - 54 dBm
Offset = ±100 kHz (adjacent channel)</td><td>-4</td><td>-8</td><td>dBm</td></tr>
</table>

Table 31. Sensitivity at 915 MHz (SMPS clock frequency= 4 MHz)

Parameter	Test condition	SMPS OFF		HPM/LPM SMPS ON		
		0.1% BER	1% BER	0.1% BER	1% BER	
Sensitivity 0.1% BER @ 2-GFSK, BT = 0.5	DR = 0.3 kbit/s, FDEV = 0.25 kHz, CHF = 1.7 kHz	-126	-128	-126	-128	dBm
	DR = 1.2 kbit/s, FDEV = 1.2 kHz, CHF = 4 kHz	-122	-124	-122	-124	
	DR = 38.4 kbit/s, FDEV = 20 kHz, CHF = 74.8 kHz	-110	-112	-110	-112	
	DR = 38.4 kbit/s, FDEV = 20 kHz, CHF = 100 kHz	-109	-111	-109	-111	
	DR = 300 kbit/s, FDEV = 150 kHz, CHF = 780 kHz	-100	-102	-100	-102	
Sensitivity 0.1% BER @ 4-GFSK BT = 0.5	DR = 4.8 ks/s, DEV = 2.4 kHz, CHF = 10 kHz	-110	-113	-110	-113	dBm
	DR = 9.6 ks/s, DEV = 4.8 kHz, CHF = 20 kHz	-107	-110	-107	-110	
	DR = 19.2 ks/s, DEV = 9.6 kHz, CHF = 40 kHz	-104	-107	-104	-107	
	DR = 300 ks/s, DEV = 300 kHz, CHF = 900 kHz	-96	-99	-96	-99	
Sensitivity 0.1% BER @ OOK	DR = 0.3 kbit/s, CHF = 1.7 kHz	-128	-131	-128	-131	dBm
	DR = 1.2 kbit/s, CHF = 4 kHz	-122	-125	-122	-125	
	DR = 38.4 kbit/s, CHF = 120 kHz	-107	-110	-107	-110	
	DR = 125 kbit/s, CHF = 400 kHz	-102	-105	-102	-105	

Table 32. Blocking, selectivity and saturation at 915 MHz

Parameter	Test condition	HPM	LPM	Unit
Selectivity and blocking 0.1% BER @ 2-GFSK, BT = 0.5, FDEV = 1.2 kHz , DR = 1.2 kbit/s, CHF = 4 kHz Wanted signal = ETSI sensitivity + 3 dB = -108 dBm. Not modulated interferer signal.	+12.5 kHz (adjacent channel)	-45	-49	dB
	-12.5 kHz (adjacent channel)	-45	-49	
	+25 kHz (alternate channel)	-45	-51	
	-25 kHz (alternate channel)	-45	-51	
	Image rejection Offset = - 600 kHz	-52	-52	
	+2 MHz	-29	-29	
	-2 MHz	-30	-30	
	±10 MHz	-19	-20	
	±15 MHz	-17	-18	
Selectivity and blocking 0.1% BER @ 2-GFSK, BT = 0.5, FDEV = 20 kHz, DR = 38.4 kbit/s, CHF = 100 kHz. Wanted signal = ETSI sensitivity + 3 dB = -94 dBm Not modulated interferer signal.	+100 kHz (adjacent channel)	-44	-50	dB
	-100 kHz (adjacent channel)	-44	-50	
	+200 kHz (alternate channel)	-45	-47	
	-200 kHz (alternate channel)	-45	-48	
	Image rejection Offset = -600 kHz	-41	-42	
	±2 MHz	-26	-26	
	±10 MHz	-18	-19	
	±15 MHz	-17	-17	
ETSI saturation at adjacent channel 0.1% BER @ 2-GFSK, BT = 0.5, FDEV 1.2 kHz, DR = 1.2 kbit/s, CHF = 4 kHz.	Wanted signal = -68 dBm Offset = ±25 kHz (adjacent channel)	-8	-12	dBm
ETSI saturation at adjacent channel 0.1% BER @ 2-GFSK, BT = 0.5, FDEV = 20 kHz , DR = 38.4 kbit/s, CHF = 100 kHz.	Wanted signal = -54 dBm Offset = ±100 kHz (adjacent channel)	-7	-11	dBm

6.3.6 RF transmitter

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to a temperature of 25 °C, V_{BAT} = 3.3 V. All performance data is referred to the reference design with a 50-ohm antenna connector.

Transmission measurements are performed for V_{DD} = 3.3 V, T_A = 25 °C, SMPS ON, SMPS frequency 4 MHz, SMPS V_{out} value dependent on the desired output power =1.4V, 16 MHz system clock, HSIPLL mode, HSE GMC setting 0x0A

TX measurements are given for HPM test conditions:

V_{DD} = 3.3 V, T_A = 25^{o} C, SMPS ON, SMPS frequency 4 MHz (unless otherwise stated), SMPS V_{out} according to output power, 16 MHz system clock, HSI mode.

Table 33. **RF transmitter characteristics**

Parameter	Test condition	RF power	Unit
Maximum output power	TX mode, SMPS = 2 V	14	dBm
	TX mode, SMPS = 1.4 V	10	
	TXHP mode, SMPS = 1.5 V PA_DEGEN_ON	16	
	TX+TXHP mode, SMPS = 2 V PA_DEGEN_ON	20	
Output power step (all modes)	All BOMs, all frequencies	0.5	dB

Table 34. **PA impedance**

Parameter	Test condition	Typ	Unit
Optimum load impedance	433 MHz 10 dBm, TX mode, Vsmps = 1.4 V	52 Ω // 35 nH	Ω
	433 MHz 14 dBm, TXHP mode, Vsmps = 1.4 V	37 Ω // 37 nH	
	433 MHz 16 dBm, TXHP mode, Vsmps = 1.6 V	37 Ω // 37 nH	
	868-929 MHz 10 dBm, TX mode, Vsmps = 1.4 V	40 Ω // 36 nH	
	868-929 MHz 14 dBm, TXHP mode, Vsmps = 1.4 V	32 Ω // 16 nH	
	868-929 MHz 16 dBm, TXHP mode, PA_DEGEN_ON, Vsmps = 1.5 V	44 Ω // 18 nH	
	902-928 MHz 20 dBm, TX+TXHP mode, PA_DEGEN_ON, Vsmps = 2.2 V	20 Ω // 6 nH	

Table 35. **Regulatory standards**

Frequency band	Suitable for compliance with:
413 - 479 MHz	ETSI EN300 220 category 1
	FCC part 15, FCC part 90
	ARIB STD-T67
826 - 958 MHz	ETSI EN300 220-2 category 1
	FCC part 15
	ARIB STD-T108

6.3.7 Harmonic emissions

TX measurements are given for HPM test conditions: V_{DD} = 3.3 V, T_A = 25 ^oC, SMPS ON, SMPS frequency 4 MHz, SMPS V_{out} according to output power, 16 MHz system clock, HSI mode.

- **10 dBm measurements conditions**: SMPS ON Vout = 1.4 V, Continuous Wave (CW), TX pin connected, TX mode, 10 dBm BOM.
- **16 dBm measurements conditions**: Continuous Wave (CW), TXHP pin connected, TXHP mode, 16 dBm BOM and PA_DGEN_ON:
  - 433 MHz band: SMPS ON Vout = 1.6 V
  - 868 MHz band: SMPS ON Vout = 1.5 V
  - 915 MHz band: SMPS ON Vout = 1.5 V
- **20 dBm measurement conditions**: Continuous Wave (CW), TX+TXHP pins connected, TX+TXHP mode, 20 dBm BOM, PA_DEGEN_ON and SMPS = 2 V for 868, 2.2 V for 915 MHz

6.3.7.1 Harmonic emission at 433 MHz

Table 36. Harmonic emission at 433 MHz

Parameter	Test condition	10 dBm	16 dBm	Unit
H1	As detailed above	10	16	dBm
H2	As detailed above	-57	-44	
H3	As detailed above	-44	-35	
H4	As detailed above	-56	-56	
H5	As detailed above	-63	-66	
H6	As detailed above	-61	-66	
H7	As detailed above	-53	-66	

6.3.7.2 Harmonic emission at 868 MHz

Table 37. Harmonic emission at 868 MHz

Parameter	Test condition	10dBm	16dBm	20dBm	Unit
H1	As detailed above	10	16	20	dBm
H2	As detailed above	-59	-42	-34	
H3	As detailed above	-60	-53	-43	
H4	As detailed above	-62	-62	-68	
H5	As detailed above	-60	-57	-52	
H6	As detailed above	-61	-44	-38	
H7	As detailed above	-62	-52	-68	

6.3.7.3 *Harmonic emission at 915 MHz*

Table 38. **Harmonic emission at 915 MHz**

Parameter	Test condition	10 dBm	16 dBm	20 dBm	Unit
H1	As detailed above	10	16	20	dBm
H2	As detailed above	-50	-42	-42	
H3	As detailed above	-58	-55	-52	
H4	As detailed above	-63	-59	-65	
H5	As detailed above	-61	-55	-46	
H6	As detailed above	-63	-34	-46	
H7	As detailed above	-61	-58	-68	

6.3.8 Frequency synthesizer

Characteristics measured over recommended operating conditions. All typical values are referred to 25 °C temperature, VBAT = 3.3 V, SMPS ON Vsmps = 1.4 V, SMPS clock frequency = 4 MHz, HSE ON, GMC 0x0A, WFI mode. The whole performance is referred to the reference design with a 50-ohm antenna connector.

Table 39. **Frequency synthesizer parameters**

Parameter	Test conditions	HPM	Unit
Frequency step size	For 433 MHz	5.72	Hz
	For 868-915 MHz	11.44	
RF carrier phase noise 433.5 MHz	10 kHz	-108	dBc/Hz
	100 kHz	-112	
	1 MHz	-130	
	10 MHz	-147	
RF carrier phase noise 868 MHz	10 kHz	-105	
	100 kHz	-108	
	1 MHz	-124	
	10 MHz	-142	
RF carrier phase noise 915 MHz	10 kHz	-104	
	100 kHz	-108	
	1 MHz	-121	
	10 MHz	-140	

6.3.9 High-speed external clock

The high-speed external oscillator must be supplied with an external 48 MHz crystal specified for a 6 to 8 pF loading capacitor. The STM32WL30xx includes internal programmable capacitances that can be used to tune the crystal frequency to compensate the PCB parasitic one.

These internal load capacitors are made by a fixed one, in parallel with a 6-bit binary weighted capacitor bank. Thanks to low CL step size (1-bit is typically 0.12 pF), very fine frequency tuning is possible. With typical XTAL sensitivity of -14 ppm/pF, it is possible to trim a 48 MHz crystal, with a resolution of 1 ppm (5 ppm max).

The STM32WL30xx guarantees a very low frequency drift due to 0.2 V supply variations, supporting long transmission times at low data rate.

Table 40. HSE frequency drift versus power supply drop

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{DRIFT}	Frequency drift versus power-supply variation	200 mV V_{DD} drop	-	±40	-	ppb

Table 41. HSE crystal requirements

Symbol	Parameter	Conditions(1)(2)	Min.	Typ.	Max.	Unit
f_{nom}	Oscillator frequency	-	-	48	-	MHz
f_{TOL}	Frequency accuracy	Initial accuracy at 25 °C	-	+/-10	-	ppm
		Over temperature -40 °C to +85 °C	-	+/-20	-	
		Over temperature +85 °C to +105 °C	-	+/-32	-	
		Aging over 10 years	-	+/-10	-	
ESR	Equivalent series resistance	-	-	-	80	Ω
C_{LOAD}	Load capacitance	-	-	8	-	pF
C_{shunt}	Shunt capacitance	-	-30%	0.71	30	
C_{motion}	Motional capacitance	-	-30%	2.03	30	
L_{motion}	Motional inductance	-	-30%	5.41	30	µH
P_D	Drive level	-	-	-	100	µW

1. *A 48 MHz XTAL is specified for a specific reference: NX1612SA. A 48 MHz XTAL is specified for a specific reference: NX1612SA.*
2. *For more information about the crystal selection, refer to the application note Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs (AN2867).*

Table 42. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{HSE}	OSCIN OSCOUT internal capacitor	-	6.7(1)	10.6(2)	14.33(3)	pF
$C_{HSEstep}$	OSCIN OSCOUT internal capacitor granularity 1-bit value	V_{BAT} = 3.3 V 27 °C, XOTUNE code between 32 and 33	-	0.12	-	pF
HSE start-up time	Startup time for amplitude stabilization	From HSE enable to amplitude ready	-	155	-	µs
G_m	Programmable trans-conductance of the oscillator at start-up	$I_{STARTUP}$ = 00	-	5.1	-	mS
		$I_{STARTUP}$ = 01	-	10.2	-	
		$I_{STARTUP}$ = 10	-	20.4	-	

1. *XOTUNE programmed at minimum code = 0*
2. *XOTUNE programmed at center code = 32*
3. *XOTUNE programmed at maximum code = 63*

6.3.10 Low speed external clock

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. The information provided in this section is based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time.

Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

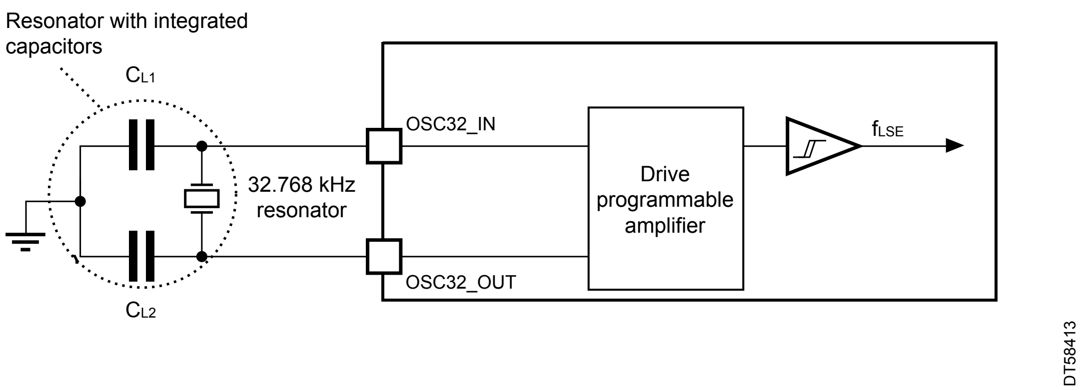
Table 43. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] =00 - Low drive capability	-	250	-	nA
		LSEDRV[1:0] =01 - Medium-low drive capability	-	315	-	
		LSEDRV[1:0] =10 - Medium-high drive capability	-	500	-	
		LSEDRV[1:0] =11 - High drive capability	-	630	-	
$G_{mcritmax}$	Maximum critical crystal gm	LSEDRV[1:0] =00 - low drive capability	-	-	0.50	µA/V
		LSEDRV[1:0] =01 - medium-low drive capability	-	-	0.75	
		LSEDRV[1:0] =10 - medium-high drive capability	-	-	1.70	
		LSEDRV[1:0] =11 - high drive capability	-	-	2.70	
$t_{SU(LSE)}$(2)	Startup time	V_{DD} stabilized	-	2	-	s

1. *Guaranteed by design - not tested in production*
2. *$t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) until a stable 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.*

For more information onthe crystal selection, refer to application note *Oscillator design guide for STM8AF/AL/S, STM32 MCUs* and MPUs (AN2867).

Figure 10. Typical application with a 32.768 kHz crystal



Note: No external resistors are required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

In bypass mode, the LSE oscillator is switched off and the input pin is a standard GPIO. The external clocksignal has to respect the I/O characteristics detailed in Section 6.3.14: I/O port characteristics. The recommend clock input waveform is shown in the figure below.

Figure 11. Low-speed external clocksource AC timing diagram

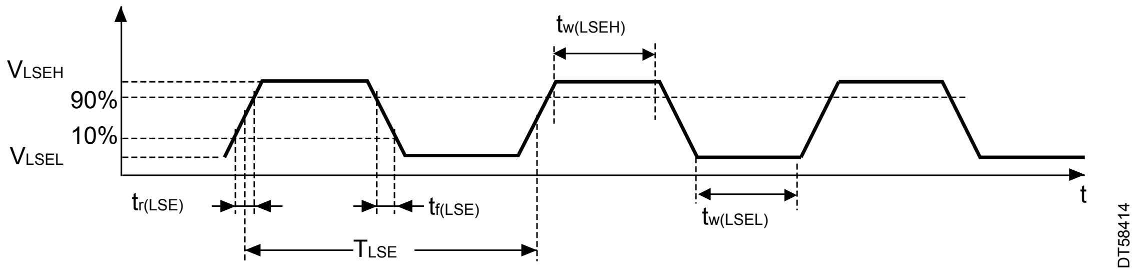


Table 44. Low-speed external user clockcharacteristics[1] – Bypass mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	21.2	32.768	44.4	kHz
V_{LSEH}	OSC32_IN input pin high- level voltage	-	0.7 x VDDx	-	V_{DDx}	V
V_{LSEL}	OSC32_IN input pin low- level voltage	-	V_{SS}	-	0.3 x V_{DDx}	V
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns
f_{tolLSE}	Frequency tolerance	Includes initialaccuracy, stability over temperature, aging and frequency pulling	–500	-	+500	ppm

1. *Guaranteed by design - not tested in production.*

6.3.11 Low-speed internal ring oscillator

Table 45. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min.[1]	Typ.[1]	Max.[1]	Unit
f_{LSI} nominal	LSI frequency	V_{DD}=3.3V T_A = 30 °C Typical corner	32.83	34.3	35.77	kHz
Δf_{LSI} / $f_{LSI(TA)}$ / T_{Range}	Frequency variation versus temperature	Standard deviation	-	140	-	ppm/ºC

1. *Evaluated by characterization - not tested in production*

6.3.12 Flash memory characteristics

The characteristics below are specified by design and not tested in production.

Table 46. Flash memory characteristics

Symbol	Parameter	Test conditions	Typ.	Max.	Unit
T_{prog}	32-bit programming time	-	20	40	µs
T_{prog_burst}	4x32-bit burst programming time	-	4x20	4x40	
t_{ERASE}	Page (2 kbyte) erase time	-	20	40	ms
t_{ME}	Mass erase time	-	20	40	
I_{DD}	Average consumption from VDD	Write mode	3	-	mA
		Erase mode	3	-	
		Mass erase	5	-	

Table 47. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min[1]	Unit
N_{END}	Endurance	TA= -40 to +105 ºC	10	kcycles
t_{RET}	Data retention	1 kcycle[2] at TA = 85 °C	30	Years
		1 kcycle[2] at TA = 105 °C	15	
		10 kcycles[2] at TA = 55 °C	30	
		10 kcycles[2] at TA = 85 °C	15	
		10 kcycles[2] at TA = 105 °C	10	

1. *Guaranteed by characterization results.*
2. *Cycling performed over the whole temperature range.*

6.3.13 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n + 1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 48. ESD absolute maximum ratings

Symbol	Parameter	Conditions	Class	Max.	Unit
VESD(HBM)	Electrostatic discharge voltage (human body model)	T_A= +25 °C, conforming to ANSI/ ESDA/JEDEC JS-001	2	2000[1]	V
VESD(CBM)	Electrostatic discharge voltage (charge device model)	T_A= +25 °C, conforming to ANSI/ ESDA/STM5.3.1 JS-002	C2a	500	

1. *TX pin can sustain 700V, TXHP pin can sustain 1000 V*

6.3.14 I/O port characteristics

Unless otherwise specified, the parameters given in the tables below are derived from tests performed under the conditions summarized in Section 6.3.1: Operating range.

Table 49. I/O static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	I/O input low level voltage	$1.62\ V < V_{DD} < 3.6\ V$	-	-	$0.3 \times V_{DD}$	V
V_{IH}	I/O input high level voltage		$0.7 \times V_{DD}$	-	-	
I_{lkg}	Input leakage current	$0 <= V_{IN} <= Max(V_{DDx})$[(1)]	-	-	±100	nA
		$Max(V_{DDx})$[(1)] $<= V_{IN} <= Max(V_{DDx})$[(1)] $+1\ V$	-	-	650	
		$Max(V_{DDx})$[(1)] $+ 1V < V_{IN} <= 5.5\ V$	-	-	200	
R_{PU}	Pull up resistor	V_{IN}=GND	25	40	55	kΩ
R_{PD}	Pull down resistor	$V_{IN}=V_{DD}$	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. *$Max(V_{DDx})$ is the maximum value among all the I/O supplies*

All I/Os are CMOS-compliant (no software configuration required).

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA and sink or source up to ±20 mA (with a relaxed V_{OL} / V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified.

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum consumption of the MCU sourced on VDD, cannot exceed the absolute maximum rating ΣIVDD.
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on GND, cannot exceed the absolute maximum rating ΣIVGND.

Table 50. Output voltage characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port[(1)] $\lvert I_{IO}\rvert = 8$ mA $V_{DD} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DD} - 0.4	-	
V_{OL}	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert = 20$ mA $V_{DD} \geq 2.7$ V	-	1.3	
V_{OH}	Output high level voltage for an I/O pin		V_{DD} - 1.3	-	
V_{OL}	Output low level voltage for an I/O pin	|IIO| = 4 mA VDD ≥ 1.62 V	-	0.4	
V_{OH}	Output high level voltage for an I/O pin		V_{DD} - 0.45	-	

1. *CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.*

6.3.15 RSTN pin characteristics

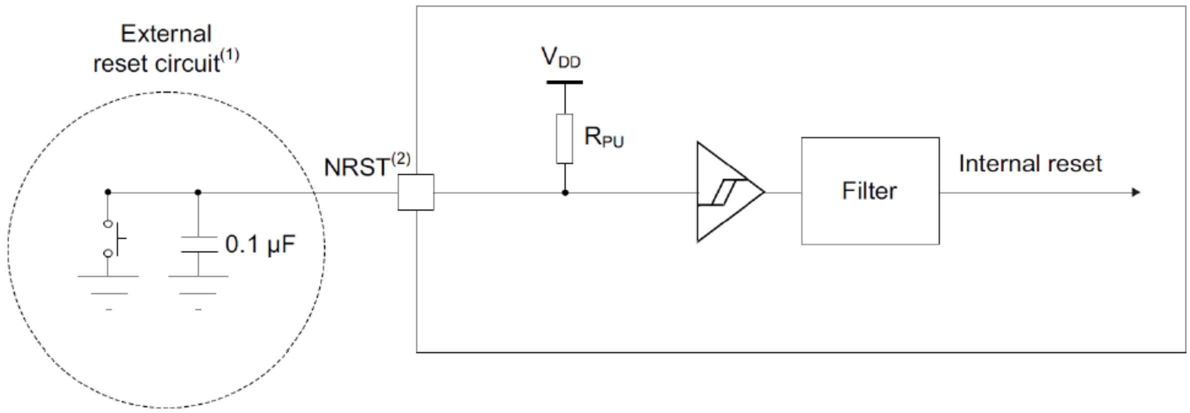
The RSTN pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, RPU.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 6.3.1: Operating range.

Table 51. **RSTN pin characteristics (specified by design - not tested in production)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(RSTN)}$	RSTN input low level voltage	-	-	-	0.3 x V_{DD}	V
$V_{IH(RSTN)}$	RSTN input high level voltage	-	0.7 x V_{DD}	-	-	
$V_{hys(RSTN)}$	RSTN Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull up equivalent resistor	V_{IN}=GND	25	40	55	kΩ

Figure 12. **Recommended RSTN pin protection**



Note:
- *The reset network protects the device against parasitic resets.*
- *The user must ensure that the level on the RSTN pin can go below the $V_{IL(RSTN)}$ maximum level specified in Table 51, otherwise the reset is not taken into account by the device.*
- *The external capacitor on RSTN must be placed as close as possible to the device.*

6.3.16 Timer characteristics

Table 52. **TIM2/16 characteristics**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$ = 64 MHz	-	15.625	-	ns
Res_{TIM}	Timer resolution		-	16	-	bit
$t_{COUNTER}$	16-bit counter clock period	$f_{TIMxCLK}$ = 64 MHz	0.015625	-	1024	µs
t_{MAX_COUNT}	Maximum possible count time	$f_{TIMxCLK}$ = 64 MHz	-	-	67.10	s

Table 53. IWDG min/max timeout period at 32 kHz (LSE)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0] = 0x000	Max timeout RL[11:0] = 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

6.3.17 SPI characteristics

The parameters given in Table 54 for SPI are derived from tests performed according to fPCLKx frequency and supply voltage conditions summarized in Table 10. Operating range.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Table 54. SPI characteristics

Symbol	Parameter[1]	Conditions	Min.	Typ.	Max.	Units
f_{SCK}	SPI clock frequency	Master mode	-	-	32	MHz
		Slave mode			32[1]	
$t_{su(NSS)}$	NSS setup time	-	4 / f_{PCLK}	-	-	-
$t_{h(NSS)}$	NSS hold time	-	2 / f_{PCLK}	-	-	-
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	1/ f_{PCLK} -1.5	1/ f_{PCLK}	1/ f_{PCLK} + 1	-
$t_{su(MI)}$	Data input setup time	Master mode	1	-	-	ns
$t_{su(SI)}$	Data input setup time	Slave mode	1	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	3	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	5	-	40	
$t_{dis(SO)}$	Data output disable time		5	-	38	
$t_{v(MO)}$	Data output valid time	Master mode	-	2	8	
$t_{v(SO)}$		Slave mode	-	12	39	
$t_{h(MO)}$	Data output hold time	Master mode	2	-	-	
$t_{h(SO)}$		Slave mode	4	-	-	

1. *Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$, which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved .*

Figure 13. SPI timing diagram - slave mode and CPHA = 0

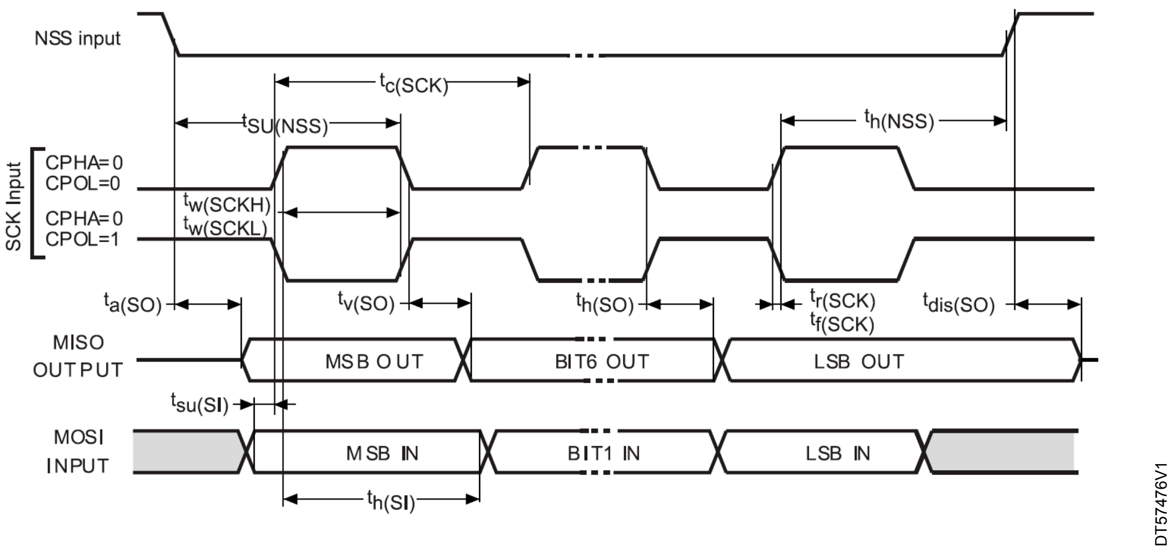


Figure 14. SPI timing diagram - slave mode and CPHA = 1

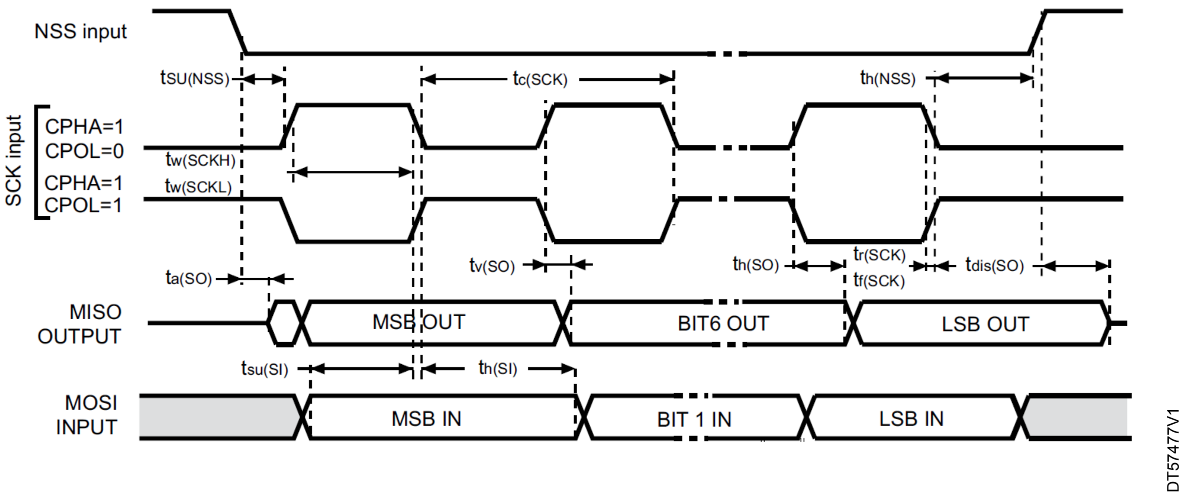
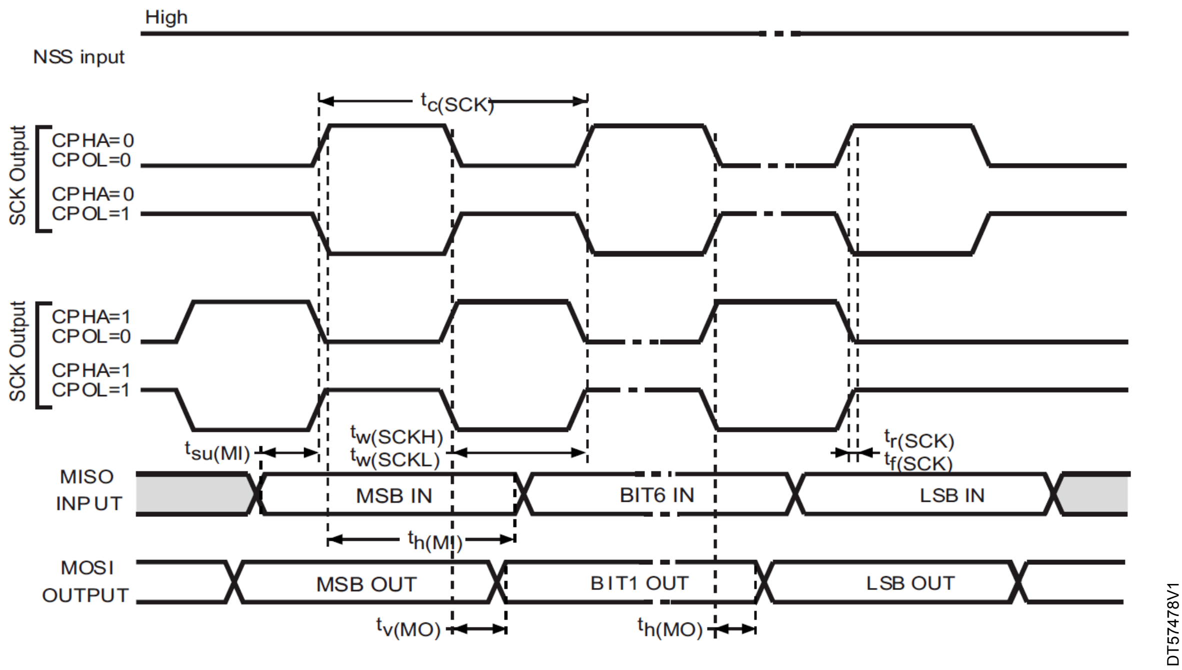


Figure 15. SPI timing diagram - master mode



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK2 packages, depending on their level of environmental compliance. ECOPACK2 specifications, grade definitions, and product status are available at: www.st.com. ECOPACK2 is an ST trademark.

7.1 Device marking

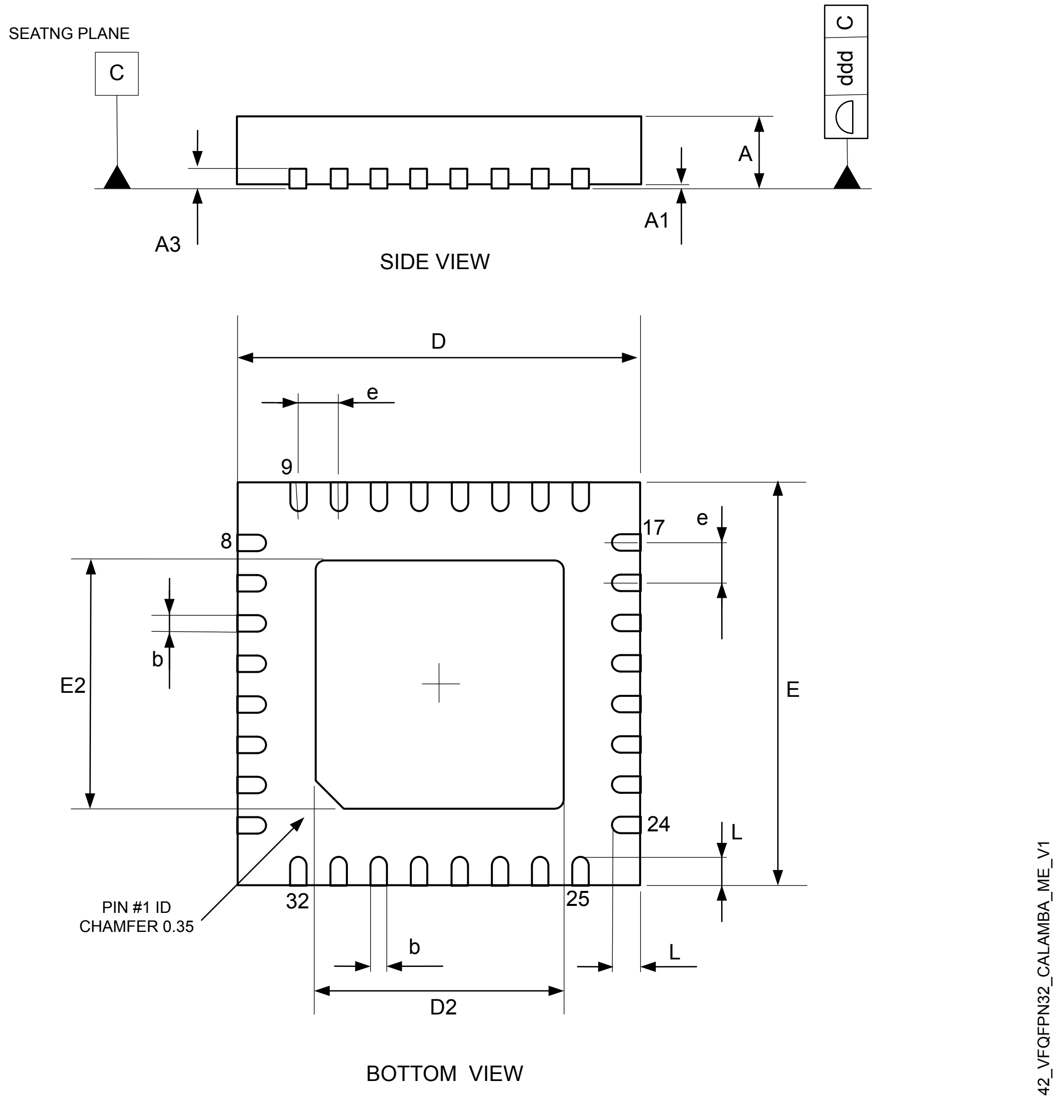
Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on http://www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.2 VFQFPN32 package information (42)

This VFQFPN is a 32 lead, 5 x 5 mm, 0.50 mm pitch, very fine pitch quad flat no lead package.

Figure 16. VFQFPN32 - Outline



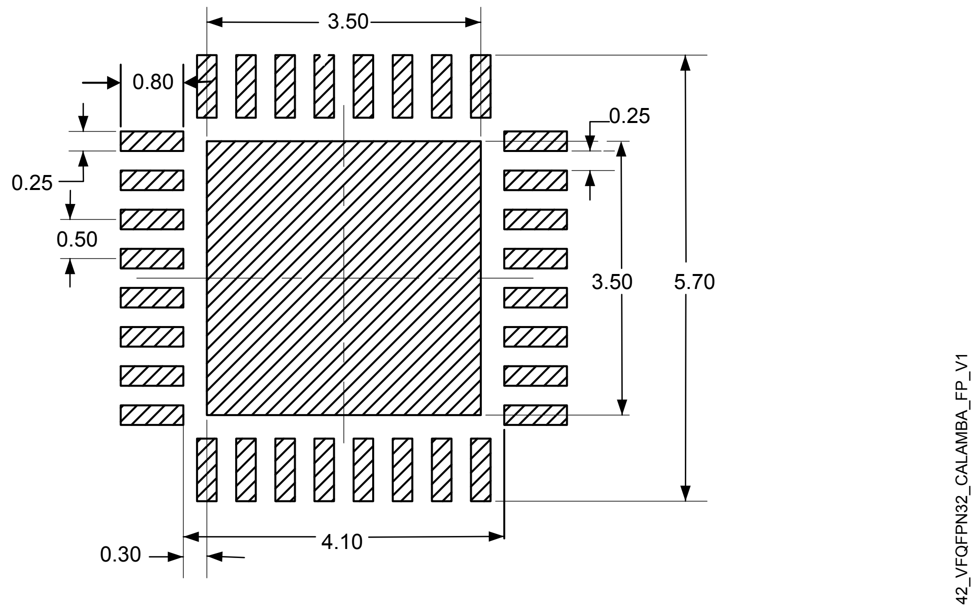
1. *Drawing is not to scale.*
2. *Package outline exclusive of any mold flashes dimensions and metal burrs.*
3. *Details of terminal 1 are optional but must be located on the top surface of the package by using either a mold or marked features.*

Table 55. VFQFPN32 - Mechanical data

Symbol	Millimetres			Inches(1)		
	Min	Typ	Max	Min	Typ	Max
A(2)	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	-	0.05	0	-	0.0020
A3	-	0.20	-	-	0.008	-
b	0.18	0.25	0.30	0.0070	0.0098	0.0118
D	4.90	5.00	5.10	0.1929	0.19	0.2008
E	4.90	5.00	5.10	0.1929	0.19	0.2008
D2	3.60	3.70	3.80	0.1417	0.1457	0.1496
E2	3.60	3.70	3.80	0.1417	0.1457	0.1496
e	-	0.50	-	-	0.0197	-
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
ddd	-	-	0.05	-	-	0.0020

1. *Values in inches are converted from mm and rounded to 3 decimal digits.*
2. *VFQFPN stands for thermally Enhanced very thin fine pitch quad flat package No lead . Very thin profile 0.80 < A ≤ 1.00 mm.*

Figure 17. VFQFPN32 - Footprint example



8 Ordering information

Table 56. Ordering information scheme

Example:	STM32	WL	30	K	C	V	6	TR

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

WL = wireless long-range

Device subfamily

30 = Modem line

Pin count

K = 32

Memory configuration

8 = 64 Kbyte flash/8 Kbyte RAM

B = 128 Kbyte flash/16 Kbyte RAM

Package(1)

V = VFQFPN

Temperature range

6 = -40 °C up to +85 °C

7 = -40 °C up to +105 °C

Frequency band options

No character = 413-479 MHz and 868-958 MHz

Packing

TR = tape and reel

1. *ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimony oxide flame retardants).*

Important security notice

The STMicroelectronics group of companies (ST) places a high value on product security, which is why the ST product(s) identified in this documentation may be certified by various security certification bodies and/or may implement our own security measures as set forth herein. However, no level of security certification and/or built-in security measures can guarantee that ST products are resistant to all forms of attacks. As such, it is the responsibility of each of ST's customers to determine if the level of security provided in an ST product meets the customer needs both in relation to the ST product alone, as well as when combined with other components and/or software for the customer end product or application. In particular, take note that:

- ST products may have been certified by one or more security certification bodies, such as Platform Security Architecture (www.psacertified.org) and/or Security Evaluation standard for IoT Platforms (www.trustcb.com). For details concerning whether the ST product(s) referenced herein have received security certification along with the level and current status of such certification, either visit the relevant certification standards website or go to the relevant product page on www.st.com for the most up to date information. As the status and/or level of security certification for an ST product can change from time to time, customers should re-check security certification status/level as needed. If an ST product is not shown to be certified under a particular security standard, customers should not assume it is certified.
- Certification bodies have the right to evaluate, grant and revoke security certification in relation to ST products. These certification bodies are therefore independently responsible for granting or revoking security certification for an ST product, and ST does not take any responsibility for mistakes, evaluations, assessments, testing, or other activity carried out by the certification body with respect to any ST product.
- Industry-based cryptographic algorithms (such as AES, DES, or MD5) and other open standard technologies which may be used in conjunction with an ST product are based on standards which were not developed by ST. ST does not take responsibility for any flaws in such cryptographic algorithms or open technologies or for any methods which have been or may be developed to bypass, decrypt or crack such algorithms or technologies.
- While robust security testing may be done, no level of certification can absolutely guarantee protections against all attacks, including, for example, against advanced attacks which have not been tested for, against new or unidentified forms of attack, or against any form of attack when using an ST product outside of its specification or intended use, or in conjunction with other components or software which are used by customer to create their end product or application. ST is not responsible for resistance against such attacks. As such, regardless of the incorporated security features and/or any information or support that may be provided by ST, each customer is solely responsible for determining if the level of attacks tested for meets their needs, both in relation to the ST product alone and when incorporated into a customer end product or application.
- All security features of ST products (inclusive of any hardware, software, documentation, and the like), including but not limited to any enhanced security features added by ST, are provided on an "AS IS" BASIS. AS SUCH, TO THE EXTENT PERMITTED BY APPLICABLE LAW, ST DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, unless the applicable written and signed contract terms specifically provide otherwise.

Revision history

Table 57. Document revision history

Date	Version	Changes
17-Feb-2025	1	Initial release.

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