4.2V TO 18V INPUT, 2A LOW IQ SYNCHRONOUS BUCK CONVERTER

Description

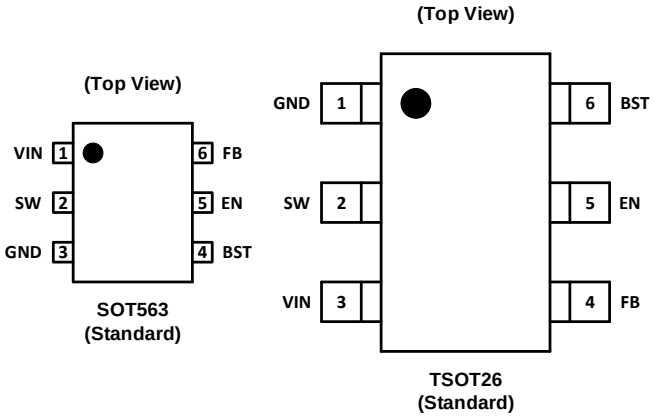
The AP62200/AP62201/AP62200T is a 2A, synchronous buck converter with a wide input voltage range of 4.2V to 18V. The device fully integrates a 90mΩ high-side power MOSFET and a 65mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

The AP62200/AP62201/AP62200T device is easily used by minimizing the external component count due to its adoption of Constant On-Time (COT) control to achieve fast transient response, easy loop stabilization, and low output voltage ripple.

The AP62200/AP62201/AP62200T design is optimized for Electromagnetic Interference (EMI) reduction. The device has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching.

The AP62200/AP62201 is available in SOT563 (Standard) and TSOT26 (Standard) packages. The AP62200T is available in a TSOT26 (Standard) package.

Pin Assignments



Features

- VIN: 4.2V to 18V
- Output Voltage (VOUT): 0.8V to 7V
- 2A Continuous Output Current
- 0.8V ± 1% Reference Voltage (T_A = +25°C)
  - AP62200 and AP62201
- 0.763V ± 1% Reference Voltage (T_A = +25°C)
  - AP62200T
- 135μA Low Quiescent Current (Pulse Frequency Modulation)
- 750kHz Switching Frequency (VIN = 12V, VOUT = 5V)
- Up to 84% Efficiency at 5mA Light Load
- Proprietary Gate Driver Design for Best EMI Reduction
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Cycle-by-Cycle Valley Current Limit
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- 5V and 12V distributed power bus supplies
- Flat screen TV sets and monitors
- White goods and small home appliances
- FPGA, DSP, and ASIC supplies
- Home audio
- Network systems
- Gaming consoles
- Consumer electronics
- General purpose point of load

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Application Circuit

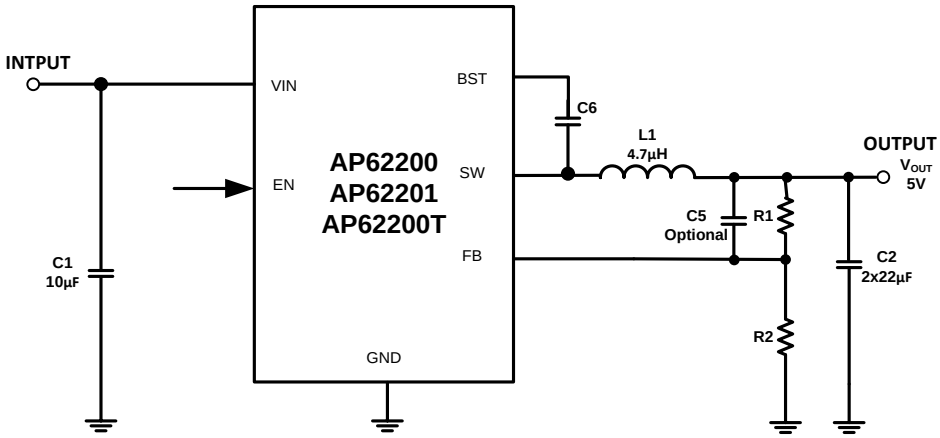


Figure 1. Typical Application Circuit

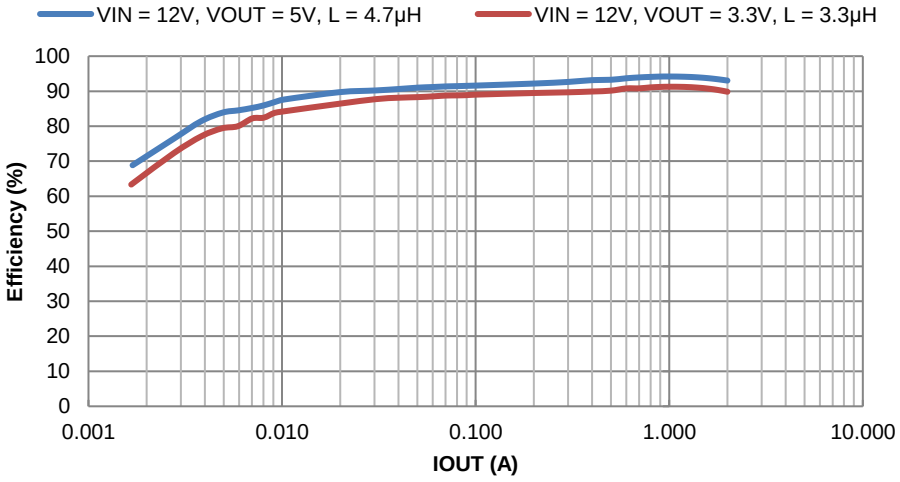


Figure 2. Efficiency vs. Output Current, AP62200/AP62200T

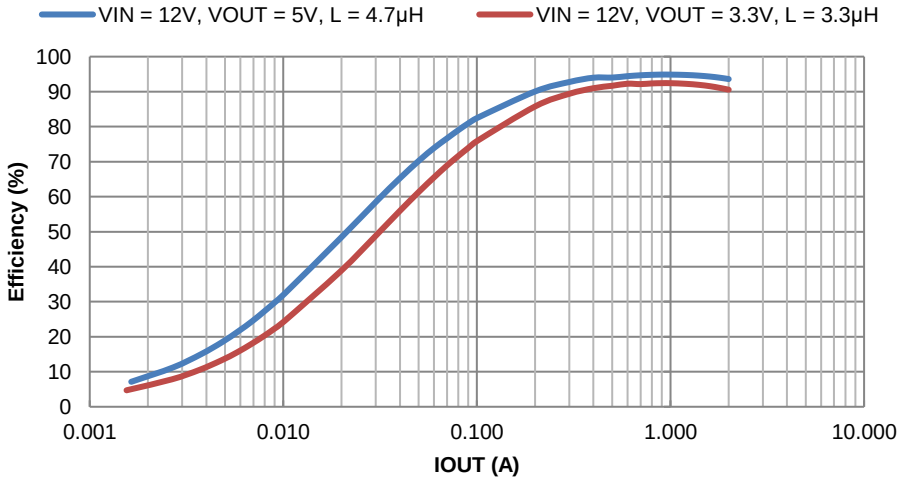


Figure 3. Efficiency vs. Output Current, AP62201

Pin Descriptions

Pin Name	Pin Number		Function
	SOT563 (Standard)	TSOT26 (Standard)	
VIN	1	3	Power Input. VIN supplies the power to the IC as well as the step-down converter power MOSFETs. Drive VIN with a 4.2V to 18V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See **Input Capacitor** section for more details.
SW	2	2	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
GND	3	1	Power Ground.
BST	4	6	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-Channel MOSFET. A 100nF capacitor is recommended from BST to SW to power the high-side driver.
EN	5	5	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Leave floating for automatic startup. The EN has a precision threshold of 1.2V for programing the UVLO. See **Enable** section for more details.
FB	6	4	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See **Setting the Output Voltage** section for more details.

Functional Block Diagram

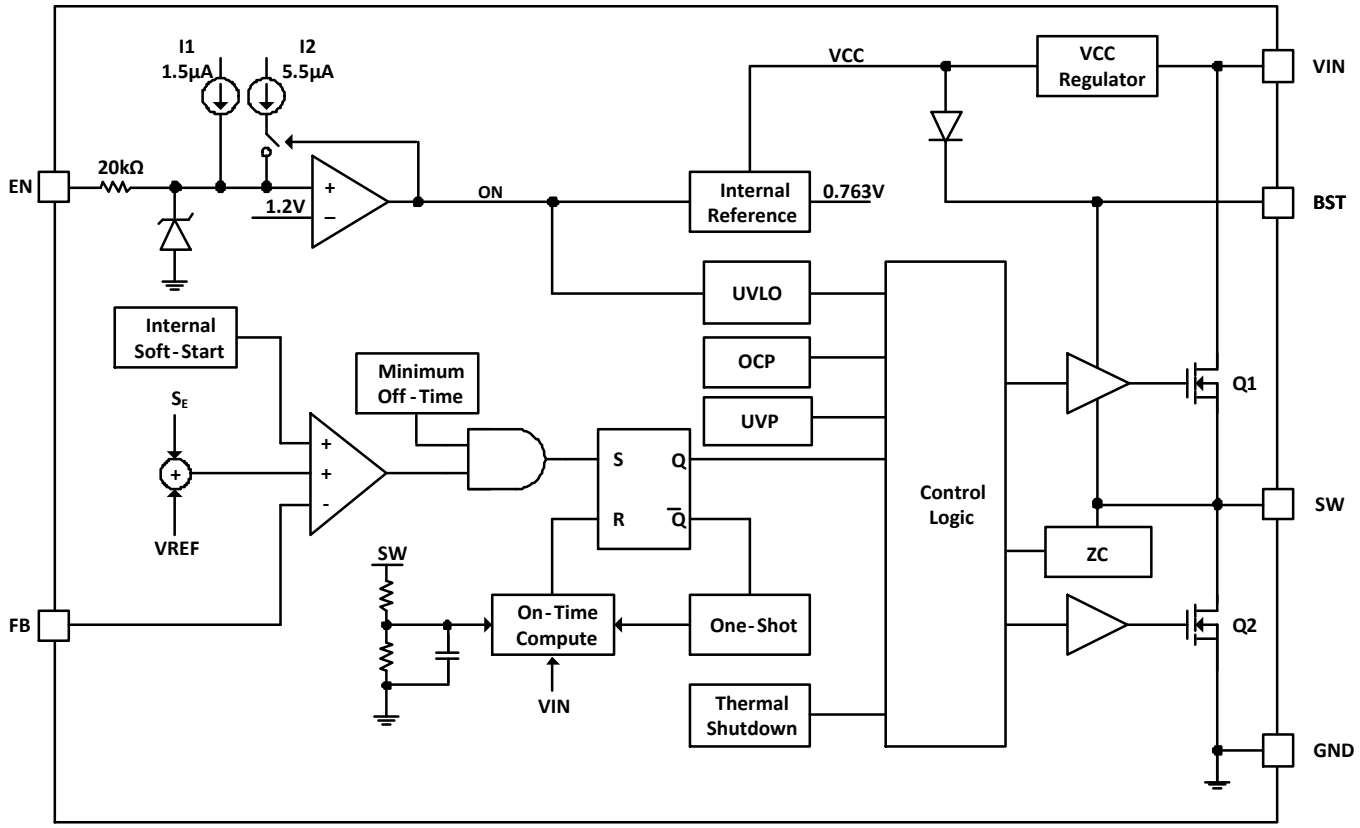


Figure 4. Functional Block Diagram

Absolute Maximum Ratings (Note 4) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +20.0 (DC)	V
		-0.3 to +22.0 (400ms)	
V_{SW}	Switch Pin Voltage	-1.0 to VIN + 0.3 (DC)	V
		-2.5 to VIN + 2.0 (20ns)	
V_{BST}	Bootstrap Pin Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
V_{EN}	Enable/UVLO Pin Voltage	-0.3 to +8.0	V
V_{FB}	Feedback Pin Voltage	-0.3 to +6.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+160	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±2000	V
CDM	Charged Device Model	±500	V

Notes: 4. Stresses greater than the *Absolute Maximum Ratings* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	SOT563 (Standard)	110	°C/W
		TSOT26 (Standard)	70	
θ_{JC}	Junction to Case	SOT563 (Standard)	8	°C/W
		TSOT26 (Standard)	12	

Note: 6. Test condition for SOT563 (Standard)/TSOT26 (Standard): Device mounted on FR-4 substrate, two-layer PCB, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (Note 7) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	4.2	18.0	V
VOUT	Output Voltage	0.8	7.0	V
T_J	Operating Junction Temperature	-40	+125	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (@ T_J = +25°C, VIN = 12V, unless otherwise specified. Min/Max limits apply across the recommended operating junction temperature range, -40°C to +125°C, and input voltage range, 4.2V to 18V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V	—	1.3	—	μA
I_Q	Quiescent Supply Current	AP62200/AP62200T: V_{FB} = 0.85V	—	135	—	μA
		AP62201: V_{FB} = 0.85V	—	270	—	μA
POR	VIN Power-on Reset Rising Threshold	—	—	3.90	4.15	V
UVLO	VIN Undervoltage Lockout Falling Threshold	—	—	3.6	—	V
$R_{DS(ON)1}$	High-Side Power MOSFET On-Resistance (Note 8)	—	—	90	—	mΩ
$R_{DS(ON)2}$	Low-Side Power MOSFET On-Resistance (Note 8)	—	—	65	—	mΩ
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 8)	From Source to Drain	2.0	2.4	2.8	A
f_{SW}	Oscillator Frequency	VOUT = 5V, CCM	—	750	—	kHz
t_{ON_MIN}	Minimum On-Time	—	—	90	—	ns
t_{OFF_MIN}	Minimum Off-Time	—	—	220	—	ns
V_{FB}	Feedback Voltage	AP62200/AP62201: T_A = +25°C, CCM	0.792	0.800	0.808	V
		AP62200/AP62201: CCM	0.784	0.800	0.816	V
		AP62200T: T_A = +25°C, CCM	0.755	0.763	0.770	V
		AP62200T: CCM	0.747	0.763	0.778	V
V_{EN_H}	EN Logic High Threshold	—	—	1.20	1.25	V
V_{EN_L}	EN Logic Low Threshold	—	1.04	1.10	—	V
I_{EN}	EN Input Current	V_{EN} = 1.5V	—	7.0	—	μA
		V_{EN} = 1V	1.0	1.5	2.0	μA
t_{SS}	Soft-Start Time	—	—	2.5	—	ms
T_{SD}	Thermal Shutdown (Note 8)	—	—	+160	—	°C
T_{Hys}	Thermal Shutdown Hysteresis (Note 8)	—	—	+20	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP62200/AP62201/AP62200T @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.)

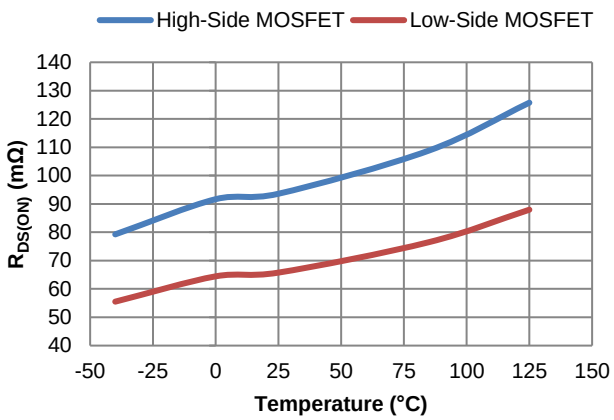


Figure 5. Power MOSFET $R_{DS(ON)}$ vs. Temperature

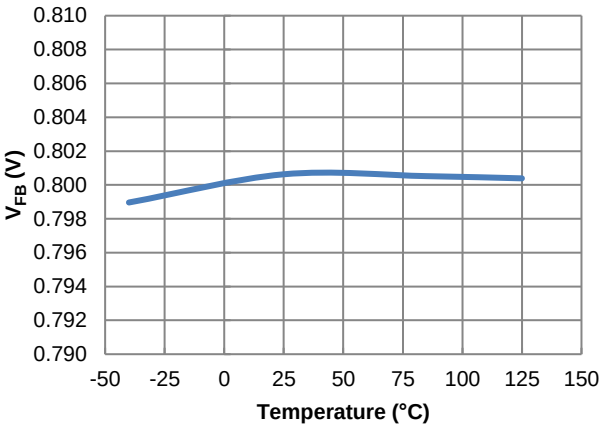


Figure 6. Feedback Voltage vs. Temperature, AP62200/AP62201

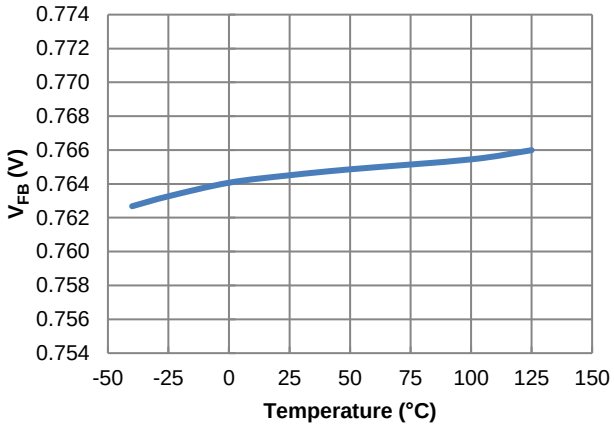


Figure 7. Feedback Voltage vs. Temperature, AP62200T

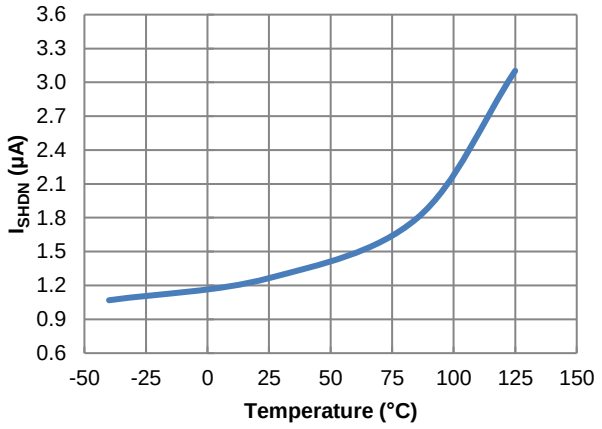


Figure 8. I_{SHDN} vs. Temperature

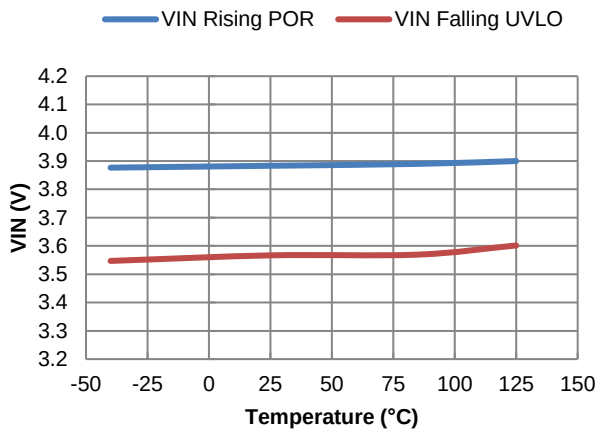


Figure 9. VIN Power-On Reset and UVLO vs. Temperature

Typical Performance Characteristics (AP62200/AP62201/AP62200T @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.) (continued)

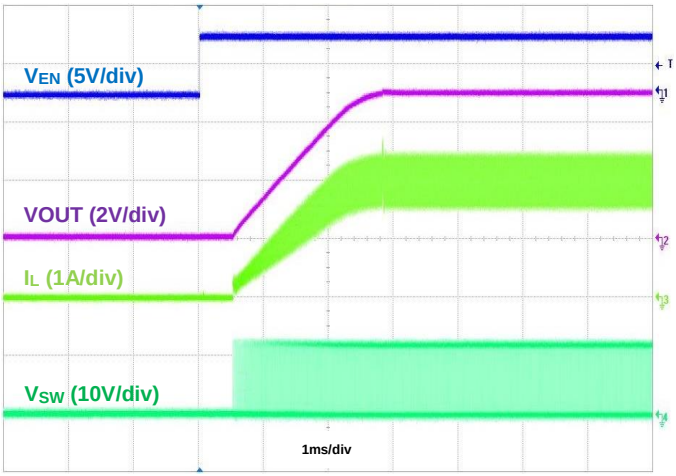


Figure 10. Startup Using EN, IOUT = 2A

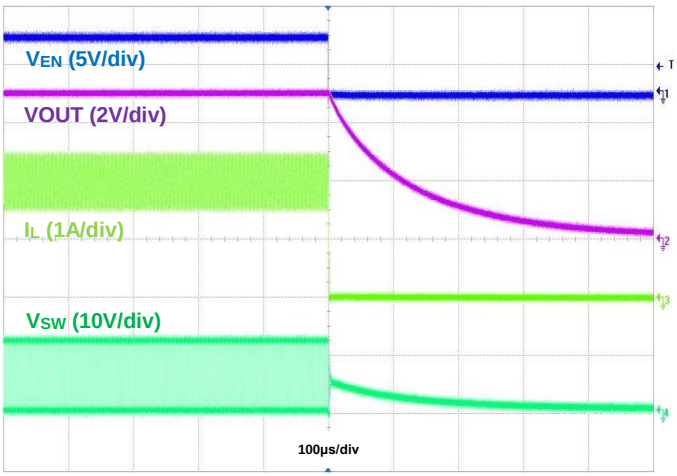


Figure 11. Shutdown Using EN, IOUT = 2A

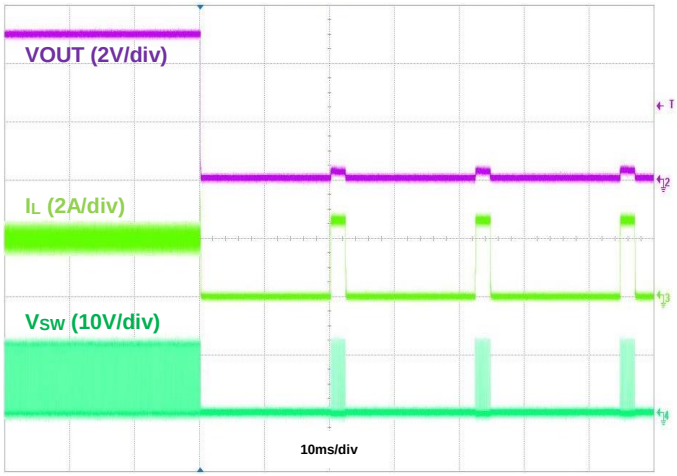


Figure 12. Output Short Protection, IOUT = 2A

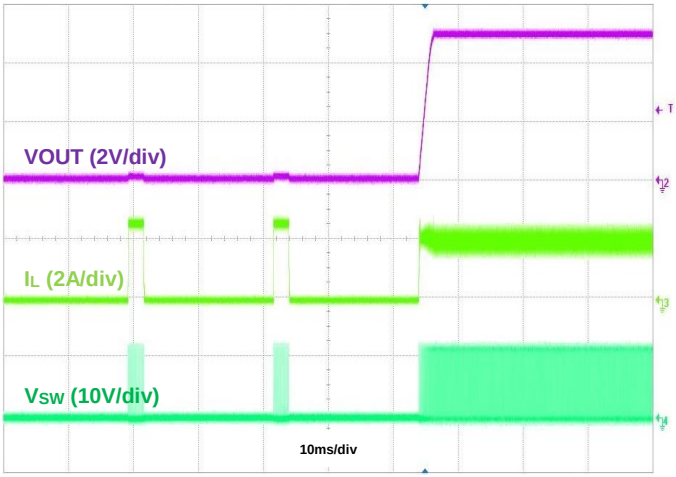


Figure 13. Output Short Recovery, IOUT = 2A

Typical Performance Characteristics (AP62200/AP62200T @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.)

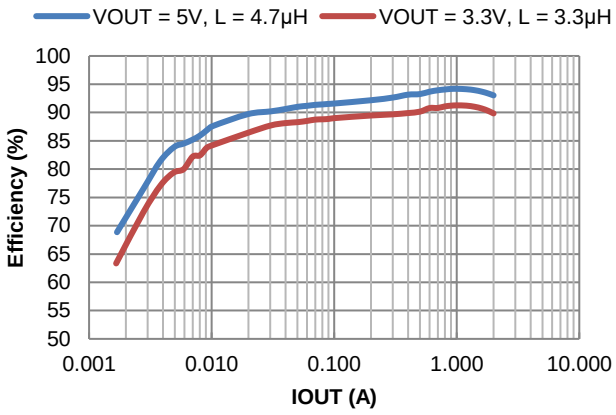


Figure 14. Efficiency vs. Output Current, VIN = 12V

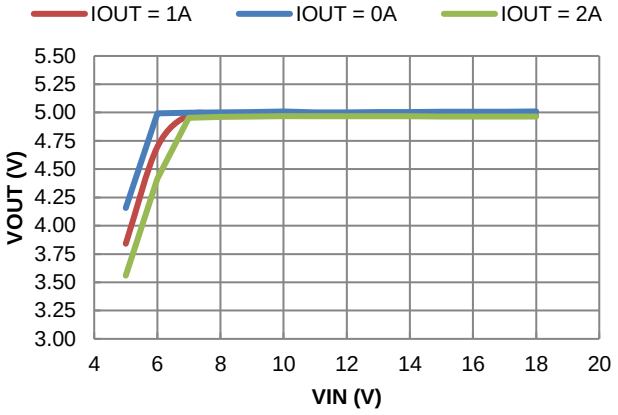


Figure 15. Line Regulation

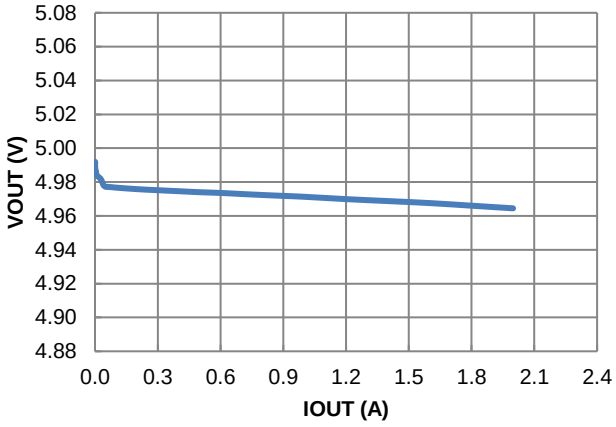


Figure 16. Load Regulation

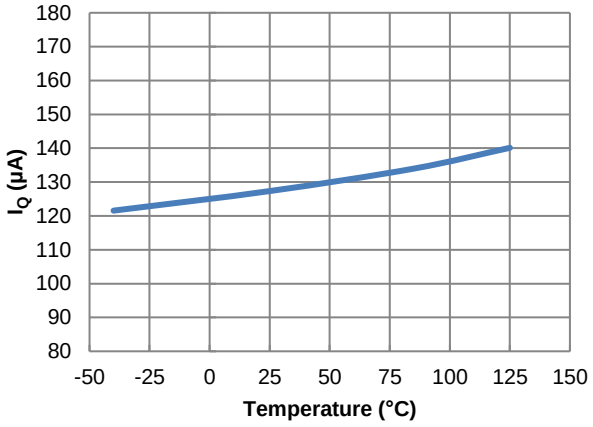


Figure 17. I_Q vs. Temperature

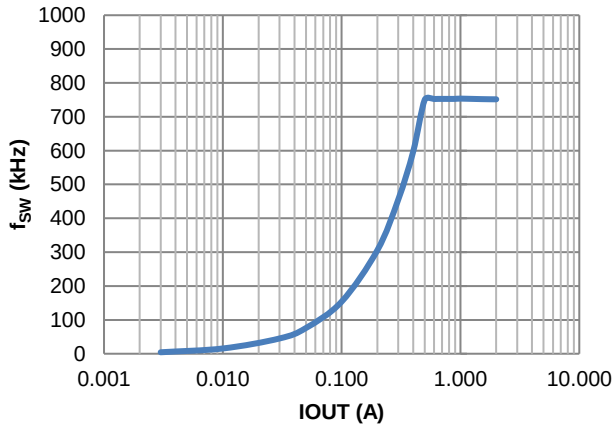


Figure 18. f_{SW} vs. Load

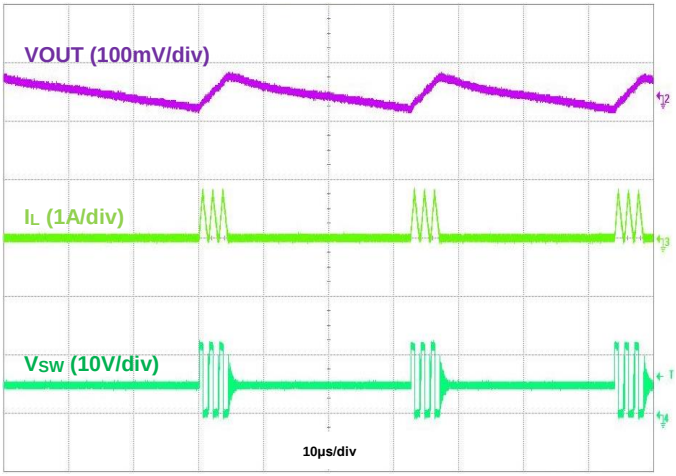


Figure 19. Output Voltage Ripple, VOUT = 5V, IOUT = 50mA

Typical Performance Characteristics (AP62200/AP62200T @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.) (continued)

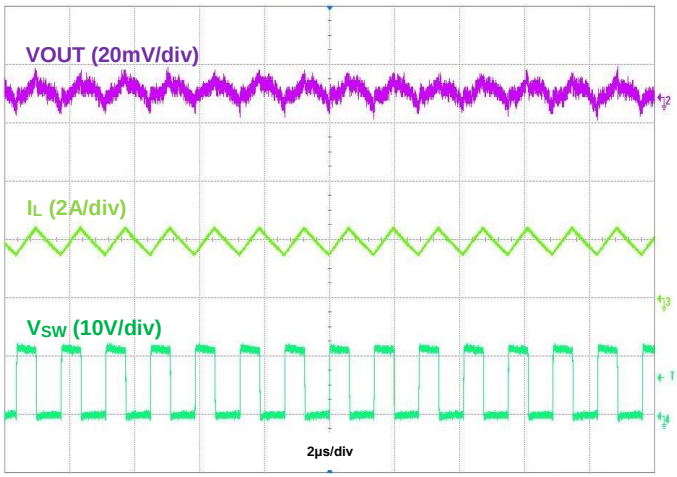


Figure 20. Output Voltage Ripple, VOUT = 5V, IOUT = 2A

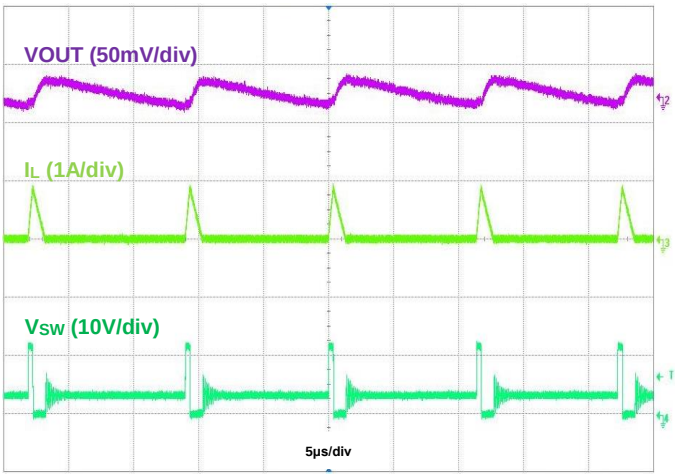


Figure 21. Output Voltage Ripple, VOUT = 3.3V, IOUT = 50mA

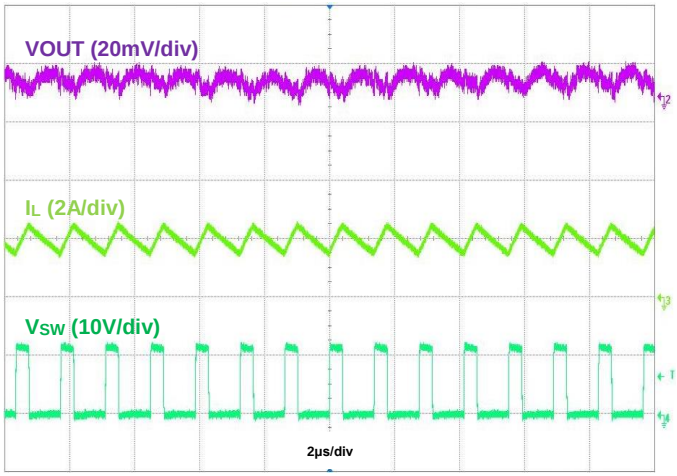


Figure 22. Output Voltage Ripple, VOUT = 3.3V, IOUT = 2A

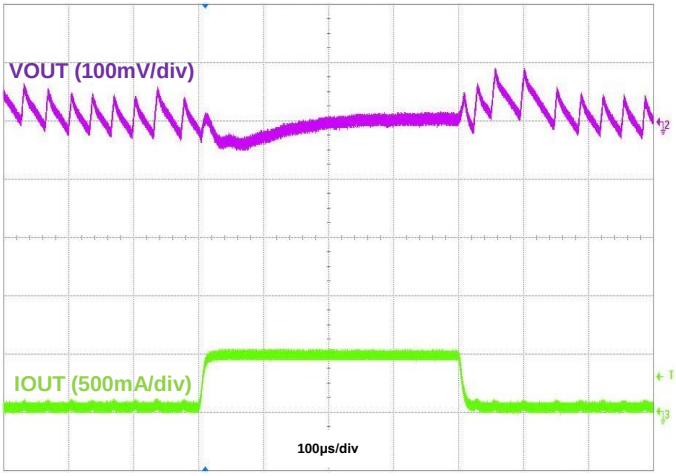


Figure 23. Load Transient, IOUT = 50mA to 500mA to 50mA

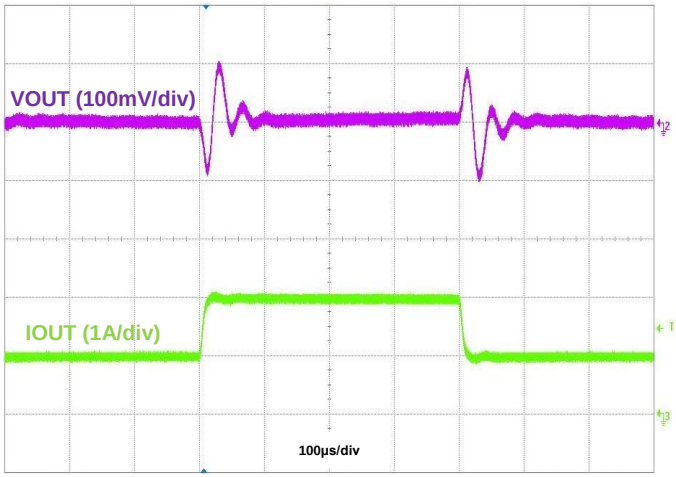


Figure 24. Load Transient, IOUT = 1A to 2A to 1A

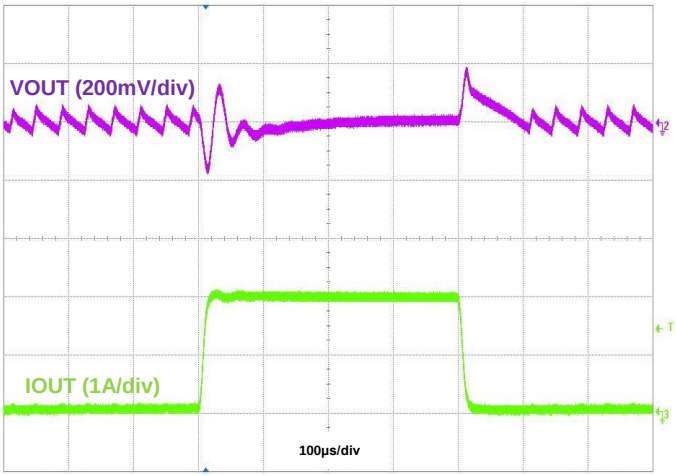


Figure 25. Load Transient, IOUT = 50mA to 2A to 50mA

Typical Performance Characteristics (AP62201 @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.)

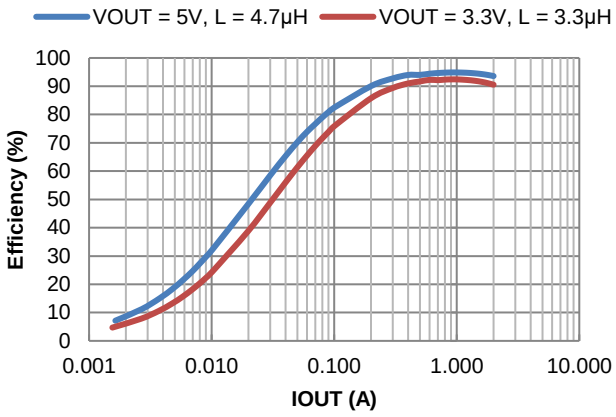


Figure 26. Efficiency vs. Output Current, VIN = 12V

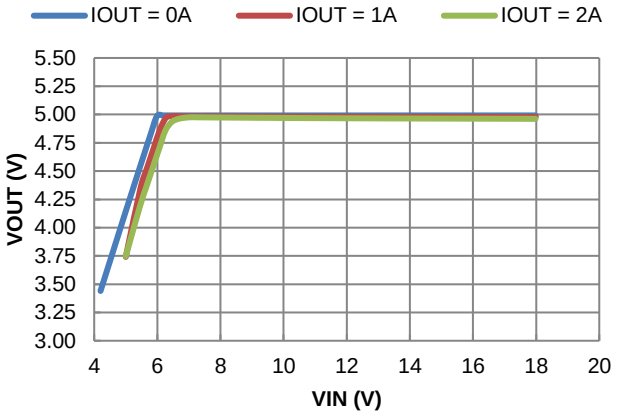


Figure 27. Line Regulation

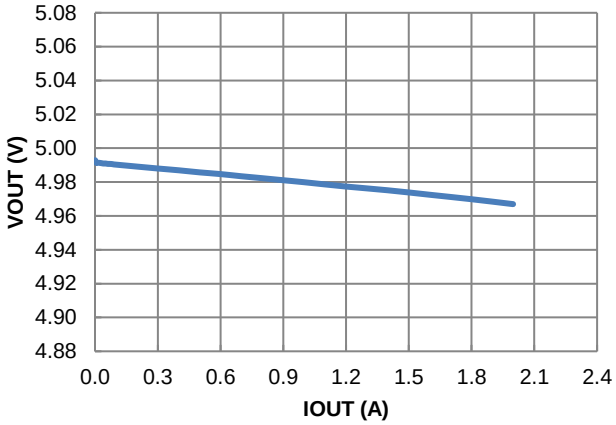


Figure 28. Load Regulation

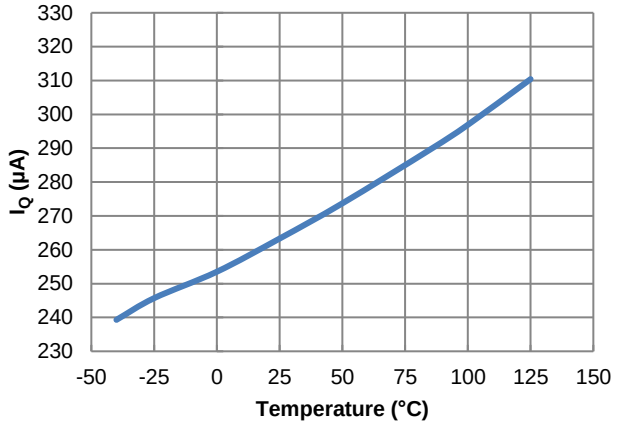


Figure 29. I_Q vs. Temperature

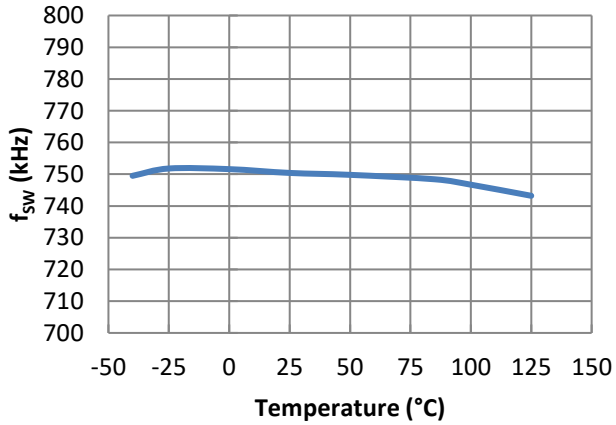


Figure 30. f_{SW} vs. Temperature, IOUT = 0A

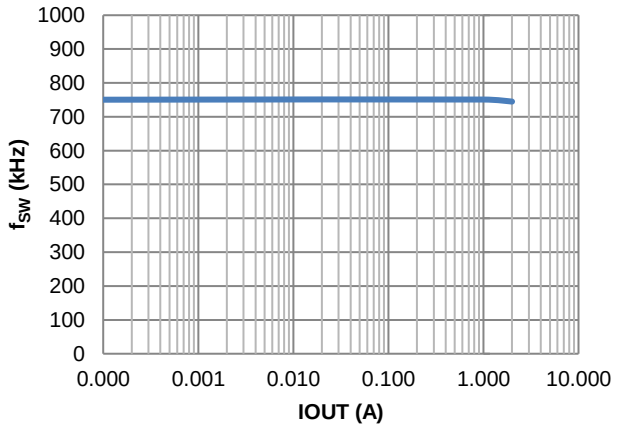


Figure 31. f_{SW} vs. Load

Typical Performance Characteristics (AP62201 @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.) (continued)

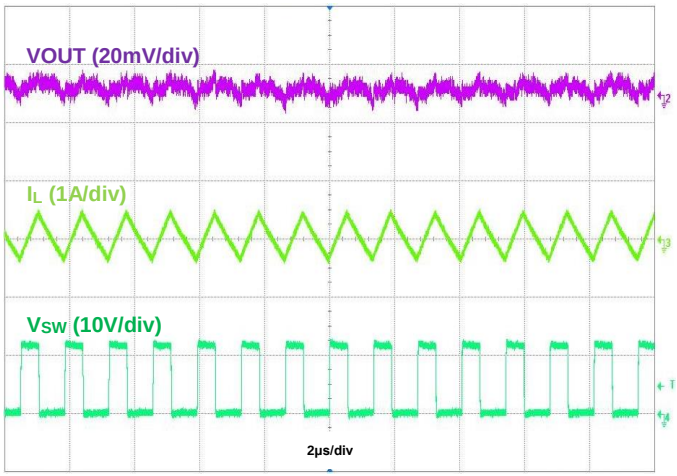


Figure 32. Output Voltage Ripple, VOUT = 5V, IOUT = 50mA

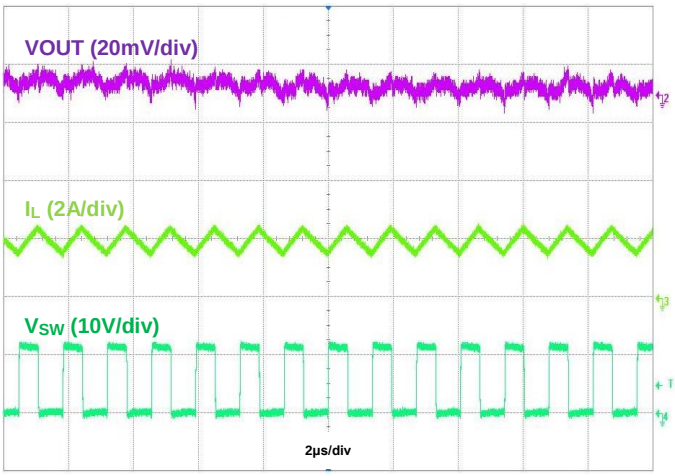


Figure 33. Output Voltage Ripple, VOUT = 5V, IOUT = 2A

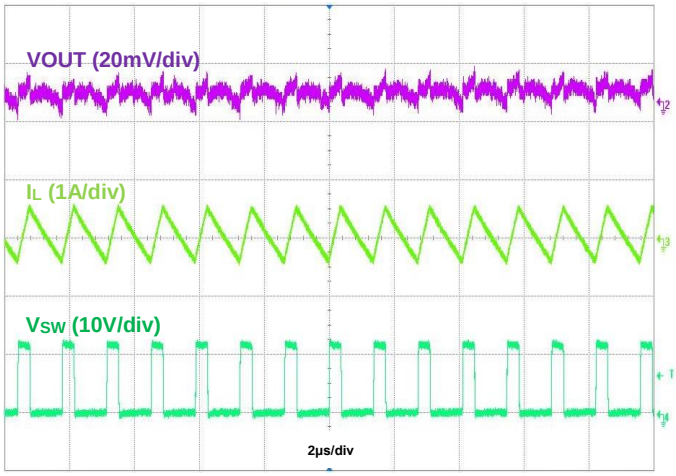


Figure 34. Output Voltage Ripple, VOUT = 3.3V, IOUT = 50mA

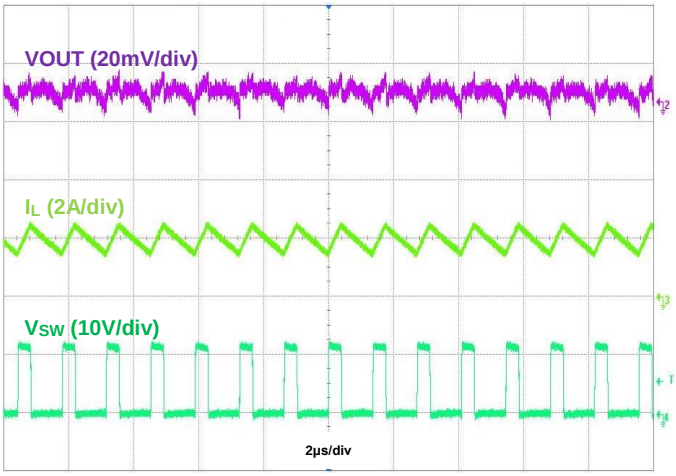


Figure 35. Output Voltage Ripple, VOUT = 3.3V, IOUT = 2A

Typical Performance Characteristics (AP62201 @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.) (continued)

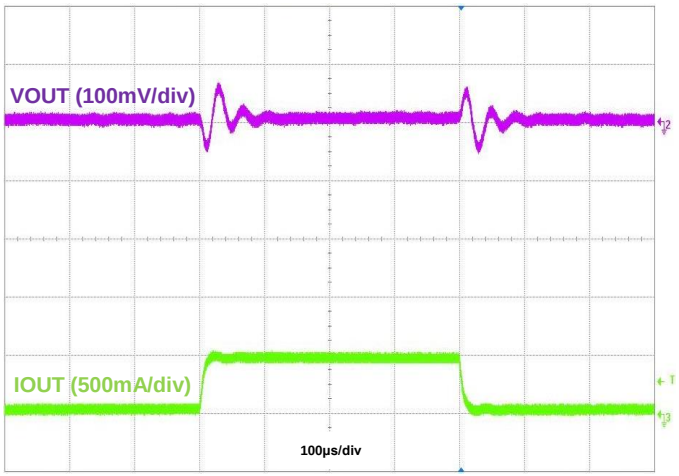


Figure 36. Load Transient, IOUT = 50mA to 500mA to 50mA

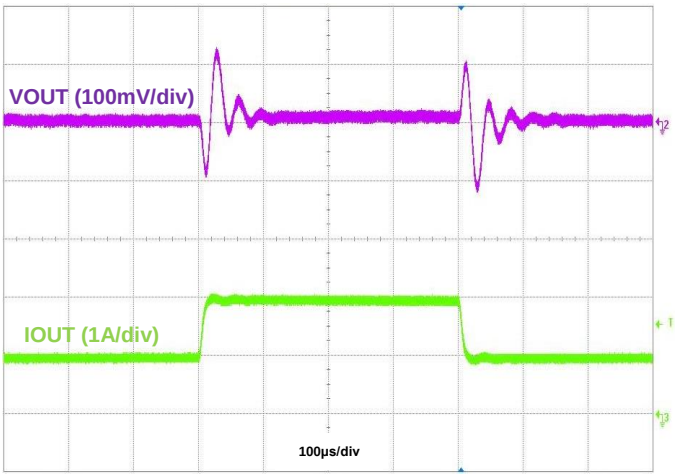


Figure 37. Load Transient, IOUT = 1A to 2A to 1A

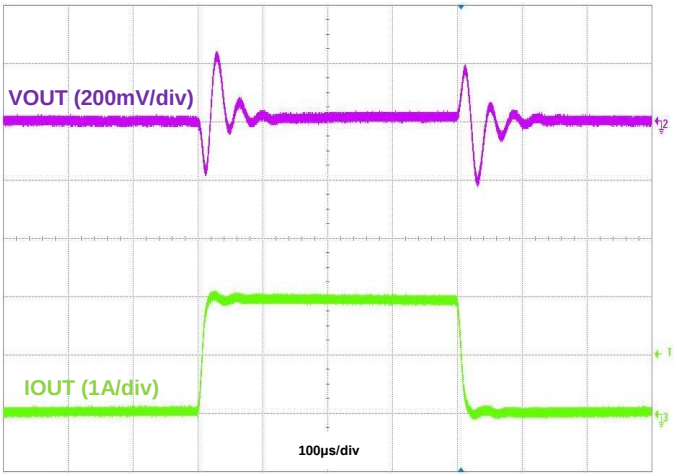


Figure 38. Load Transient, IOUT = 50mA to 2A to 50mA

Application Information

1 Pulse Width Modulation (PWM) Operation

The AP62200/AP62201/AP62200T device is a 4.2V-to-18V input, 2A output, EMI friendly, fully integrated synchronous buck converter. Refer to the block diagram in Figure 4. The device employs constant on-time control to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the one-shot pulse turns on the high-side power MOSFET, Q1, for a fixed on-time, t_{ON}. This one-shot on-pulse timing is calculated by the converter's input voltage and output voltage to maintain a pseudo-fixed frequency over the input voltage range. When Q1 is on, the inductor current rises linearly and the device charges the output capacitor. Q1 turns off after the fixed on-time expires, and the low-side power MOSFET, Q2, turns on. Once the output voltage drops below the output regulation, Q2 turns off. The one-shot timer is then reset and Q1 turns on again. The on-time is inversely proportional to the input voltage and directly proportional to the output voltage. It is calculated by the following equation:

$$\mathbf{t_{ON} = \frac{VOUT}{VIN \cdot f_{SW}}} \qquad \textbf{Eq. 1}$$

Where:

- VIN is the input voltage
- VOUT is the output voltage
- f_{SW} is the switching frequency

The off-time duration is t_{OFF} and starts after the on-time expires. The off-time expires when the feedback voltage decreases below the reference voltage, which then triggers the on-time duration to start again. The minimum off-time is 220ns typical.

In order to provide a small output ripple during light load conditions, the AP62201 operates in PWM regardless of output load.

2 Pulse Frequency Modulation (PFM) Operation

The AP62200/AP62200T enters PFM operation at light load conditions for high efficiency. During light load conditions, the regulator automatically reduces the switching frequency. As the output current decreases, so too does the inductor current. The inductor current, I_L, eventually reaches 0A, marking the boundary between Continuous Conduction Mode (CCM) and Discontinuous Condition Mode (DCM). During this time, both Q1 and Q2 are off, and the load current is provided only by the output capacitor. When V_{FB} becomes lower than 0.8V for AP62200 or 0.763V for AP62200T, the next cycle begins, and Q1 turns on. Because the AP62200/AP62200T works in PFM during light load conditions, it can achieve power efficiency of up to 84% at a 5mA load condition.

Likewise, as the output load increases from light load to heavy load, the switching frequency increases to maintain the regulation of the output voltage. The transition point between light and heavy load conditions can be calculated using the following equation:

$$\mathbf{I_{LOAD} = \left(\frac{VIN - VOUT}{2L}\right) \cdot t_{ON}} \qquad \textbf{Eq. 2}$$

Where:

- L is the inductor value

The quiescent current of AP62200/AP62200T is 135μA typical under a no-load, non-switching condition.

3 Enable

When disabled, the device shutdown supply current is only 1.3μA. When applying a voltage greater than the EN logic high threshold (typical 1.2V, rising), the AP62200/AP62201/AP62200T enables all functions and the device initiates the soft-start phase. An internal 1.5μA pull-up current source connected from the internal LDO-regulated VCC to the EN pin guarantees that if EN is left floating, the device still automatically enables once the voltage reaches the EN logic high threshold. The AP62200/AP62201/AP62200T has a built-in 2.5ms soft-start time to prevent output voltage overshoot and inrush current. When the EN voltage falls below its logic low threshold (typical 1.1V, falling), the internal SS voltage discharges to ground and device operation disables.

The EN pin can also be used to program the undervoltage lockout thresholds. See **Undervoltage Lockout (UVLO)** section for more details.

Application Information (continued)

3 Enable (continued)

Alternatively, a small ceramic capacitor can be added from EN to GND. When EN is not driven externally, this capacitor increases the time needed for the EN pin voltage to reach its logic high threshold, which delays the startup of the output voltage. This is useful when sequencing multiple power rails to minimize input inrush current. When the EN pin voltage starts from 0V, the amount of capacitance for a given delay time is approximated by:

$$C_d[nF] \approx 0.278 \cdot t_d[ms] \quad \text{Eq. 3}$$

Where:

- C_d is the time delay capacitance in nF
- t_d is the delay time in ms

4 Electromagnetic Interference (EMI) Reduction with Ringing-Free Switching Node

In some applications, the system must meet EMI standards. In relation to high frequency radiation EMI noise, the switching node's (SW's) ringing amplitude is especially critical. To dampen high frequency radiated EMI noise, the AP62200/AP62201/AP62200T device implements a proprietary, multi-level gate driver scheme that achieves a ringing-free switching node without sacrificing the switching node's rise and fall slew rates as well as the converter's power efficiency.

5 Adjusting Undervoltage Lockout (UVLO)

Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AP62200/AP62201/AP62200T device has a UVLO comparator that monitors the input voltage and the internal bandgap reference. The AP62200/AP62201/AP62200T disables if the input voltage falls below 3.6V. In this UVLO event, both the high-side and low-side power MOSFETs turn off.

Some applications may desire higher VIN UVLO threshold voltages than is provided by the default setup. A 5.5µA hysteresis pull-up current source on the EN pin along with an external resistive divider (R3 and R4) configures the VIN UVLO threshold voltages as shown in Figure 39.

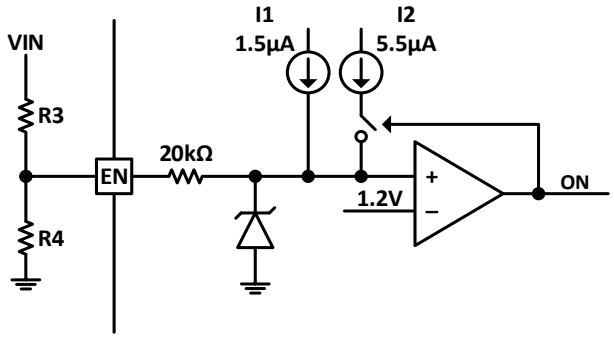


Figure 39. Programming UVLO

The resistive divider resistor values are calculated by:

$$R3 = \frac{0.917 \cdot V_{ON} - V_{OFF}}{5.625\mu A} \quad \text{Eq. 4}$$

$$R4 = \frac{1.1 \cdot R3}{V_{OFF} - 1.1V + 7\mu A \cdot R3} \quad \text{Eq. 5}$$

Where:

- V_{ON} is the rising edge VIN voltage to enable the regulator and is greater than 4.15V
- V_{OFF} is the falling edge VIN voltage to disable the regulator and is greater than 3.85V

Application Information (continued)

6 Overcurrent Protection (OCP)

The AP62200/AP62201/AP62200T has cycle-by-cycle valley current limit protection by sensing the current through the internal low-side power MOSFET, Q2. While Q2 is on, the internal sensing circuitry monitors its conduction current. The overcurrent limit has a corresponding voltage limit, V_{LIMIT}. When the voltage between GND and SW is lower than V_{LIMIT} due to excessive current through Q2, the OCP triggers, and the controller turns off Q2. During this time, both Q1 and Q2 remain off. A new switching cycle begins only when the voltage between GND and SW rises above V_{LIMIT}. If Q2 consistently hits the valley current limit for 2.5ms or the VFB is less than 495mV (UVP threshold), the buck converter enters hiccup mode and shuts down. After 20ms of down time, the buck converter restarts powering up. Hiccup mode reduces the power dissipation in the overcurrent condition.

Because the $R_{DS(ON)}$ values of the power MOSFETs increase with temperature, V_{LIMIT} has a temperature coefficient of 0.4%/°C to compensate for the temperature dependency of $R_{DS(ON)}$.

7 Thermal Shutdown (TSD)

If the junction temperature of the device reaches the thermal shutdown limit of +160°C, the AP62200/AP62201/AP62200T shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (+140°C typical), the device initiates a normal power-up cycle with soft-start.

8 Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$\mathbf{T_{RISE} = PD \cdot (\theta_{JA})} \qquad \textbf{Eq. 6}$$

Where:

- PD is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$\mathbf{T_J = T_A + T_{RISE}} \qquad \textbf{Eq. 7}$$

Where:

- T_A is the ambient temperature of the environment

Application Information (continued)

8 Power Derating Characteristics (continued)

For the SOT563 (Standard) and TSOT26 (Standard) packages, the θ_{JA} is 110°C/W and 70°C/W, respectively. The actual junction temperature should not exceed the maximum recommended operating junction temperature of +125°C when considering the thermal design. Figure 40 and Figure 41 show typical derating curves versus ambient temperature.

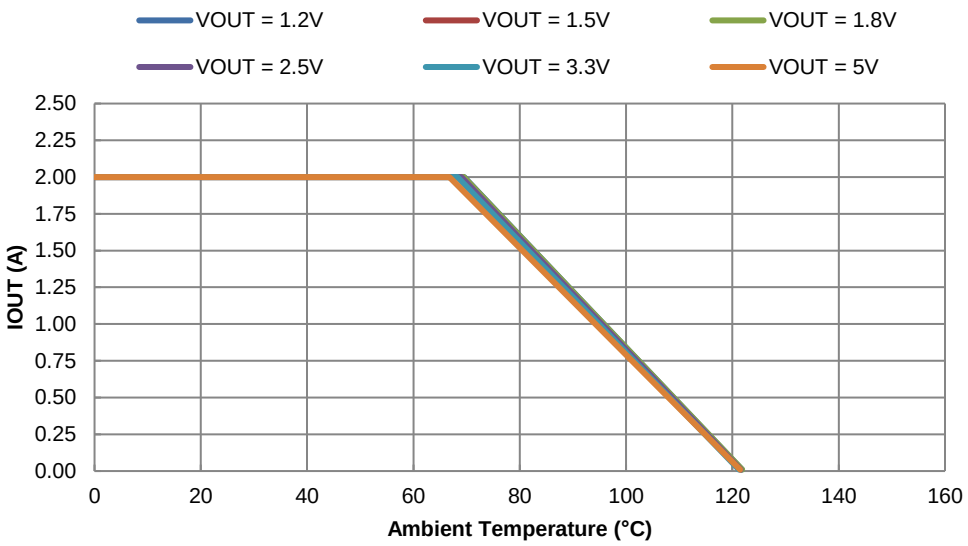


Figure 40. Output Current Derating Curve vs. Ambient Temperature, SOT563 (Standard) Package, VIN = 12V

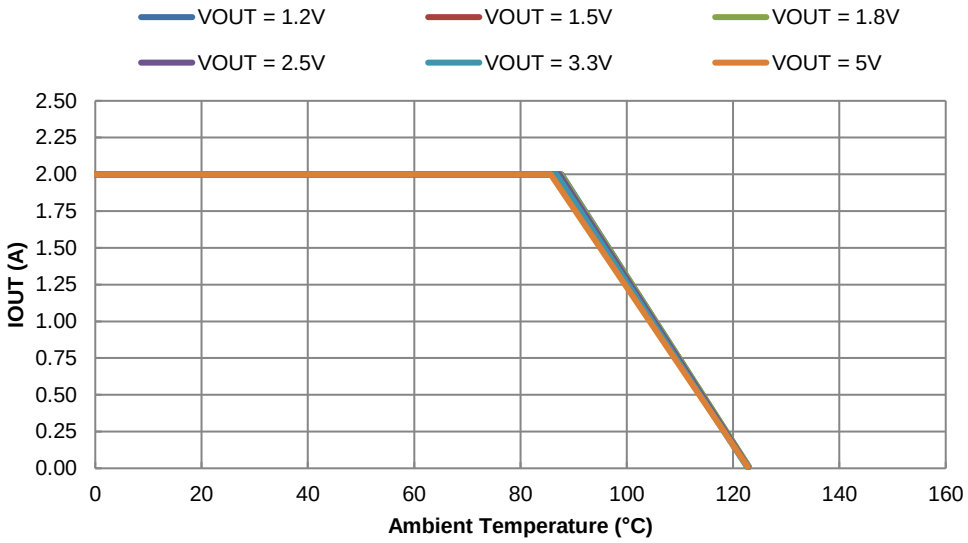


Figure 41. Output Current Derating Curve vs. Ambient Temperature, TSOT26 (Standard) Package, VIN = 12V

Application Information (continued)

9 Setting the Output Voltage

The AP62200/AP62201/AP62200T has adjustable output voltages, starting from 0.8V for AP62200/AP62201 and 0.763V for AP62200T, using an external resistive divider. The resistor values of the feedback network are selected based on a design trade-off between efficiency and output voltage accuracy. There is less current consumption in the feedback network for high resistor values, which improves efficiency at light loads. However, values too high cause the device to be more susceptible to noise affecting its output voltage accuracy. R1 can be determined by the following equation:

$$\mathbf{R1 = R2 \cdot \left(\frac{VOUT}{V_{FB}} - 1\right)} \quad \textbf{Eq. 8}$$

Where:

- V_{FB} is the feedback voltage

Table 1 shows a list of recommended component selections for common AP62200/AP62201/AP62200T output voltages referencing Figure 1. Consult Diodes Incorporated for other output voltage requirements.

Table 1. Recommended Component Selections

AP62200/AP62201/AP62200T								
Output Voltage (V)	AP62200/AP62201 R1 (kΩ)	AP62200T R1 (kΩ)	R2 (kΩ)	L (µH)	C1 (µF)	C2 (µF)	C5 (pF) (Optional)	C6 (nF)
1.2	4.99	5.76	10	2.2	10	2 x 22	Open	100
1.5	8.66	9.76	10	2.2	10	2 x 22	Open	100
1.8	12.4	13.7	10	3.3	10	2 x 22	10 - 100	100
2.5	21.5	22.6	10	3.3	10	2 x 22	10 - 100	100 - 220
3.3	31.6	33.2	10	3.3	10	2 x 22	10 - 100	100 - 330
5.0	52.3	56.2	10	4.7	10	2 x 22	10 - 100	100 - 330

10 Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$\mathbf{L = \frac{VOUT \cdot (VIN - VOUT)}{VIN \cdot \Delta I_L \cdot f_{SW}}} \quad \textbf{Eq. 9}$$

Where:

- ΔI_L is the inductor current ripple
- f_{SW} is the buck converter switching frequency

For AP62200/AP62201/AP62200T, choose ΔI_L to be 30% to 50% of the maximum load current of 2A.

The inductor peak current is calculated by:

$$\mathbf{I_{L_{PEAK}} = I_{LOAD} + \frac{\Delta I_L}{2}} \quad \textbf{Eq. 10}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal power MOSFETs. Therefore, choosing an inductor with the appropriate saturation current rating is important. For most applications, it is recommended to select an inductor of approximately 1.2µH to 4.7µH with a DC current rating of at least 35% higher than the maximum load current. For highest efficiency, the inductor's DC resistance should be less than 50mΩ. Use a larger inductance for improved efficiency under light load conditions.

Application Information (continued)

11 Input Capacitor

The input capacitor reduces both the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor must sustain the ripple current produced during the on-time of Q1. It must have a low ESR to minimize power dissipation due to the RMS input current.

The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor with an RMS current rating greater than half of the maximum load current.

Due to large dI/dt through the input capacitor, electrolytic or ceramic capacitors with low ESR should be used. If using a tantalum capacitor, it must be surge protected or else capacitor failure could occur. Using a ceramic capacitor of 10µF or greater is sufficient for most applications.

12 Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady-state and sets the off-time to minimum to supply more current to the load. However, the inductor limits the change to increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady-state and increases the off-time to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the excess current from the inductor during this time.

The effective output capacitance, COUT, requirements can be calculated from the equations below.

The ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated by:

$$\mathbf{VOUT_{Ripple}} = \Delta \mathbf{I_L} \cdot \left(\mathbf{ESR} + \frac{\mathbf{1}}{\mathbf{8} \cdot \mathbf{f_{sw}} \cdot \mathbf{COUT}} \right) \quad \textbf{Eq. 11}$$

An output capacitor with large capacitance and low ESR is the best option. For most applications, a 22µF to 68µF ceramic capacitor is sufficient. To meet the load transient requirements, the calculated COUT should satisfy the following inequality:

$$\mathbf{COUT} > \mathbf{max}\left(\frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Overshoot}} \cdot \mathbf{VOUT}}, \frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Undershoot}} \cdot (\mathbf{VIN} - \mathbf{VOUT})} \right) \quad \textbf{Eq. 12}$$

Where:

- I_{Trans} is the load transient
- $\Delta V_{Overshoot}$ is the maximum output overshoot voltage
- $\Delta V_{Undershoot}$ is the maximum output undershoot voltage

13 Bootstrap Capacitor

To ensure proper operation, a ceramic capacitor must be connected between the BST and SW pins to supply the drive voltage for the high-side power MOSFET. A 100nF ceramic capacitor is sufficient for most applications. In the cases where output voltage is higher than 3V, a 330nF is recommended to help maintain stable voltage from BST to SW.

Layout

PCB Layout

1. The AP62200/AP62201/AP62200T works at 2A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 42 and Figure 43 for more details.

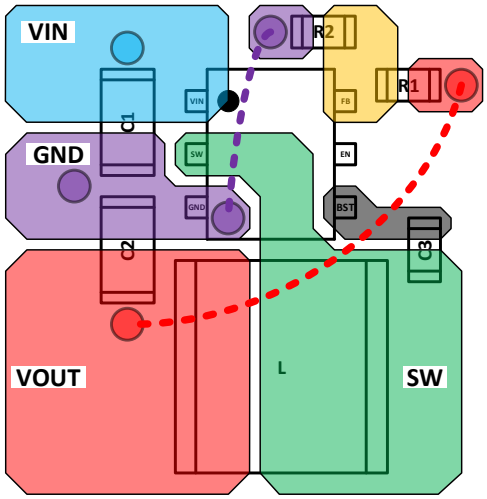


Figure 42. Recommended PCB Layout, SOT563 (Standard)

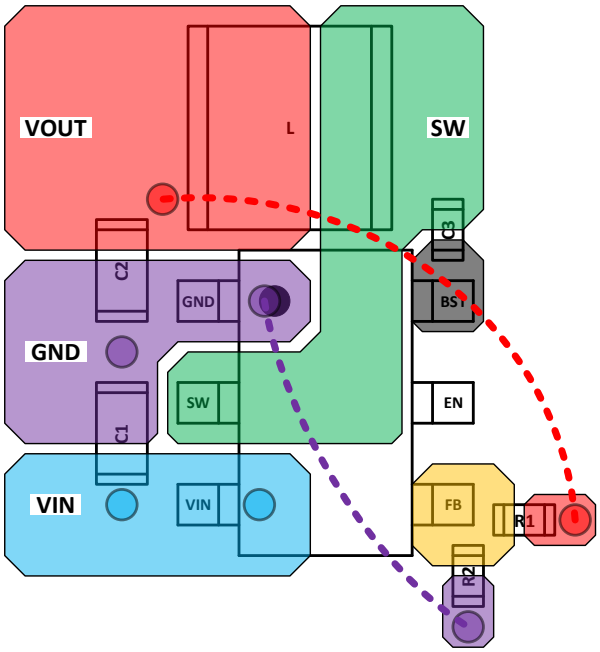
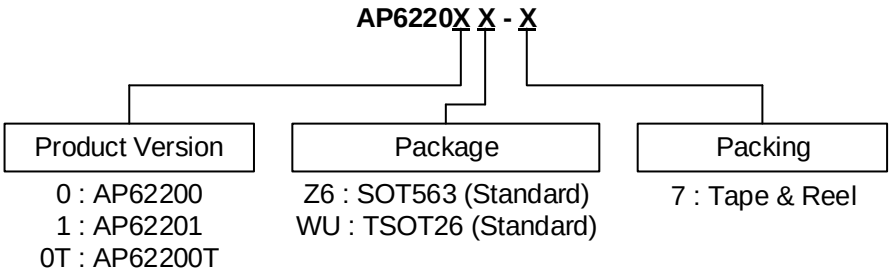


Figure 43. Recommended PCB Layout, TSOT26 (Standard)

Ordering Information

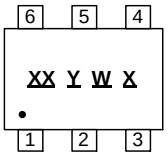


Part Number	Package	Operation Mode	V_{FB} (V)	Package Code	Packing	
					Qty.	Carrier
AP62200Z6-7	SOT563 (Standard)	PFM/PWM	0.800	Z6	3000	7" Tape and Reel
AP62200WU-7	TSOT26 (Standard)	PFM/PWM	0.800	WU	3000	7" Tape and Reel
AP62201Z6-7	SOT563 (Standard)	PWM Only	0.800	Z6	3000	7" Tape and Reel
AP62201WU-7	TSOT26 (Standard)	PWM Only	0.800	WU	3000	7" Tape and Reel
AP62200TWU-7	TSOT26 (Standard)	PFM/PWM	0.763	WU	3000	7" Tape and Reel

Marking Information

SOT563 (Standard)/TSOT26 (Standard)

(Top View)



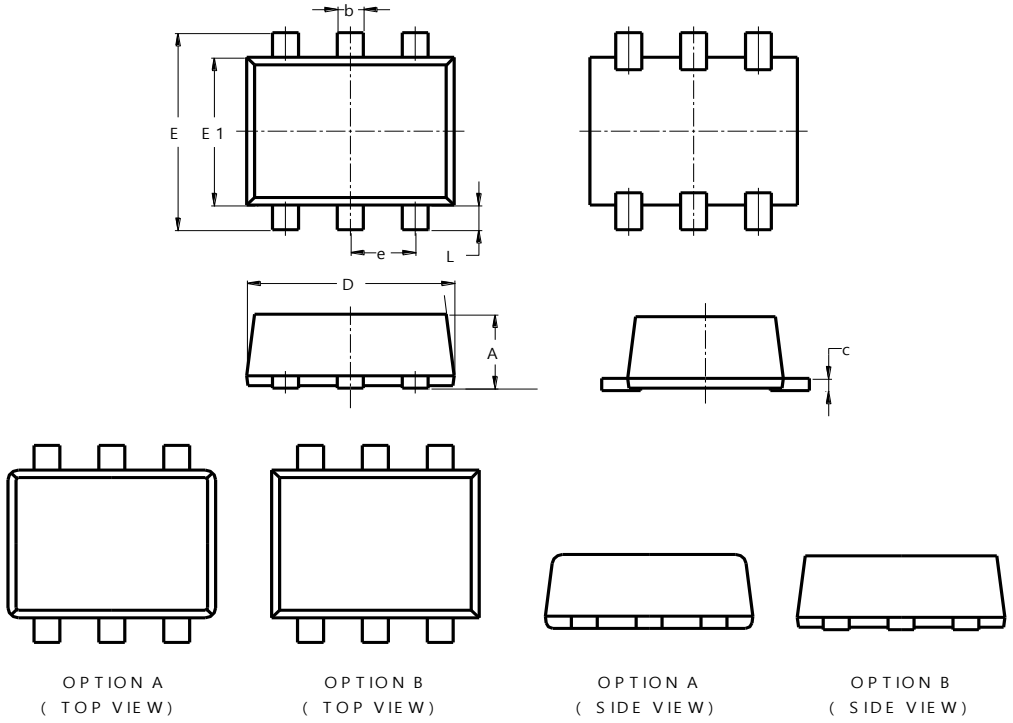
XX : Identification Code
Y : Year 0 to 9
W : Week : A to Z : 1 to 26 Week;
a to z : 27 to 52 Week; z Represents
52 and 53 Week
X : Internal Code

Part Number	Package	Identification Code
AP62200Z6-7	SOT563 (Standard)	HA
AP62200WU-7	TSOT26 (Standard)	HB
AP62201Z6-7	SOT563 (Standard)	HS
AP62201WU-7	TSOT26 (Standard)	HT
AP62200TWU-7	TSOT26 (Standard)	TN

Package Outline Dimensions

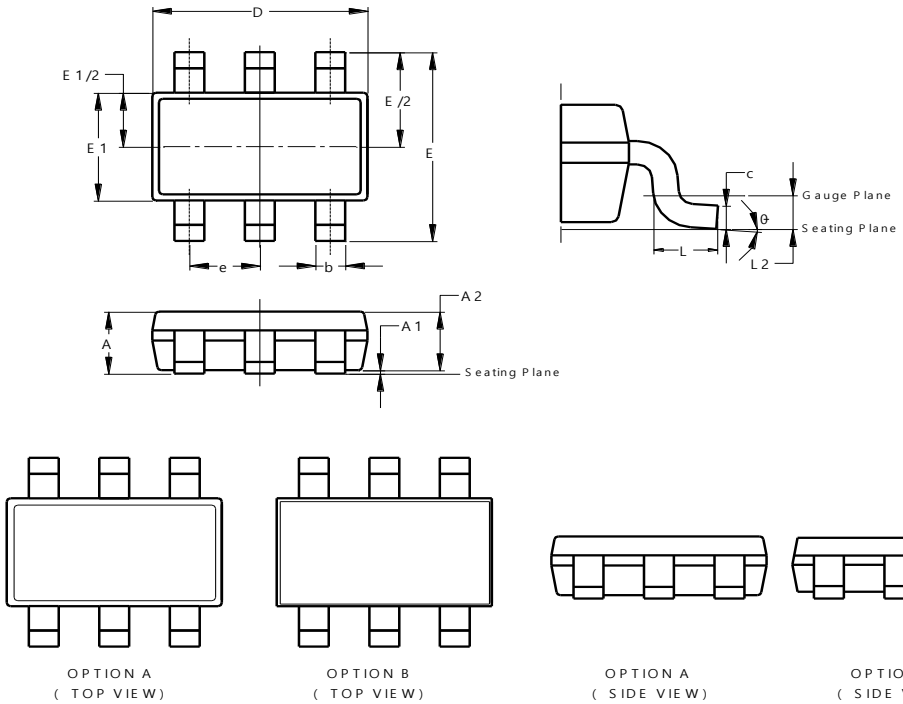
Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT563 (Standard)



SOT563 (Standard)			
Dim	**Min**	**Max**	**Typ**
A	0.53	0.60	—
b	0.15	0.30	0.20
c	0.10	0.18	0.11
D	1.50	1.70	1.60
E	1.50	1.70	1.60
E1	1.10	1.30	1.20
e	0.50 BSC		
L	0.10	0.30	0.20
All Dimensions in mm			

TSOT26 (Standard)

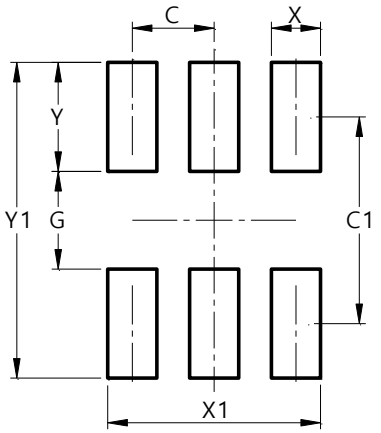


TSOT26 (Standard)			
Dim	**Min**	**Max**	**Typ**
A	—	1.00	—
A1	0.00	0.10	—
A2	0.75	0.90	0.80
D	2.70	3.10	2.90
E	2.60	3.00	2.80
E1	1.50	1.70	1.60
b	0.30	0.50	0.44
c	0.11	0.20	0.16
e	0.95 BSC		
L	0.30	0.50	0.40
L2	0.25 BSC		
θ	0°	8°	4°
All Dimensions in mm			

Suggested Pad Layout

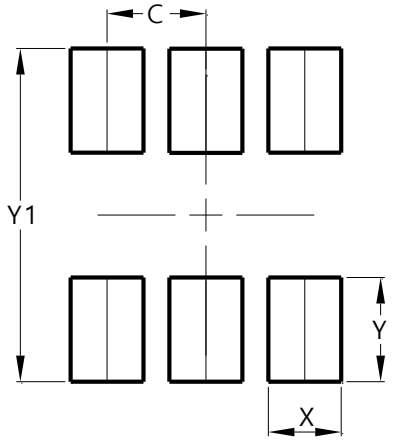
Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT563 (Standard)



Dimensions	Value (in mm)
C	0.500
C1	1.270
G	0.600
X	0.300
X1	1.300
Y	0.670
Y1	1.940

TSOT26 (Standard)



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.200

Mechanical Data

SOT563 (Standard)

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.003 grams (Approximate)

TSOT26 (Standard)

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.013 grams (Approximate)

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