Gate Driver Providing Galvanic Isolation Series

Isolation Voltage 2500 Vrms 1ch Gate Driver Providing Galvanic Isolation for GaN HEMT

BM6GD11BFJ-LB

General Description

This product is a rank product for the industrial equipment market. This is the best product for use in these applications.

BM6GD11BFJ-LB is a 1-channel gate driver with built-in isolation, capable of driving GaN HEMTs at high speeds. It has an isolation voltage of 2500 Vrms, a maximum input/output delay time of 60 ns, and a minimum input pulse width of 65 ns.
The output driver pins on the source and sink sides are separated. These pins generate a switching waveform with slew rate at the rising and falling edges individually adjusted by inserting a resistor between the gate pins of the GaN HEMT.
In addition, an under-voltage lockout function (UVLO) is built into the input side (between VCC1 and GND1) and the output side (between VCC2 and GND2), respectively.

Key Specifications

- Isolation Voltage: 2500 Vrms
- Input Voltage Range: 4.5 V to 5.5 V
- Output Voltage (Gate Drive Voltage) Range: 4.5 V to 6.0 V
- Maximum I/O Delay Time: 60 ns
- Minimum Input Pulse Width: 65 ns
- Operating Temperature Range: -40 °C to +125 °C

Package

Package	W (Typ) x D (Typ) x H (Max)
SOP-JW8	4.9 mm x 6.0 mm x 1.65 mm

Features

- Built-in Galvanic Isolation
- Under-voltage Lockout Function

Applications

- Industrial Equipment
- GaN HEMT Gate Drive Applications
- AC Adapters
- Server Power Supplies

Typical Application Circuit

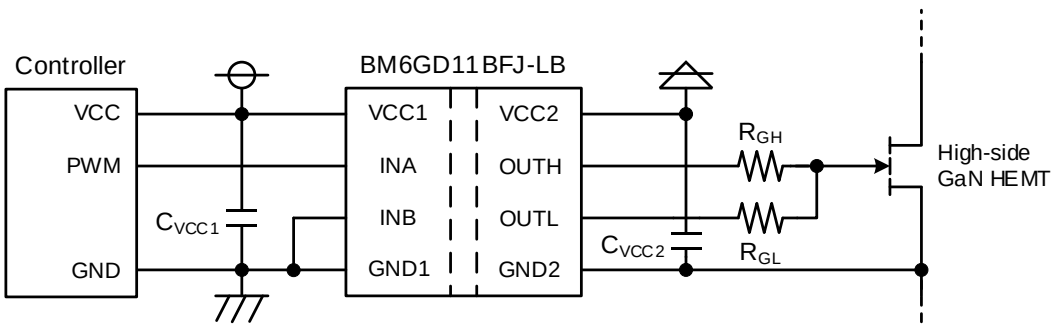


Figure 1. Basic Application Circuit Diagram (High-side GaN HEMT driver)

Contents

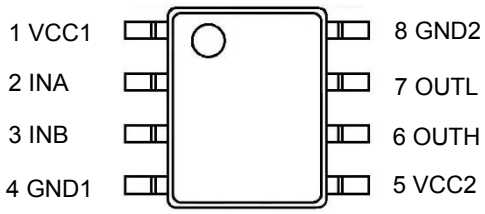
Recommended Range of External Constants

Pin Name	Symbol	Recommended Value			Unit	Conditions
		Min	Typ	Max		
Between VCC1 and GND1	C_{VCC1} *(Note 1)*	0.1	1.0	-	µF	Ceramic capacitors recommended.
Between VCC2 and GND2	C_{VCC2} *(Note1)(Note 2)*	1.0	-	-	µF	Ceramic capacitors recommended. Drive gate capacitance = 1 nF.

(Note 1) C_{VCC1}, C_{VCC2}: The capacitance of the capacitor should be set so that it does not fall below the minimum value in consideration of temperature characteristics and DC bias characteristics.
(Note 2) C_{VCC2}: The capacitance value required to supply the gate drive current for GaN HEMTs.

Pin Configuration

SOP-JW8
(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function
1	VCC1	Input side power supply pin.
2	INA	Control input pin A.
3	INB	Control input pin B.
4	GND1	Input side ground pin.
5	VCC2	Output side power supply pin.
6	OUTH	Source side output pin for gate driving.
7	OUTL	Sink side output pin for gate driving.
8	GND2	Output side ground pin.

1. VCC1 (Input side power supply pin)
   Power supply pin at the input side. Connect a bypass capacitor between GND1 pin and this pin to suppress voltage fluctuations due to the IC's internal transformer drive current.

2. GND1 (Input side ground pin)
   Ground pin at the input side.

3. VCC2 (Output side power supply pin)
   Power supply pin at the output side. Connect a bypass capacitor between GND2 pin and this pin to suppress voltage fluctuations due to gate drive current.

4. GND2 (Output side ground pin)
   Ground pin at the output side.

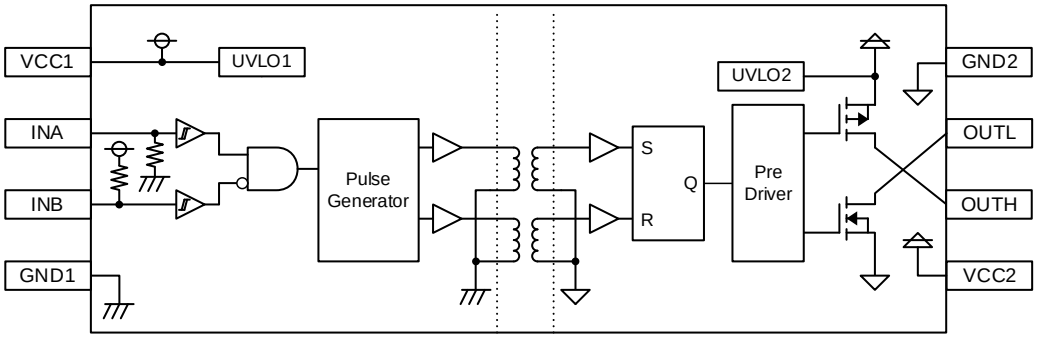
Pin Descriptions – continued

5. INA, INB (Control input pin)
   These pins determine the output logic.
   When INB is fixed to the GND1 pin, the OUTH pin and the OUTL pin are non-inverted from the INA pin.
   The INB pin can be used to disable the drive control.
   The INA pin and the INB pin are the VCC1 pin and the GND1 pin reference inputs, while the OUTH pin and the OUTL pin are the VCC2 pin and the GND2 pin reference outputs.

Input		Output	
INB	INA	OUTH	OUTL
L	L	Hi-Z	L
L	H	H	Hi-Z
H	L	Hi-Z	L
H	H	Hi-Z	L

6. OUTH, OUTL (Output pin for gate drive)
   Output pins for gate drive. The OUTH pin is a source output and the OUTL pin is a sink output.

Block Diagram



Description of Block

1. UVLO1
   This circuit monitors the supply voltage between the VCC1 pin and the GND1 pin at the input side to prevent malfunction at low voltage. When the supply voltage drops below a specified threshold voltage, the OUT pin (when the OUTH pin and the OUTL pin are shorted) is fixed to a 'Low' logic level.

2. INA, INB Input I/O Circuit
   The INA pin has a pull-down resistor to the GND1 pin and the INB pin has a pull-up resistor to the VCC1 pin. When INB = L, the gate drive control signal input from the INA pin is transmitted through a transformer and through to the OUT pin reflecting forward logic.

3. Pulse Generator
   The control signal inputs from the INA pin and the INB pin generate pulse signals that drive the transformer internally. The transformer's output pulse signals then become inputs to the SR latch circuit in the subsequent stage.

4. Isolation Transformer
   This is a built-in transformer circuit integrated to the gate driver that provides isolation between the input and output sides.

5. UVLO2
   This circuit monitors the supply voltage between the VCC2 pin and the GND2 pin at the output side, preventing malfunction at low voltage. When the supply voltage drops below a specified threshold voltage, the OUT pin (when the OUTH pin and the OUTL pin are shorted) is fixed to a 'Low' logic level.

6. Pre Driver
   This circuit drives the PMOS FET and NMOS FET at the final stage, which generates outputs at the OUTH pin and the OUTL pin.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Side Supply Voltage	V_{CC1}	-0.3 to +7.0*(Note 1)*	V
Output Side Supply Voltage	V_{CC2}	-0.3 to +7.0*(Note 2)*	V
INA Pin Input Voltage	V_{INA}	-0.3 to +VCC1+0.3 or +7.0*(Note 1)*	V
INB Pin Input Voltage	V_{INB}	-0.3 to +VCC1+0.3 or +7.0*(Note 1)*	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

(Note 1) Relative to GND1.
(Note 2) Relative to GND2.

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*
Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SOP-JW8				
Input Side Junction to Ambient	θ_{JA1}	202.0	111.6	°C/W
Output Side Junction to Ambient	θ_{JA2}	202.5	111.6	°C/W
Input Side Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT1}	68	48	°C/W
Output Side Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT2}	72	42	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Side Supply Voltage	V_{CC1}*(Note 5)*	4.5	5.0	5.5	V
Output Side Supply Voltage	V_{CC2}*(Note 6)*	4.5	-	6.0	V
Minimum Input Pulse Width (INA, INB)	t_{INMIN}	65	-	-	ns
Operating Temperature	Topr	-40	-	+125	°C

(Note 5) Relative to GND1.
(Note 6) Relative to GND2.

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Unit
Insulation Resistance (V_{IO} = 500 V)	R_S	> 10^9	Ω
Insulation Withstand Voltage (1 min)	V_{ISO}	2500	Vrms
Insulation Test Voltage (1 s)	V_{ISO}	3000	Vrms

Electrical Characteristics

(Unless otherwise specified Ta = -40 °C to +125 °C, V_{CC1} = 4.5 V to 5.5 V, V_{CC2} = 4.5 V to 6.0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Input Side Circuit Current 1	I_{CC11}	0.25	0.46	1.00	mA	INA = L, INB = H
Input Side Circuit Current 2	I_{CC12}	1.20	2.80	6.00	mA	INA = H, INB = L
Output Side Circuit Current 1	I_{CC21}	0.25	0.50	1.00	mA	OUT = L (OUTL = OUTH)
Output Side Circuit Current 2	I_{CC22}	0.20	0.40	0.90	mA	OUT = H (OUTL = OUTH)
Logic Block						
Logic High Level Input Voltage	V_{INH}	2.0	-	V_{CC1}	V	INA, INB
Logic Low Level Input Voltage	V_{INL}	0	-	0.8	V	INA, INB
Logic Pull Down Resistance	R_{IND}	25	50	100	kΩ	INA
Logic Pull Up Resistance	R_{INU}	25	50	100	kΩ	INB
Output						
OUTH ON Resistance (Source)	R_{ONH}	0.60	1.35	3.00	Ω	I_{OUT} = -40 mA
OUTL ON Resistance (Sink)	R_{ONL}	0.25	0.80	1.70	Ω	I_{OUT} = +40 mA
OUT Maximum Current (Source)	$I_{OUTMAXH}$	2.0	3.0	-	A	V_{CC2} = 5 V, Guaranteed by design
OUT Maximum Current (Sink)	$I_{OUTMAXL}$	2.0	3.0	-	A	V_{CC2} = 5 V, Guaranteed by design
Turn-on Propagation Delay Time	t_{PONA}	25	45	60	ns	INA = PWM, INB = L
	t_{PONB}	25	45	60	ns	INA = H, INB = PWM
Turn-off Propagation Delay Time	t_{POFFA}	25	45	60	ns	INA = PWM, INB = L
	t_{POFFB}	25	45	60	ns	INA = H, INB = PWM
Propagation Delay Distortion	t_{PDISTA}	-10	0	+10	ns	t_{POFFA} - t_{PONA}
	t_{PDISTB}	-10	0	+10	ns	t_{POFFB} - t_{PONB}
Part-to-part Skew	t_{SK-PP}	-	-	12	ns	Same temperature, Guaranteed by design
Output Rise Time	t_{RISE}	-	8	-	ns	OUT - GND2 = 1 nF
Output Fall Time	t_{FALL}	-	8	-	ns	OUT - GND2 = 1 nF
Common Mode Transient Immunity	V_{CMTI}	150	-	-	kV/μs	V_{CM} = 1500 V, Guaranteed by design
Protection Functions						
VCC1 UVLO OFF Voltage	V_{UVLO1H}	3.35	3.50	3.65	V	At VCC1 pin voltage rising
VCC1 UVLO ON Voltage	V_{UVLO1L}	-	3.40	-	V	At VCC1 pin voltage falling
VCC1 UVLO Hysteresis Voltage	$V_{UVLOHYS1}$	0.05	0.10	0.20	V	V_{UVLO1H} - V_{UVLO1L}
VCC1 UVLO Mask Time	$t_{UVLO1MSK}$	1.0	2.5	4.0	μs	
VCC2 UVLO ON Voltage	V_{UVLO2L}	3.7	3.9	4.1	V	At VCC2 pin voltage falling
VCC2 UVLO OFF Voltage	V_{UVLO2H}	-	4.2	-	V	At VCC2 pin voltage rising
VCC2 UVLO Hysteresis Voltage	$V_{UVLOHYS2}$	0.2	0.3	0.4	V	V_{UVLO2H} - V_{UVLO2L}
VCC2 UVLO Mask Time	$t_{UVLO2MSK}$	1.0	3.0	6.0	μs	

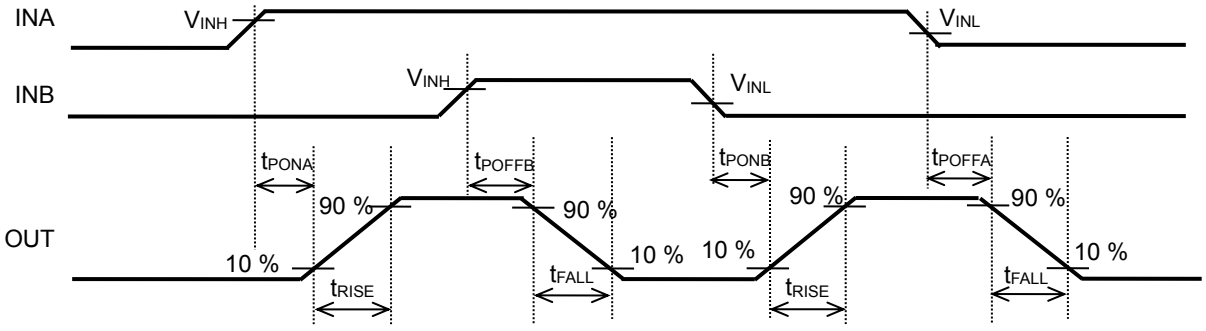


Figure 2. Input/Output Operation Timing Chart

Typical Performance Curves

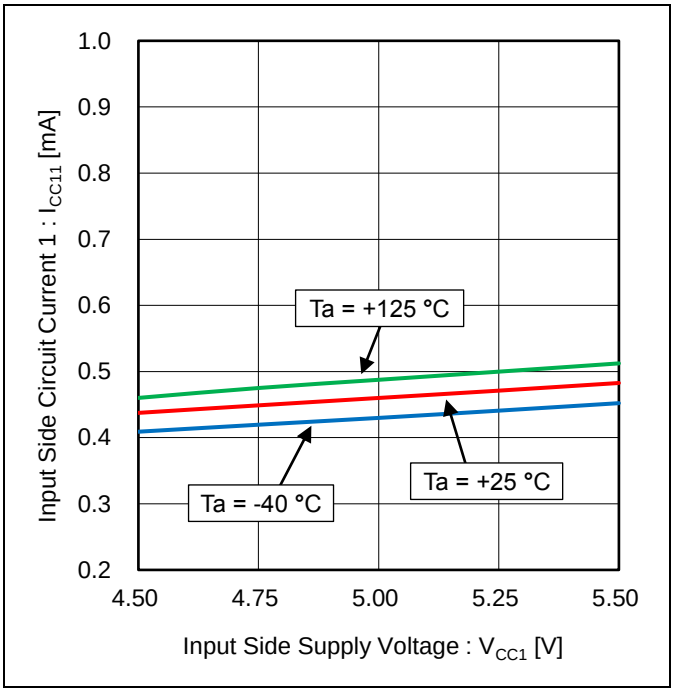


Figure 3. Input Side Circuit Current 1 vs Input Side Supply Voltage

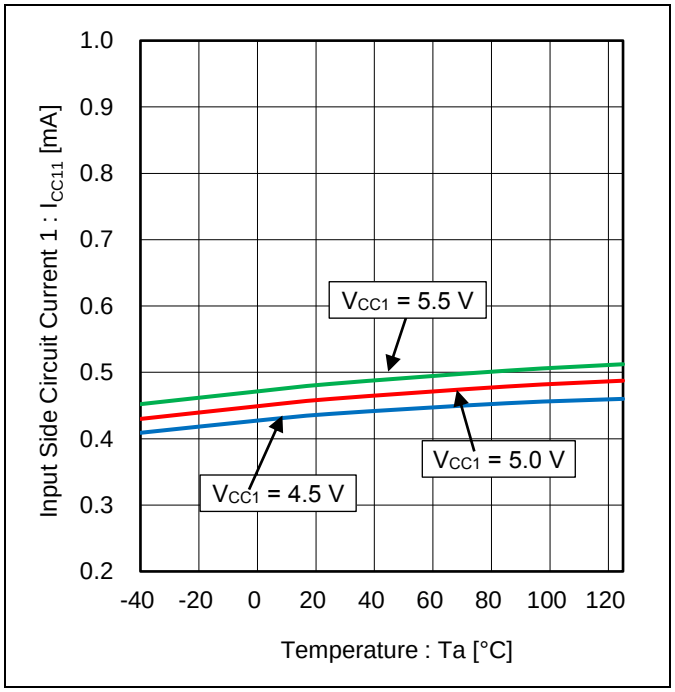


Figure 4. Input Side Circuit Current 1 vs Temperature

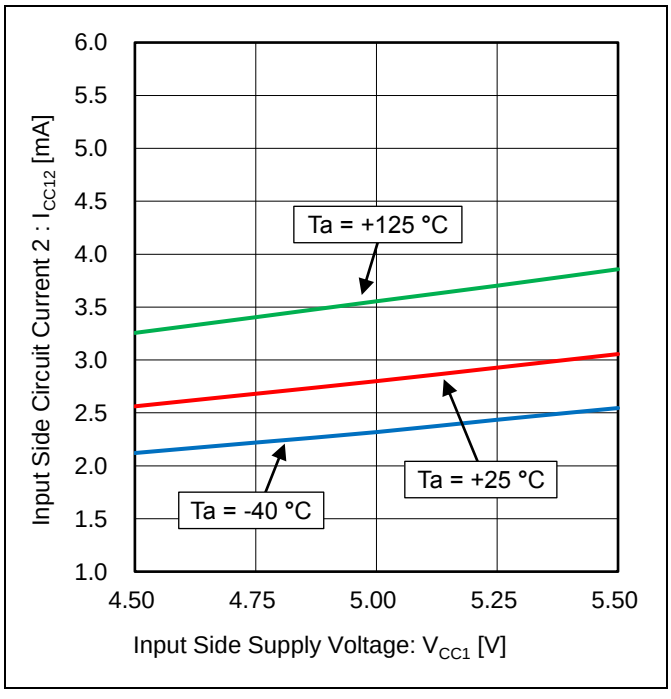


Figure 5. Input Side Circuit Current 2 vs Input Side Supply Voltage

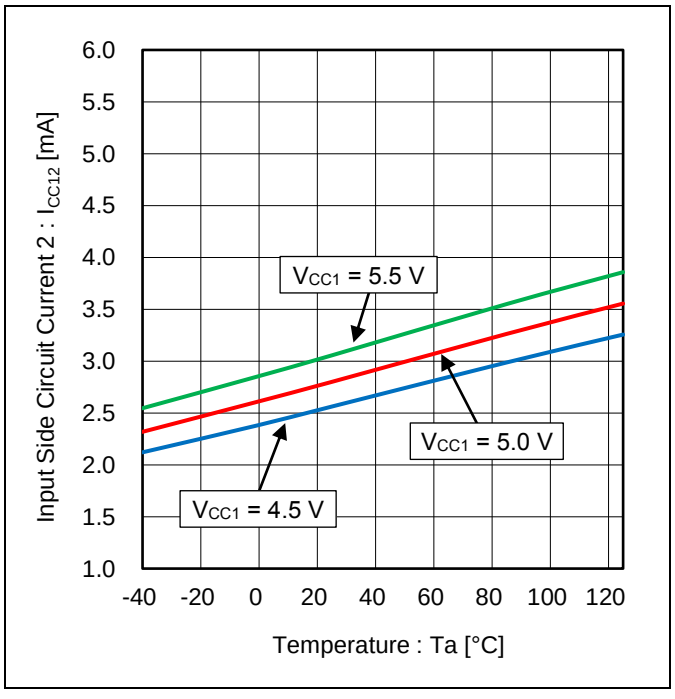


Figure 6. Input Side Circuit Current 2 vs Temperature

Typical Performance Curves – continued

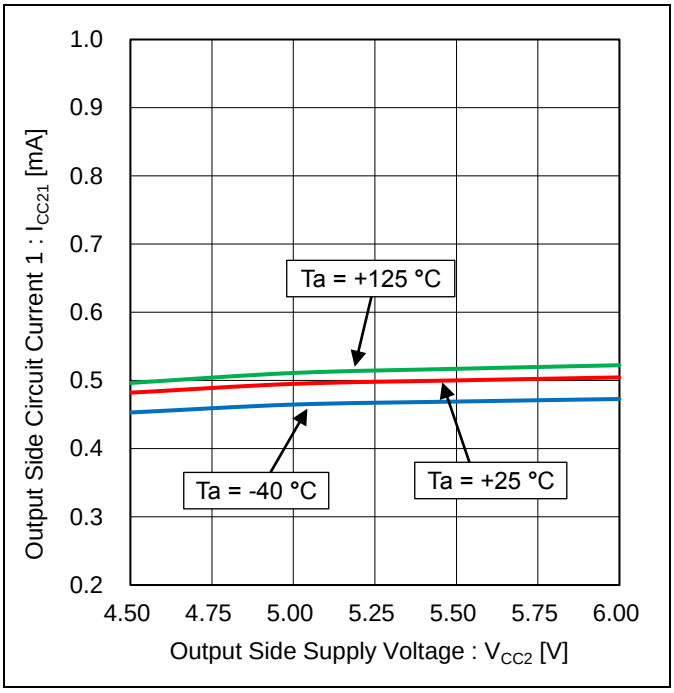


Figure 7. Output Side Circuit Current 1 vs Output Side Supply Voltage (OUT = L)

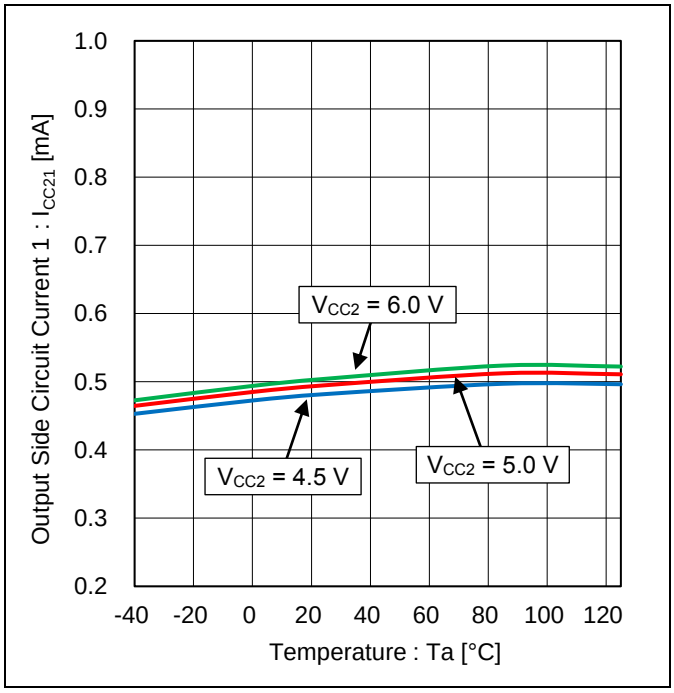


Figure 8. Output Side Circuit Current 1 vs Temperature (OUT = L)

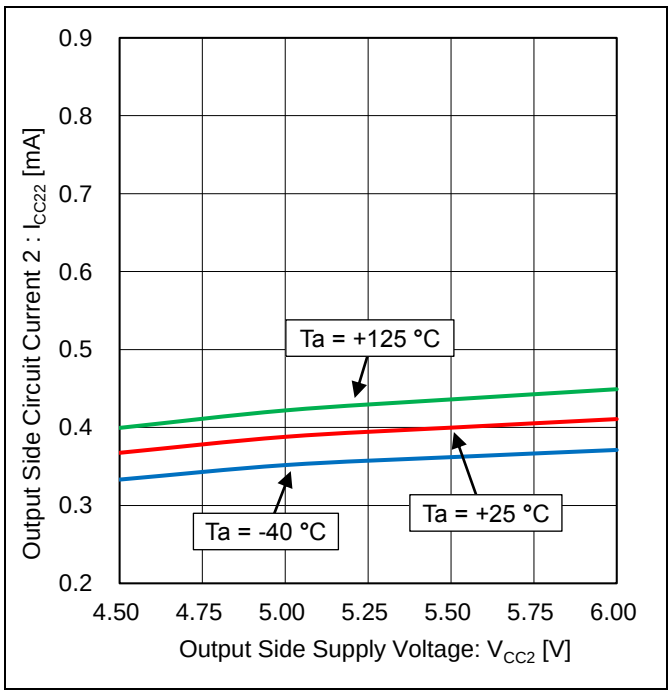


Figure 9. Output Side Circuit Current 2 vs Output Side Supply Voltage (OUT = H)

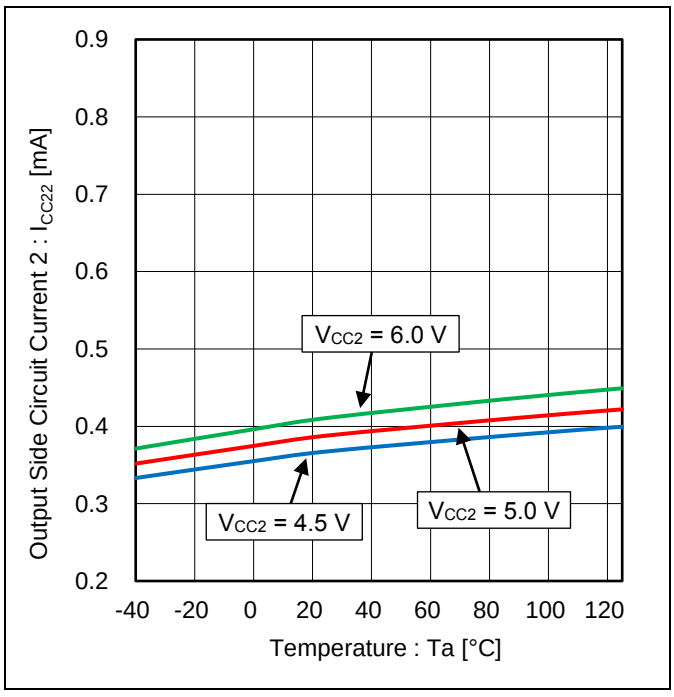


Figure 10. Output Side Circuit Current 2 vs Temperature (OUT = H)

Typical Performance Curves – continued

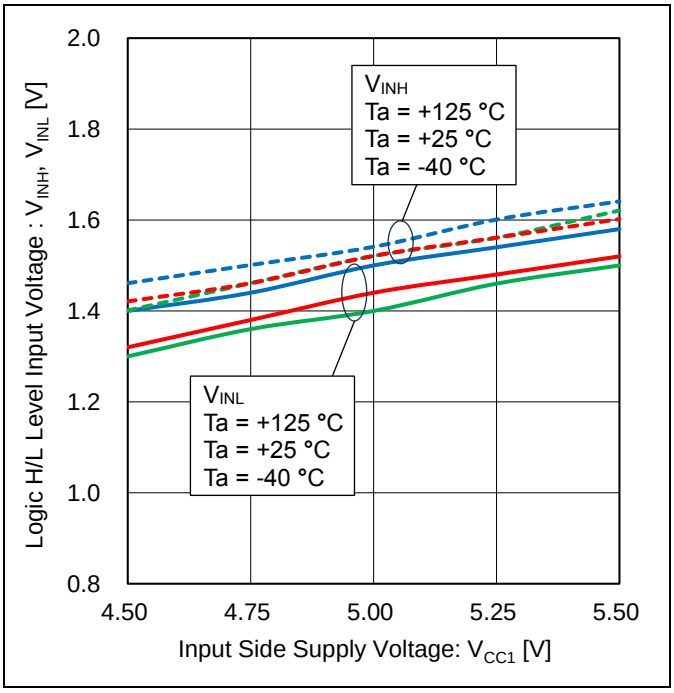


Figure 11. Logic (INA/INB) H/L Level Input Voltage vs Input Side Supply Voltage

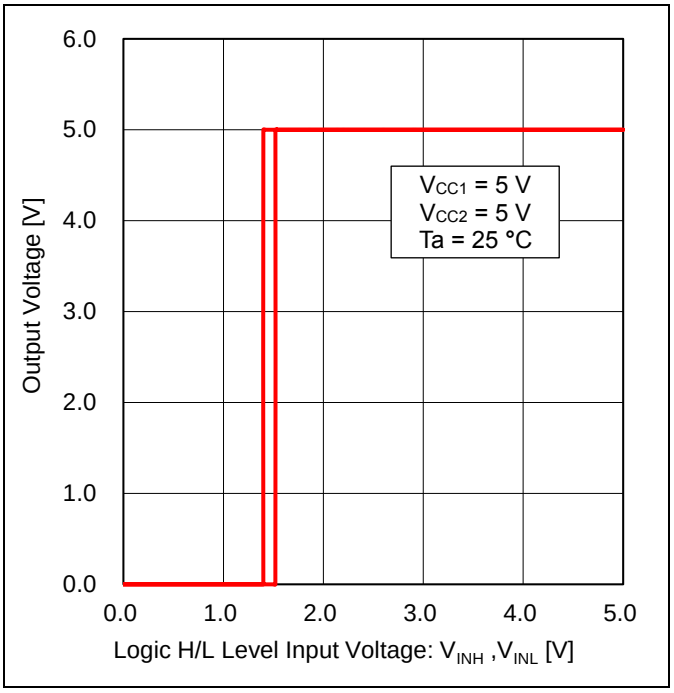


Figure 12. Output Voltage vs Logic H/L Level Input Voltage (V_{CC1} = 5 V, V_{CC2} = 5 V, Ta = 25 ˚C)

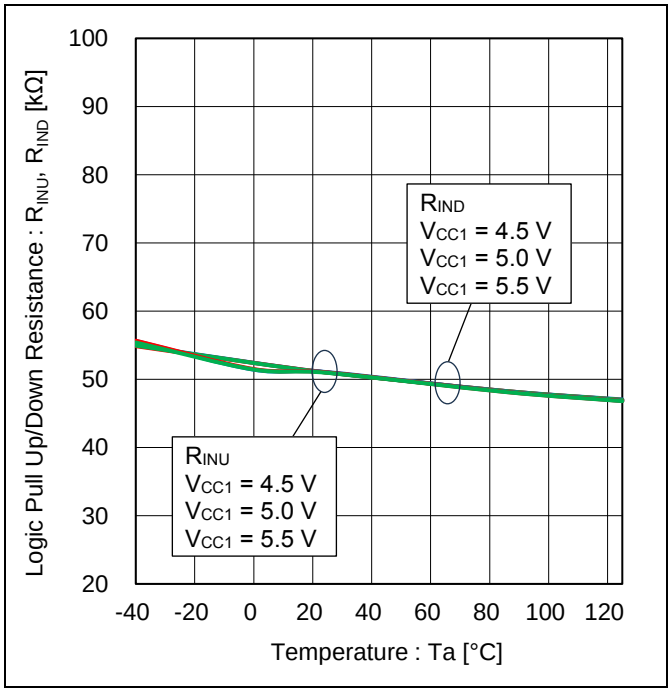


Figure 13. Logic Pull Up/Pull Down Resistance vs Temperature

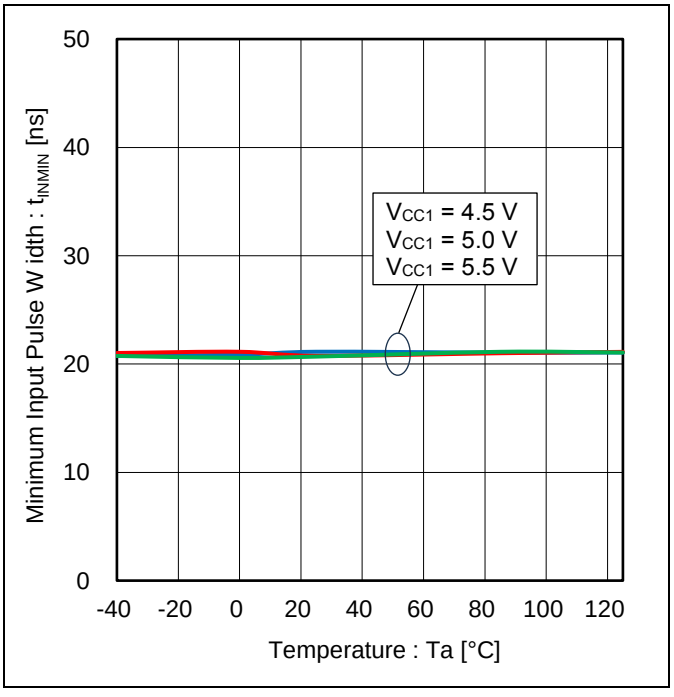


Figure 14. Minimum Input Pulse Width vs Temperature

Typical Performance Curves – continued

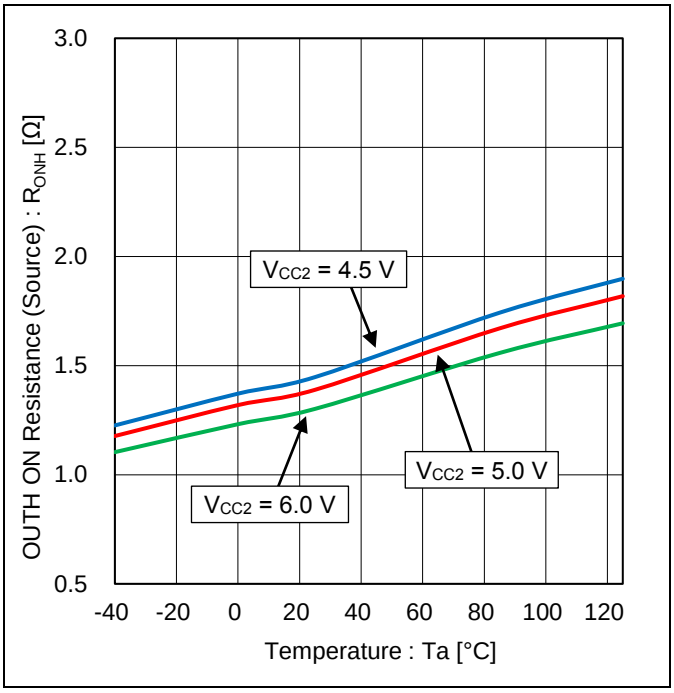


Figure 15. OUTH ON Resistance (Source) vs Temperature

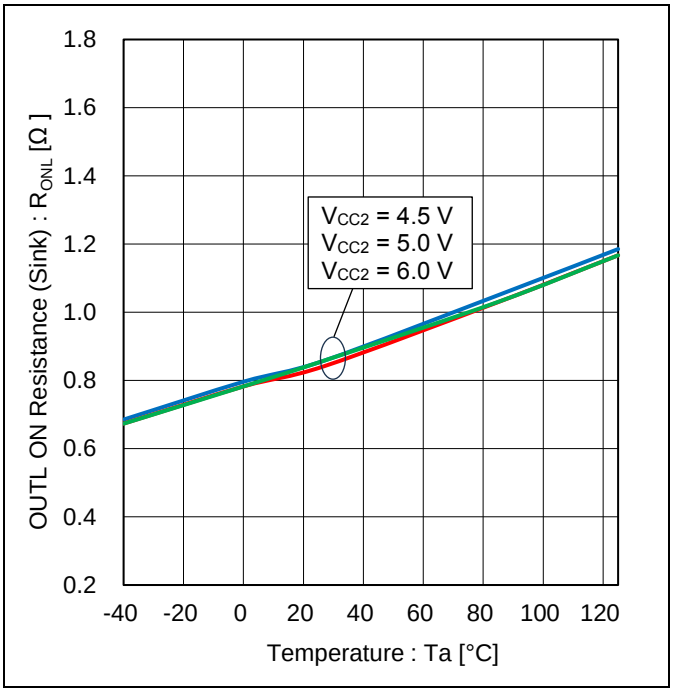


Figure 16. OUTL ON Resistance (Sink) vs Temperature

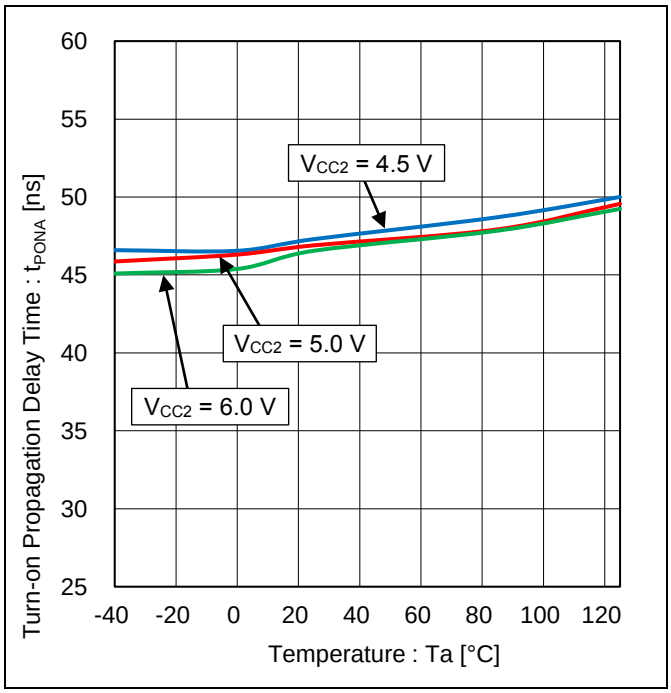


Figure 17. Turn-on Propagation Delay Time vs Temperature (INA = PWM, INB = L)

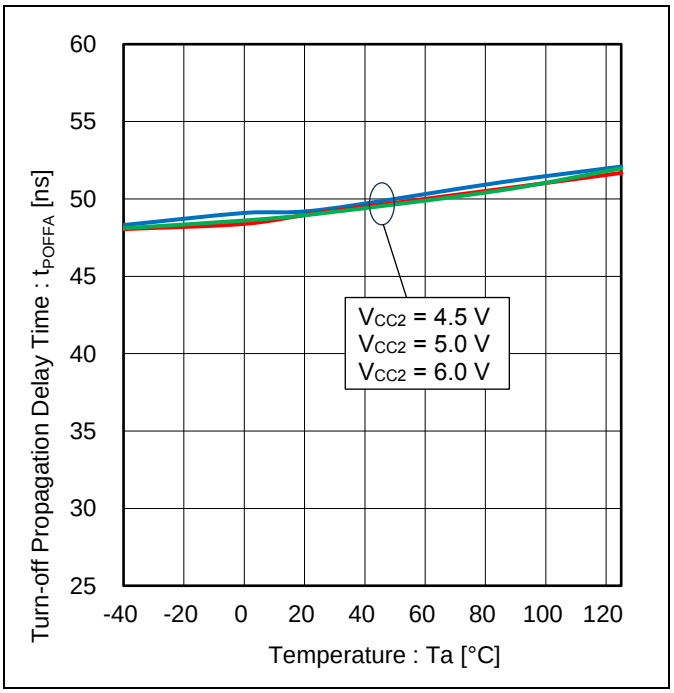


Figure 18. Turn-off Propagation Delay Time vs Temperature (INA = PWM, INB = L)

Typical Performance Curves – continued

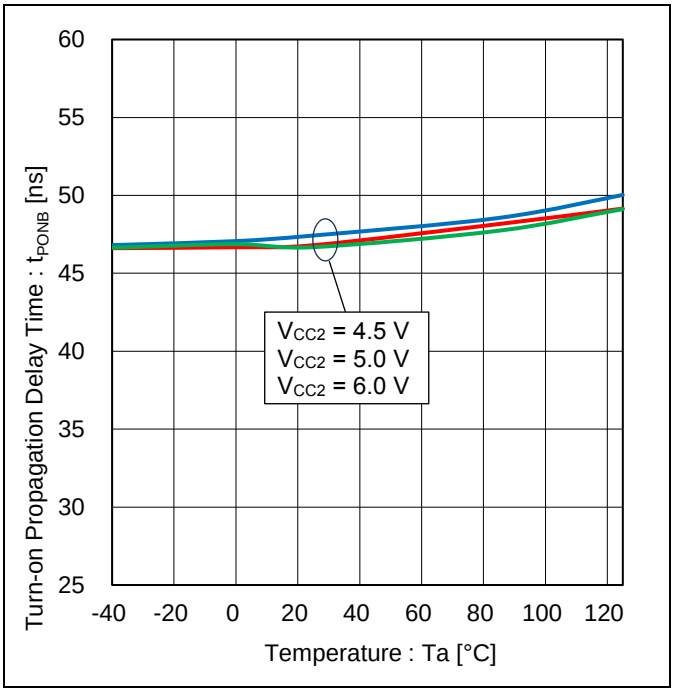


Figure 19. Turn-on Propagation Delay Time vs Temperature (INA = H, INB = PWM)

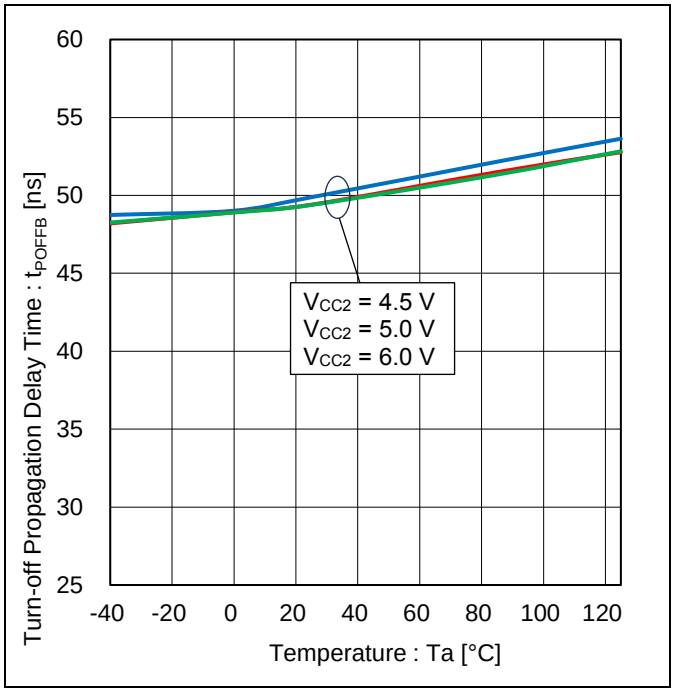


Figure 20. Turn-off Propagation Delay Time vs Temperature (INA = H, INB = PWM)

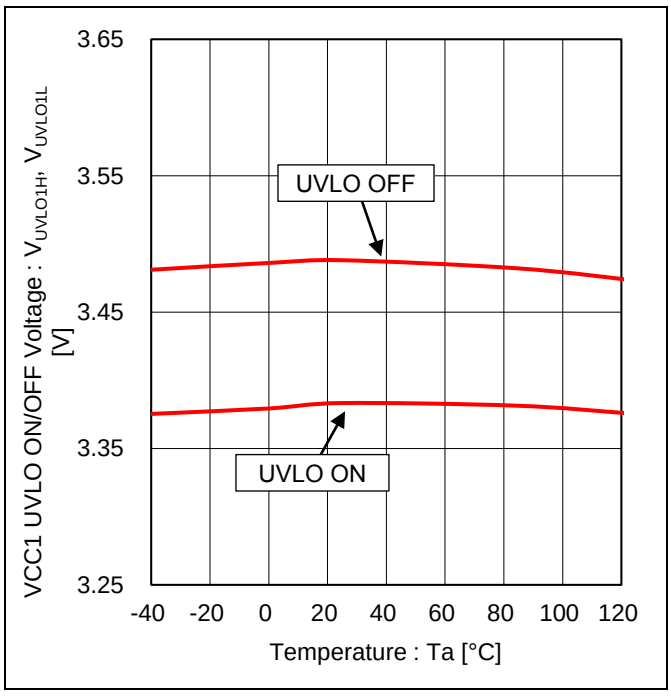


Figure 21. VCC1 UVLO ON/OFF Voltage vs Temperature

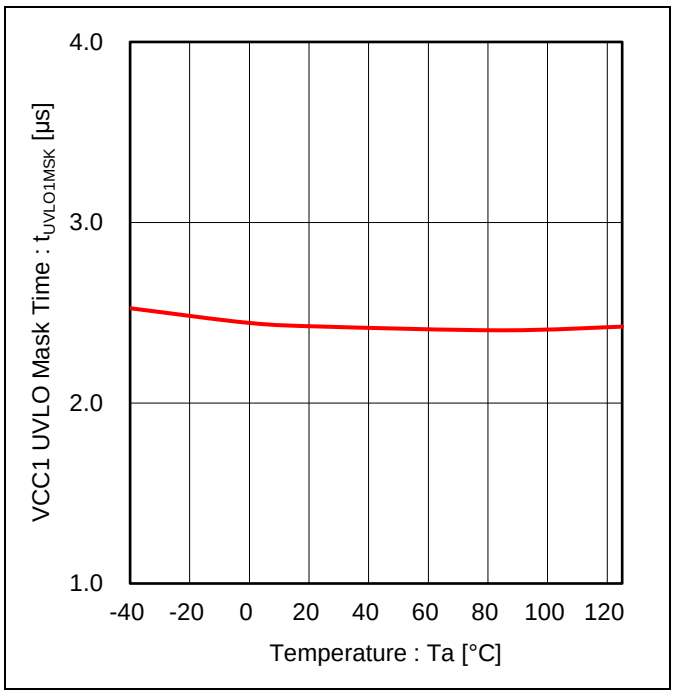


Figure 22. VCC1 UVLO Mask Time vs Temperature

Typical Performance Curves – continued

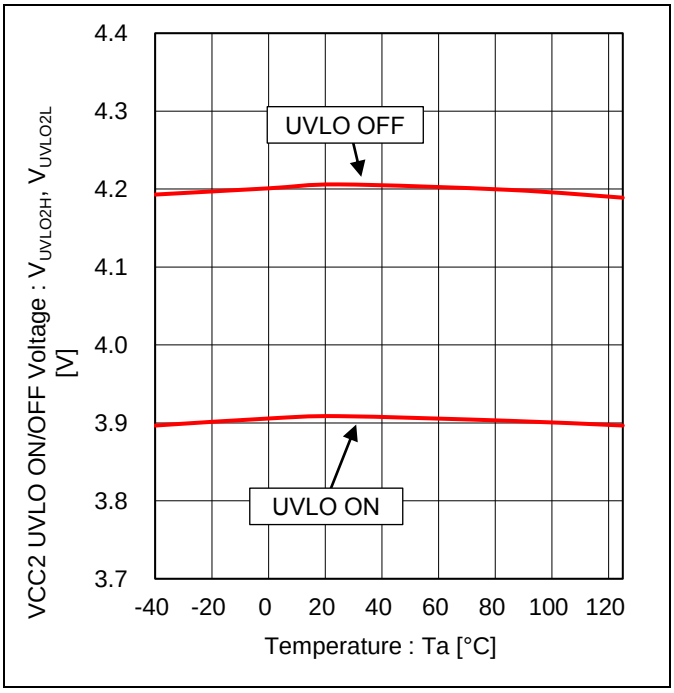


Figure 23. VCC2 UVLO ON/OFF Voltage vs Temperature

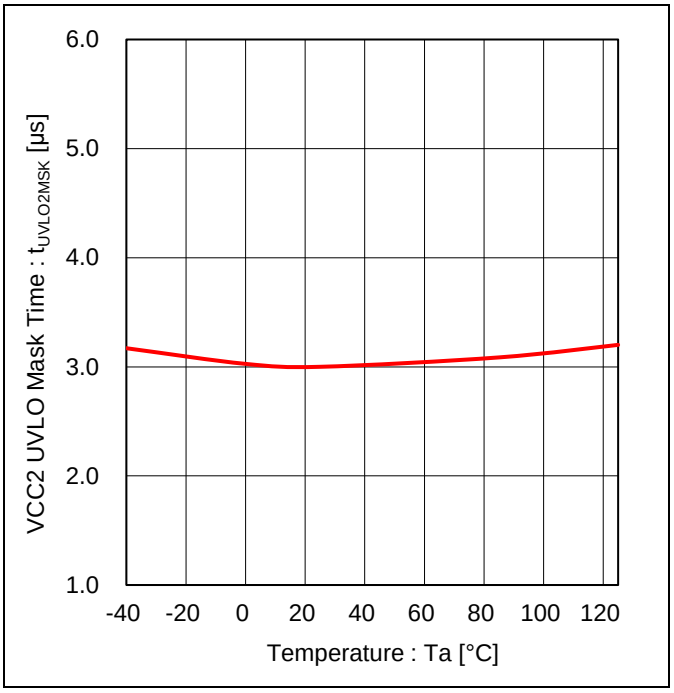


Figure 24. VCC2 UVLO Mask Time vs Temperature

Timing Chart

1. Under-voltage Lockout (UVLO) Function

Each VCC pin at the input and output side of BM6GD11BFJ-LB has built-in protection to prevent malfunction at low voltage. When the supply voltage drops below the UVLO ON voltage (Typ 3.4 V at the input side, Typ 3.9 V at the output side), the gate drive voltage becomes a 'Low' logic level state. When the supply voltage rises above the UVLO OFF voltage, the IC returns to the normal state. To prevent malfunction due to noise, mask times $t_{UVLO1MSK}$ (Typ 2.5 µs) and $t_{UVLO2MSK}$ (Typ 3.0 µs) are integrated at both the input and output sides. After UVLO is released at the input side, the OUT pin (where the OUTL pin and the OUTH pin are shorted) = H can be generated after the next input signal switching time.

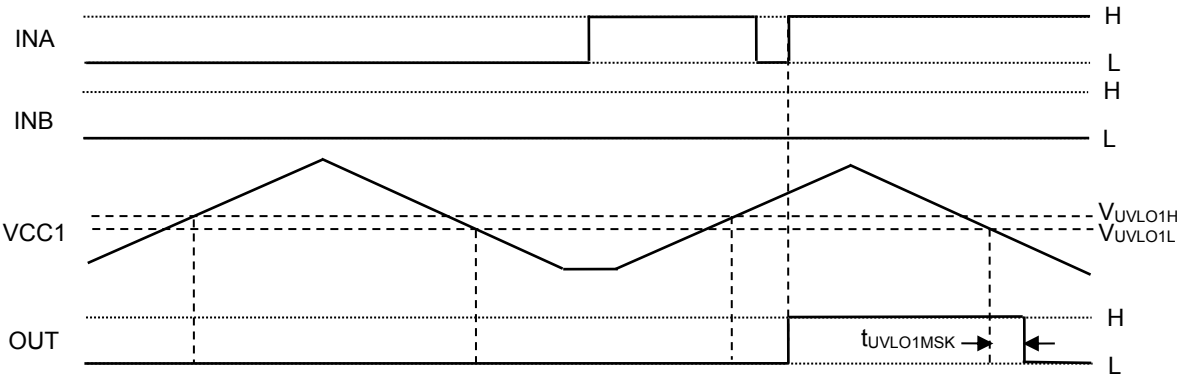


Figure 25. Input Side UVLO Function Operation Timing Chart

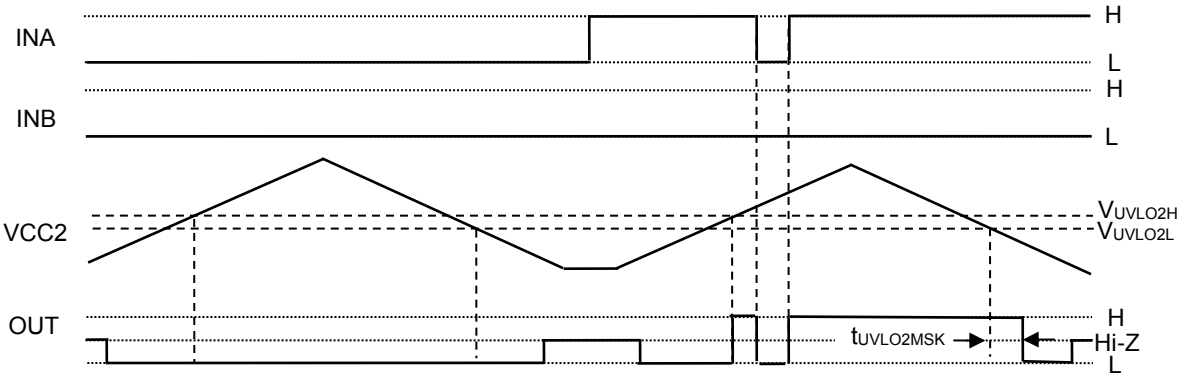


Figure 26. Output Side UVLO Function Operation Timing Chart

Timing Chart – continued

2. Input/Output Condition Table

No.	Status	Input				Output	
		VCC1	VCC2	INB	INA	OUTH	OUTL
1	VCC1UVLO	UVLO	X	X	X	Hi-Z	L
2	VCC2UVLO	X	UVLO	X	X	Hi-Z	L
3	INB Active	○	○	H	X	Hi-Z	L
4	Normal operation INA = L input	○	○	L	L	Hi-Z	L
5	Normal operation INA = H input	○	○	L	H	H	Hi-Z

○: VCC1 or VCC2 > UVLO, X: Don't care

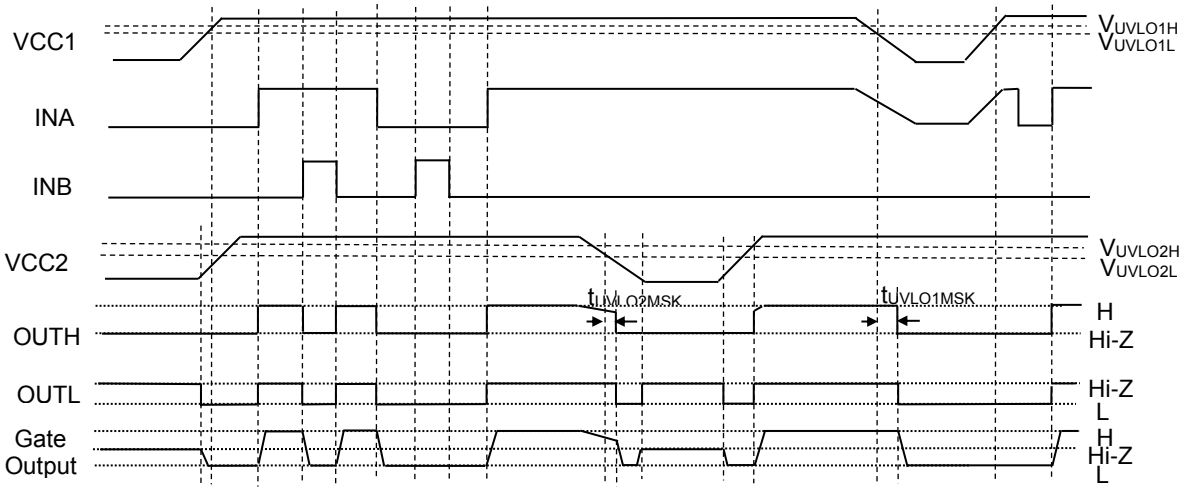


Figure 27. Input-Output Timing Chart

Application Example

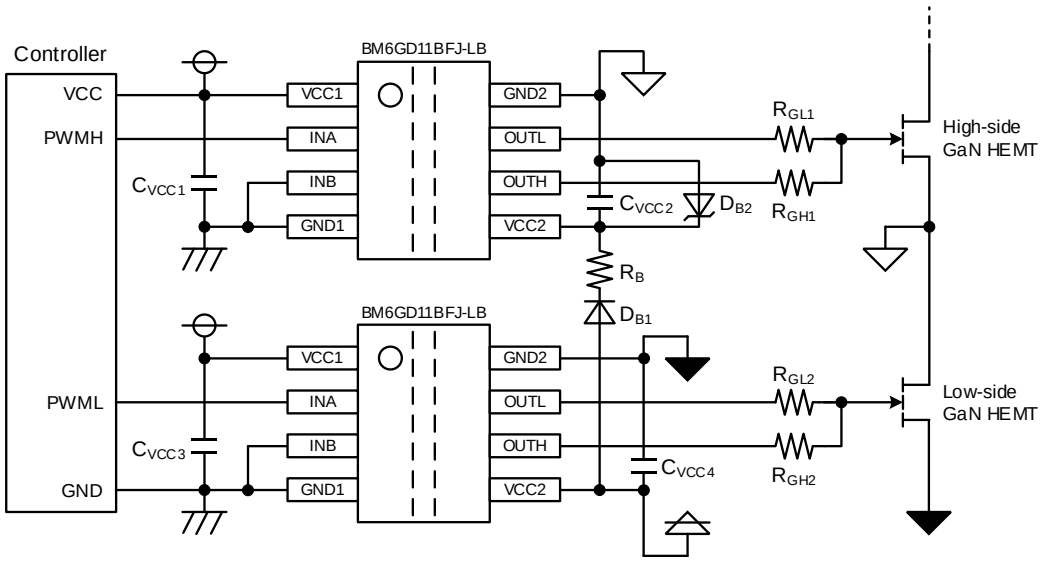


Figure 28. GaN HEMT Drive Application Circuit (Half-bridge configuration)

This gate driver has separate output driver pins for the source and sink sides, and the slew rate of the rising and falling edge of the switching waveform can be individually adjusted by inserting resistors between the gate pins of the GaN HEMT.
The gate resistors R_{GH}/R_{GL} should be selected according to the switching speed of the power device.
Since the switching time (t_{SW}) is taken as the time it takes for the voltage to finish leveling off, the turn-on gate resistance R_{GH} is calculated by the following equation.

$$I_G = \frac{Q_{gs}+Q_{gd}}{t_{SW}} \quad [A] \quad [1]$$

$$R_{TOTAL(ON)} = R_{PON} + R_{GH} = \frac{VCC-V_{GS(TH)}}{I_G} \quad [\Omega] \quad [2]$$

$$t_{SW} = \frac{Q_{gs}+Q_{gd}}{I_G} = \frac{(Q_{gs}+Q_{gd})(R_{PON}+R_{GH})}{(VCC-V_{GS(TH)})} \quad [s] \quad [3]$$

Where:
I_G is the Current through the gate of a power device.
Q_{gs} is the Gate-Source charge of power devices.
Q_{gd} is the Gate-to-drain charge of power devices.
$V_{GS(TH)}$ is the Threshold voltage of power devices.

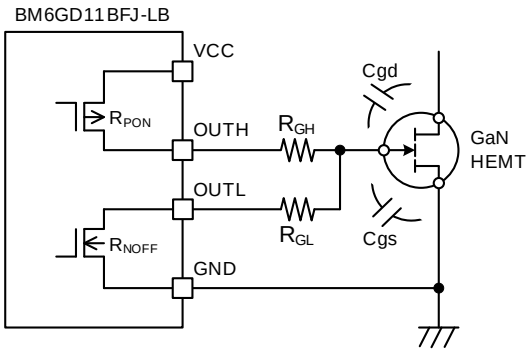


Figure 29. Gate Drive Equivalent Circuit

Application Example – continued

The slew rate (dV_D/dt) at the output can be determined by the turn-on gate resistance value. The slew rate of a power device uses the following equation.

$$\frac{dV_D}{dt} = \frac{I_G}{C_{rss}} \quad [V/s] \quad [4]$$

Where:
C_{rss} is the Feedback capacitance of power devices.

Substituting equation [4] into equation [2], the gate resistance becomes

$$R_{TOTAL(ON)} = R_{PON} + R_{GH} = \frac{VCC - V_{GS(TH)}}{C_{rss} \times \frac{dV_D}{dt}} \quad [\Omega] \quad [5]$$

$$R_{GH} = \frac{VCC - V_{GS(TH)}}{C_{rss} \times \frac{dV_D}{dt}} - R_{PON} \quad [\Omega] \quad [6]$$

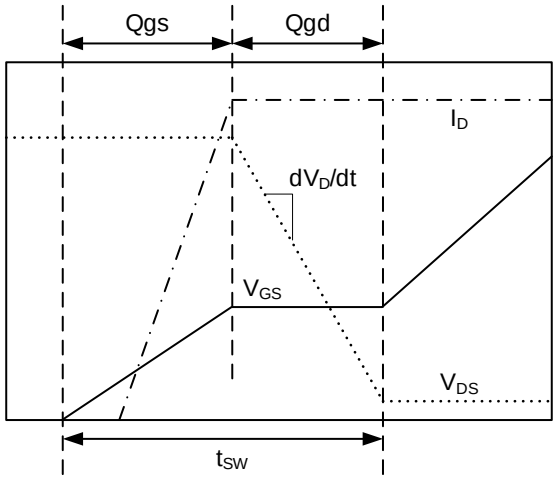


Figure 30. Gate Charging Characteristics of Power Devices

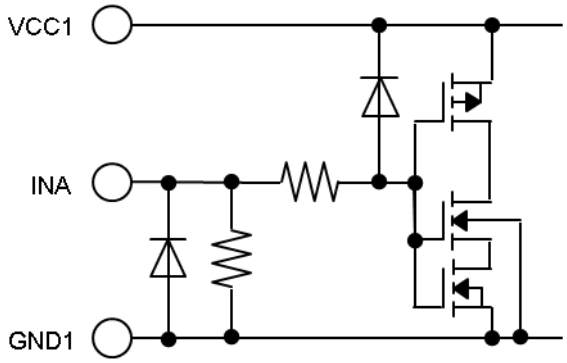
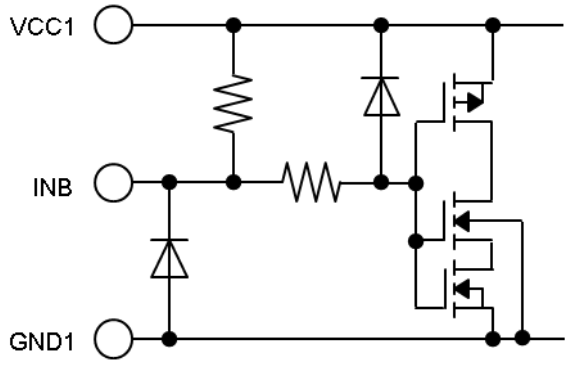
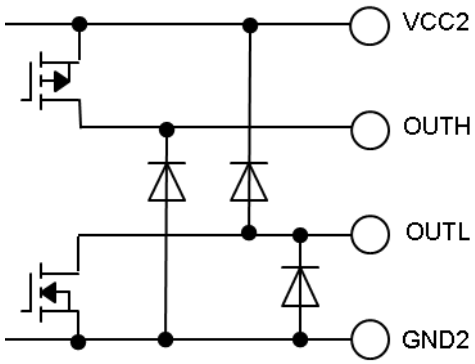
When a power device is off, current flows through Cgd when another power device turns on. At this time, the gate resistance value (R_{GL}) should be set so that the gate voltage does not exceed the threshold (and cause self-turn on).

$$V_{GS(TH)} \geq (R_{NOFF} + R_{GL}) \times I_G = (R_{NOFF} + R_{GL}) \times C_{gd} \times \frac{dV_D}{dt} \quad [V] \quad [7]$$

$$R_{GL} \leq \frac{V_{GS(TH)}}{C_{gd} \times \frac{dV_D}{dt}} - R_{NOFF} \quad [\Omega] \quad [8]$$

Each set value obtained from the above formulas should be determined after a thorough evaluation with consideration to the design margin.

I/O Equivalence Circuits

Pin No	Pin Name (Pin Function)	I/O Equivalence Circuits
2	INA (Control input pin A)	
3	INB (Control input pin B)	
6	OUTH (Source side output pin)	
7	OUTL (Sink side output pin)	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

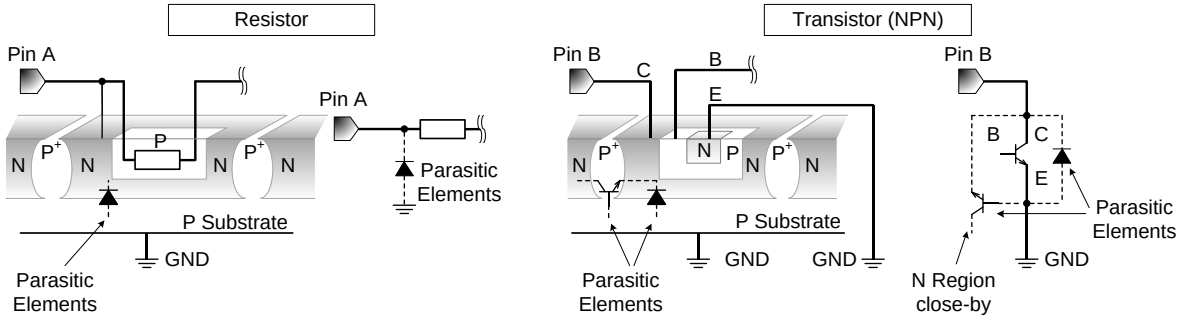


Figure 31. Example of IC Structure

11. Ceramic Capacitor

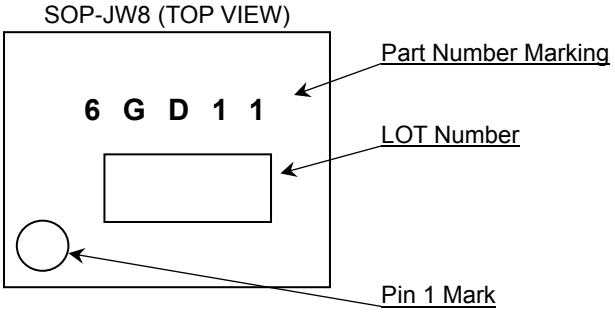
When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

B M 6 G D 1 1 B F J	-	L B E 2

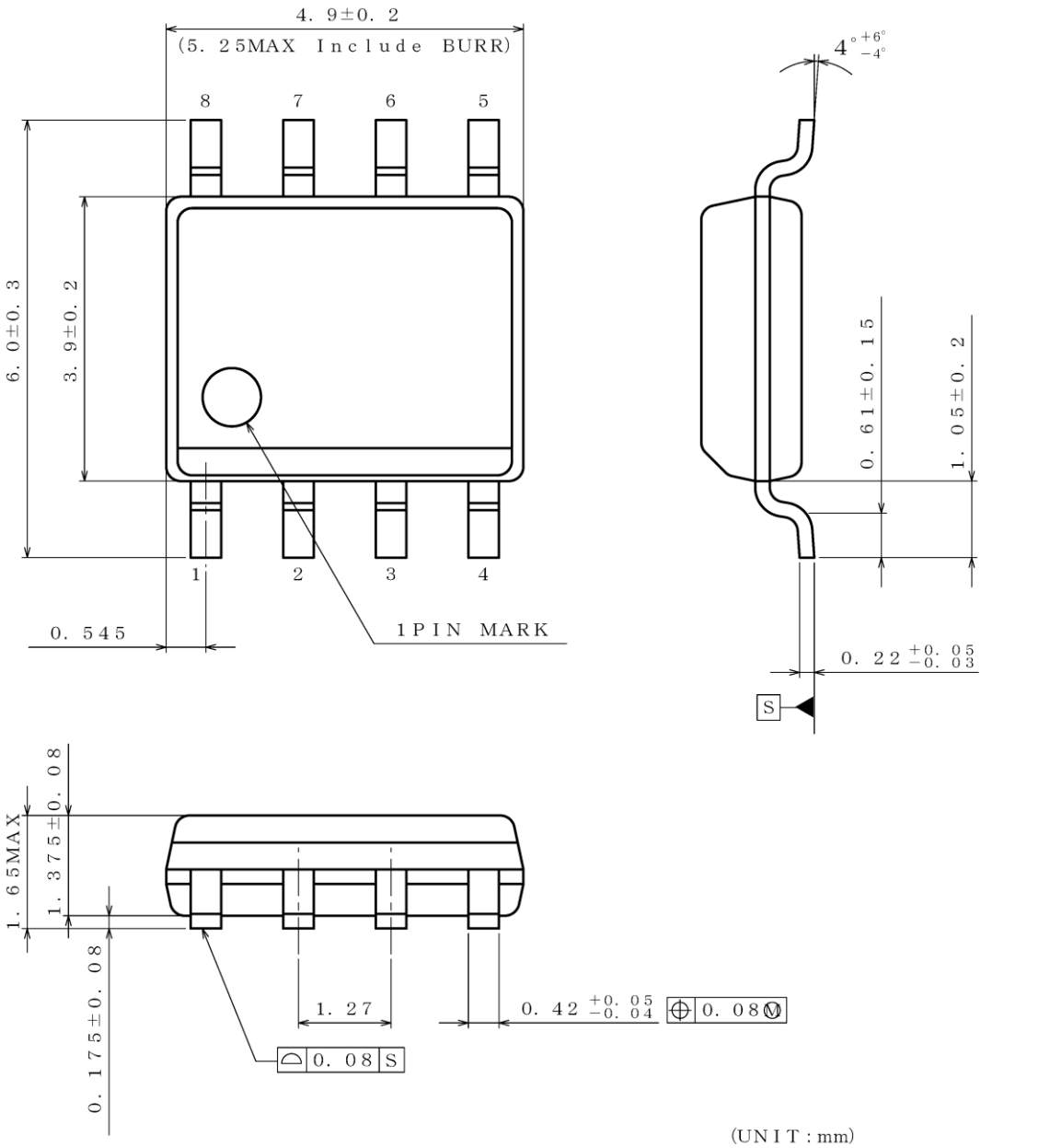
- Part Number
- Package
  FJ: SOP-JW8
- Product Class
  LB for Industrial Applications
  Packaging and forming specification
  E2: Embossed tape and reel

Marking Diagram



Physical Dimension and Packing Information

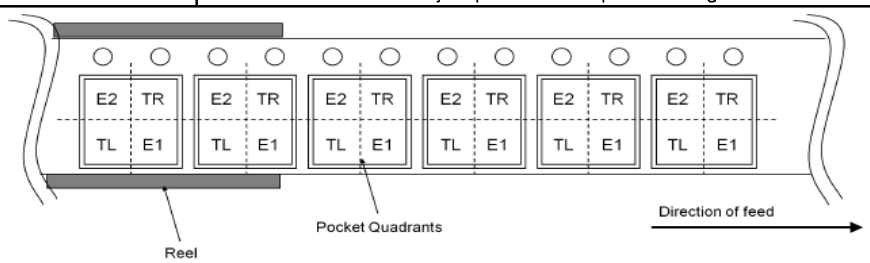
Package Name	SOP-JW8



(UNIT : mm)
PKG : SOP−JW8
Drawing No. EX084−5002

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
25.Nov.2024	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

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   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

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