DATE: July 14, 2025

PCN #: 2742

PCN Title: Additional AT Site CAT, Die/FAB Change with Data Sheet Change, Bump Process Change

Dear Customer:

This is an announcement of change(s) to products that are currently being offered by Diodes Incorporated.

We request that you acknowledge receipt of this notification within 30 days of the date of notification by contacting your local Diodes sales representative. If you require samples for evaluation purposes, please submit a corresponding request within 30 days as well. Otherwise, samples may not be built prior to the implementation of the announced change(s).

The change(s) announced in this PCN will not be implemented prior to the target implementation date, i.e. 90 days from the stated notification date, unless Diodes receives written customer approval before that date.

Previously agreed upon customer specific product and/or process change requirements will be addressed separately.

For questions or clarification regarding this PCN, please contact your local Diodes sales representative.

Sincerely,

Diodes Incorporated PCN Team

PRODUCT CHANGE NOTICE PCN-2742-REV1

Notification Date:	Implementation Date:	Product Family:	Change Type:	PCN #:
July 14, 2025	October 13, 2025	Analog	Additional AT Site CAT, Die/FAB Change with Data Sheet Change, Bump Process Change	**2742**

TITLE

Additional AT Site CAT, Die/FAB with Data Sheet Change, Bump Process Change

DESCRIPTION OF CHANGE

This PCN is being issued to notify customers that in order to assure continuity of supply, Diodes Incorporated has qualified additional Diodes internal A/T Site CAT located in Chengdu, China, a Die/Fab Change (Die UX31F62001 fabricated by Seiko Epson located in Suwa-Gun, Nagano, Japan to Die UX3AF62002 fabricated by SK Key Foundry FAB4 in Cheongju, South Korea) resulting in a Datasheet Spec Limit Change (Output Duty Cycle), a change to the Bump Process from Solder Printing to Solder Plating, and change in wafer backside processing from Wafer Backside Coating (WBC) to Wafer Backside Lamination (WBL).

Full electrical characterization and reliability testing have been completed on representative part numbers to ensure there is no change to product reliability, device functionality or electrical specifications in the datasheet unless specified in Table 1 and Table 1A below.

IMPACT

Continuity of Supply - There will be no change to the Form, Fit, or Function of affected products unless specified.

PRODUCTS AFFECTED

Table 1 – Die/FAB Change - UX31F62001 fabricated by Seiko Epson located in Suwa-Gun, Nagano, Japan to Die UX3AF62002 fabricated by SK Key Foundry FAB4 in Cheongju, South Korea) resulting in a Datasheet Spec Limit Change (Output Duty Cycle); see Table 1A

Table 2 - Change to Bump Process (Remove Ni)

Table 3 - Additional AT Site (CAT) with PdCu wire

Table 4 - Change Bumping Process (Solder Printing to Solder Plating), and Change in wafer backside processing from Wafer Backside Coating (WBC) to Wafer Backside Lamination (WBL).

WEB LINKS

Manufacturer's Notice:	https://www.diodes.com/quality/product-change-notices/diodes-product-change-notices/
For More Information Contact:	https://www.diodes.com/about/contact-us/contact-sales/
Data Sheet:	https://www.diodes.com/catalog/

DISCLAIMER

Unless a Diodes Incorporated Sales representative is contacted in writing within 30 days from the notification date of this PCN, all changes described in this announcement are considered approved.

Table 1 – Die/FAB Change - UX31F62001 (Epson) to UX3AF62002 (Key Foundry FAB4) resulting in Datasheet Spec Limit Change (Output Duty Cycle) See Table 1A					
PI6CXG06F62AFBEIEX					

Table 2 - Change Bump Process (Remove Ni)					
AP62150WU-7	AP62200TWU-7	AP62200WU-7	AP62201WU-7		

Table 3 - Additional AT Site (CAT) with PdCu wire					
74AUP2G04FZ4-7	74AUP2G06FZ4-7	74AUP2G07FZ4-7	74AUP2G14FZ4-7	74AUP2G17FZ4-7	74AUP2G3404FZ4-7
74AUP2G34FZ4-7	74AVC1T45FZ4-7	74LVC1G3157FZ4-7	74LVC1T45FZ4-7	AZV3001AFZ4-7	AZV3001FZ4-7

Table 4 - Change Bumping Process (Solder Printing to Solder Plating) and Wafer Backside Coating from WBC to WBL					
AP7350-12CF4-7	AP7350-15CF4-7	AP7350-185CF4-7	AP7350-18CF4-7	AP7350-25CF4-7	AP7350-27CF4-7
AP7350-28CF4-7	AP7350-30CF4-7	AP7350-33CF4-7	AP7350-45CF4-7	AP7350D-12CF4-7	AP7350D-15CF4-7
AP7350D-185CF4-7	AP7350D-18CF4-7	AP7350D-23CF4-7	AP7350D-25CF4-7	AP7350D-27CF4-7	AP7350D-28CF4-7
AP7350D-30CF4-7	AP7350D-33CF4-7	AP7350D-45CF4-7			

Table 1A

Current Datasheet (rev 1)

AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Clock output frequency			156.25		MHz
F_{STAB}	Frequency stability				±25	ppm
T_r	Output rise time	From 20% to 80%		150		ps
T_f	Output fall time	From 80% to 20%		150		ps
T_{ODC}	Output duty cycle	Generator mode	48		52	%
V_{PP}	Output swing Single-ended	LVPECL outputs	400			mV
		LVDS outputs	250			
		HCSL outputs	520			
T_{PHASEJ}	Phase jitter RMS	LVPECL		0.07	0.1	ps
		LVDS		0.09	0.12	
		HCSL		0.09	0.15	
V_{CROSS}	Absolute crossing voltage	HCSL	160		460	mV
DV_{CROSS}	Total variation of crossing voltage	HCSL			140	mV
T_{SK}	Output Skew	6 outputs devices, outputs in same bank, with same load, at DUT.		40		ps
T_{OD}	Valid to HiZ		200			ns
T_{OE}	HiZ to valid		200			ns
T_{start}	Start-Up Time	Counted from V_{DD} reaches 90%			10	ms

New Datasheet (rev 2)

AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Clock output frequency			156.25		MHz
F_{STAB}	Frequency stability				±25	ppm
T_r	Output rise time	From 20% to 80%		150		ps
T_f	Output fall time	From 80% to 20%		150		ps
T_{ODC}	Output duty cycle	Generator mode	45		55	%
V_{PP}	Output swing Single-ended	LVPECL outputs	400			mV
		LVDS outputs	250			
		HCSL outputs	520			
T_{PHASEJ}	Phase jitter RMS	LVPECL		0.07	0.1	ps
		LVDS		0.09	0.12	
		HCSL		0.09	0.15	
V_{CROSS}	Absolute crossing voltage	HCSL	160		460	mV
DV_{CROSS}	Total variation of crossing voltage	HCSL			140	mV
T_{SK}	Output Skew	6 outputs devices, outputs in same bank, with same load, at DUT.		40		ps
T_{OD}	Valid to HiZ		200			ns
T_{OE}	HiZ to valid		200			ns
T_{start}	Start-Up Time	Counted from V_{DD} reaches 90%			10	ms