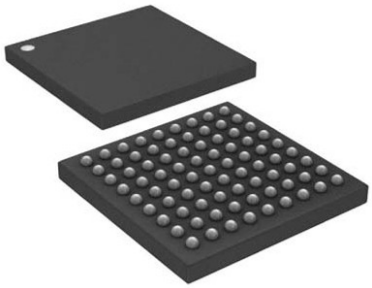
STA8135G

Datasheet

Teseo V family industrial triple-band multi-constellation GNSS precise engine receiver



TFBGA160 7x11x1.2 mm
0.65 mm ball pitch

Product status link
STA8135G

Product summary
Order code
STA8135GTR
Temperature range
-40 °C to +85 °C
Package
TFBGA160 7x11x1.2 mm
Packing
Tray, Tape and reel

Features

- STMicroelectronics 5th generation positioning receiver with 80 tracking channels and 4 fast acquisition channels compatible with 6 constellations: GPS, Galileo, GLONASS, BeiDou, QZSS, NAVIC (former IRNSS)
- Triple band L1, L2, L5, E6 and L-band single package solution
- SBAS systems: WAAS, EGNOS, MSAS, GAGAN, BeiDou
- Code phase, carrier phase, doppler frequency measurement
- Antenna sensing
- PPS output
- Notch filter for anti-jamming
- ARM® Cortex® M7 core:
  - Maximum clock frequency 314 MHz
  - 16 kB I-cache and 16 kB D-cache
  - 64 kB I-TCM and 384 kB D-TCM, core clock speed
  - Nested vector interrupt controller
  - JTAG debugging capability
  - 256 Kbyte system RAM
- 32-channel DMA
- Memory interfaces:
  - SFC (Octal/Quad serial flash controller, SDR)
  - SD multimedia card
- Serial interfaces:
  - 3 x UART
  - Synchronous serial port (SPI supported)
  - I^2C
  - 2x multimode serial interfaces
  - 2x CAN controllers
- Core peripherals:
  - 2x multi-timer units
  - Watchdog timer
  - 1x extended function timers
  - 32 kHz oscillator real-time clock
  - AES decipher hardware accelerator
- Power management unit, with separate power supply domain and on-chip LDO and high voltage/low voltage monitors:
  - Backup voltage domain 1.62 to 3.6 V with LDO for always-on core supply and HV/LV detectors, and dedicated IO-ring0
  - Main voltage domain 1.62 to 3.6 V with LDO for switchable logic domain and HV/LV detectors for 85 °C maximum ambient temperature operations
  - Separate RF domain with dedicated LDO
  - IO-ring1 1.8 or 3.3 V capable, and dedicated 1.8 V LDO
  - IO-ring2 3.3 V ±10% capable
  - Fail-safe GPIOs available

- Secure-digital multimedia memory card interfaces (SDMMC)
- USB 2.0 full speed (12 Mb/s) with integrated physical layer transceiver
- ESD: 2 kV (HBM) and 500 V (CDM)

Description

The STA8135G is part of the Teseo V family and it is a multi-band multi-constellation positioning receiver IC able to manage all the GNSS constellations such as GPS, Galileo, GLONASS, BeiDou, NAVIC (former IRNSS) and QZSS, in L1, L2, L5, and E6 frequency bands.

1 Overview

The STA8135G is part of the Teseo V family: it is a MultiChipModule (MCM) combining both STA8100GA and STA5635A in a single package.

It is a multi-band multi-constellation positioning receiver IC able to manage all the GNSS constellations such as GPS, Galileo, GLONASS, BeiDou, NAVIC (former IRNSS) and QZSS, in L1, L2, L5, and E6 frequency bands.

The STA8135G is able to manage most of the GNSS bands (L1, L2, L5, E6) allowing even to receive simultaneously three frequencies L1/L2/L5 or L1/L5/E6 in a single package without the need of any external RF front-end.

The STA5635A integrated RF front-end supports L-band corrections signal reception.

It provides the precise raw measurements of all the visible GNSS satellites to the main host via serial interface to let any possible precise position algorithm run. STA8135G also provides an autonomous precision positioning calculation to the main host using all the satellites constellations.

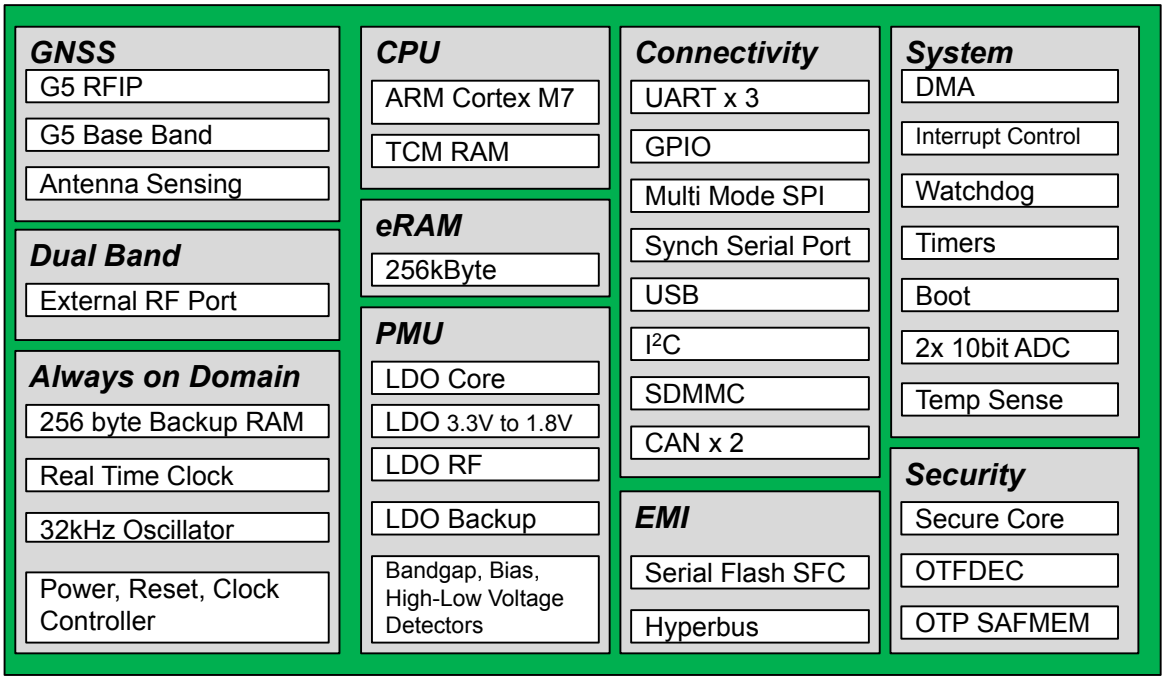
It embeds separated LDOs to supply the analog parts, the digital core, and the IO ring of the device facilitating requirements to external power supply.

The chip is manufactured in CMOS technology and housed in a TFBGA package 160 balls 7x11 mm body size 0.65 mm pitch.

2 Block diagram and pin description

2.1 Block diagram

Figure 1. **STA8135G block diagram**



2.2 Package

TFBGA160 balls with 7x11x1.2 mm body size and 0.65 mm ball pitch.

2.3 Ball list

Note: All balls have alternate functionalities, which can be selected by relevant registers.

Table 1. **Power supply pins**

Symbol	I/O voltage	I/O	Description	Ball
VRF_IN	1.62 to 3.6 V	PWR	LDO RF power input - IO ring RF	M10
VRF_OUT	1.2 V	PWR	LDO RF power output	N10
VCC_LNA	1.2 V	PWR	LNA power input	T10
VCC_PLL	1.2 V	PWR	RF VCC power input	T8
VBK_IN(1)	1.62 to 3.6 V	PWR	LDO backup power input - IO ring 0	R6
VBK_OUT	1.2 V	PWR	LDO backup power output	N5
VCORE_IN	1.62 to 3.6 V	PWR	LDO core power input	F3, P3
VDD_EXT_REG	1.2 V	PWR	LDO core power output	F1, N4, N7, R2, R3
VIO2_IN	3 to 3.6 V	PWR	LDO IO ring 2 power input - IO ring 2	G1, H1, J10
VIO1_EXT	1.72 to 1.98 V or 3 to 3.6 V	PWR	LDO IO ring 1 power output or IO ring 1 input	M3, N3, P2, T2

Symbol	I/O voltage	I/O	Description	Ball
V2V5_OUT	2.5 V	PWR	LDO core 2.5 V output	F5
GND_PMU	GND	GND	Main voltage regulator ground	G2
GND_BKP_PMU	GND	GND	Backup voltage regulator ground	P5
GND_TSENS	GND	GND	Temperature sense block ground	D10
GND_RF	GND	GND	RF ground	P9, R9, M8, N8, P8, R8
GND	GND	GND	Ground	F8, M7, N6, M4, E3, E4, T3, F2
LDO_1V1_OUT_0(2)	1.1 V	PWR	LDO 1.1 V OUT_0	A1
PLL_VCCp_0(2)	1.2 V	PWR	RF VCC_0 power input	A3
LDO_RF_OUT_1V1_0(2)	1.1 V	PWR	LDO RF_0 power output	A4
LDO_IN_3V3_1V8_0(2)	1.70 or 3.6 V	PWR	LDO RF_0 power input - (LDO_RFin_0)	A5
RFA_IF_VCC_0(2)	1.2 V	PWR	RFA_IF_VCC_0	A7
LNA_VCC_0(2)	1.2 V	PWR	LNA_VCC_0	A9
RF_GND_0(2)	GND	GND	RF_GND_0	B5, B6, B7, B8, B9, C7
GND_0(2)	GND	GND	GND_0	B4, C4, D3, D5
LDO_1V8_OUT_0(2)	1.8 V	PWR	LDO_1V8_OUT_0	B1
LDOS_VCC_0(2)	3 to 3.6 V	PWR	LDO_0 power input	C1
LNA_GND_0	GND	GND	LNA ground	A10, C10

1. *Backup power shall be applied at the same time or before VCORE_IN, not after.*
2. *Pins names with trailing _0 are related to RF chip.*

Table 2. Main function pins

Symbol	I/O voltage(1)	I/O	Description	Ball	Reset state
EXT_REG_SEL	VCORE_IN	I	LDO core disable. When high, the LDO Core is off. The Core must be supplied by an external power through VDD_EXT_REG balls.	C3	NA
TEST	IOring2	I	TEST - JTAG enable. In mission/application mode this pin must be connected to GND.	D4	Hi-Z/PD
RTC_XTI	VBK_IN/IOring0	I	If 32 kHz oscillator is enabled then input of the 32 kHz oscillator amplifier circuit. Else CMOS input as electrical characteristic table. Both cases, it is the reference for real time clock counter circuitry.	T5	NA
RTC_XTO	VBK_IN/IOring0	O	Output of the oscillator amplifier circuit.	T6	NA
RESETn	VBK_IN/IOring0	I	Reset input with Schmitt-Trigger characteristics and noise.	R5	Hi-Z/PD
WAKEUP	VBK_IN/IOring0	I	When high, the device will wakeup and exit from standby mode. It has higher priority compared to Standby_in pin. Wakeup from standby mode.	P6	Hi-Z
STANDBY_IN(2)	VBK_IN/IOring0	I	When low, the chip is forced in standby mode.	R7	Hi-Z
STANDBY_OUT	VBK_IN	O	When low, it indicates the device is in standby mode.	P7	Hi-Z

1. *In standby mode , if VIO1 and VIO2 are powered, GPIOs have no driving capabilities and no PD/PU is active.*
2. *If VCORE_IN is removed before STANDBY_IN has switched from high to low, STANDBY_OUT remains high level, even if device enters in standby mode.*

Table 3. RF front-end pins

Symbol	I/O voltage	I/O	Description	Ball
ANTSens2/AIN1	IO ring RF	I	Antenna sensing - TPp_S1	M9
ANTSens1/AIN0	IO ring RF	I	Antenna sensing - TPn_S2	N9
LNA_IN	LNA VCC	I	LNA input	T9
LNA_OUT	LNA VCC	O	LNA output	R10
RFA_IN	VRFOUT	I	RFA input	P10
TCXO_IN	PLL VCC	I	TCXO input	T7
XTAL_IN_0	PLL VCC	I	TCXO_0 input	A2
RFA_IN_0	VRFOUT	I	RFA_0 input	A6
LNA_OUT_0	LNA_VCC_0	O	LNA_0 output	A8
LNA_IN_0	LNA_VCC_0	I	LNA_0 input	B10
TP_N_SENSE2_0	IO ring RF	I	Antenna sensing - TPIF_N_0	B2
TP_P_SENSE1_0	IO ring RF	I	Antenna sensing - TPIF_P_0	B3
CHIP_EN_0	IO ring RF	I	Chip_En_0	C2
TCXO_CLK_0	PLL_VCCp_0	I	TCXO_CLK_0 input	D1

Table 4. RF chip reserved

Symbol	I/O voltage(1)	I/O	Description	Ball
Reserved8	IO ring1 (FS)	I	Reserved8	K6
Reserved7	IO ring1 (FS)	I/O	Reserved7 - ball L6 works as SPI slave interrupt pin in case the integrated STA5635 is used for L-band correction reception	L6
Reserved6	IOring1 (FS)	I	Reserved6	H6
Reserved5	IO ring1 (FS)	I	Reserved5	J2
Reserved4	IO ring1 (FS)	I	Reserved4	J3
Reserved3	IO ring1 (FS)	I	Reserved3	E6
Reserved2	IOring1 (FS)	I	Reserved2	F6
Reserved1	IO ring1 (FS)	I	Reserved1	K4

1. *(FS) Fail Safe IO*

Table 5. Communication interface pins

Symbol	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
GPIO6	IO ring 2 (FS)	I/O	Default	GPIO 6	-	D2	PD
		I	ALT A	CAN0_RX	CAN receiver		-
		O	ALT B	-	-		-
		I/O	ALT C	I2C_SDA	I_2C data		-
GPIO5	IO ring 2 (FS)	I/O	Default	GPIO 5	-	G3	PD
		O	ALT A	CAN0_TX	CAN transmitter		-
		I	ALT B	SFC_DQS	Serial flash controller DQS		-
		I/O	ALT C	I2C_CLK	I^2C clock		-
GPIO32	IO ring 2 (FS)	I/O	Default	GPIO 32	-	E8	PD

Symbol	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
GPIO32	IO ring 2 (FS)	O	ALT A	-	-	E8	-
		O	ALT B	UART0_TX	UART0 transmitter		-
		O	ALT C	PPS_OUT	Pulse per second output		-
MSP1_clk_out	IO ring 1 (FS)	I/O	Default	GPIO 91	-	L3	PD
		O	ALT A	MSP1_clk_out	MSP1 master clock		-
		I	ALT B	SPI_CLK	SPI clock		-
		O	ALT C	CLK_OUT	Clock output		-
MSP1_CS	IO ring 1 (FS)	I/O	Default	GPIO 90	-	M5	PD
		I/O	ALT A	MSP1_CS	MSP1 master chip select		-
		I	ALT B	SPI_CSn	SPI chip select		-
		I	ALT C	UART2_RX	UART2 receiver		-
MSP1_Din	IO ring 1 (FS)	I/O	Default	GPIO 94	-	L4	PD
		I	ALT A	MSP1_Din	MSP1 data input		-
		I	ALT B	SPI_SI	SPI chip select		-
		O	ALT C	OCTOSPI_CLKn	Octo SPI clock inverted		-
MSP1_Dout	IO ring 1 (FS)	I/O	Default	GPIO 95	-	L5	PD
		O	ALT A	MSP1_Dout	MSP1 data output		-
		O	ALT B	SPI_SO	SPI data output		-
		O	ALT C	UART2_TX	UART2 transmitter		-
JTAG-TRSTn	IO ring 2 (FS)	I/O	Default	JTAG-TRSTn/GPIO 0	JTAG reset	D7	PD
		O	ALT A	PPS_OUT	Pulse per second output		-
		I	ALT B	-	-		-
		I	ALT C	Timer_OCMPA	Timer A input		-
JTAG-TCK	IO ring 2 (FS)	I/O	Default	JTAG-TCK/GPIO 1	JTAG clock	C8	PD
		I	ALT A	SPI_CK	SPI slave clock		-
		O	ALT B	MSP0_clk_out	MSP0 master clock		-
		I	ALT C	Timer_ICAPA1	Timer A input		-
JTAG-TMS	IO ring 2 (FS)	I/O	Default	JTAG-TMS/GPIO 2	JTAG TMS	D6	PU
		I	ALT A	SPI_CS	SPI slave chip select		-
		O	ALT B	MSP0_Din	MSP0 data input		-
		O	ALT C	UART0_RTS	UART0 RTS		-
JTAG-TDI	IO ring 2 (FS)	I/O	Default	JTAG-TDI/GPIO 3	JTAG data input	D8	PU
		I	ALT A	SPI_SI	SPI data input		-
		I/O	ALT B	MSP0_Dout	MSP0 data output		-
		O	ALT C	UART0_CTS	UART0 CTS		-
JTAG-TDO	IO ring 2 (FS)	I/O	Default	JTAG-TDO/GPIO 4	JTAG data output	E7	PD
		O	ALT A	SPI_SO	SPI data output		-
		O	ALT B	MSP0_CS	MSP0 chip select		-
		I	ALT C	PPS_IN	PPS input		-
UART1_RX	IO ring 2	I/O	Default	USB_DM	USB minus	K8	PD
		I	ALT A	UART1_RX	UART1 receiver		-

Symbol	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
UART1_RX	IO ring 2	I/O	ALT B	I2C_SDA	I²C data	K8	-
		I	ALT C	CAN1_RX	CAN1 receiver		-
UART1_TX	IO ring 2	I/O	Default	USB_DP	USB positive	K9	PD
		O	ALT A	UART1_TX	UART1 transmitter		-
		I/O	ALT B	I2C_CLK	I²C clock		-
		O	ALT C	CAN1_TX	CAN1 transmitter		-
UART2_RX	IO ring 2 (FS)	I/O	Default	GPIO 89	-	E1	PD
		I	ALT A	UART2_RX	UART2 receiver		-
		I/O	ALT B	-	-		-
		O	ALT C	-	-		-
UART2_TX	IO ring 2 (FS)	I/O	Default	GPIO 88	-	E2	PD
		O	ALT A	UART2_TX	UART2 transmitter		-
		I/O	ALT B	-	-		-
		O	ALT C	-	-		-
GPIO67	IO ring 2	I/O	Default	GPIO 67	-	C9	PD
		O	ALT A	-	-		-
		I/O	ALT B	UART0_RX	UART0 receiver		-
		I	ALT C	PPS_IN	Pulse per second input		-
GPIO8	IO ring 2	I/O	Default	GPIO 8	-	C5	PD
		I	ALT A	MII_TX_EN	-		-
		O	ALT B	i_g5rf_MONITOR_LDO_sig	-		-
		O	ALT C	I_sign2	-		-
GPIO7	IO ring 2	I/O	Default	GPIO 7	-	C6	PD
		O	ALT A	MII_TX_CLK	-		-
		O	ALT B	i_g5rf_MONITOR_PLL_sig	-		-
		O	ALT C	I_sign	-		-
GPIO43	IO ring 2	I/O	Default	GPIO 43	-	E5	PD
		O	ALT A	Timer_ICAPA	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO92	IO ring 2	I/O	Default	GPIO 92	-	F10	PD
		I	ALT A	MSP1_clk_in	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO77	IO ring 2	I/O	Default	GPIO 77	-	F4	PD
		I	ALT A	CAN1_RX	-		-
		-	ALT B	MII_PTP_AUX_TS_TRIG0	-		-
		-	ALT C	-	-		-
GPIO48	IO ring 2	I/O	Default	GPIO 48	-	F7	PD
		O	ALT A	MSP0_clk_out	-		-
		-	ALT B	-	-		-

Symbol	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
GPIO48	IO ring 2	-	ALT C	-	-	F7	-
GPIO76	IO ring 2	I/O	Default	GPIO 76	-	G4	PD
		O	ALT A	CAN1_TX	-		-
		-	ALT B	MII_MDC_O	-		-
		-	ALT C	-	-		-
GPIO47	IO ring 2	I/O	Default	GPIO 47	-	G5	PD
		O	ALT A	MSP0_CS	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO51	IO ring 2	I/O	Default	GPIO 51	-	G6	PD
		I	ALT A	MSP0_Din	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO52	IO ring 2	I/O	Default	GPIO 52	-	G7	PD
		O	ALT A	MSP0_Dout	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO86	IO ring 2	I/O	Default	GPIO 86	-	H2	PD
		O	ALT A	UART1_TX	UART1 transmitter		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO87	IO ring 2	I/O	Default	GPIO 87	-	H3	PD
		I	ALT A	UART1_RX	UART1 receiver		-
		-	ALT B	MII_PTP_AUX_TS_TRIG1	-		-
		-	ALT C	-	-		-
GPIO78	IO ring 2	I/O	Default	GPIO 78	-	H4	PD
		O	ALT A	MMC_CLK	-		-
		I	ALT B	TCXO_CLK	-		-
		O	ALT C	CLK_64_FO	-		-
GPIO50	IO ring 2	I/O	Default	GPIO 50	-	H5	PD
		O	ALT A	MSP0_L/R	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO37	IO ring 2	I/O	Default	GPIO 37	-	J1	PD
		I	ALT A	UART0_RX	UART0 receiver		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO42	IO ring 2	I/O	Default	GPIO 42	-	K1	PD
		-	ALT A	-	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-

Symbol	I/O voltage(1)	I/O	AF	Function	Description	Ball	Reset
GPIO38	IO ring 2	I/O	Default	GPIO 38	-	K2	PD
		O	ALT A	UART0_TX	UART0 transmitter		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO44	IO ring 2	I/O	Default	GPIO 44	-	K3	PD
		O	ALT A	Timer_OCMPA	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO49	IO ring 2	I/O	Default	GPIO 49	-	K5	PD
		O	ALT A	MSP0_clk_in	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO23	IO ring 2	I/O	Default	GPIO 23	-	L1	PD
		O	ALT A	SFC_SIO1	-		-
		-	ALT B	-	-		-
		I/O	ALT C	OCTOSPI_SIO1	-		-
GPIO24	IO ring 2	I/O	Default	GPIO 24	-	L2	PD
		O	ALT A	SFC_SIO2	-		-
		-	ALT B	GPIO 24	-		-
		I/O	ALT C	OCTOSPI_SIO2	-		-
GPIO26	IO ring 2	I/O	Default	GPIO 26	-	M1	PD
		O	ALT A	SFC_SIO4	-		-
		-	ALT B	MMC_CLK	-		-
		I/O	ALT C	OCTOSPI_SIO4	-		-
GPIO27	IO ring 2	I/O	Default	GPIO 27	-	M2	PD
		O	ALT A	SFC_SIO5	-		-
		-	ALT B	MMC CMD	-		-
		I/O	ALT C	OCTOSPI_SIO5	-		-
GPIO22	IO ring 2	I/O	Default	GPIO 22	-	N1	PD
		O	ALT A	SFC_SIO0	-		-
		-	ALT B	-	-		-
		-	ALT C	OCTOSPI_SIO0	-		-
GPIO25	IO ring 2	I/O	Default	GPIO 25	-	N2	PD
		O	ALT A	SFC_SIO3	-		-
		-	ALT B	-	-		-
		I/O	ALT C	OCTOSPI_SIO3	-		-
GPIO61	IO ring 2	I/O	Default	GPIO 61	-	P4	PD
		O	ALT A	SFC_CSN	-		-
		-	ALT B	-	-		-
		O	ALT C	OCTOSPI_RWDS	-		-
GPIO62	IO ring 2	I/O	Default	GPIO 62	-	T1	PD

Symbol	I/O voltage[1]	I/O	AF	Function	Description	Ball	Reset
GPIO62	IO ring 2	O	ALT A	SFC_CLK	-	T1	-
		I/O	ALT B	GPIO 62	-		-
		O	ALT C	OCTOSPI_CLK	-		-
GPIO28	IO ring 1	I/O	Default	GPIO 28	-	T4	PU
		I/O	ALT A	SFC_SIO6	-		-
		-	ALT B	-	-		-
		I/O	ALT C	OCTOSPI_SIO6	-		-
GPIO29	IO ring 1	I/O	Default	GPIO 29	-	P1	PD
		I/O	ALT A	SFC_SIO7	-		-
		-	ALT B	-	-		-
		I/O	ALT C	OCTOSPI_SIO7	-		-
GPIO41	IO ring 1	I/O	Default	GPIO 41	-	J6	PD
		-	ALT A	-	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-
GPIO63	IO ring 1	I/O	Default	GPIO 63	-	R1	PD
		-	ALT A	-	-		-
		-	ALT B	-	-		-
		-	ALT C	-	-		-

1. *(FS) Fail Safe IO*

Table 6. RF chip SPI interface

Symbol	I/O voltage	I/O	AF	Function	Description	Ball	Reset
GPIO33[1]	RF chip	I	Default	SPI_CLK_0	SPI slave clock	D9	-
GPIO34[1]	RF chip	I	Default	SPI_DI_0	SPI slave data input	F9	-
GPIO35[1]	RF chip	O	Default	SPI_DO_0	SPI slave data output	E10	PD
GPIO36[1]	RF chip	I	Default	SPI_CS_0	SPI slave chip select	E9	PD

1. *RF chip SPI.*

Table 7. Reserved

Symbol	I/O voltage	I/O	Description	Ball	Reset
Reserved22	IO ring 1	O	Reserved22	H7	Hi-Z/PD
Reserved20	IO ring 1	I/O	Reserved20	G10	Hi-Z/PD
Reserved21	IO ring 1	I/O	Reserved21	H10	Hi-Z/PD
Reserved19	IO ring 1	O	Reserved19	J5	Hi-Z/PD
Reserved18	IO ring 1	O	Reserved18	J4	Hi-Z/PD
Reserved17	IO ring 1	I/O	Reserved17	G9	Hi-Z/PD
Reserved16	IO ring 1	I/O	Reserved16	G8	Hi-Z/PD
Reserved15	IO ring 1	I/O	Reserved15	H8	Hi-Z/PD
Reserved14	IO ring 1	I/O	Reserved14	H9	Hi-Z/PD
Reserved13	IO ring 1	I/O	Reserved13	J8	Hi-Z/PD

Symbol	I/O voltage	I/O	Description	Ball	Reset
Reserved12	IO ring 1	I/O	Reserved12	J7	Hi-Z/PD
Reserved11	IO ring 1	I/O	Reserved11	K7	Hi-Z/PD
Reserved10	IO ring 1	I/O	Reserved10	J9	Hi-Z/PD

Table 8. ADC

Symbol	I/O voltage	I/O	Description	Ball	Reset
ADC6	-	I	ADC channel 6	K10	-
ADC0	-	I	ADC channel 0	L10	-
GND_ADC	-	GND	ADC ground	L7	-
ADC4	-	I	ADC channel 4	L8	-
ADC2	-	I	ADC channel 2	L9	-
VADC_IN	-	I	ADC voltage	M6	-
Reserved23	-	-	Reserved23	R4	-

3 General description

3.1 Multi-constellation and multi-band

The constellations that STA8135G supports are the following ones:

- GPS (L1 C/A, L2C, and L5)
- GLONASS (L1OF, L2OF)
- BeiDou (B1C, B1I, B2a, B2I)
- GALILEO (E1, E5a, E5b, E6)
- QZSS (L1 C/A, L2C, L5)
- NAVIC - former IRNSS (L5)

Carrier phase raw measurements are also provided.

STA8135G supports a wide range of combinations of such signals and bands without the need of external RF front end. The most important GNSS user cases that can be supported by STA8135G are listed in the below table. Each of those cases would require a dedicated firmware.

Table 9. GNSS user cases

Constellation	GPS/QZSS			Glonass		BeiDou			Galileo				NAVIC	SBAS
Frequency	L1 C/A	L2C	L5	L1OF	L2OF	B1I	B2I	B2A	E1	E5b	E5A	E6	L5	L1 C/A
Case 0	X	X	-	X	X	X	-	-	X	-	-	-	-	X
Case 1	X	X	-	X	-	X	X	-	X	-	-	-	-	X
Case 2	X	X	-	X	-	X	-	-	X	X	-	-	-	X
Case 3	X	-	X	X	-	X	-	X	X	-	-	-	-	X
Case 4	X	-	X	X	-	X	-	-	X	-	X	-	-	X
Case 5	X	-	X	X	-	X	-	-	X	-	-	-	X	X
Case 6	X	-	X	-	-	-	-	-	X	-	X	X	-	X
Case 7	X	-	X	-	-	X	-	X	X	-	-	-	X	X
Case 8	X	-	X	-	-	X	-	-	X	-	X	-	-	X
Case 9	X	X	X	-	-	X	X	X	-	-	-	-	-	X
Case 10	X	X	X	-	-	-	-	-	X	X	X	-	-	X

Note: Maximum 80 satellites tracked simultaneously.

3.2 RF front end (G5RF)

The integrated RF front-end is able to support different bands (L1, L2, L5, and E6) thanks to a programmable and flexible RF-IF chain driven by a fractional PLL.

The RF_IF chain is followed by a 3-bit ADC able to convert the IF signal to Sign (SIGN) and Magnitude (MAG1, MAG0) bit. The MAG bit is internally integrated in order to control the variable gain amplifiers.

3.3 Multi-band multi-constellation base band (G5BB) processor

STA8135G integrates G5BB proprietary IP, which is the STMicroelectronics latest generation high-sensitivity baseband processor fully compliant with all different constellations and bands: GPS, Galileo, GLONASS, BeiDou, NAVIC (former IRNSS) and QZSS systems.

3.4 L-band reception path

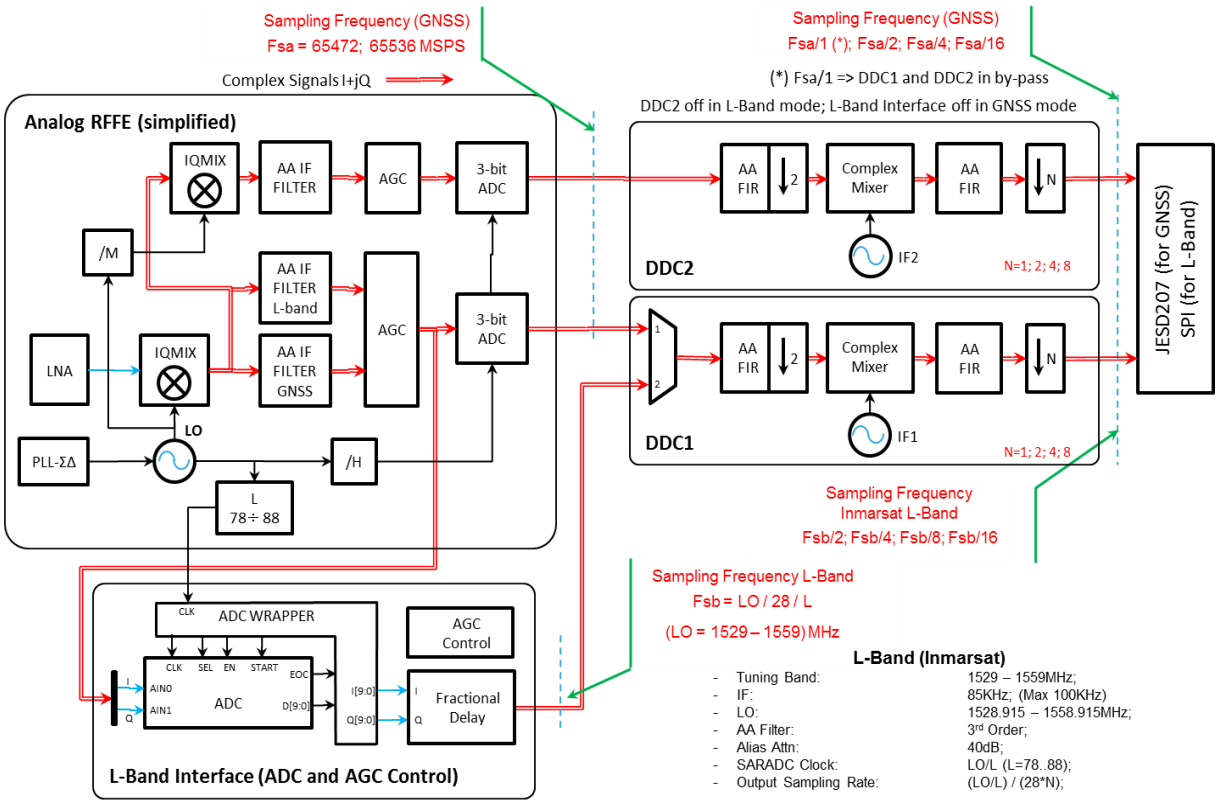
The STA8135G can manage L-band signals for correction service through the integrated STA5635.

In this case the RFA_IN_0 input is dedicated to the L-band signal reception. The tuning range is 1529 – 1559 MHz. External components along the RF chain like LNA, SAW filter, coupler or diplexer should be compliant to L-band signal.

To perform this task, a digital down conversion (DDC) and decimation chain is used to shift the selected L-band channel to zero-IF and to provide a proper output sampling rate to the external host processor for digital demodulation and signal processing.

After proper programming, the L-band digital serial samples are output through the SPI slave interface DO ball (SPI_DO_0, E9).

Figure 2. RF chip DDC block diagram



3.5 MCU sub system

The Cortex® M7 core masters the system resources (memories, registers, and external memory controllers) through the AXI, AHB and APB interconnections present in the SOC.

3.5.1 Caches

The size of instruction and data cache used for ARM® sub-system in STA8135G is 16 KB each.

3.5.2 TCM

ARM® Cortex® M7 has a TCM Control Unit (TCU) with TCM interfaces and an AHB slave (AHBS) interface for system access to TCMs. These TCM memories are integrated outside the ARM® sub-system. STA8135G has 64 KB ITCM memory and 384 KB of DTCM memory.

In the DTCM memory 160 KB is dedicated for ARM® usage and the remaining 224 KB DTCM is shared between the ARM® sub-system and the G5BB module.

ARM® provides access to TCM memories through an AHB slave interface. This AHBS interface is connected to the AMBA infrastructure in STA8135G so that DMA present on the bus can access the TCM memories MCU.

3.5.3 Nested vector interrupt controller (NVIC)

This nested vector interrupt controller (NVIC) allows the operative system interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. It provides a software interface to the interrupt system. ARM® Cortex® M7 has NVIC module for handling the interrupts. The NVIC supports 128 interrupts with 16 levels of priority, which can be changed dynamically. The software can control each request line to generate software interrupts.

3.5.4 AXI bus

AXI Bus matrix handles major high bandwidth transactions for STA8135G. It connects the SRAM, boot ROM and external memory controllers, which provide access to the external Flash. ARM® acts as a master on this bus with the highest priority.

3.6 APB peripherals

3.6.1 APB bridge 2 peripherals

AHB to APB Bridge 2 sits on AHB bus matrix 0 as a slave and is used to connect peripherals. These slaves will be accessed by AHB masters connected to AHB bus matrix 0.

The peripherals connected to APB 2 are: UART2, MSP1, GPIO PORT 2, MTU1.

3.6.2 APB bridge 1 peripherals

AHB to APB bridge 1 sits on AHB bus matrix 0 as a slave and is used to connect peripherals. These slaves will be accessed by AHB masters connected to AHB bus matrix0.

The peripherals connected to APB 1 are UART1, EFT0, EFT1, GPIO PORT 0 and 1, MTU0, OTP, SSP, Thermal sensor, Watchdog timer.

3.6.3 APB bridge 0 peripherals

AHB to APB bridge 0 sits on AHB bus matrix 0 as a slave and is used to connect peripherals. These slaves will be accessed by AHB masters connected to AHB bus matrix0.

The peripherals connected to APB 0 are the ones on the always on domain: PRCC always ON, RTC.

3.6.4 AHB slave devices

There are some AHB slave devices which are connected to AHB bus matrix 0.

3.7 eSRAM

256 KB of embedded RAM are available on top of the TCM RAM.

The eSRAM is directly connected to the MCU through the AXI bus. It can be used for data and instruction.

3.8 Serial flash memory controller (SFC)

The serial flash memory controller supports single, quad and octal memories. It can be used for in place execution thanks to direct memory mapping.

Table 10. SQI memory interface (power fail-safe IOs)

Symbol	I/O voltage	I/O	Description	Ball	Reset state
SFC_CLK	IO ring1	O	Serial flash memory controller clock	T1	Hi-Z/PD
SFC_CSN	IO ring1	O	Serial flash memory controller chip select	P4	Hi-Z/PD
SFC_SIO0	IO ring1	I/O	Serial flash memory controller data IO 0	N1	Hi-Z/PD
SFC_SIO1	IO ring1	I/O	Serial flash memory controller data IO 1	L1	Hi-Z/PD
SFC_SIO2	IO ring1	I/O	Serial flash memory controller data IO 2	L2	Hi-Z/PD
SFC_SIO3	IO ring1	I/O	Serial flash memory controller data IO 3	N2	Hi-Z/PD
SFC_SIO4	IO ring1	I/O	Serial flash memory controller data IO 4	M1	Hi-Z/PD

Symbol	I/O voltage	I/O	Description	Ball	Reset state
SFC_SIO5	IO ring1	I/O	Serial flash memory controller data IO 5	M2	Hi-Z/PD
SFC_SIO6	IO ring1	I/O	Serial flash memory controller data IO 6	T4	Hi-Z/PD
SFC_SIO7	IO ring1	I/O	Serial flash memory controller data IO 7	P1	Hi-Z/PD

Note: These interface IOs are alternate functions A of GPIOs.

3.9 SSP

STA8135G has one synchronous serial ports (SSPs). The SSP is a master or slave interface that enables synchronous serial communication with slave or master peripherals having one of the following:

- Serial peripheral interface bus standards
- Synchronous serial protocol bus standards
- Micro-wire interface bus standards
- Unidirectional interface

In both master and slave configurations, the SSP has the following features:

- Parallel-to-serial conversion on data written to an internal 32-bit wide, 32-location deep transmit FIFO
- Serial-to-parallel conversion on received data, buffering it in a 32-bit wide, 32-location deep receive FIFO
- Programmable data frame size from 4 to 32 bits
- Programmable clock bit rate and pre-scaler
- Programmable clock phase and polarity in SPI mode
- Support for direct memory access (DMA)

3.10 UART

The UARTx performs serial-to-parallel conversion on data asynchronously received from a peripheral device on UARTx_RX pin, and parallel-to-serial conversion on data written by CPU for transmission on UARTx_TX pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 64 data byte for transmission, and 64 data byte with 4-bit status (break, frame, parity, and overrun) to receive. FIFOs may be burst-loaded or emptied by the system processor or DMA, from one to sixteen words per transfer.

3.11 Watchdog timer (WDT)

Watchdog timer (WDT) provides a way of recovering from software crashes. The watchdog clock is used to generate a regular interrupt (Irq_wdt), depending on a programmed value.

The watchdog monitors the interrupt and asserts a reset signal (WDOGRES) if the interrupt remains unserviced for the entire programmed period. The WDT is counting down at a fixed frequency of 32.768 kHz.

The watchdog timer peripheral can be used as free-running timer or as watchdog to resolve processor malfunctions due to hardware or software failures.

Feature set overview:

- 16-bit down counter
- 8-bit clock pre-scaler
- Safe reload sequence
- Free-running timer mode
- End of counting interrupt generation

3.12 GPIO

There are 34 GPIOs in this device.

The GPIO block provides programmable inputs or outputs. Each input or output can be controlled in two modes:

- Software mode through an APB bus interface
- Alternate function mode, where GPIO becomes a peripheral input or output line

Any GPIO input can be independently enabled or disabled (masked) for interrupt generation. User can select for each GPIO which edge (rising, falling, both) will trigger an interrupt.

A de-bouncing logic can be enabled for each GPIO to filter glitches on IOs before going to the Interrupt generation and CPU read value.

All GPIOs are fail safe to avoid leakage consumption in any condition even when the ring is off and the external line is logic level high.

3.13 Multi timer unit (MTU)

Multi timer unit consists of eight timers. Each timer is clocked by MXTAL frequency divided by 8 (which means 2.4 MHz with a 19.2 MHz crystal) or REFCLK (32.768 kHz) inputs.

3.13.1 MTU feature overview

- The Multi timer unit provides access to four interrupt generating programmable 32-bit free-running decrementing counters (FRCs) allowing up to four counts to be performed in parallel.
- The FRCs have their own clock input, allowing the counters to run from a much slower clock than the system clock.
- In each FRC the 32-bit counter is split up into two 16-bit counters.

3.14 RTC

This is an always-on power domain dedicated to RTC logic (backup system) with 256 bytes SRAM and supplied with a dedicated voltage regulator.

The RTC provides a high resolution clock which can be used for GPS. It keeps the time when the system is inactive and can be used to wake up the system when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

RTC features:

- 47-bit counter clocked by 32.768 kHz clock
- 32-bit for the integer part (seconds) and 15-bit for the fractional part
- The integer part and the fractional part are readable independently
- The counter, once enabled, can be stopped
- Integer part load register (32-bit)
- Fractional part load register (15-bit)
- Load bit to transfer the content of the entire load register (integer + fractional part) to the 47-bit counter

Once set by the MCU this bit is cleared by the hardware to signal to the MCU that the RTC has been updated.

3.15 MSP

STA8135G has one multi mode serial port (MSP).

The following section describes the functionalities of the MSP unit.

The multi mode serial port (MSP) is a synchronous transmitter serial interface.

The MSP provides:

- Element (data) sizes of 8, 10, 12, 14, 16, 20, 24, and 32 bits, LSB or MSB first
- Programmable frequency shift clock for data transfer
- Direct interface to SPI compliant devices
- Transmit first-in, first-out memory buffers (FIFOs), 32 bits wide, 8 locations deep

3.16 Direct memory access (DMA)

The DMAC is an advanced microcontroller bus architecture (AMBA) compliant to System-on-Chip (SoC) peripheral. The DMAC is an AMBA AHB module, and connects to the advanced high-performance bus (AHB).

Module key features:

- Eight DMA channels. Each channel can support an unidirectional transfer.
- The DMAC provides 32 peripheral DMA request lines.
- Single DMA and burst DMA request signals.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
- Scatter or gather DMA support through the use of linked lists.
- Hardware DMA channel priority. DMA channel 0 has the highest priority and channel 31 has the lowest priority.
- If requests from two channels become active at the same time, the channel with the highest priority is serviced first.
- AHB slave DMA programming interface to the DMA control registers.
- Two AHB bus masters for transferring data.
- Programmable DMA burst size.
- Working on AHB clock.

3.17 Temperature sensor

Temperature measurement range is -40 to 85 °C. It uses integrated bandgap reference and 8-bit ADC.

The temperature sensor provides two threshold registers. Writing in these registers and enabling the threshold mode compare the temperature recorded with the threshold value. If the temperature is higher than the upper threshold register or lower than the lower threshold register, it generates an interrupt if enabled.

Table 11. Temperature sensor

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Tsens	Sensitivity	-	-	-	1	°C
Tacc(1)	Accuracy	Calibration performed at Ta = 85 °C °C	±3(2)	-	± 10	°C

1. *Best accuracy is at calibrated temperature.*
2. *Limited by manufacturing calibration environment.*

3.18 Serial boot pins

UART2-TX (Boot0) pin is used to select the boot configuration of Cortex® M7. The ROM code starts the boot process which then polls the PRCC register (UART2-TX) which has already latched the UART2-TX pin (E2 ball) status after latch reset.

Based on this register value the code is loaded from one of the two options as given in the table below:

Table 12. Boot peripheral selection

Pin	ROM action
UART2-TX = 0	Boot from flash memory - SFC controller
UART2-TX = 1	Boot from peripheral - UART

3.19 Reset

After a reset, the Cortex® M7 is woken-up by the ROM code.

The PRCC module is used to sequence through all the steps needed to properly reset the device and prepare it to fetch the first instruction of the user application code.

STA8135G has the following reset options:

- Pad reset: SoC will have active low chip reset (RESET) pad. Low (zero) status on this pad will keep device in the reset. Assertion of this pin low should be minimum of 5 ms.

- Power on reset: the power on reset circuitry is embedded in the main voltage regulator built on HV supply (VCORE_IN) of the regulator. It ensures all voltage monitors are under reset state until the VCORE_IN (or VDD_EXT_REG) minimum voltage is reached.
- Hardware resets: the internal voltage regulator embeds multiple LVD (low voltage detector) and HVD (high voltage detector) which are used in the reset sequence.
- Soft reset: different peripherals present on STA8135G can be reset independently through the registers present inside the PRCC module.

3.20 CAN interface

CAN sub-system comprises two fully independent FD-CAN controllers: CAN0 and CAN1. Both controllers conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015. Maximum data bit rate supported is 1 Mbit/s.

3.21 I^2C high speed controller

One I^2C high speed controller interface is capable of master/slave modes in multi-master environment. It is DMA capable and the multiple baud rates supported are: 100/400/1000/3400 Kbits/s.

3.22 Full speed USB 2.0

It supports 12 Mbps (full speed) and 1.5 Mbps (low speed) serial data transmission according to USB 2.0 OTG controller specification.

3.23 SDMMC (secure digital multi media card controller)

The SDMMC card host interface provides an interface between the APB peripheral bus and Multi Media cards (MMC), SD memory cards, SDIO cards, and CE-ATA devices.

4 Electrical specifications

4.1 Main chip

4.1.1 Absolute maximum ratings

Table 13. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VRF_IN	Supply voltages	-0.3	3.9	V
VCORE_IN	Supply voltages	-0.3	3.9	V
VBK_IN	Supply voltages	-0.3	3.9	V
VIO_IN	Supply voltages	-0.3	3.9	V
VDD_EXT_REG(1)	Supply voltages	-0.3	1.4	V
T_J	Junction operating temperature	-40	125	°C
TS	Storage temperature	-55	150	°C
ESDHBM	Electro static discharge - Human body model	-	±2	kV
ESDCDM(2)	Electro static discharge - Charge device model	-	±500	V
LU	Latch Up	-100	+100	mA

1. *EXT_REG_SEL = high.*
2. *RFA_IN ESDCDMMax is ±50 V. LNA_IN ESDCDM Max is ±250 V.*

4.1.2 Electrical characteristics

Table 14. Operating junction temperature range

Parameter	Min.	Typ.	Max.	Unit
Junction temperature	-40	27	125	°C

Table 15. VDD_EXT_REG - external core power supply

Parameter	Min.	Typ.	Max.	Unit	Comment
External core power supply (VDD_EXT_REG)	1.14	-	1.32	V	EXT_SEL_REG = High

Table 16. Backup PMU - Functional specifications

Specification	Min.	Typ.	Max.	Unit	Comment
LDO_BK					
Input voltage (VBK_IN)	1.62	3.3	3.6	V	
Output voltage (VBK_OUT)	1.10	1.2	1.26	V	
Load current at normal mode			2	mA	
LDO power consumption at normal mode (1)			20	µA	
LDO power down consumption (1)			1	µA	
External capacitance (VBK_OUT) (1)	0.5	1	1.2	µF	

Specification	Min.	Typ.	Max.	Unit	Comment
Line regulation			10	mV	
Load regulation VO = 1.2 V max at Iout = 0 mA VO = 1.1 V max at Iout = 2 mA			100	mV	
Start-up time (1)			600	µs	-
VBK_IN slew rate	0.04		40 (1)	ms	In case VBK_IN = 3.3 V add 100 Ω series resistor and 1 µF capacitor to GND to the VBK_IN pin

1. *Specified by design, not tested in production.*

Table 17. Main PMU - Functional specifications

Specification	Min.	Typ.	Max.	Unit	Comment
LDO_CORE					
Input voltage (VCORE_IN)	1.62	3.3	3.6	V	
Output voltage (VCORE_OUT available at balls VDD_EXT_REG)	1.14	1.2	1.30	V	EXT_REG_SEL = low (VDD_EXT_REG)
Load current (mA)			450	mA	
LDO power consumption (1)		-	200	µA	
LDO power down consumption(1)			4	µA	
External capacitance (VCORE_OUT) (1)	2.35	4.7	6.35	µF	EXT_REG_SEL = low (VDD_EXT_REG)
Line regulation			10	mV	
Load regulation			70	mV	
Load current transient (1)			150/100	mA/nS	
Start-up time (1)		15		µs	
LDO IO					
Input voltage (VIO2_IN)	3	3.3	3.6	V	
Output voltage (VIO1_EXT)	1.72	1.80	1.90	V	
Load current			90	mA	
LDO power consumption (1)			200	µA	
LDO power down consumption (1)			4	µA	
External capacitance (1)	1.1	2.2	3	µF	
Line regulation	-	-	10	mV	
Load regulation	-	-	100	mV	
Load current transient (1)	-	-	90/100	mA/ns	
Start-up time(1)	-	25	-	µs	
LDO_RF					
VRF_IN	1.62	3.3	3.6	V	
VRF_OUT	1.05	1.15	1.25	V	
Load current on VRF_OUT		27		mA	

1. *Specified by design, not tested in production.*

Table 18. Current consumption

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IBK_Normal	Current consumption at V_{BK_IN} in normal mode	V_{BK_IN} = 3.3 V			1	mA
IBK_Standby	Current consumption at V_{BK_IN} in standby mode	V_{BK_IN} = 3.3 V T_{AMB} = - 40 C°			45	µA
ICORE_Functional_85	Current consumption at VCORE_IN with ST reference application design running	VCORE_IN = 3.3 VEXT_REG_SEL = Low Max. ambient temperature = 85 °C			300(1)	mA
ICC_VRFIN	Current consumption at VRF_IN	VRF_IN = 3.3 V AllRF block ON, with VCC_LNA and VCC_PLL connected to VRF_OUT on PCB. Tamb = 25 °C		28		mA
ICC_VRFIN_off	Current consumption at VRF_IN with G5RF in standby (off)	VRF_IN = 3.3 VAll RF block OFF, with VCC_LNA and VCC_PLL connected to VRF_OUT on PCB. Tamb = 25 °C		150		µA

1. *Maximum current at VCORE is limited by maximum junction temperature at 125 °C (which depends on application printed circuit board).*

Table 19. RF Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LNA						
Gp	Power gain	L1 band	-	15	-	dB
		L5 band	-	15	-	
NF	Noise figure(1)	L1 band	-	2.5	-	dB
		L5 band	-	2.5	-	
LNA $P_{\_1dB}$	Input compression point	-	-	-16	-	dBm
RFA - MIXER - IF FILTER - VGA						
GpRFA	RFA voltage gain	Max gain		15		dB
		Min gain		5		dB
GC	Conversion gain (from RFA in to ADC input)	VGA and RFA at max gain		90		dB
		VGA and RFA at min gain		40		
VGA	VGA dynamic range			50		dB
$P_{\_1dB}$	RF-IF-VGA input compression Point	In band RFA max VGA max		-100		dBm
		In band RFA max VGA min		-50		
NF_{RF-IF}	RF-IF-VGA noise figure(1)	VGA and RFA at max gain in L1 - L5 - L band		5		dB
BW	-1 dB high freq. corner IF filter	Set corner #1		13		MHz
ATT	Aliasing frequency rejection	F = 51 MHz (corner #1)	20			dB

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Fractional synthesizer - VCO						
TCXO in	TCXO frequency			26		MHz
R_{DIV}	Reference divider range		1		63	
N_{DIV}	Loop divider range		56		2047	
Frac	PLL fractionality			18		bit
F_{LO}	LO operating frequency		2300		3300	MHz

1. *Specified by design, not tested in production.*

Table 20. Electrical characteristics of digital input and output buffers

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Input and output buffers						
V_{IH_1V8}	CMOS input high level		0.65 x V_{18_IO}		0.3 + V_{18_IO}	V
V_{IL_1V8}	CMOS input low level		-0.3		0.35 x V_{18_IO}	V
V_{IH_3V3}	CMOS input high level		2.0		0.3 + V_{33_IO}	V
V_{IL_3V3}	CMOS input low level		-0.3		0.8	V
C_{IN}	CMOS input capacitance				3	pF
V_{OH}	CMOS output high level	At max. I_{OH}	V_{IO} -0.4		-	V
V_{OL}	CMOS output low level	At max. I_{OL}			0.4	V
I_{OL}/I_{OH} IO ring1 and PPS_OUT	Driving current to sustain V_{OL}/V_{OH}	V_{OL}/V_{OH}	0		4	mA
I_{OL}/I_{OH} IO ring2 but PPS_OUT	Driving current to sustain V_{OL}/V_{OH}	V_{OL}/V_{OH}	0		2	mA
t_{RISE}(1)	CMOS output rise time with CL = 15 pF, from 10 to 90%; 3.3 V	2 mA max. current drive		3		ns
		4 mA max. current drive		2		
t_{FALL}(1)	CMOS output fall time with CL = 15 pF, from 90 to 10%; 3.3 V	2 mA max. current drive		3		ns
		4 mA max. current drive		2		

1. *Specified by design, not tested in production.*

4.2 RF chip (integrated STA5635)

4.2.1 Parameter conditions

Unless otherwise specified, all voltages are referred to GND.

4.2.2 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices.

STA8135G parts are tested at T = -40 °C and T =85 °C.

4.2.3 Typical values

Unless otherwise specified, typical data are based on Tamb = 25 °C, LDO_IN_3V3_1V8_0 = LDOS_VCC_0 = 3.3 V, LDO_RF_OUT_1V1_0 = LDO_1V1_OUT_0 = 1.1 V and LDO_1V8_OUT_0 = 1.8 V.

Table 21. Electrical characteristics (TJ = 25 °C unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply						
VCC_RF	Voltage supply for LDO_RF		3.0	3.3	3.6	V
VCC_IO	Voltage supply for IO, LDO_1V8 and LDO_DIG		3.0	3.3	3.6	V
ICCRF	Analog blocks current consumption	All blocks ON	17	28	39	mA
ICCIO	Digital and IO current consumption	It depends on IO activity	0.5	33		mA
ICC_STBY	Stand-by power consumption.	All blocks OFF, only VCC_RF and VCC_IO supplied		4	6	µA
Voltage regulator						
LDO_RF	Regulator output voltage		1.0	1.1	1.2	V
LDO_DIG	Regulator output voltage		1.0	1.1	1.2	V
LDO_1V8	Regulator output voltage		1.62	1.8	1.98	V
LNA						
Gp	Power gain	L1	10.5	17	24	dB
		L2 - L5 - L band	10.5	18	25	
NF	Noise figure(1)	L1		1.7		dB
		L2 - L5 - L band		1.7		
P1dB	Input compression point		-15			dBm
RFA - MIXER - IF FILTER - VGA						
GpRFA	RFA voltage gain(1)	Max gain		20		dB
		Min gain		0		dB
GC	Conversion gain (from RFAin to ADC input)	VGA and RFA at max gain	60	82	90	dB
		VGA and RFA at min gain	12	26	38	
ΔVGA	VGA dynamic range		35	48	60	dB
P_1dB	RF-IF-VGA input Compression point	In band RFA max VGA max		-105		dBm
		In band RFA max VGA min		-55		dBm
NFRF-IF	RF-IF-VGA noise figure(1)	VGA and RFA at max gain in L1-L2-L5 band		5		dB
BW	-1dB high freq corner IF filter	Set corner #1		13		MHz
ATT	Aliasing frequency rejection	F = 52 MHz (corner #1)	20			dB
Cristal oscillator - Fractional synthesizer - VCO						
FTCXO	TCXO frequency			26		MHz
PTCXO_IN	Reference input signal sensitivity	TCXO_IN pin DC blocked requested.	-20			dBm
RDIV	Reference divider range		1		63	
NDIV	Loop divider range		56		2047	
Frac	PLL fractionality			18		bit

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
FLO	LO operating frequency		2300		3300	MHz

1. *Specified by design, not tested in production.*

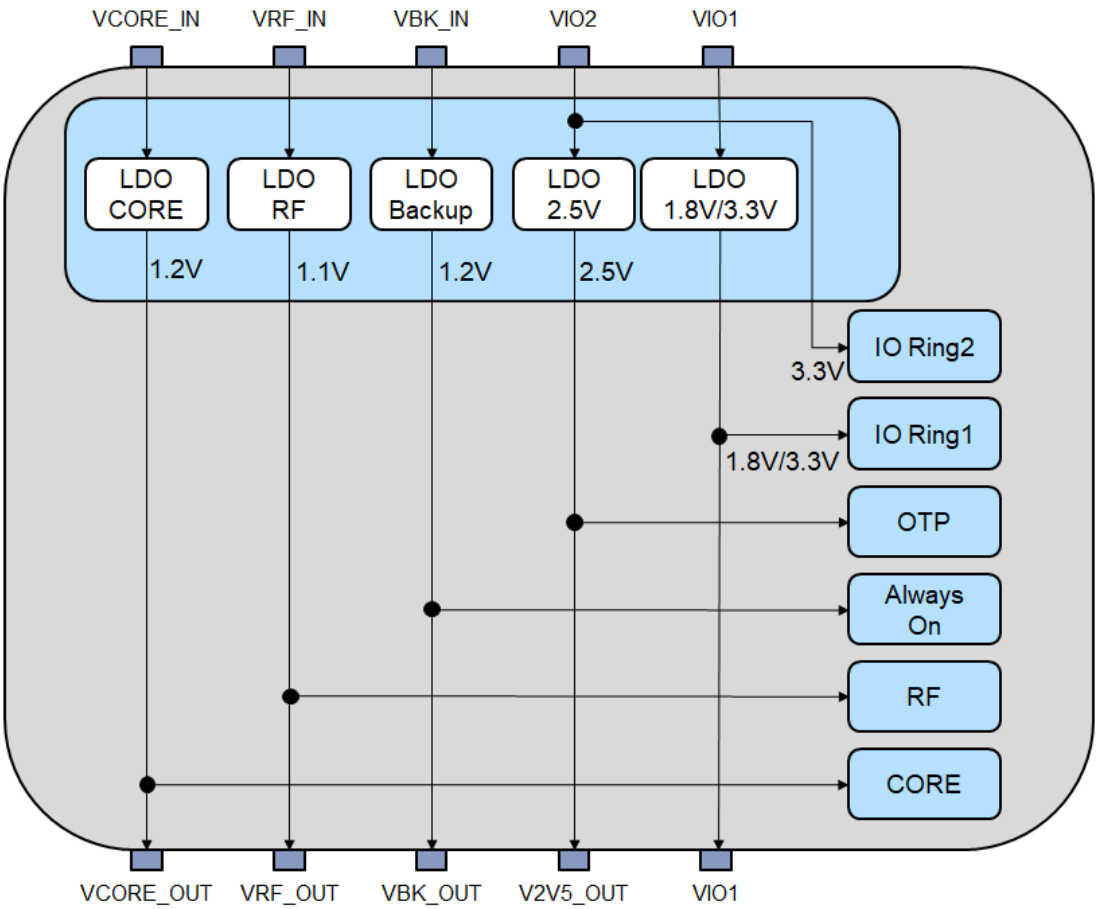
4.3 Power management unit (PMU) - main chip

STA8135G - main chip - embeds 5 voltage regulators (LDO):

Table 22. LDO on-chip regulators

LDO	Supply regions	Input voltage	Typical output voltage at 25 °C
CORE LDO	Core	VCORE_IN = 1.62 – 3.6 V	1.2 V
LDO2v5	Safmem, temp sensor	VIO_IN = 3.3 V	2.5 V
IO LDO	IOring 1	VIO_IN = 3.3 V	1.8 V
BACKUP LDO	Always on	VBK_IN = 1.62 - 3.6 V	1.2 V
RFLDO	RF	VRF_IN = 1.62 - 3.6 V	1.15 V

Figure 3. LDO on-chip regulators dependencies



4.3.1 Power regions

STA8135G - main chip - has six major power regions. The modules present inside each power region are listed below.

- Always on backup region: 1.2 V
  - prcc_backup
  - RTC
  - Backup RAM 256 bytes
- Switchable region: 1.2 V
  - ARM® core
  - Other digital IPs
- RF: 1.15 V
- OTP: 2.5 V
- IO ring1: 1.8 V or 3.3 V
- IO ring2: 3.3 V

IO ring1 is set at 1.8 V when supplied by the internal IO LDO. If a 3.3 V supply is applied at VIO1_EXT the IO ring1 is set at 3.3 V (bypassing the internal IO LDO).

The switchable power region can be supplied by an external voltage regulator directly at pin VDD_EXT_REG. The integrated LDO CORE has to be switched off by forcing EXT_REG_SEL to high voltage.

It is not possible to use the internal Core LDO at +85 °C ambient with application where 3.3 V is used as the input voltage of LDO Core (VCORE_IN).

4.4 Power management and start-up strategy RF chip

The supply available on board of 3.3 V (or 1V8) has to be applied to VCC_RF, VCC_IO and CHIP_EN (with an RC network) pins.

With power supply applied but CHIP_EN inactive the chip is in stand-by mode consuming just a minimal leakage current. Applying CHIP_EN High, turns on the LDOs, immediately after the xtal oscillator and after a delay (td) the rest of the device is activated. It is mandatory to add an RC circuit referred to 3.3 V main supply on CHIP_EN ball in order to delay the enable of the internal LDOs in respect to 3.3 V supply rise.

Figure 4. Power configuration

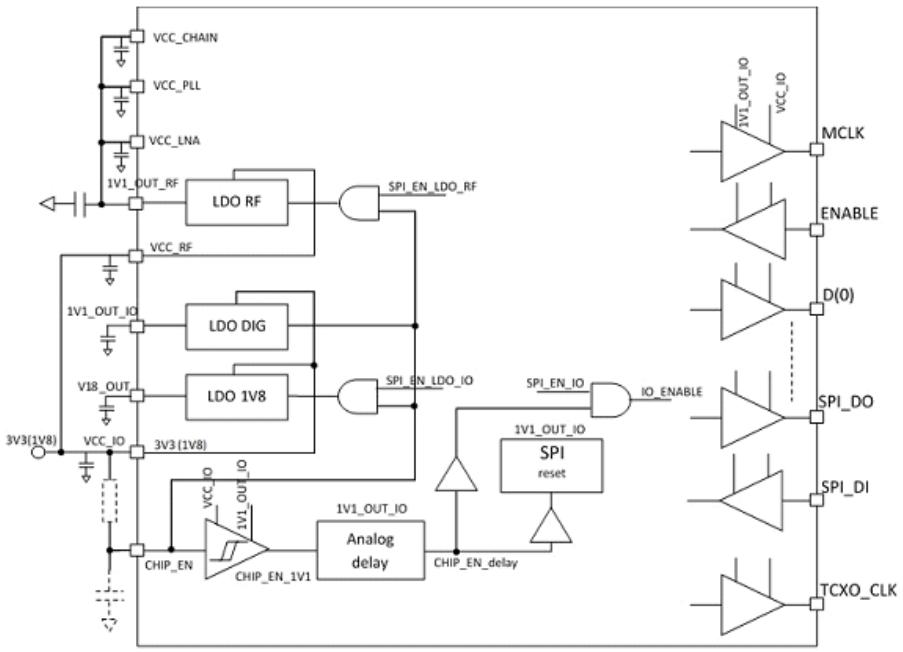
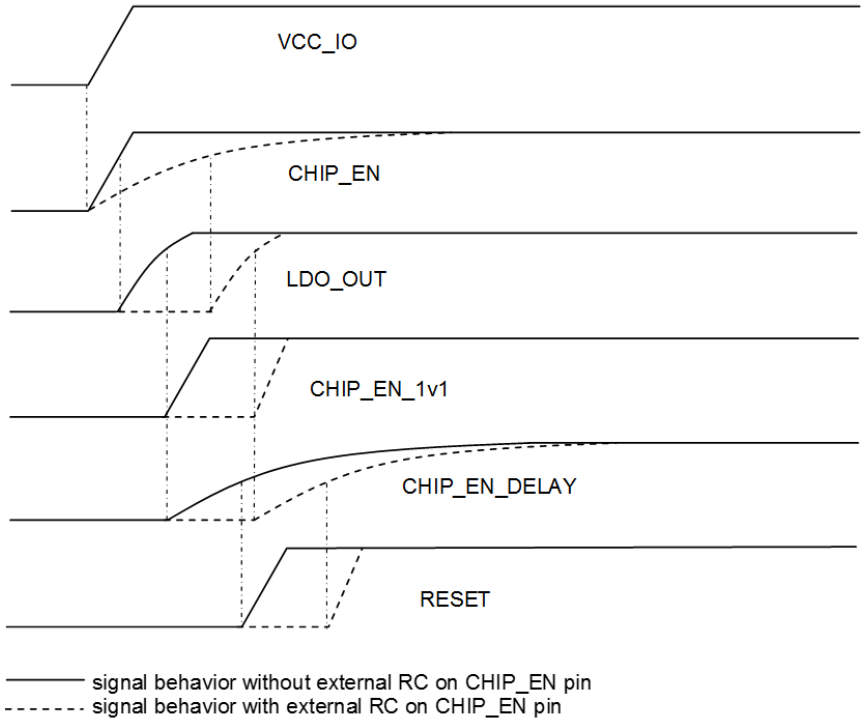


Figure 5. **Power-up strategy**



4.5 RTC32.768 kHz oscillator specifications

The 32.768 kHz OSCI32 oscillator is connected between RTC_XTI (oscillator amplifier input) and RTC_XTO (oscillator amplifier output). It also requires two external capacitors of 18 pF (using crystal with recommended characteristics as per Table 23) as shown in the Figure 6.

The recommended oscillator specifications are shown in the table below:

Table 23. **Crystal recommended specifications**

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SXTAL}	Crystal frequency		32.768		kHz
LM_{SXTAL}	Motion inductance(1)	3500	5	6500	kHz
CM_{SXTAL}	Motional capacitance(1)	4.0	5.0	6.0	fF
CO_{SXTAL}	Shunt capacitance(1)	1.0	1.3	1.6	pF
ESR	Resonance resistance(1)			80	kΩ
CL	External load capacitance		18 ±2%		pF

1. *Specified by design, not tested in production.*

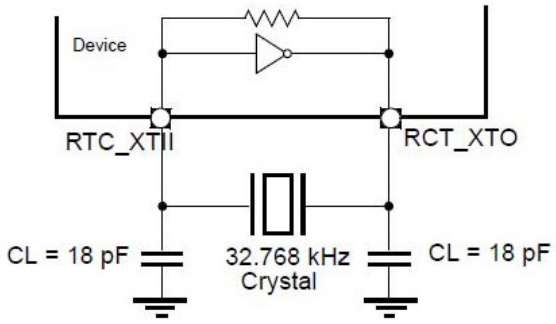
The following table provides the oscillator amplifier specifications.

Table 24. Oscillator amplifier specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_S	Startup time(1)		0.3	0.6	s
DL	Drive level(1)		-	< 0.1	µW
RLC	Required load capacitance(1)		12.5		pF
GO	Startup conductance	22.5	33.6	60	µA/V

1. *Specified by design, not tested in production.*

Figure 6. 32.768 kHz crystal connection



To drive the 32.768 kHz crystal pins from an external clock source:

- Disable the oscillator (bit28-OSCI_EN = 0b in PRCC_BACKUP_REG0 register). This disables the internal inverter, thus reducing the power consumption to minimum.
- Drive the RTC_XTI pin with a square signal or a sine wave.

Table 25. Characteristics of external slow clock input

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{JIT} (CC)	Cycle-to-cycle jitter	-70		70	ps
T_{JIT} (per)	Period jitter	-70		70	ps
-	Variation	-500		500	ppm
T_{DUTY}	Duty cycle	45		55	%

4.6 Power up timing sequence

Figure 7. **Power up timing diagram**

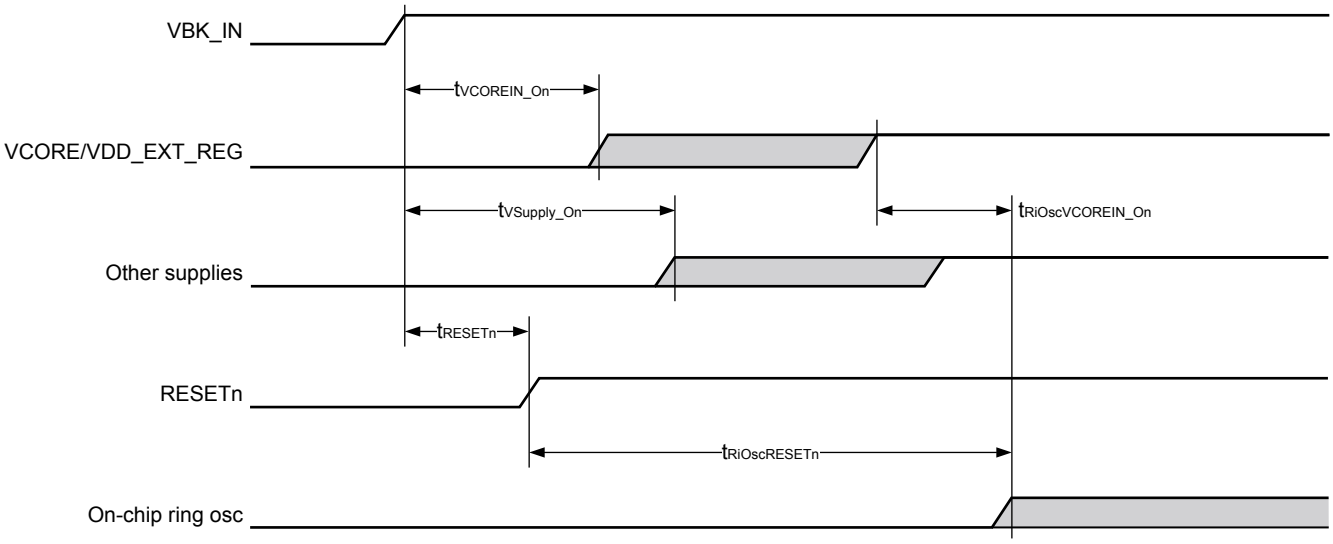


Table 26. **Power up timing data**

Symbol	Condition	Min.	Max.	Unit	Comment
$t_{VCORE\_IN\_On}$	VBK_IN > 1.62 V	0 (1)	-	ms	Time from the power-on of VBK_IN to the power-on of VCORE_IN or VDD_EXT_REG
$t_{VSupply\_On}$	VBK_IN > 1.62 V	0 (2)	-	ms	Time from the power-on of VBK_IN to the power-on of other supplies
t_{RESETn}	VBK_IN > 1.62 V	4	-	ms	Time from the power-on of VBK_IN to RESETn going high
$t_{RiOscRESETn}$	VCORE_IN > 1.62 V or VDD_EXT_REG > 1.14 V	0.5	-	ms	Time from RESETn going high to the on-chip ring oscillator start up
$t_{RiOscVCOREIN\_On}$	RESETn = high	0.5	-	ms	Time from VCORE or VDD_EXT_REG applied to the on-chip ring oscillator start up

1. *The simultaneous power-on of VBK_IN and VCORE_IN or VDD_EXT_REG is allowed and tested.*
2. *The simultaneous power-on of VBK_IN and other supplies is allowed and tested*

4.7 Digital interface AC timing characteristics

Figure 8. **Clock block diagram**

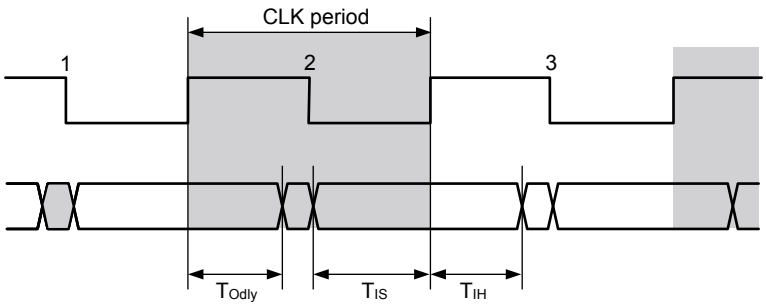


Table 27. **Clock data**

Symbol	Comment
CLK period	Clock time period
t_{Odly}	Output data delay from rising clock edge, unless differently specified
t_{IS}	Input data setup time to rising clock edge, unless differently specified
t_{IH}	Input data hold time from rising clock edge, unless differently specified

4.7.1 SQIO

Table 28. **SQIOSDR mode (feedback mode)**

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	-	78.5	MHz	25 pF	-
	CLK period	12.74	-	ns	-	-
	CLK duty cycle	40	60	%	-	-
Input	TIS	0.5	-	ns	-	-
	TIH	2.5	-	ns	-	-
Output	Todly	-2.5	2.4	ns	25 pF	-

Note: Specified by design, not tested in production.

Table 29. **SQIODTR mode (DQS mode for flash memory read operations)**

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	-	65	MHz	25 pF	Flash memory clock frequency
	CLK period	15.38	-	ns	-	-
	CLK duty cycle	40	60	%	-	-
Input	TIS	0	-	ns	-	-
	TIH	0	-	ns	-	
Output	Todly	-1.25	1.8	ns	25 pF	-

Note: Specified by design, not tested in production.

4.7.2 SPI

Table 30. **SPI (controller mode)**

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	-	19.625	MHz	25 pF	-
	CLK period	50.95	-	ns	-	-
	CLK duty cycle	40	60	%	-	-
Input	TIS	10	-	ns	-	-
	TIH	2	-	ns	-	-
Output	Todly	2	10	ns	25 pF	-

Note: Specified by design, not tested in production.

4.7.3 MSP controller mode

Table 31. MSP0 controller mode

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	-	9.8125	MHz	25 pF	-
	CLK period	101.9	-	ns	-	-
	CLK duty cycle	40	60	%	-	-
Input	TIS	10	-	ns	-	-
	TIH	4	-	ns	-	-
Output	Todly	0	10	ns	25 pF	-

Note: Specified by design, not tested in production.

Table 32. MSP0 target mode

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	-	9.8125	MHz	25 pF	-
	CLK period	101.9	-	ns	-	-
	CLK duty cycle	40	60	%	-	-
Input	TIS	10	-	ns	-	-
	TIH	4	-	ns	-	-
Output	Todly	0	14.5	ns	25 pF	-

Note: Specified by design, not tested in production.

Table 33. MSP1 target mode

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	-	9.8125	MHz	25 pF	-
	CLK period	101.9	-	ns	-	-
	CLK duty cycle	40	60	%	-	-
Input	TIS	7	-	ns	-	-
	TIH	4	-	ns	-	-
Output	Todly	0	14	ns	25 pF	-

Note: Specified by design, not tested in production.

4.7.4 JTAG

Table 34. JTAG characteristics

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	-	26	MHz	25 pF	-
	CLK period	38.4	-	ns	-	-
	CLK duty cycle	40	60	%	-	-
Input	TIS	5	-	ns	-	-

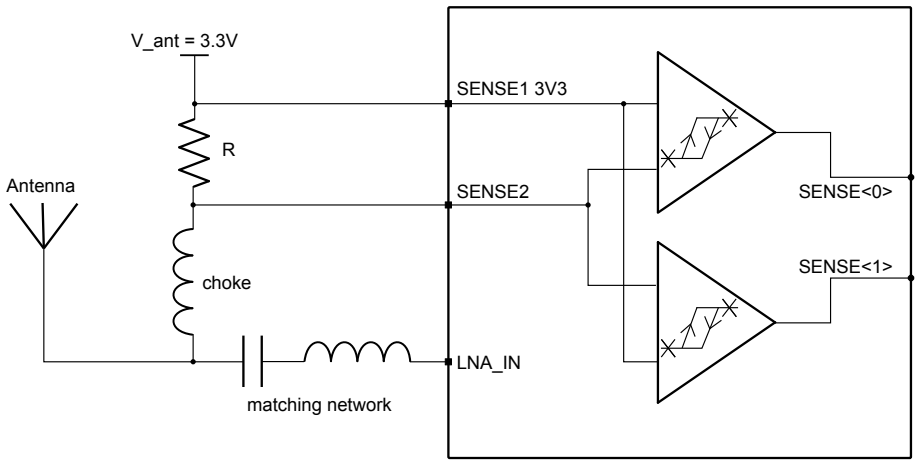
Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Input	TIH	5.5	-	ns	-	-
Output	Todly	-3	15	ns	25 pF	-

Note: Specified by design, not tested in production.

5 Antenna sensing

The following figure shows an example of an antenna sensing circuit working with a 3.3 V antenna. The input voltage range must be between VRF_IN and GND.

Figure 9. Antenna sensing configuration



The STA8135G uses two comparators with hysteresis for antenna sensing. If a voltage of 3.3 V supplies the antenna, the antenna sensing block must be connected as illustrated in the above figure.

Antenna monitoring can also be implemented using the ADC embedded in the STA8135G. (Ask ST for the dedicated application note for further details.)

6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 TFBGA160 (7x11x1.2 mm) package information

Figure 10. TFBGA160 (7x11x1.2 mm) package outline

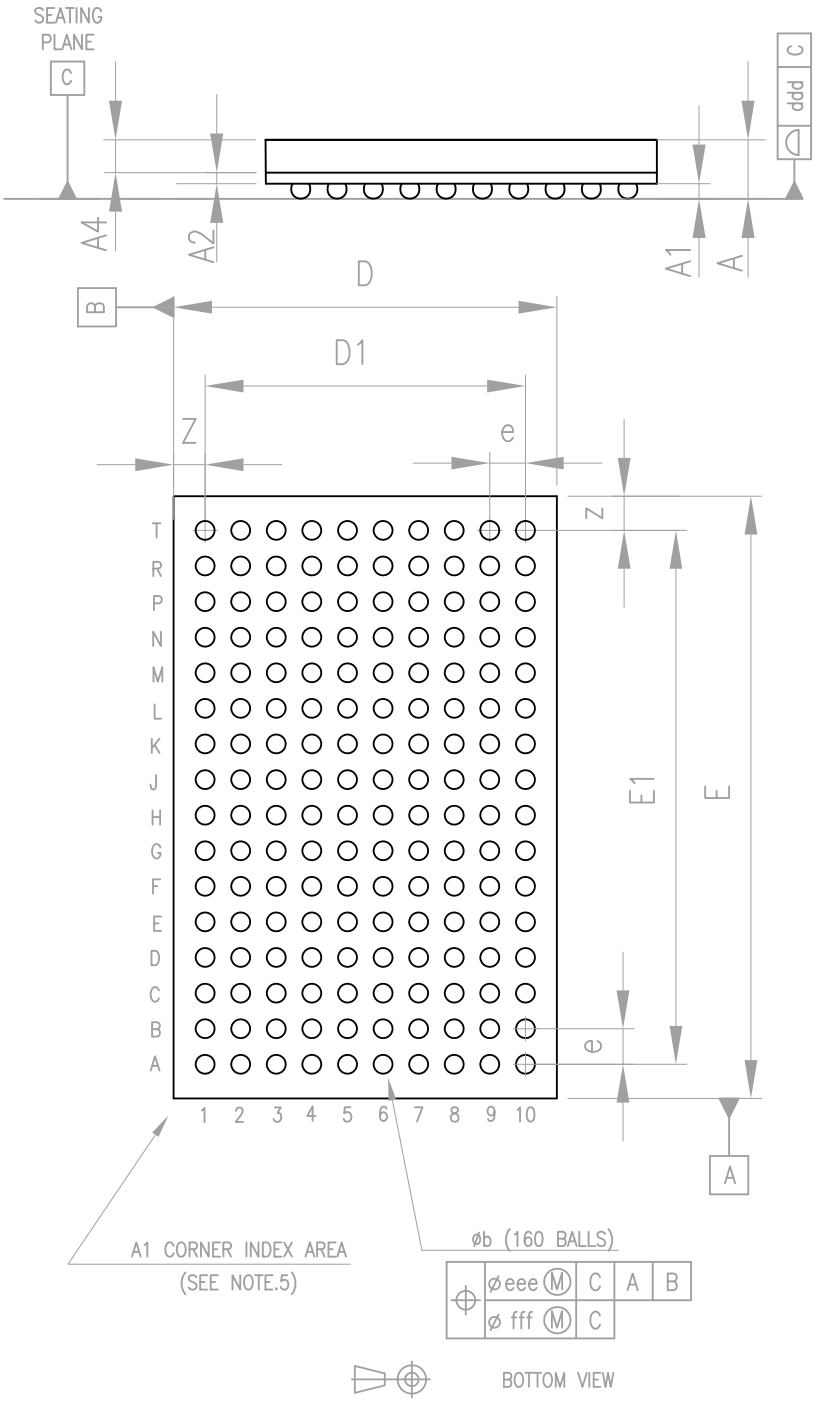


Table 35. TFBGA160 (7x11x1.2 mm) package mechanical data

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
A(1)	-	-	1.20
A1	0.20	-	-
A2	-	0.27	-
A4	-	0.585	-
b(2)	0.30	0.35	0.40
D	6.85	7.00	7.15
D1	-	5.85	-
E	10.85	11.00	11.15
E1	-	9.75	-
e	-	0.65	-
Z (along X axis)	-	0.575	-
z (along Y axis)	-	0.625	-
ddd	-	-	0.10
eee(3)	-	-	0.15
fff(4)	-	-	0.08

1. *TFBGA stands for Thin Profile Fine Pitch Ball Grid Array.*
   - *Thin Profile: The total profile height (Dim A) is measured from the seating plane to the top of the component.*
   - *The maximum total package height is calculated by the following methodology: A Max. = A1 Typ + A3 Typ + A4 Typ + √ (A1²+A3²+A4² tolerance values).*
   - *Thin profile: 1.00 mm < A ≤ 1.20 mm / Fine pitch: e < 1.00 mm pitch.*
2. *The typical ball diameter before mounting is 0.35 mm.*
3. *The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.*
4. *The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.*

Revision history

Table 36. **Document revision history**

Date	Revision	Changes
03-Mar-2025	1	Initial release.

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