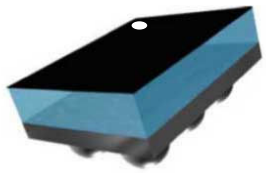
MLPF-WL-03D3

Datasheet

Low pass filter matched to STM32WL3xxx in low power mode, 10 dBm, 413-479 MHz, 4-layers and 2-layers PCB



Chip scale package on glass 5 bumps

Product status link
MLPF-WL-03D3

Features

- Integrated impedance matching to STM32WL3xxx
- 50 Ω nominal impedance on antenna side
- Deep rejection harmonic filter
- Low insertion loss
- Small footprint
- Low profile ≤ 630 µm after reflow
- High RF performances
- RF BOM and area reduction
- ECOPACK2 compliant component

Applications

- STM32WL3 sub-GHz wireless microcontrollers

Description

The MLPF-WL-03D3 integrates an impedance matching network and harmonics filter. The matching impedance network has been tailored to maximize the RF performances of STM32WL3xxx. The MLPF-WL-03D3 uses STMicroelectronics IPD technology on non-conductive glass substrate, which optimizes RF performances.

1 Characteristics

Table 1. Absolute ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
P_{IN}	Input power RF_{IN}	25	dBm
V_{ESD}	ESD ratings human body model (JESD22-A114-C), all I/O one at a time while others connected to GND	2000	V
T_{OP}	Operating temperature	-40 to +105	°C

Table 2. Impedances (T_{amb} = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Z_{RX}	Rx STM32WL3xxx single-ended impedance	-	Matched to STM32WL3xxx	-	Ω
Z_{TX}	Tx STM32WL3xxx single-ended impedance	-	Matched to STM32WL3xxx	-	Ω
Z_{ANT}	Antenna impedance	-	50	-	Ω

Table 3. Electrical characteristics and RF performances (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
f	Frequency range		413	433	479	MHz
IL_{RX}	Rx Insertion Loss $\|S_{21}\|$			1.55	2.10	dB
IL_{TX}	Tx Insertion Loss $\|S_{21}\|$			1.40	2.10	dB
RL_{ANT_RX}	Rx Return Loss $\|S_{11}\|$ on antenna		12	23		dB
RL_{ANT_TX}	Tx Return Loss $\|S_{11}\|$ on antenna		13	24		dB
Att	Harmonic rejection levels $\|S_{21}\|$	Attenuation at 2f0	45	50		dB
		Attenuation at 3f0	57	62		
		Attenuation at 4f0	47	58		
		Attenuation at 5f0	44	50		
		Attenuation at 6f0	42	47		
		Attenuation at 7f0	41	46		
		Attenuation at 8f0	38	45		
		Attenuation at 9f0	37	45		
		Attenuation at 10f0	33	45		

1.1 RF performances

Figure 1. Transmission in TX mode (dB)

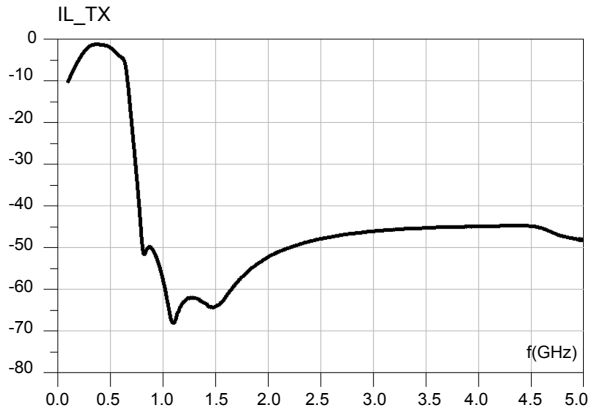


Figure 2. Insertion loss in TX mode (dB)

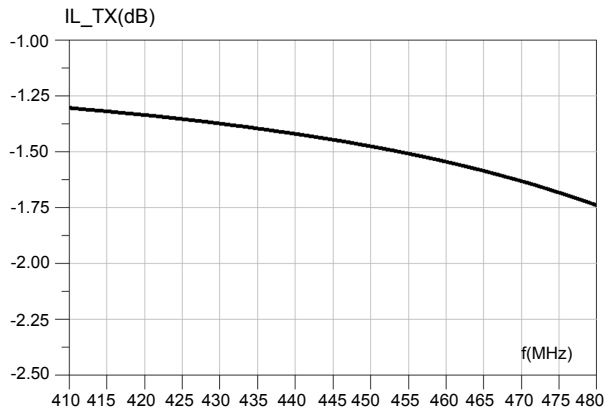


Figure 3. Insertion loss in RX mode (dB)

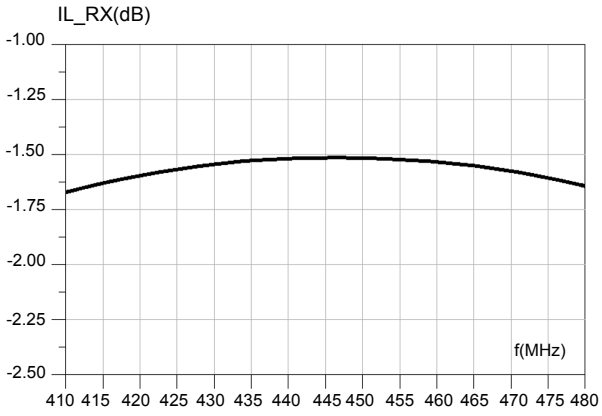


Figure 4. Return loss on antenna in TX mode (dB)

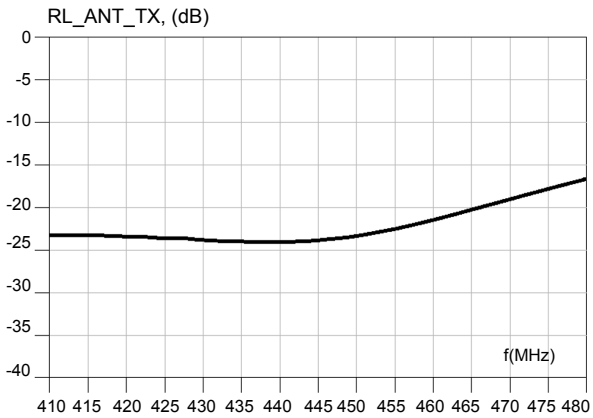
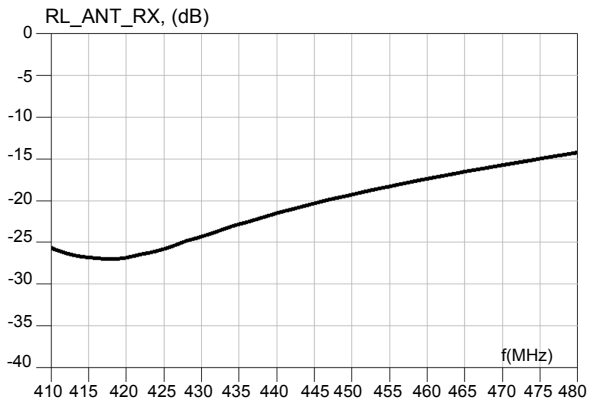


Figure 5. Return loss on antenna in RX mode (dB)



2 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 CSPG package information

Figure 6. CSPG 5 bumps package outline (bottom view - bumps up)

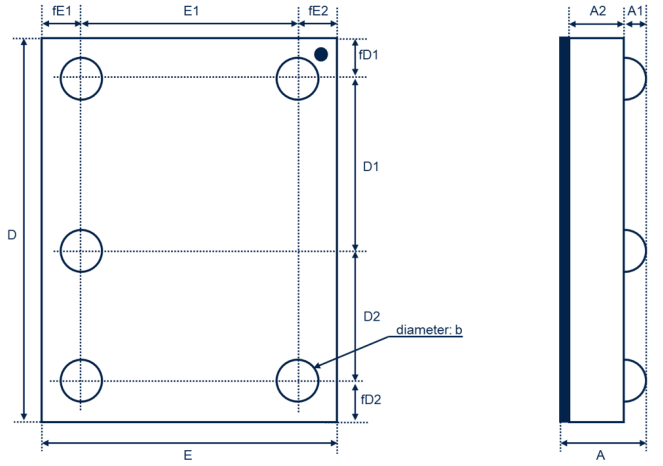


Table 4. CSPG 5 bumps mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.580	0.630	0.680
A1	0.180	0.205	0.230
A2	0.380	0.400	0.420
b	0.230	0.255	0.280
D	1.820	1.870	1.920
D1		0.800	
D2		0.600	
E	1.420	1.470	1.520
E1		1.000	
fD1		0.235	
fD2		0.235	
fE1		0.235	
fE2		0.235	

Figure 7. Marking

Dot, ST logo
ECOPACK® Grade
xx = marking
z = manufacturing location
yww = datecode
(y = year
ww = week)

Figure 8. Top view

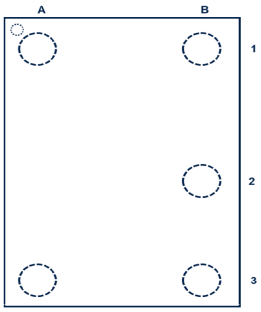


Table 5. Pad description top view (pads down)

Pad ref	Pad name	Description
A1	TX	TX input
A3	RX	RX output
B1	GND_TX	TX ground
B2	ANT	Antenna
B3	GND_RX	RX ground

Figure 9. Tape and reel outline

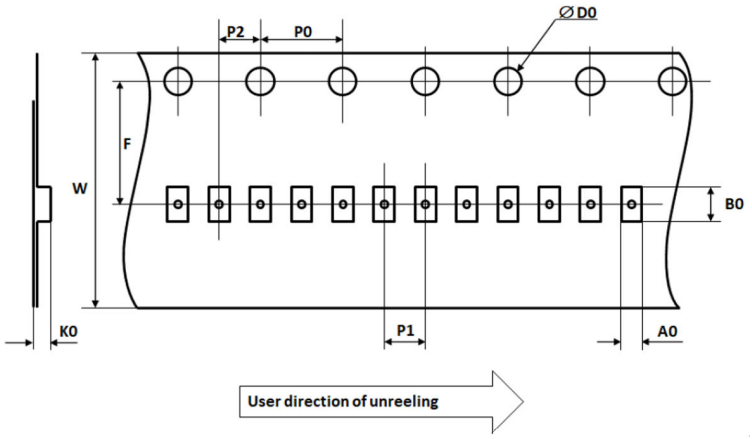


Table 6. Tape and reel mechanical data

Ref	Dimensions (millimeters)		
	Min	Typ	Max
A0	1.06	1.09	1.12
B0	1.66	1.69	1.72
D0	1.40	1.50	1.60
F	3.45	3.50	3.55
K0	0.69	0.72	0.75
P0	3.90	4.00	4.10
P1	1.95	2.00	2.05
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

3 Recommendation on PCB assembly

3.1 Land pattern

Figure 10. **PCB land pattern overview**

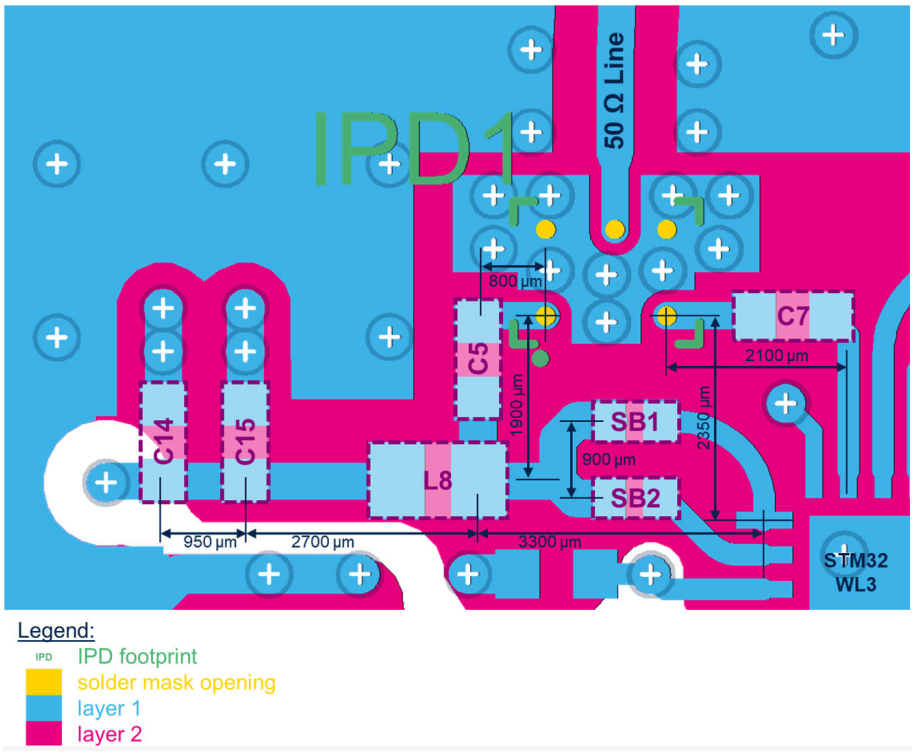


Table 7. **Reference BOM dedicated to the 4-layers PCB for the low band in low power mode: 10 dBm at 433 MHz**

Component	Value	Unit	Description
C5	100	pF	Tx DC block capacitor
C7	10	pF	Rx DC block capacitor
C14	100	pF	Tx decoupling capacitor
C15	100	nF	Tx decoupling capacitor
L8	18	nH	Tx biasing inductor
SB1	∞	Ω	TX_HP open
SB2	0	Ω	TX short

Table 8. Reference BOM dedicated to the 2-layers PCB for the low band in low power mode: 10 dBm at 433 MHz

Component	Value	Unit	Description
C5	100	pF	Tx DC block capacitor
C7	100	pF	Rx DC block capacitor
C14	100	pF	Tx decoupling capacitor
C15	100	nF	Tx decoupling capacitor
L8	24	nH	Tx biasing inductor
SB1	∞	Ω	TX_HP open
SB2	18	nH	Tx inductor

Figure 11. PCB land pattern recommendations

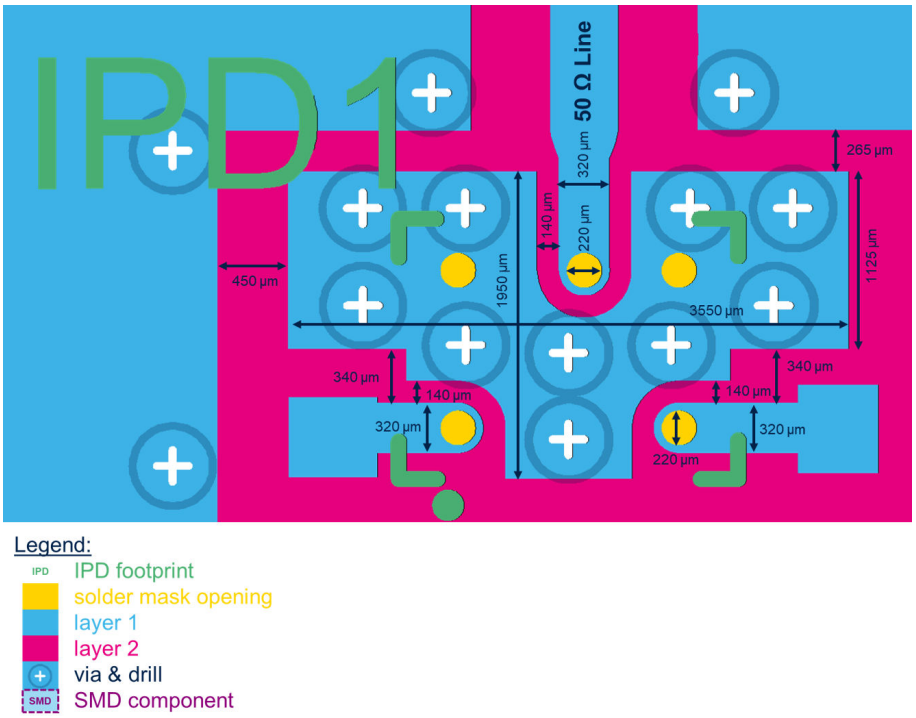


Table 9. RF transmission line characteristic impedances

RF transmission line	Value	Unit	Description
Antenna	50	Ω	Line between MLPF ANT pin and antenna

The layout around the IPD has to be followed as closely as possible.

The antenna line physical dimension has to be tuned according to a specific PCB stack up, if different from the one presented in the datasheet, to keep expected characteristic impedance values.

The dimensions of the lines were calculated considering the ground plane on layer 2.

The ground plane on the top layer is mandatory in front of the MLPF, with shape and definition generating the best possible equipotentiality.

The vias and drills density needs to be maximized near the MLPF area to ensure optimal RF performances, at least 10 vias and drills between the L2 ground plane and the L1 ground plane below the IPD.

The land pattern at layers 1 must be respected as described Figure 11.

Figure 12. PCB stack-up recommendations for 4-layers

Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	Solder Resist	0.010mm	3.5
1	Top Layer	Copper	0.041mm	
	Dielectric 1	Core-028	0.254mm	4.4
2	Signal Layer 1	Copper	0.018mm	
	Dielectric 2	FR4	0.914mm	4.4
3	Signal Layer 2	Copper	0.018mm	
	Dielectric 3	Core-028	0.254mm	4.4
4	Bottom Layer	Copper	0.041mm	
	Bottom Solder	Solder Resist	0.010mm	3.5
	Bottom Overlay			

The PCB stack-up presented above is the one that was used to validate the product. The PCB dimensions should be as close as possible to the recommendations, particularly for the thickness of the dielectric between the layer 1 and the layer 2 (for example, Dielectric 1 for 4-layers) keeping values within ±30 % (between 180 µm and 330 µm for 4-layers).

The other dimensions can vary without having a major impact on the overall functioning of the product.

Figure 13. PCB stack-up recommendations for 2-layers

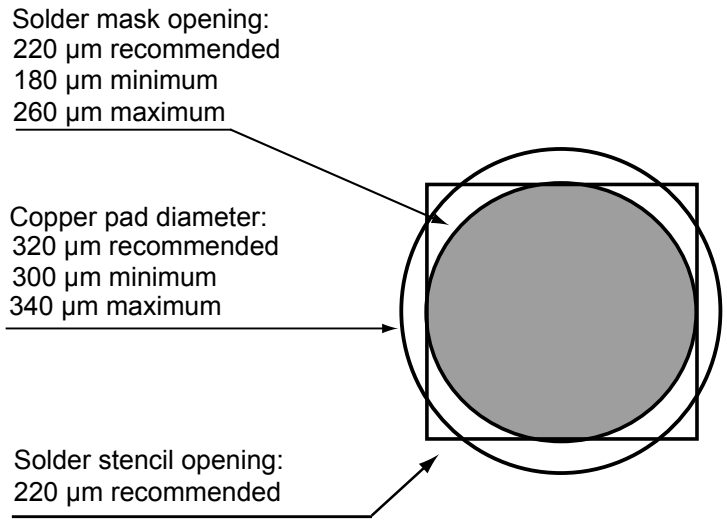
Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	Solder Resist	0.010mm	3.5
1	Top Layer	Copper	0.041mm	
	Dielectric 2	FR4	0.914mm	4.3
2	Bottom Layer	Copper	0.041mm	
	Bottom Solder	Solder Resist	0.010mm	3.5
	Bottom Overlay			

The PCB stack-up presented above is the one that was used to validate the product. The PCB dimensions should be as close as possible to the recommendations, particularly for the thickness of the dielectric between the layer 1 and the layer 2 (for example, Dielectric 2 for 2-layers) keeping values within ±30 % (between 650 µm and 1200 µm for 2-layers).

The other dimensions can vary without having a major impact on the overall functioning of the product.

3.2 Stencil opening design

Figure 14. **Footprint - 3 mils stencil - solder mask defined**



3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38 µm.

3.4 Placement

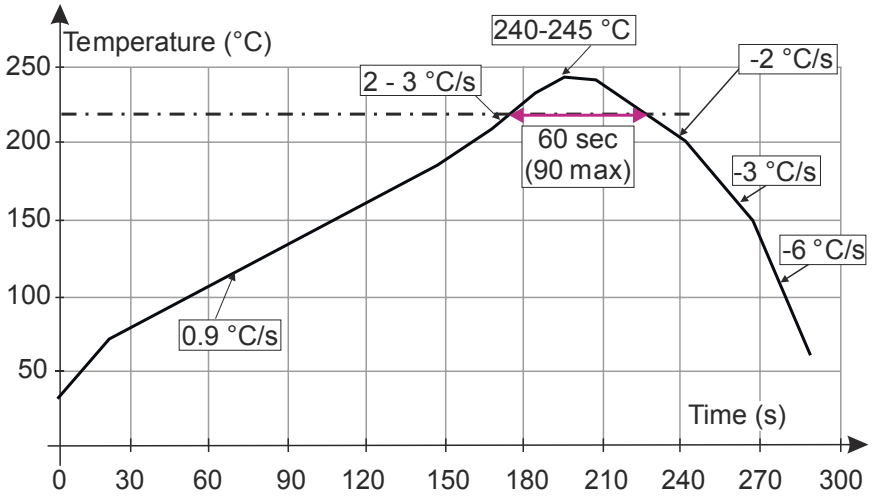
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

Figure 15. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Note: More information is available in the application note:

- *AN2348 Flip-Chip: "Package description and recommendations for use"*

4 Ordering information

Table 10. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
MLPF-WL-03D3	UL	CSPG	2.782 mg	5000	Tape and reel (7")

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
12-May-2025	1	Initial release.