Product Change Notification: SYST-09ZBWI898

Date:

16-Jul-2025

Product Category:

Ethernet Bridges

Notification Subject:

LAN7430/7431 Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-09ZBWI898_Affected_CPN_07162025.pdf
SYST-09ZBWI898_Affected_CPN_07162025.csv

Notification Text:

SYST-09ZBWI898

Microchip has released a new Document for the LAN7430/7431 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at **LAN7430/7431 Silicon Errata and Data Sheet Clarification**.

Notification Status: Final

Description of Change:

Added new erratum, Module 2.

Impacts to Data Sheet: None

Change Implementation Status: Complete

Date Document Changes Effective: 16 Jul 2025

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices::N/A

Attachments:

LAN7430/7431 Silicon Errata and Data Sheet Clarification

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Affected Catalog Part Numbers (CPN)

LAN7430/Y9X

LAN7431/YXX

LAN7430-I/Y9X

LAN7430-I/Y9XVAO

LAN7431-I/YXX

LAN7431-V/YXX

LAN7431-V/YXXV03

LAN7431-V/YXXVAO

LAN7431T-V/YXX

LAN7431T-V/YXXV01

LAN7431T-V/YXXV02

LAN7431T-V/YXXVAO

LAN7430T/Y9X

LAN7431T/YXX

LAN7430T-I/Y9X

LAN7430T-I/Y9XVAO

LAN7431T-I/YXX

LAN7430/7431

LAN7430/7431 Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for the LAN7430/7431 family of devices, which includes the following:

- LAN7430
- LAN7431

The silicon errata discussed in this document are for silicon revisions listed in Table 1. A summary of LAN7430/7431 silicon errata is provided in Table 2.

TABLE 1: AFFECTED SILICON REVISIONS

Part Number	Revision
LAN7430, LAN7431	B0, B1

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary	Affected SKU
1.	VLAN_TYPE register not checked and compared with the default value, 0x8100	ALL
2.	Unable to disable LAN7431 25 MHz reference clock (REFCLK_25 pin)	LAN7431

Silicon Errata Issue

Module 1: VLAN_TYPE register not checked and compared with the default value, 0x8100

DESCRIPTION

The VLAN_TYPE register will not be checked and compared with the default value, 0x8100. The VLAN_TYPE register will accept either the default value (0x8100) or the input value. The device will check if the value is either 0x8100 or another input value, but it will not match an input value with the default value of 0x8100.

END USER IMPLICATIONS

The device cannot support a tag in tag frames if the types are not both the same value.

Work around

There is no work around.

PLAN

This erratum will not be corrected in a future revision.

Module 2: Unable to disable LAN7431 25 MHz reference clock (REFCLK_25 pin)

DESCRIPTION

The REFCLK25_EN bit (bit 24 of the HW_CFG register), intended to enable/disable the 25 MHz reference clock, does not function properly. This results in the inability to disable the 25 MHz reference clock (REFCLK_25 pin).

END USER IMPLICATIONS

The REFCLK_EN bit cannot be used to disable to the 25 MHz reference clock (REFCLK_25). Instead, an alternate work around must be used.

Work around

In the LAN7431, GPIO11 is the alternate function on the REFCLK_25 pin. It is possible to “disable” the REFCLK_25 by activating the GPIO11 alternate function and driving a constant value.

To configure REFCLK_25 as GPIO11, clear bit 27 of the GPIO_CFG1 register (Address: 0x54). Next, set the GPIO buffer type by configuring the pad type to either push/pull or open drain, which is controlled by bit 11 of the GPIO_CFG1 register (Address: 0x54). For a push/pull driver, set the register; for an open drain driver, clear the bit. To set the GPIO direction as output, set bit 27 of the GPIO_CFG0 register (Address: 0x50). Finally, to drive a constant high or low signal onto the pin, configure bit 11 of the GPIO_CFG0 register (Address: 0x50) accordingly.

This can be performed as an EEPROM configuration, driver initialization code, or register write during run time.

PLAN

This erratum will not be corrected in a future revision.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000822B (07-09-25)	Module 2.	Added new erratum
DS80000822A (10-04-19)	All	Initial release

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