

ICL8830 high-frequency GaN controller for LED lighting

Single stage PFC flyback controller compatible with GaN technology



About this document

Scope and purpose

High power density and miniaturization are the main trends in power conversion. High frequency operation helps shrink the size of the key passive components. The “High power density, QR flyback solution” engineering report [3] describes many aspects of designing high power density switching mode power supply (SMPS). GaN switches allow operating at much higher switching frequency (300-500 kHz and even higher) without increased losses thanks to very low parasitic capacitances (C_{oss} , C_{iss} , and C_{rss}) and no body diode recovery losses.

The ICL8830 controller is designed to be operated with GaN switches and it enables you to achieve the switching frequencies mentioned above with extremely precise timing control. The product is pin-to-pin compatible with Infineon’s well-known ICL88XX controller family and can easily be integrated into existing designs with minimal changes. High frequency operation needs special attention to magnetics design, PCB layout, parasitic elements, and electromagnetic interference EMI.

The document presents the design aspects of LED drivers based on ICL8830 with GaN switches, such as loss optimization, EMI filter improvement, and system limitation.

Intended audience

This document is intended for engineers designing a high power density LED driver based on Infineon’s ICL8830 controller and GaN flyback switch.

Table of contents

Table of contents

About this document.....	1
Table of contents.....	2
1 System description.....	3
2 Design hints.....	4
2.1 Limits	4
2.2 Transformer design	6
2.3 EMI filter design	7
2.4 ICL8830 operating with CoolGaN™ drive devices.....	9
2.5 Aspects of using a CoolGaN™ transistor	10
References.....	11
Revision history.....	12
Disclaimer.....	13

System description

1 System description

Nowadays, the majority of LED lighting applications are based on a two stage concept:

- The first stage is responsible for power factor correction, PFC and isolation. The PFC flyback topology is used in constant voltage mode (CV)
- The second stage is a buck converter operating in constant current mode (CC) which is responsible for current regulation, low frequency 100 and 120 Hz ripple suppression and dimming

The system block diagram is shown in [Figure 1](#). To improve system efficiency (by up to 3%), it is recommended to use the headroom control feedback described in the [document](#).

Since the primary stage is the main contributor to system size (up to 70-80% of the LED driver), you will need to take a closer look at and address the following design points:

- Normally the primary stage operates at a switching frequency of up to 150 kHz. It is mostly connected to the EN IEC 55015 limit curve. At frequencies higher than 150 kHz, the limit drops down by 17.5 dB. Hence, the line filter requirements get much higher while the design also becomes much more complex compared to the standard frequency operation
- The second limitation to maximum switching frequency is related to switching losses and fast control. Using GaN switches significantly reduces switching losses due to small parasitic capacitances. Soft-switching topologies like CrCM with valley switching help reduce switching losses and improve EMI. The new ICL8830 controller offers GaN switch driving and control with precise valley detection and minimum delay
- The transformer design needs additional attention. Increasing switching frequency proportionally increases the snubber losses, so the leakage inductance must be minimized to avoid additional losses. Therefore, it is recommended to use high-frequency magnetic materials

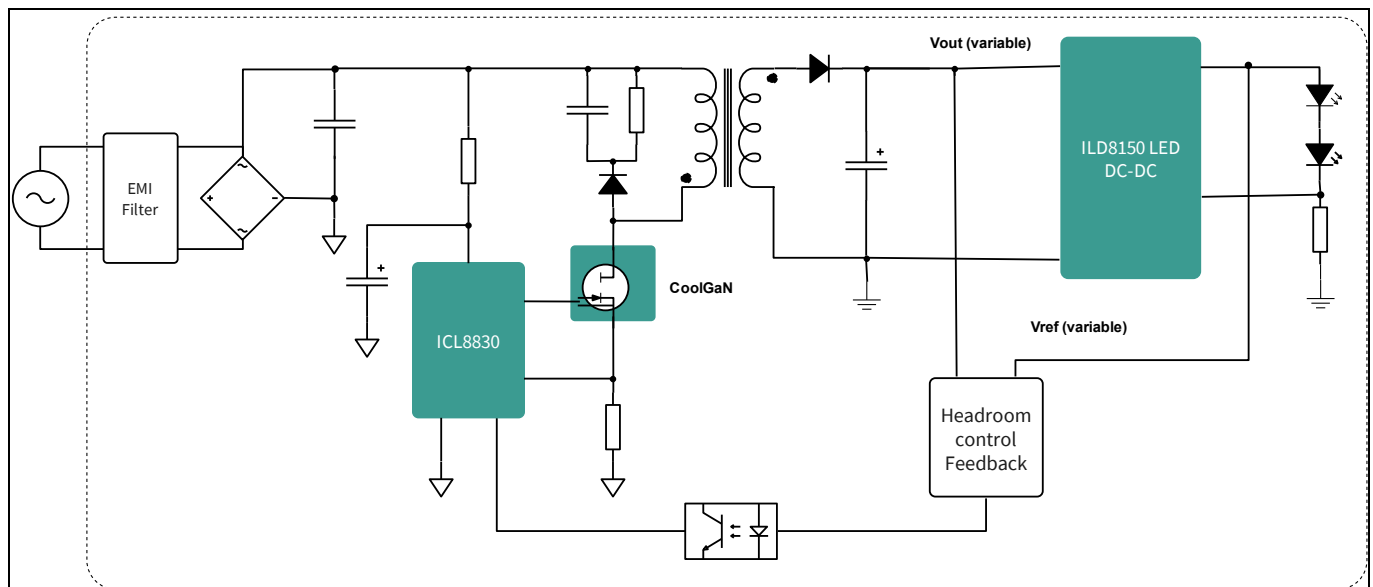


Figure 1 System block diagram

Design hints

2 Design hints

2.1 Limits

Switching frequency f_{SW} limit relates to the valley detection and delay t_{ZCDGD} between the signal from ZCD to GD pins, as shown in Figure 2. t_{ZCDGD} should be less than or equal to half of an oscillation period, T_{OSC} .

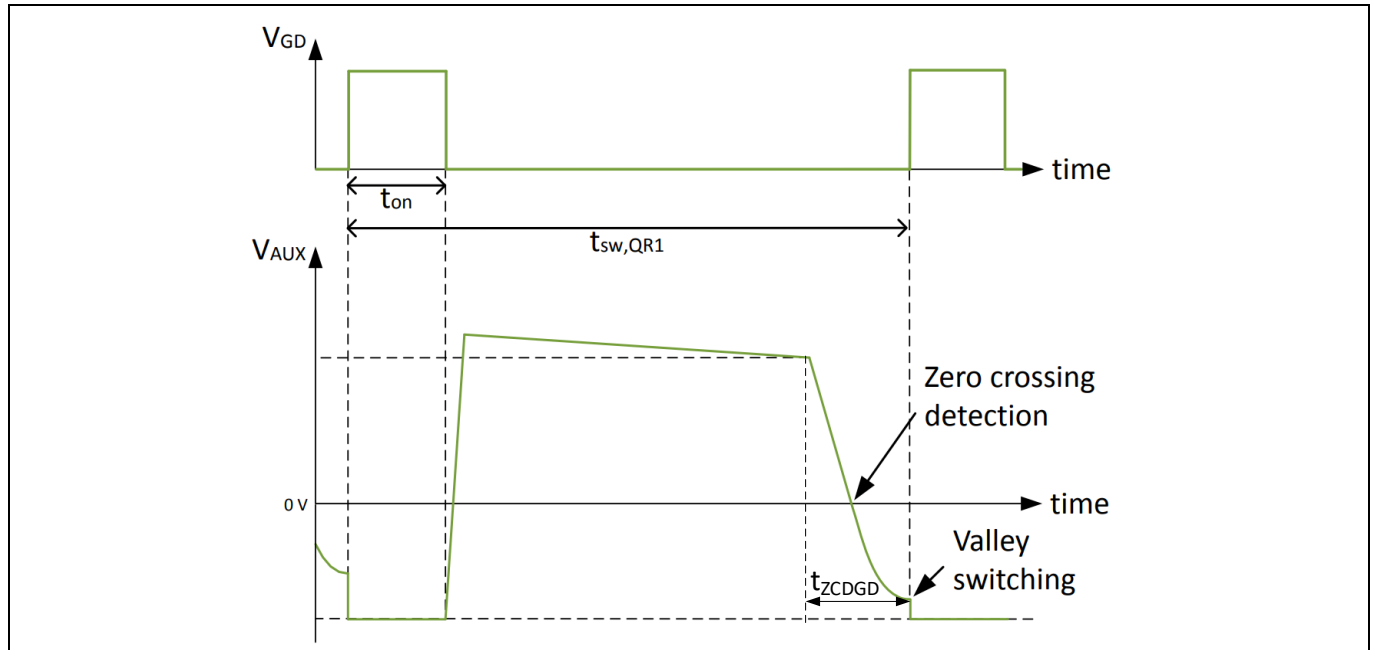


Figure 2 Zero crossing detection

The borderline for the oscillation frequency that is properly detected is about 2 MHz. If t_{ZCDGD} is a little bigger than half of T_{OSC} , it results in a small delay in the IC valley detection. If T_{OSC} is smaller than t_{ZCDGD} , the controller is unable to properly perform valley detection. The misdetection might lead to valley jumping or losing control. Figure 3 shows two cases – little delay and valley jumping. Figure 4 shows valley detection and control loss.

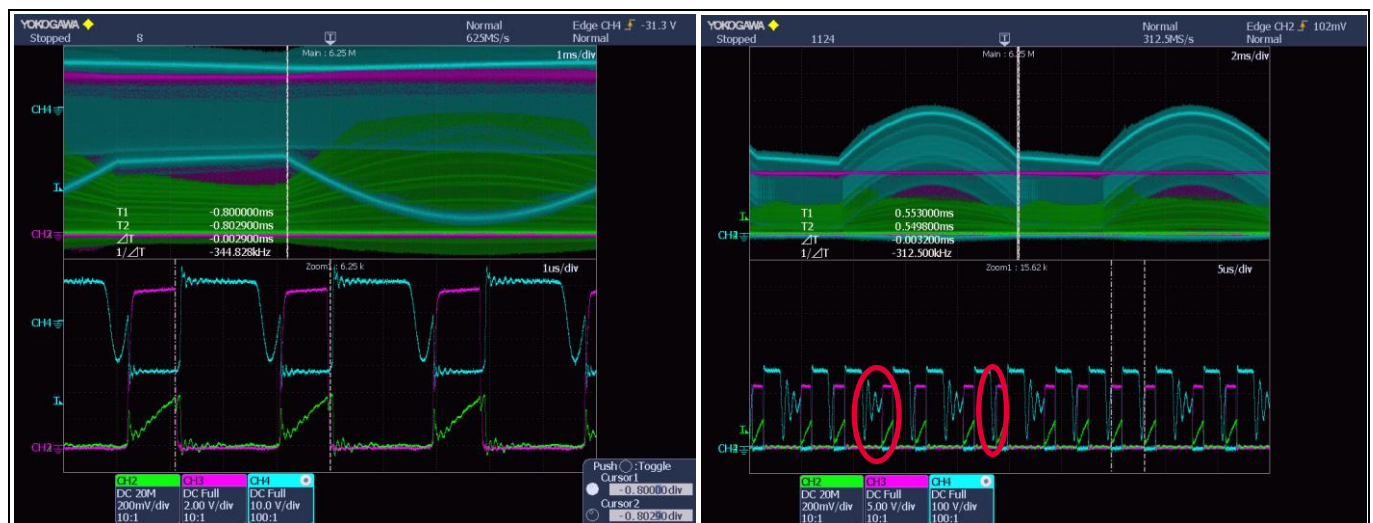


Figure 3 Valley detection delay Pink – Gate, Blue – Drain, Green – Shunt

Design hints

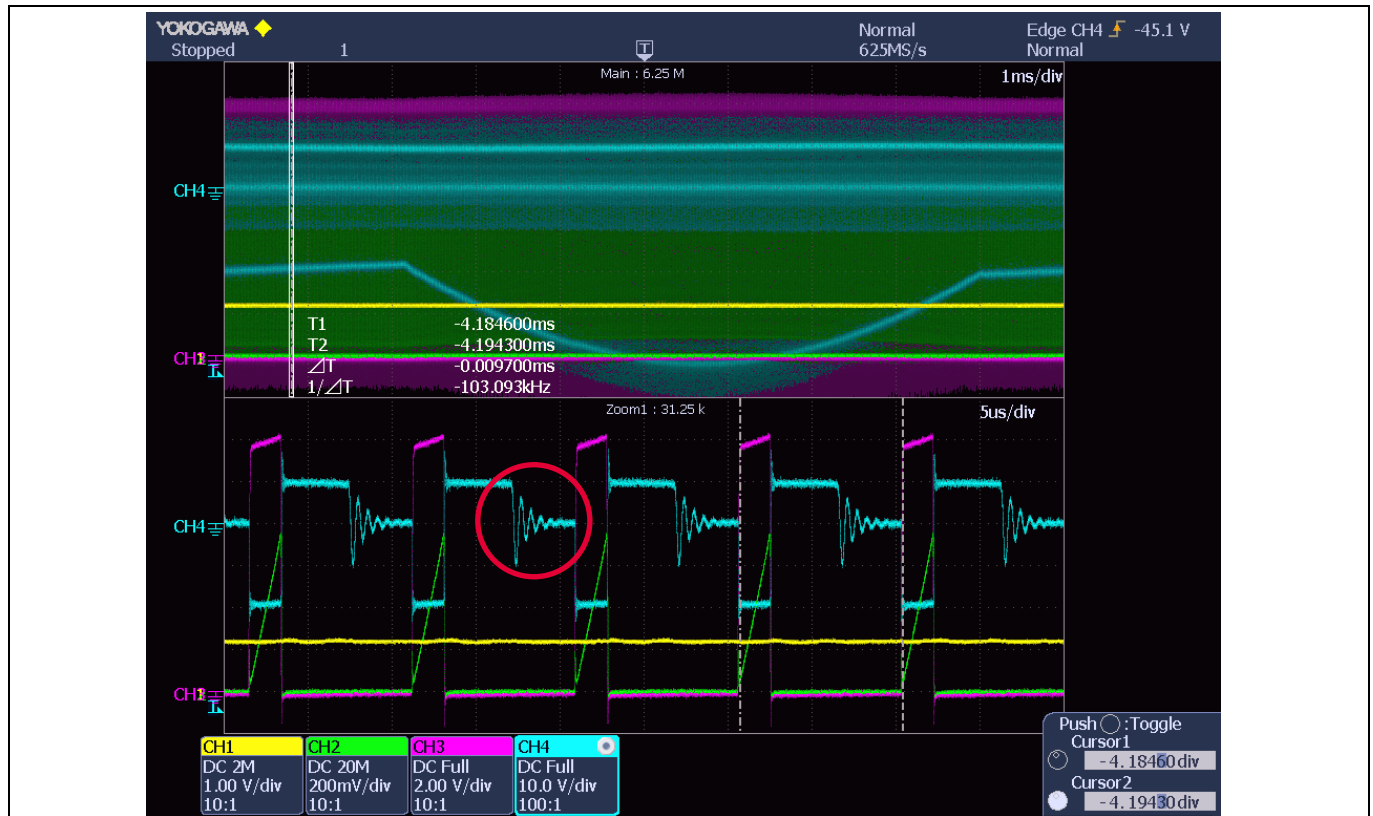


Figure 4 Valley misdetection **Pink** – Gate, **Blue** – Drain, **Green** – Shunt

- The oscillation frequency is calculated using **Equation 1**,

$$F = \frac{1}{2\pi\sqrt{L_p C_{sum}}}$$

$$C_{sum} = C_{oss}(V) + C_{trans} + C_{rect}/n^2$$

Equation 1 Oscillation frequency calculation

Where,

L_p – Primary winding inductance

C_{sum} – Sum of the $C_{oss}(V)$ as a function of the V_{ds} voltage

C_{trans} – Parasitic transformer capacitance and

C_{rect}/n^2 – Rectifier-reflected capacitance

n – Transformer turns ratio

- The C_{sum} assumption is the first step. A proper voltage and R_{DS_ON} class GaN switch was chosen. Use the $C_{o(tr)}$ (effective output capacitance, time related) from the datasheet. C_{rect} can also be found in the rectifier datasheet. The transformer turns ratio (n) can be calculated using the ICL88xx [calculation tool](#). C_{trans} depends on transformer construction and may vary from 30 to 300 pF. 30-40 pF is used for classic transformers with layers interleaving and 100-300 pF is used for planar transformer (the numbers are based on practice)
- Based on C_{sum} , L_p primary inductance and other components are calculated using the [calculation tool](#)

Design hints

- The resistor at the TD pin defines the delay t_{ZCDGD} , the minimum value that can be achieved is 18 kΩ without an active startup circuit and 12 kΩ with an active startup circuit

2.2 Transformer design

High frequency operation requires additional attention to the transformer design. The core losses are significantly increased at higher switching frequencies. Figure 4 shows the core losses for different magnetic materials, winding losses (copper losses), and total losses for a 50 W design classic transformer. It is clear that high frequency materials like N49 or equivalent are to be used to minimize losses.

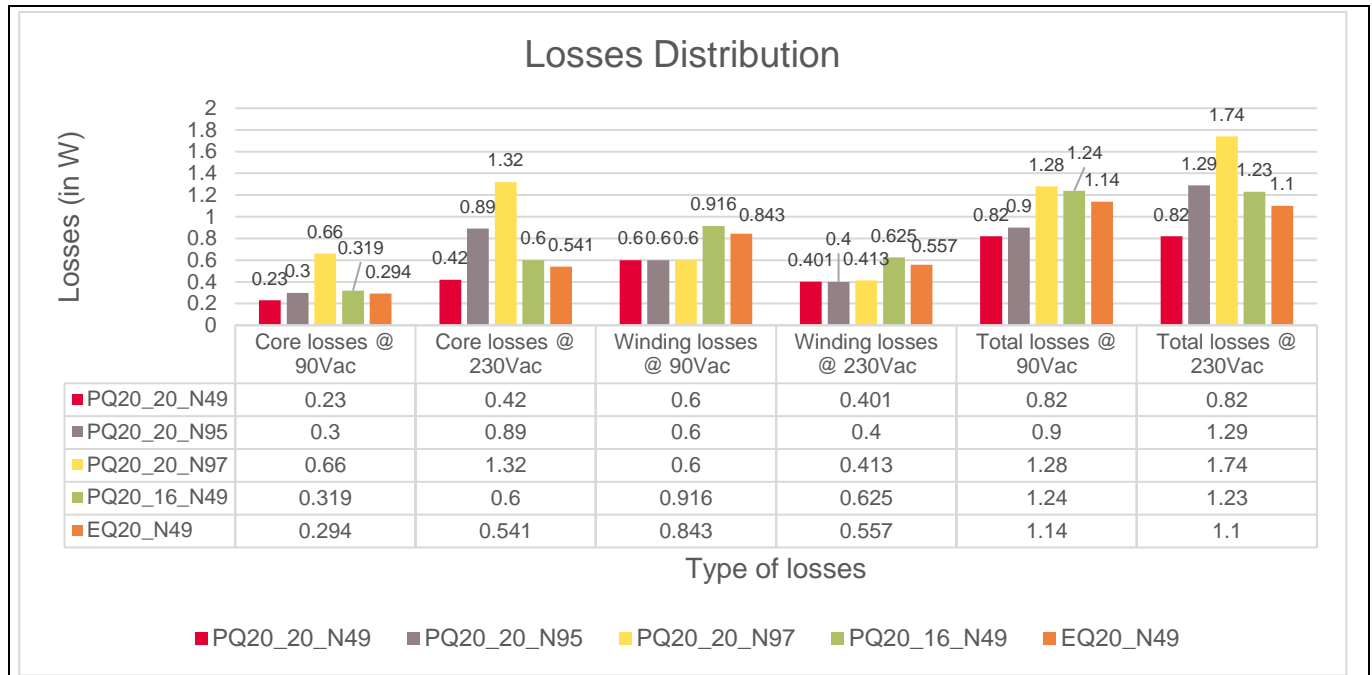


Figure 5 Loss distribution for different magnetic materials simulated by the **Frenetic simulator**

Losses in the snubber are calculated by Equation 2,

$$P_{Snub} = \frac{1}{4} \times L_{leak} \times I_{Q1.MAXPK}^2 \times f_{SW} \times \frac{V_R + V_{SPIKE}}{V_{SPIKE}}$$

Equation 2 Snubber losses calculation equation

where L_{leak} is the leakage inductance.

As you can observe, the snubber losses increase proportionally with the switching frequency. If you increase switching frequency from 50 kHz to 500 kHz, keeping the same leakage inductance, the power dissipated by the snubber increases by ten times. Transformers with good interleaving of primary and secondary windings may achieve the best result for leakage inductance ($\geq 1\%$). This number is reasonable for classic 50-100 kHz switching frequency designs, but not good enough for high frequency designs.

As a result, a planar transformer, one that by design achieves a smaller leakage inductance, is a better solution. Leakage inductance for planar transformers is in the range of 0.1 - 0.3% (based on practical design), which makes the technology suitable for this application. A drawback of planar transformers is a higher C_{trans} interwinding capacitance compared to wire-wound transformers.

Design hints

How does it affect the operation and performance in this application?

Turn-on losses are calculated using [Equation 3](#)

$$P_{turn_on} = \frac{1}{2} \times C_{sum} \times U_{DS_valley}^2 \times f_{SW}$$

Equation 3 Turn-on losses calculation equation

U_{DS_valley} at low-line 115 V_{AC} is typically about zero, which means P_{turn_on} losses are also close to zero. At high-line 230 V_{AC} U_{DS_valley} varies from 0 to 200 V. Since the U_{DS_valley} voltage squared term is the dominant losses component in the equation, C_{sum} only has a minor effect.

C_{trans} Increases by four to ten times, it makes it dominating in the C_{sum} . If you assume the oscillating frequency at the same level of 2 MHz, it allows you to proportionally decrease L_p primary inductance by two to four times. As a result, the transformer size is decreased. It also leads to a proportional f_{SW} switching frequency increase up to a ≤ 1 MHz range. At the MHz range, the EMI filter and passive components get much smaller and cheaper, drastically reducing the system size and cost.

2.3 EMI filter design

The following aspects need to be considered in the EMI filter design to comply with EN IEC 55015, where the limit curve drops down by 17.5 dB at frequencies higher than 150 kHz and 27 dB at 550 kHz:

- Conducted emissions (EMC) are measured before the EMI filter, as shown in [Figure 6](#), to define the spectrum

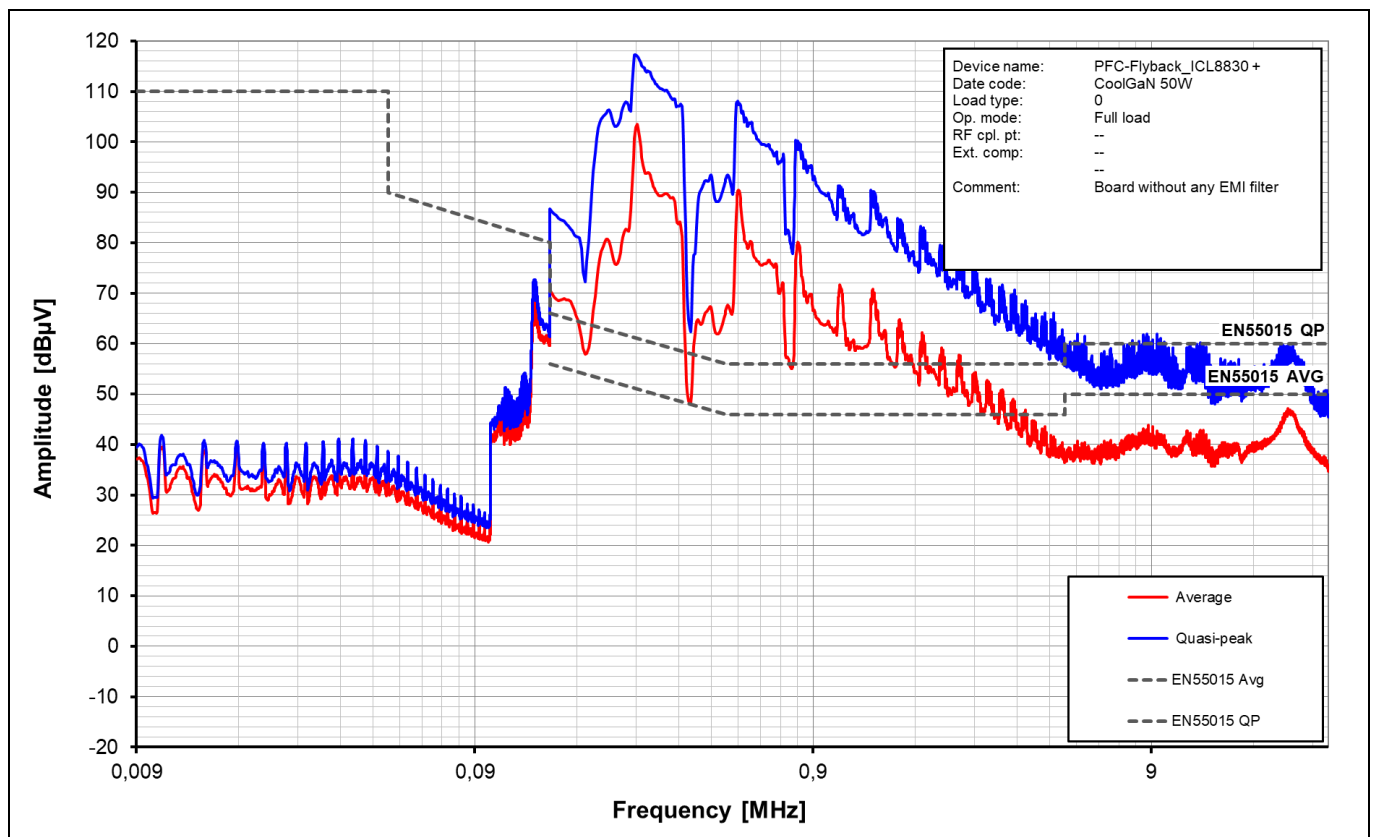


Figure 6 EMC measurement before the EMI filter

When the spectrum is defined, the common mode choke is chosen for the EMI filter with a center attenuation frequency at the noise peak and proper attenuation at the peak point to dump noise under the limit with the

ICL8830 high-frequency GaN controller for LED lighting

Single stage PFC flyback controller compatible with GaN technology

Design hints

margin. For instance, if the peak point is 300 kHz and a 70 dB minimum attenuation is needed, [744869161273](#) perfectly fits for the task with the peak attenuation of 75 dB, as shown in [Figure 7](#).

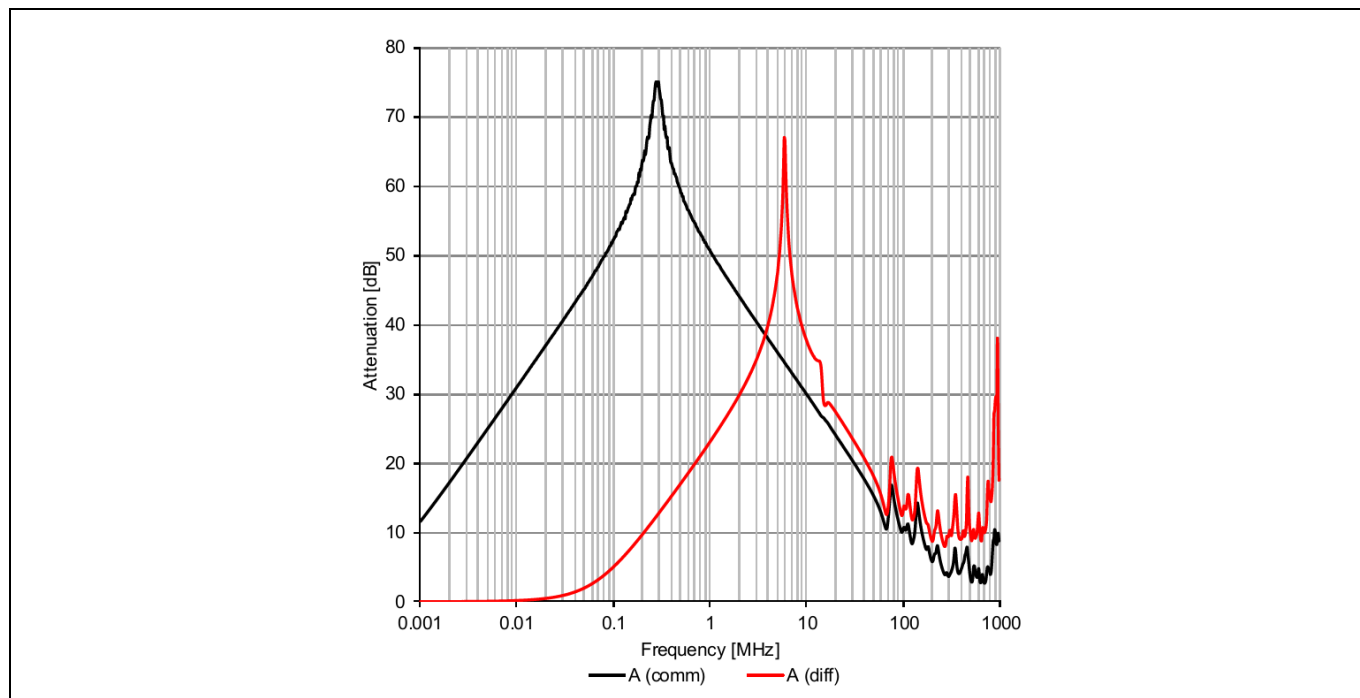


Figure 7 [744869161273](#) attenuation characteristics

- The final EMC measurement for a 50 W design is shown in [Figure 8](#)



Figure 8 EMC measurement for a 50 W design

Design hints

2.4 ICL8830 operating with CoolGaN™ drive devices

CoolGaN™ drive devices have many advantages compared to discrete GaN devices:

- Gate driver integration makes PCB layout much easier. The main challenge of the gate path grounding is solved by the driver integration
- Integrated current sensing eliminates the additional losses on the shunt resistor

Figure 9 shows the block diagram of ICL8830 with CoolGaN™ drive device; the key point to consider is the R_{CS} calculation.

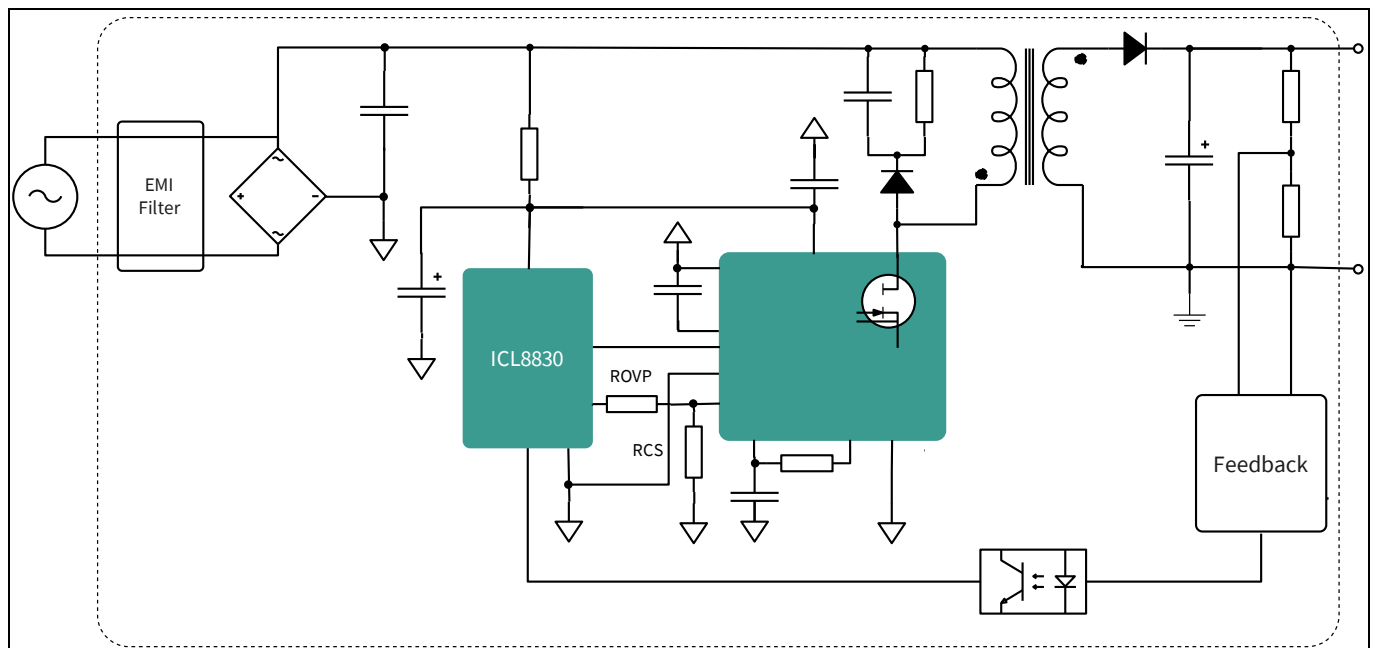


Figure 9 ICL8830 with integrated CoolGaN™

The R_{CS} is calculated using Equation 4,

$$R_{CS} = \frac{V_{OCP1} \times M}{I_{PRI-MAX(PK)}}$$

Equation 4 R_{CS} calculation

Where,

V_{OCP1} = Overcurrent threshold

$I_{PRI-MAX(PK)}$ = Primary maximum peak current

M = Current mirroring coefficient

The R_{OVP} is calculated using Equation 5. The equation is modified from [4] since R_{OVP} and R_{CS} are connected in a series.

Design hints

$$R_{OVP} = \frac{V_{OCP1}}{I_{CS,OVP}} - R_{CS}$$

Equation 5 R_{OVP} calculation

2.5 Aspects of using a CoolGaN™ transistor

- GIT GaN devices can be connected directly driven by ICL8830, as shown in Figure 10. The gate driving component calculation is described in this whitepaper [5].

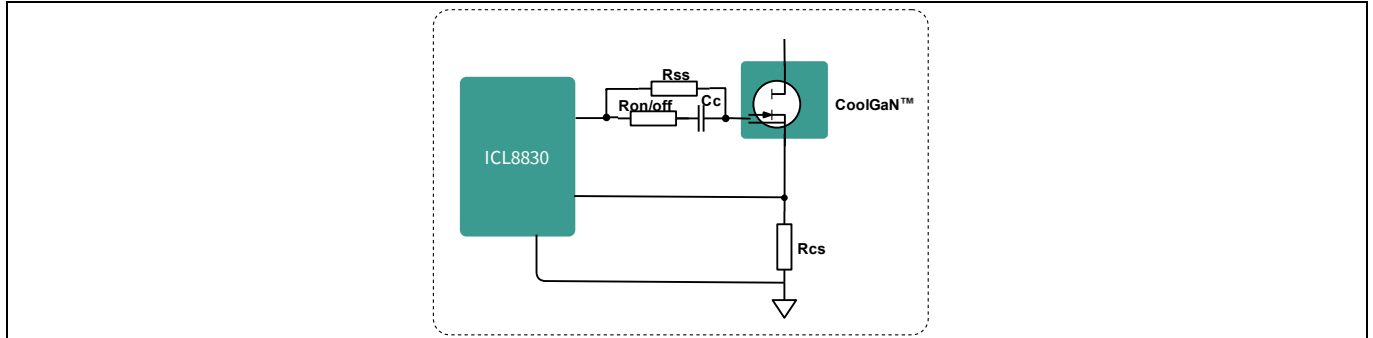


Figure 10 ICL8830 gate drive connection to GIT GaN

- The PCB layout for GaN applications is critical since the circuit operates at high dV/dt and di/dt . Incorrect PCB layout may lead to circuit misoperation and cause an EMI issue. The PCB layout guide is described in the design guide [4] and reference design [3]

GaN switches do not have the avalanche effect like Si MOSFETs and hence can withstand high voltage spikes without damage, as typically defined in the datasheet. But short repetitive overvoltage stress in combination with high junction temperature affects the GaN device lifetime. This whitepaper [6] explains the degradation mechanism in GaN devices. Since LED lighting needs long operations (10-15 years) without failure, it is not recommended to exceed the absolute maximum drain-to-source voltage.

References

References

- [1] Infineon Technologies AG: Datasheet - *ICL8830*; [Available online](#)
- [2] Infineon Technologies AG: *Design Calculation Tool LED Controller ICL88XX*; [Available online](#)
- [3] Infineon Technologies AG: Engineering report - *ICL8810 high power density PSU for LED lighting*; [Available online](#)
- [4] Infineon Technologies AG: Design Guide - *ICL88xx flyback design guide*; [Available online](#)
- [5] Infineon Technologies AG: Whitepaper - *Gate drive configurations for GaN power transistors*; [Available online](#)
- [6] Infineon Technologies AG: Whitepaper - *Reliability and qualification of high-voltage CoolGaN™ GIT HEMTs*; [Available online](#)

ICL8830 high-frequency GaN controller for LED lighting

Single stage PFC flyback controller compatible with GaN technology



Revision history

Revision history

Document revision	Date	Description of changes
V 1.0	2025-05-12	Initial release

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-05-12

Published by

Infineon Technologies AG

81726 Munich, Germany

**© 2025 Infineon Technologies AG.
All Rights Reserved.**

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

AN165544

Important notice

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.