

DDR5 SDRAM SODIMM/CSODIMM Addendum

**MTC8C1084S1SC, MTC8C1084S1VC – 16GB
16Gb Die Revision H**

Features

Information provided here is in addition to or supercedes information provided in the Micron DDR5 SODIMM/CSODIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 SODIMM/CSODIMM core data sheet
- 262-pin, DDR5 small outline dual in-line memory module (DDR5 SODIMM/CSODIMM)
- Fast data transfer rate:
PC5-5600, PC5-6400, PC5-7200, PC5-8000
- 16GB (2Gig x 64)
- Single-rank
- 32 internal banks; 8 groups of 4 banks each

Options

- Operating temperature
 - Commercial ($0^{\circ}\text{C} \leq T_{\text{OPER}} \leq 95^{\circ}\text{C}$)
- Frequency/CAS latency
 - 0.357ns @ CL = 46 (DDR5-5600)
 - 0.312ns @ CL = 52 (DDR5-6400)
 - 0.277ns @ CL = 58 (DDR5-7200)
 - 0.250ns @ CL = 64 (DDR5-8000)

Marking

C

56B

64B

72B

80B

Figure 1: 262-Pin DDR5 SODIMM (R/C-A0)

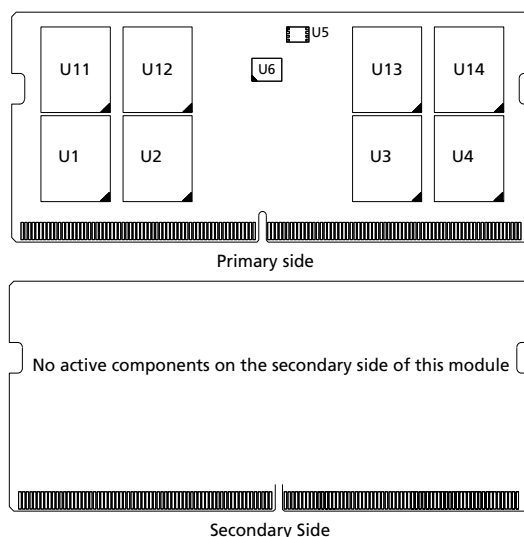


Figure 2: 262-Pin DDR5 CSODIMM (R/C-A0)

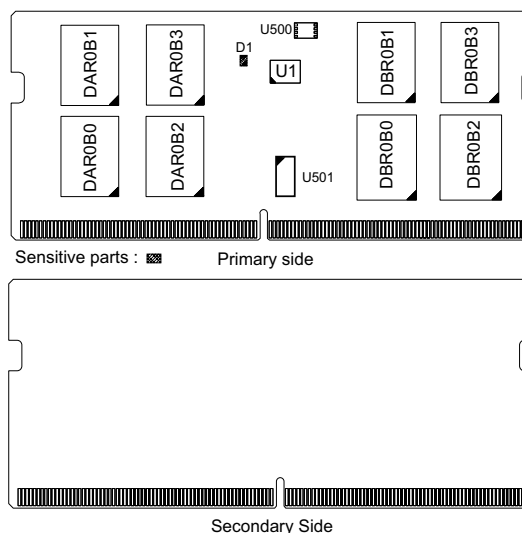


Table 1: Addressing

Parameter	16GB
Row address ¹	64K (R0-R15)
Column address ¹	1K (C0-C9)
Device bank group address ¹	8 (BG0-BG2)
Device bank address per bank group ¹	4 (BA0-BA1)
Device configuration	16Gb (2Gb x 8), 32 banks
Module rank address	1 (CS0_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.

Table 2: Part Numbers and Timing Parameters – 16GB Modules

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL _n RCD _n RP)	Designation ²
MTC8C1084S1SC56BH1	16GB	2Gb x 64	44.8 GB/s	0.357ns/5600 MT/s	46-45-45	Production
MTC8C1084S1VC64BH1	16GB	2Gb x 64	51.2 GB/s	0.312ns/6400 MT/s	52-52-52	Production
MTC8C1084S1VC72BH1	16GB	2Gb x 64	57.6 GB/s	0.277ns/7200 MT/s	58-58-58	Preliminary
MTC8C1084S1VC80BH1	16GB	2Gb x 64	64.0 GB/s	0.250ns/8000 MT/s	64-64-64	Advance

Notes: 1. Base device: MT60B2G8, 16Gb DDR5 SDRAM Die Revision H. The data sheet for the base device can be found on [micron.com](https://www.micron.com).

2. **Production:** Although considered final, these specifications are subject to change as further product development and data characterization sometimes occur. **Preliminary:** For evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications. **Advance:** Contains initial descriptions of products still under development. For evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications.

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DQ Map

Table 3: SODIMM Component-to-Module DQ Map (R/C-A0)

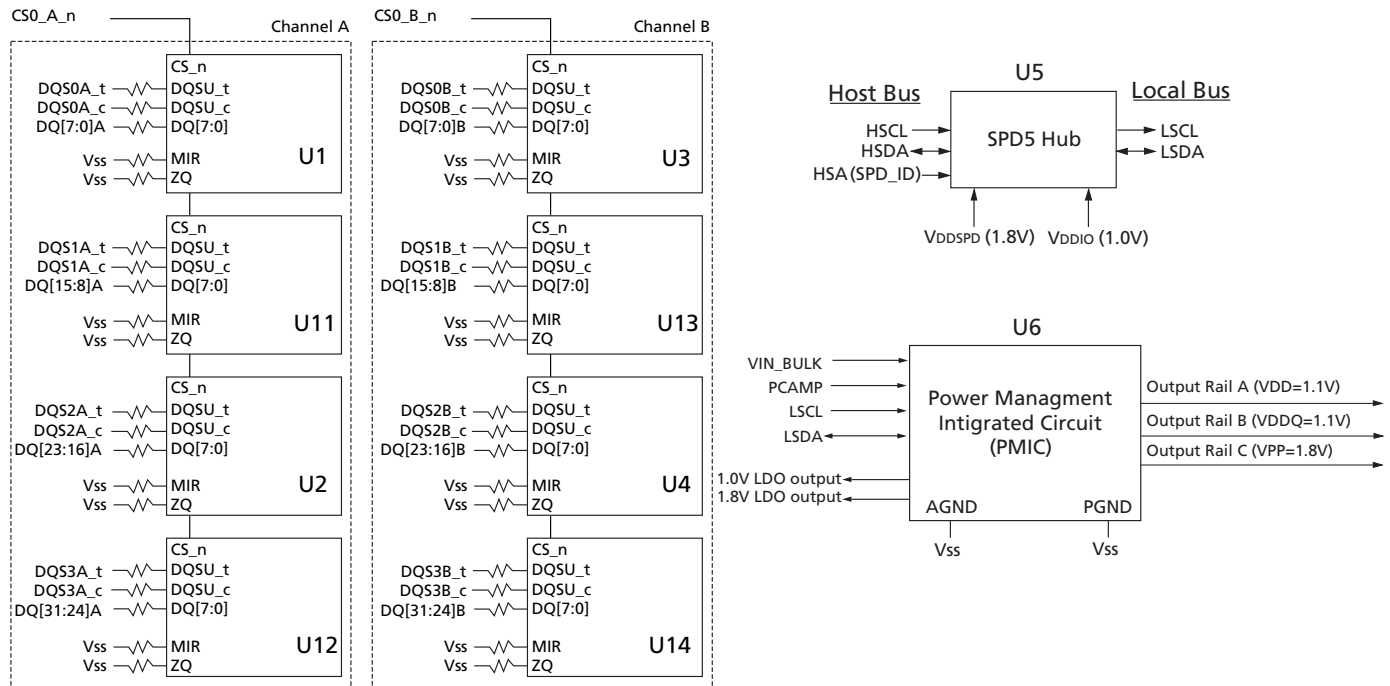
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	0A	11	U2	0	16A	53
	1	1A	12		1	17A	54
	2	2A	15		2	18A	57
	3	3A	16		3	19A	58
	4	6A	27		4	22A	69
	5	5A	26		5	21A	68
	6	4A	23		6	20A	65
	7	7A	30		7	23A	72
U3	0	0B	179	U4	0	16B	221
	1	1B	180		1	17B	222
	2	2B	183		2	18B	225
	3	3B	184		3	19B	226
	4	6B	195		4	22B	237
	5	5B	194		5	21B	236
	6	4B	191		6	20B	233
	7	7B	198		7	23B	240
U11	0	9A	34	U12	0	25A	76
	1	8A	31		1	24A	73
	2	11A	38		2	27A	80
	3	10A	35		3	26A	77
	4	15A	50		4	31A	92
	5	12A	45		5	28A	87
	6	13A	46		6	29A	88
	7	14A	49		7	30A	91
U13	0	9B	202	U14	0	25B	244
	1	8B	199		1	24B	241
	2	11B	206		2	27B	248
	3	10B	203		3	26B	245
	4	15B	218		4	29B	256
	5	12B	213		5	28B	255
	6	13B	214		6	31B	260
	7	14B	217		7	30B	259

Table 4: CSODIMM Component-to-Module DQ Map (R/C-A0)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
DAR0B0	0	0A	11	DAR0B1	0	9A	34
	1	1A	12		1	8A	31
	2	2A	15		2	11A	38
	3	3A	16		3	10A	35
	4	6A	27		4	15A	50
	5	5A	26		5	12A	45
	6	4A	23		6	13A	46
	7	7A	30		7	14A	49
DAR0B2	0	16A	53	DAR0B3	0	25A	76
	1	17A	54		1	24A	73
	2	18A	57		2	27A	80
	3	19A	58		3	26A	77
	4	22A	69		4	31A	92
	5	21A	68		5	28A	87
	6	20A	65		6	29A	88
	7	23A	72		7	30A	91
DBR0B0	0	0B	179	DBR0B1	0	9B	202
	1	1B	180		1	8B	199
	2	2B	183		2	11B	206
	3	3B	184		3	10B	203
	4	6B	195		4	15B	218
	5	5B	194		5	12B	213
	6	4B	191		6	13B	214
	7	7B	198		7	14B	217
DBR0B2	0	16B	221	DBR0B3	0	25B	244
	1	17B	222		1	24B	241
	2	18B	225		2	27B	248
	3	19B	226		3	26B	245
	4	22B	237		4	29B	256
	5	21B	236		5	28B	255
	6	20B	233		6	31B	260
	7	23B	240		7	30B	259

Functional Block Diagram

Figure 3: Functional Block Diagram (R/C-A0)



- Notes:
1. The ZQ ball on each DDR5 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
 2. Functional block diagram is for reference only.

Revision History

Rev. B – 06/2025

- Part number corrected in Table 2

Rev. A – 02/2025

- Initial release

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