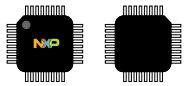
MCXE245/246/247

Robust 5V Arm Cortex M4F MCU with up to 2MB flash

Rev. 2 — 14 July 2025 Product Data Sheet



48LQFP

7 x 7 x 1.4 mm, 0.5 mm

64LQFP

10 x 10 x 1.4 mm, 0.5 mm

100LQFP

14 x 14 x 1.4 mm, 0.5 mm

144LQFP

20 x 20 x 1.4 mm, 0.5 mm

Features

Operating characteristics

- Voltage range: 2.7 V to 5.5 V
- Ambient temperature range: -40 °C to 105 °C for HSRUN mode, -40 °C to 125 °C for RUN mode

Arm™ Cortex-M4F 32-bit CPU

- Supports up to 112 MHz frequency (HSRUN mode) with 1.25 Dhrystone MIPS per MHz
- Arm Core based on the Armv7 Architecture and Thumb®-2 ISA
- Integrated Digital Signal Processor (DSP)
- Configurable Nested Vectored Interrupt Controller (NVIC)
- Single Precision Floating Point Unit (FPU)

Clock interfaces

- 4 - 40 MHz fast external oscillator (SOSC) with up to 50 MHz DC external square input clock in external clock mode
- 48 MHz Fast Internal RC oscillator (FIRC)
- 8 MHz Slow Internal RC oscillator (SIRC)
- 128 kHz Low Power Oscillator (LPO)
- Up to 112 MHz (HSRUN) System Phased Lock Loop (SPLL))
- Up to 20 MHz TCLK and 25 MHz SWD_CLK
- 32 kHz Real Time Counter external clock (RTC_CLKIN)

Power management

- Low-power Arm Cortex-M4F with excellent energy efficiency
- Power Management Controller (PMC) with multiple power modes: HSRUN, RUN, STOP, VLPR, and VLPS
- Clock gating and low power operation supported on specific peripherals.

Memory and memory interfaces

- Up to 2 MB program flash memory with ECC
- 64 KB FlexNVM for data flash memory with ECC and EEPROM emulation
- Up to 256 KB SRAM with ECC
- Up to 4 KB of FlexRAM for use as SRAM or EEPROM emulation
- Up to 4 KB Code cache to minimize performance impact of memory access latencies
- QuadSPI with HyperBus™ support

Mixed-signal analog

- Up to two 12-bit Analog-to-Digital Converter (ADC) with up to 32 channel analog inputs per module

- One Analog Comparator (CMP) with internal 8-bit Digital to Analog Converter (DAC)

Debug functionality

- Serial Wire JTAG Debug Port (SWJ-DP) combines
- Debug Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Test Port Interface Unit (TPIU)
- Flash Patch and Breakpoint (FPB) Unit

Human-Machine Interface (HMI)

- Up to 128 GPIO pins with interrupt functionality
- Non-Maskable Interrupt (NMI)

Communications interfaces

- Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART/LIN) modules with DMA support and low power availability
- Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
- Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
- Up to three FlexCAN modules (with optional CAN- FD support)
- FlexIO module for emulation of communication protocols and peripherals (UART, I2C, SPI, I2S, LIN, PWM, etc).
- Up to one 10/100Mbps Ethernet with IEEE1588 support and two Synchronous Audio Interface (SAI) modules

Safety

- IEC61508: ready for system SIL2 using Safe Assure™ documentation and SW libraries
- IEC60730: Class B certified
- Error-Correcting Code (ECC) on flash and SRAM memories
- System Memory Protection Unit (System MPU)
- Cyclic Redundancy Check (CRC) module
- Internal watchdog (WDOG)
- External Watchdog monitor (EWM) module

Security

- Accelerator (CSEC) implements a comprehensive set of cryptographic functions as described in the SHE (Secure Hardware Extension) Functional Specification.
- 128-bit Unique Identification (ID) number

Timing and control

- Up to eight independent 16-bit FlexTimers (FTM) modules, offering up to 64 standard channels (IC/OC/PWM)
- One 16-bit Low Power Timer (LPTMR) with flexible wake up control
- Two Programmable Delay Blocks (PDB) with flexible trigger system
- One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
- 32-bit Real Time Counter (RTC)

Package

- 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, 144-pin LQFP package options

DMA

- 16 channel DMA with up to 63 request sources using DMAMUX

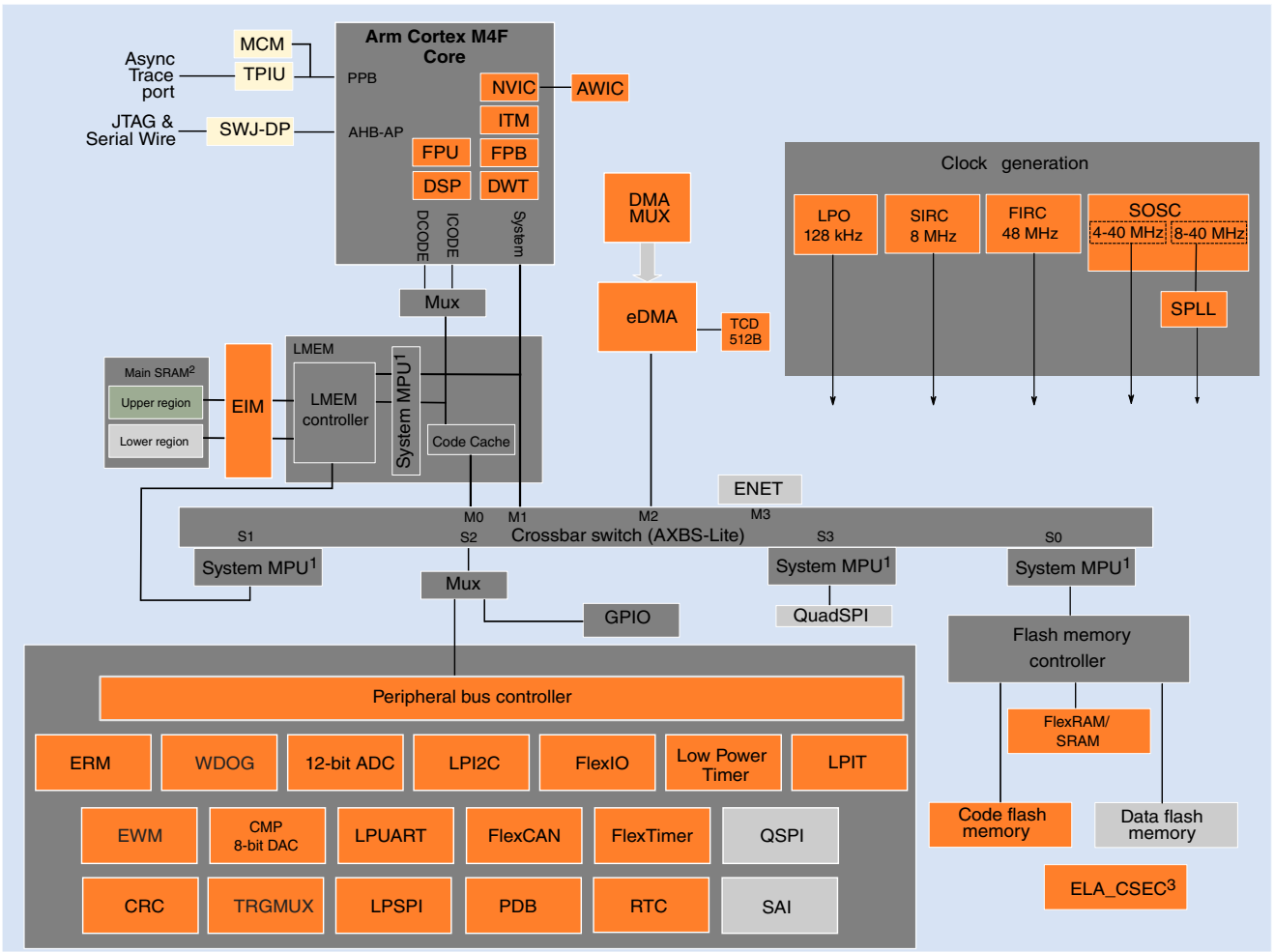
Notes

- EdgeLock Accelerator (CSEC) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute EdgeLock Accelerator (CSEC) or EEPROM writes/erase.
- The following two attachments are available with the Datasheet:
  - MCXE24x_Orderable_Part_Number_ List.xlsx
  - MCXE24x_Power_Modes_Configuration.xlsx

Table of Contents

1 Block diagram

Following figure shows superset high level architecture block diagram of MCXE24x series respectively. Other devices within the family have a subset of the features. See Feature comparison for chip specific values.



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Each Crossbar master (Core, DMA, Ethernet) can be assigned different access rights to each protected memory region. The Arm M4 core version in this family does not integrate the Arm Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the table 1 :MCXE24x product series comparison

3: EdgeLock Accelerator (CSEC) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device need to switch to RUN mode (80 MHz) to execute EdgeLock Accelerator (CSEC) or EEPROM writes/erase.

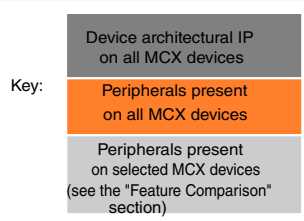


Figure 1. High-level architecture diagram for the MCXE24x family

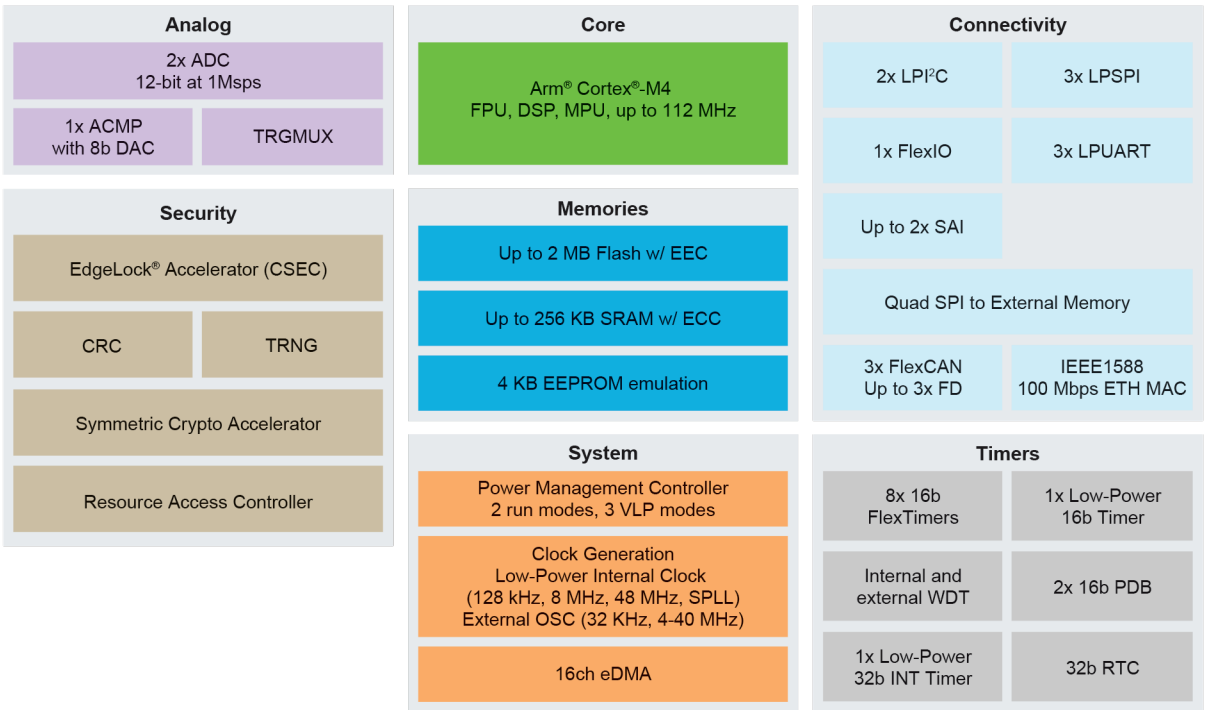


Figure 2. MCX E24x Series - Block diagram

2 Feature comparison

The following figure summarizes the memory, peripherals and packaging options for the MCXE24x devices. All devices which share a common package are pin-to-pin compatible.

NOTE

Availability of peripherals depends on the pin availability in a particular package. For more information see *IO Signal Description Input Multiplexing sheet(s)* attached with Reference Manual.

Table 1. MCXE24x product series comparison

	Feature	MCXE245	MCXE246	MCXE247
Compute	Core	Arm® Cortex™-M4F		
	Frequency	80 MHz (RUN mode) or 112 MHz (HSRUN mode) [1]		
	DMIPS	Up to 140 DMIPS		
	IEC 61508	QM (Safe Assure)		
	IEEE-754 FPU	●		
	Cache	4 KB		

Table continues on the next page...

Table 1. MCXE24x product series comparison (continued)

	Low power modes	●		
	HSRUN mode	●		
	DMA	●		
Memory	Flash	512 KB	1 MB	2 MB [2]
	Error Correcting Code (ECC)	●		
	System RAM (including FlexRAM and MTB)	64 KB	128 KB	256 KB
	FlexRAM (also available as system RAM)	4 KB		
	EEPROM emulated by FlexRAM	4 KB (up to 64 KB D-Flash)		3
	External memory interface	4		QuadSPI incl. HyperBus™
Analog	12-bit SAR ADC (1 Msps each)	2x (16)	2x (24)	2x (32)
	Comparator with 8-bit DAC	1x		
Digital	Peripheral speed	up to 112 MHz (HSRUN)		
	10/100 Mbps IEEE-1588 Ethernet MAC	-	-	1x
	Serial Audio Interface (AC97, TDM, I2S)	-	-	2x
	Low Power UART/LIN (LPUART) (Supports LIN protocol versions 1.3, 2.0, 2.1, 2.2A, and SAE J2602)	3x		
	Low Power SPI (LPSPI)	3x		
	Low Power I2C (LPI2C)	1x		2x
	FlexCAN (CAN-FD IEC/CD 11898-1)	3x (1x with FD)	3x (2x with FD)	3x (3x with FD)
	FlexIO (8 pins configurable as UART, SPI, I2C, I2S)	1x		
Security	EdgeLock Accelerator (CSEC)	●		
Safety	Crossbar	●		
	External Watchdog Monitor (EWM)	●		
	Memory Protection Unit (MPU)	●		
	CRC module	1x		
	Watchdog	1x		
Timers	Low Power Interrupt Timer (LPIT)	1x		
	FlexTimer (16-bit counter) 8 channels	4x (32)	6x (48)	8x (64)
	Low Power Timer (LPTMR)	1x		
	Real Time Counter (RTC)	1x		
Motor Control	Programmable Delay Block (PDB)	2x		
	Trigger mux (TRGMUX)	1x (64)	1x (73)	1x (81)
Debug	Debug & trace	SWD, JTAG (ITM, SWV, SWO)		SWD, JTAG (ITM, SWV, SWO), ETM
General	Number of I/Os	up to 89	up to 128	up to 128
	Single supply voltage	2.7 - 5.5 V		
	Ambient Operation Temperature (Ta)	-40°C to +125°C(RUN mode), -40°C to +105°C(HSRUN mode)		

Table continues on the next page...

Table 1. MCXE24x product series comparison (continued)

	Packages[5]	48-pin LQFP, 64-pin LQFP, 100-pin LQFP	64-pin LQFP, 100-pin LQFP, 144-pin LQFP	100-pin LQFP[6], 144-pin LQFP
	Ecosystem (IDE, compiler, debugger)	NXP MCUXpresso, IAR, MDK		

1. No write or erase access to Flash module, including Security (EdgeLock Accelerator) and EEPROM commands, are allowed when device is running at HSRUN mode (112MHz) or VLPR mode.
2. Available when EEEPROM, EdgeLock Accelerator and Data Flash are not used. Else only up to 1,984 kB is available for Program Flash.
3. 4 KB (up to 512 KB D-Flash as a part of 2 MB Flash). Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash. See chapter FTFC for details.
4. Not implemented
5. See Dimensions section for package drawings
6. QuadSPI is only supported on 144-pin LQFP

3 Ordering information

3.1 Selecting orderable part number

Not all part number combinations are available. See the attachment *MCXE24x_Orderable_Part_Number_ List.xlsx* attached with the Datasheet for a list of standard orderable part numbers.

3.2 Ordering information

Part Number[1]	Embedded Memory		Core Frequency	CAN FD	Security	FlexTimer	Ethernet	GPIOs	Pacakge
	Flash Size	RAM Size							
MCXE245VLF MCXE245VLFR	512 KB	64 KB	112 MHz	3x (1x with FD)	ELA_CSEC[2]	4x	-	43	LQFP48
MCXE245VLH MCXE245VLHR			112 MHz	3x (1x with FD)	ELA_CSEC	4x	-	58	LQFP64
MCXE245VLL MCXE245VLLR			112 MHz	3x (1x with FD)	ELA_CSEC	4x	-	89	LQFP100
MCXE246VLH MCXE246VLHR	1 MB	128 KB	112 MHz	3x (2x with FD)	ELA_CSEC	6x	-	58	LQFP64
MCXE246VLL MCXE246VLLR			112 MHz	3x (2x with FD)	ELA_CSEC	6x	-	89	LQFP100

Table continues on the next page...

Part Number[1]	Embedded Memory		Core Frequency	CAN FD	Security	FlexTimer	Ethernet	GPIOs	Pacakge
	Flash Size	RAM Size							
MCXE246VLQ MCXE246VLQR			112 MHz	3x (2x with FD)	ELA_CSEC	6x	-	128	LQFP144
MCXE247VLL MCXE247VLLR	2 MB	256 KB	112 MHz	3x (3x with FD)	ELA_CSEC	8x	1x	89	LQFP100
MCXE247VLQ MCXE247VLQR			112 MHz	3x (3x with FD)	ELA_CSEC	8x	1x	128	LQFP144

1. To confirm current availability of orderable part numbers, go to http://www.nxp.com and perform a part number search or contact NXP sales, distributor, e-tailer.
2. ELA_CESC is EdgeLock Accelerator (CSEC)

4 General

4.1 Absolute maximum ratings

NOTE

- Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in the following table for specific conditions.
- Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.
- All the limits defined in the datasheet specification must be honored together and any violation to any one or more will not guarantee desired operation.
- Unless otherwise specified, all maximum and minimum values in the datasheet are across process, voltage, and temperature.

Table 2. Absolute maximum ratings for MCXE24x series

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{DD}[2]	2.7 V - 5. 5V input supply voltage	—	-0.3	5.8 [3]	V
V_{REFH}	3.3 V / 5.0 V ADC high reference voltage	—	-0.3	5.8 [3]	V
$I_{INJPAD\_DC\_ABS}$[4]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	—	-3	+3	mA

Table continues on the next page...

Table 2. Absolute maximum ratings for MCXE24x series (continued)

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{IN_DC}	Continuous DC Voltage on any I/O pin with respect to V_{SS}	—	-0.8	5.8[5]	V
$I_{INJSUM\_DC\_ABS}$	Sum of absolute value of injected currents on all the pins (Continuous DC limit)	—	—	30	mA
T_{ramp}[6]	ECU supply ramp rate	—	0.5 V/min	500 V/ms	—
T_{ramp_MCU}[7]	MCU supply ramp rate	—	0.5 V/min	100 V/ms	—
T_A[8]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	-55	165	°C
$V_{IN\_TRANSIENT}$	Transient overshoot voltage allowed on I/O pin beyond $V_{IN\_DC\ limit}$	—	—	6.8 [9]	V

1. All voltages are referred to V_{SS} unless otherwise specified.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. 60 seconds lifetime – No restrictions i.e. the part is not held in reset and can switch.

   10 hours lifetime – The part is held in reset by an external circuit i.e. the part cannot switch.

   The supply should be kept in operating conditions and once out of operating conditions, the device should be either reset or powered off.

   Operation with supply between 5.5 V and 5.8 V not in reset condition is allowed for 60 seconds cumulative over lifetime, the part will operate with reduced functionality.

   Operation with supply between 5.5 V and 5.8 V but held in reset condition by external circuit is allowed for 10 hours cumulative over lifetime.

   If the given time limits or supply levels are exceeded, the device may get damaged.
4. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.
5. While respecting the maximum current injection limit
6. This is the Electronic Control Unit (ECU) supply ramp rate and not directly the MCU ramp rate. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
7. This is the MCU supply ramp rate and the ramp rate assumes that the MCXE24x HW design guidelines are followed. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
8. T_J (Junction temperature)=125 °C. Assumes T_A=125 °C for RUN mode

   T_J (Junction temperature)=125 °C. Assumes T_A=105 °C for HSRUN mode

   - Assumes maximum θJA for 2s2p board. See Thermal characteristics
9. 60 seconds lifetime; device in reset (no outputs enabled/toggling)

4.2 Voltage and current operating requirements

NOTE

Device functionality is guaranteed up to the LVR assert level, however electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics would be degraded when voltage drops below 2.7 V

Table 3. Voltage and current operating requirements for MCXE24x series 1

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}[2]	Supply voltage	2.7 [3]	5.5	V	4
V_{DD_OFF}	Voltage allowed to be developed on V_{DD} pin when it is not powered from any external power supply source.	0	0.1	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	4
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	4
V_{REFH}	ADC reference voltage high	2.7	V_{DDA} + 0.1	V	5
V_{REFL}	ADC reference voltage low	-0.1	0.1	V	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	6
$I_{INJPAD\_DC\_OP}$[7]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-3	+3	mA	
$I_{INJSUM\_DC\_OP}$	Continuous total DC input current that can be injected across all I/O pins such that there's no degradation in accuracy of analog modules: ADC and ACMP (See section Analog Modules)	—	30	mA	

1. Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V, temperature = 25 °C and typical silicon process unless otherwise stated.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. MCXE247 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged MCXE247 is guaranteed to operate from 2.97 V. All other MCXE24 family devices operate from 2.7 V in all modes.
4. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.
5. V_{REFH} should always be equal to or less than V_{DDA} + 0.1 V and V_{DD} + 0.1 V
6. Open drain outputs must be pulled to V_{DD}.
7. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.

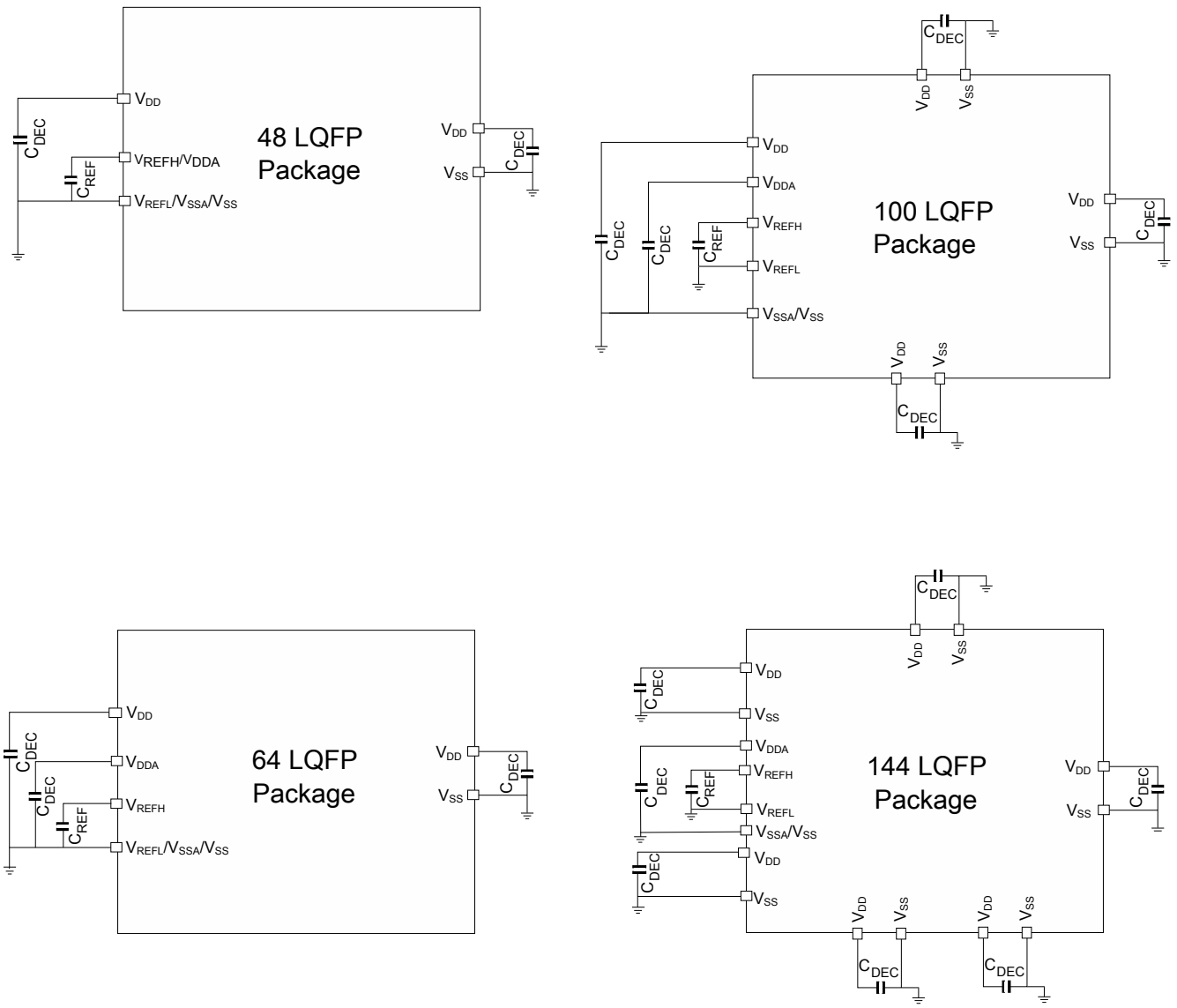
4.3 Thermal operating characteristics

Table 4. Thermal operating characteristics for MCXE24x series

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ V\text{-}Grade\ Part}$[1,2]	Ambient temperature under bias	–40	—	125	°C
$T_{J\ V\text{-}Grade\ Part}$[3,4]	Junction temperature under bias	–40	—	125	°C

1. The device may operate at maximum T_A rating as long as T_J maximum of 125 °C is not exceeded. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA}$ * chip power dissipation.
2. T_a = 125 °C is for RUN mode only.
3. The device operating specification is not guaranteed beyond 125 °C T_J.
4. The maximum operating requirement applies to all chapters unless otherwise specifically stated.

4.4 Power and ground pins



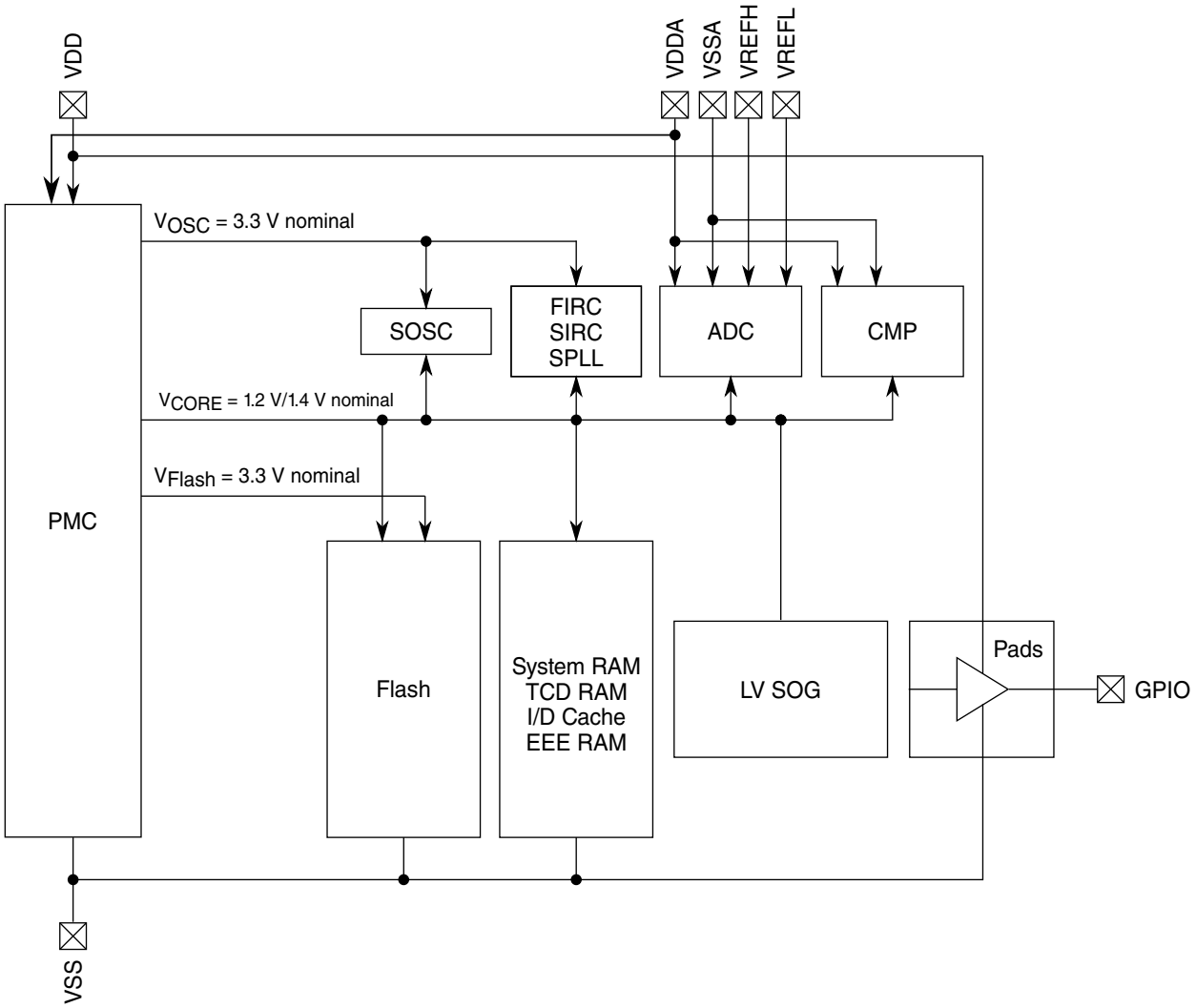
NOTE: V_{DD} and V_{DDA} must be shorted to a common source on PCB

Figure 3. Pinout decoupling

Table 5. Supplies decoupling capacitors 1, 2

Symbol	Description	Min. 3	Typ.	Max.	Unit
C_{REF}, 4, 5	ADC reference high decoupling capacitance	70	100	—	nF
C_{DEC} 5, 6, 7	Recommended decoupling capacitance	70	100	—	nF

1. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC. All V_{SS} pins should be connected to common ground at the PCB level.
2. All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
3. Minimum recommendation is after considering component aging and tolerance.
4. For improved performance, it is recommended to use 10 µF, 0.1 µF and 1 nF capacitors in parallel.
5. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
6. Contact your local Field Applications Engineer for details on best analog routing practices.
7. The filtering used for decoupling the device supplies must comply with the following best practices rules:
    - The protection/decoupling capacitors must be on the path of the trace connected to that component.
    - No trace exceeding 1 mm from the protection to the trace or to the ground.
    - The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
    - The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.



*Note: VSSA and VSS are shorted at package level

Figure 4. Power diagram

4.5 LVR, LVD and POR operating requirements

Table 6. V_{DD} supply LVR, LVD and POR operating requirements for MCXE24x series[1]

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVR}	LVR falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V_{LVR_HYST}	LVR hysteresis	—	45	—	mV	2
V_{LVR_LP}	LVR falling threshold (VLPS/VLPR modes)	1.97	2.22	2.44	V	
V_{LVD}	Falling low-voltage detect threshold	2.8	2.875	3	V	
V_{LVD_HYST}	LVD hysteresis	—	50	—	mV	2

Table continues on the next page...

Table 6. V_{DD} supply LVR, LVD and POR operating requirements for MCXE24x series[1] (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW}	Falling low-voltage warning threshold	4.19	4.305	4.5	V	
V_{LVW_HYST}	LVW hysteresis	—	75	—	mV	2
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	

1. In 3.3 V range, the VLVW is always set since supply remains below VLVW range. Hence PMC.LVDSC2[LVWIE] should remain cleared while device operates in 3.3 V range.
2. Rising threshold is the sum of falling threshold and hysteresis voltage.

4.6 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

Table 7. Clock configuration

RUN mode	
Clock source	FIRC
SYS_CLK/CORE_CLK	48 MHz
BUS_CLK	48 MHz
FLASH_CLK	24 MHz
HRUN mode	
Clock source	SPLL
SYS_CLK/CORE_CLK	112 MHz
BUS_CLK	56 MHz
FLASH_CLK	28 MHz
VLPR mode	
Clock source	SIRC
SYS_CLK/CORE_CLK	4 MHz
BUS_CLK	4 MHz
FLASH_CLK	1 MHz
STOP1/STOP2 mode	
Clock source	FIRC
SYS_CLK/CORE_CLK	48 MHz
BUS_CLK	48 MHz
FLASH_CLK	24 MHz
VLPS mode	
	All clock source disabled (FIRC/SOSC/SPLL)

Table 8. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 2.7 V to execution of the first instruction across the operating temperature range of the chip.	—	325	—	µs
	VLPS → RUN	8	—	17	µs
	STOP1 → RUN	0.07	0.075	0.08	µs
	STOP2 → RUN	0.07	0.075	0.08	µs
	VLPR → RUN	19	—	26	µs
	VLPR → VLPS	5.1	5.7	6.5	µs
	VLPS → VLPR	18.8	23	27.75	µs
	RUN → Compute operation	0.72	0.75	0.77	µs
	HSRUN → Compute operation	0.3	0.31	0.35	µs
	RUN → STOP1	0.35	0.38	0.4	µs
	RUN → STOP2	0.2	0.23	0.25	µs
	RUN → VLPS	0.3	0.35	0.4	µs
	RUN → VLPR	3.5	3.8	5	µs
	VLPS → Asynchronous DMA Wakeup	105	110	125	µs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	Pin reset → Code execution	—	214	—	µs

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations. Attached *MCXE24x_Power_Modes _Configuration.xlsx* details the modes used in gathering the power consumption data stated in the following table Table 9. For full functionality refer to table: Module operation in available power modes of the *Reference Manual*.

Table 9. Power consumption (Typicals unless stated otherwise) [1]

Chip/Device	Ambient Temperature (°C)		VLPS (µA) [2]		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [3]		IDD/MHz (µA/MHz) [4]
			Peripherals disabled [5]	LPTMR enabled	Peripherals disabled [6]	Peripherals enabled use case 1[6]	Peripherals enabled use case 2[7]			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
MCXE245	25	Typ	29.8	42	1.48	1.50	2.91	7	7.7	19.7	26.9	25.1	33.3	30.2	39.6	43.3	55.6	378
	85	Typ	150	159	1.72	1.85	3.08	7.2	8.1	20.4	27.1	26.1	33.5	30.5	40	43.9	56.1	381
		Max	359	384	2.60	2.65	NA	9.2	9.9	23.2	29.6	29.3	36.2	34.8	42.1	46.3	59.7	435
	105	Typ	256	273	1.80	2.10	3.23	7.8	8.5	20.6	27.4	26.6	33.8	31.2	40.5	44.8	57.1	390
		Max	850	900	2.65	2.70	NA	10.3	11.1	23.9	30.6	30.3	37.3	35.6	43.5	47.9	61.3	445
	125	Typ	NA	NA	NA	NA	3.65	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	1960	1998	3.18	3.25	NA	12.9	13.8	26.9	33.6	35	40.3	38.7	46.8	NA		484
MCXE246	25	Typ	37	47	1.57	1.61	3.3	8	9.2	23.4	31.4	30.5	40.2	36.2	47.6	52	68.3	452
	85	Typ	207	209	1.79	1.83	3.54	8.9	10.1	24.4	32.4	31.5	41.3	37.2	48.7	53.3	69.8	465
		Max	974	981	3.32	3.38	NA	12.7	13.9	29.3	37.9	36.7	47	42.4	54.4	60.3	78	530
	105	Typ	419	422	1.99	2.04	3.78	9.8	11	25.3	33.4	32.5	42.2	38.1	49.6	54.4	70.8	477
		Max	2004	2017	4.06	4.13	NA	17.1	18.3	34.1	42.6	41.3	51.4	46.9	58.8	65.7	82.8	587
	125	Typ	NA	NA	NA	NA	4.44	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	3358	3380	5.28	5.38	NA	22.6	23.7	40.2	48.8	47.3	57.4	52.8	64.8	NA		660
MCXE247[8]	25	Typ	38	54	2.17	2.20	3.45	8.5	9.6	27.6	34.9	35.5	45.3	42.1	57.7	60.3	83.3	526
	85	Typ	336	357	2.30	2.35	3.74	10.1	11.1	29.1	37.0	36.8	46.6	43.4	59.9	62.9	88.7	543
		Max	1660	1736	3.48	3.55	NA	14.5	15.6	34.8	43.6	41.9	53.9	48.7	65.1	70.4	96.1	609

Table continues on the next page...

Table 9. Power consumption (Typicals unless stated otherwise) 1 (continued)

Chip/Device	Ambient Temperature (°C)		VLPS (µA) [2]		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [3]		IDD/MHz (µA/MHz) [4]
			Peripherals disabled [5]	LPTMR enabled	Peripherals disabled [6]	Peripherals enabled use case 1 [6]	Peripherals enabled use case 2 [7]			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
	105	Typ	560	577	2.49	2.54	4.03	10.9	11.9	29.8	37.8	37.6	47.5	45.2	61.5	63.8	89.1	565
		Max	2945	2970	4.40	4.47	NA	18.0	19.0	38.4	46.8	44.9	55.3	51.6	66.8	73.6	97.4	645
	125	Typ	NA	NA	NA	NA	4.85	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	3990	4166	6.00	6.08	NA	23.4	24.5	44.3	52.5	50.9	61.3	57.5	71.6	NA		719

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V, temperature = 25 °C and typical silicon process unless otherwise stated. All output pins are floating and On-chip pulldown is enabled for all unused input pins.
2. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
3. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.
4. Values mentioned for MCXE24x devices are measured at RUN@80 MHz with peripherals disabled.
5. With PMC_REGSC[CLKBIASDIS] set to 1. See Reference Manual for details.
6. Data collected using RAM
7. Numbers on limited samples size and data collected with Flash
8. The **MCXE247** data points assume that ENET/QuadSPI/SAI etc. are inactive.

Table 10. VLPS additional use-case power consumption at typical conditions 1, 2, 3

Use-case	Description	Temp.	Device			Unit
			MCXE245	MCXE246	MCXE247	
VLPS and RTC	• Clock source: LPO or RTC_CLKIN	25	31	38	40	µA
		85	170	227	356	µA
		105	290	460	600	µA
		125	680	810	1250	µA
VLPS and LPUART TX/RX	• Clock source: SIRC • Transmiting or receiving continuously using DMA • Baudrate: 19.2 kbps	25	230	250	250	µA
		85	400	410	490	µA
		105	550	600	850	µA
		125	1070	1250	1960	µA
VLPS and LPUART wake-up	• Clock source: SIRC • Wake-up address feature enabled • Baudrate: 19.2 kbps	25	138	146	146	µA
		85	240	280	350	µA
		105	400	480	600	µA
		125	580	1000	1280	µA
VLPS and LPI2C master	• Clock Source: SIRC • Transmit/receive using DMA • Baudrate: 100 kHz	25	690	820	900	µA
		85	960	1220	1370	µA
		105	1250	1660	2060	µA
		125	1980	2860	3690	µA
VLPS and LPI2C slave wake-up	• Clock source: SIRC • Wake-up address feature enabled • Baudrate: 100 kHz	25	260	270	280	µA
		85	340	410	510	µA
		105	430	610	810	µA
		125	760	1170	1540	µA
VLPS and LPSPI master [4]	• Clock source: SIRC • Transmit/receive using DMA • Baudrate: 500 kHz	25	3.19	3.75	4.11	mA
		85	3.7	4.35	4.93	mA
		105	4.2	4.93	5.74	mA
		125	4.63	5.97	7.38	mA
VLPS and LPIT	• Clock source: SIRC • 1 channel enable • Mode: 32-bit periodic counter	25	114	120	130	µA
		85	250	260	320	µA
		105	410	440	570	µA
		125	750	910	1280	µA

1. All power numbers listed in this table are typical power numbers
2. Current numbers are quoted for a certain application code and may vary on user configuration and silicon process variation.
3. The power numbers are not strictly for the VLPS mode operation alone, but also includes power due to periodic wakeup. The power therefore includes wakeup plus VLPS mode activity. This leads to greater dependence of power numbers on application code.
4. The single LPSPI used is LPSPI1 in MCXE24x devices.

The following table shows the power consumption targets for **MCXE247** in various mode of operations measure at 3.3 V.

Table 11. Power consumption at 3.3 V

Chip/Device	Ambient Temperature (°C)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA)[1]	
			Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI	Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI
MCXE247	25	Typ	67.3	79.1	89.8	105.5
	85	Typ	67.4	79.2	95.6	105.9
		Max	82.5	88.2	109.7	117.4
	105	Typ	68.0	79.8	96.6	106.7
		Max	80.3	89.1	109.0	119.0
	125	Max	83.5	94.7	NA	

1. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.

4.8 ESD and latch-up protection characteristics

Symbol	Description	Min.	Max.	Unit
V_{HBM}	Electrostatic discharge voltage, human body model[1], [2],	– 4000	4000	V
V_{CDM}	Electrostatic discharge voltage, charged-device model[1], [3]			
	All pins except the corner pins	– 500	500	V
	Corner pins only	– 750	750	V
I_{LAT}	Latch-up current at ambient temperature of 125 °C[4]	– 100	100	mA

1. Device failure is defined as: "If after exposure to ESD pulses, the device does not meet specification requirements."
2. This parameter is tested in conformity with JEDEC-JS-001.
3. This parameter is tested in conformity with JEDEC-JS-002
4. This parameter is tested in conformity with JEDEC-JESD78.

4.9 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

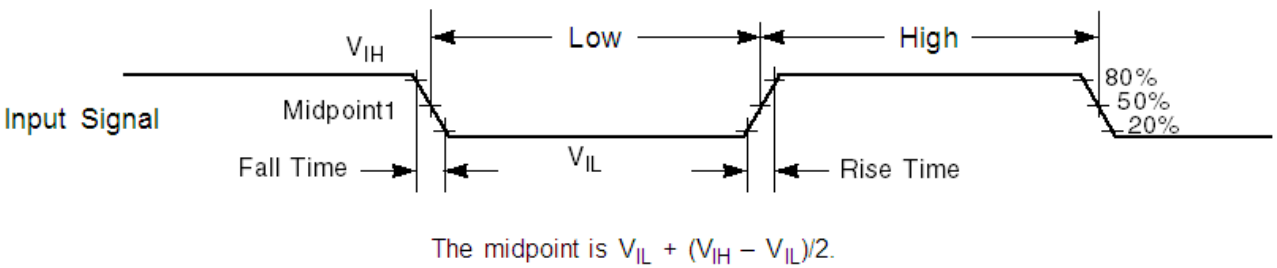


Figure 5. Input signal measurement reference

5.2 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 12. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	3
WFRST	$\overline{\text{RESET}}$ input filtered pulse	—	10	ns	4
WNFRST	$\overline{\text{RESET}}$ input not filtered pulse	Maximum of (100 ns, bus clock period)	—	ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. Maximum length of $\overline{\text{RESET}}$ pulse which will be the filtered by internal filter only if PCR_PTA5[PFE] is at its reset value of 1'b1.
5. Minimum length of $\overline{\text{RESET}}$ pulse, guaranteed not to be filtered by the internal filter only if PCR_PTA5[PFE] is at its reset value of 1'b1. This number depends on the bus clock period also. In this case, minimum pulse width which will cause reset is 250 ns. For faster clock frequencies which have clock period less than 100 ns, the minimum pulse width not filtered will

be 100 ns. After this filtering mechanism, the software has an option to put additional filtering in addition to this, by means of PCM_RPC register and/or PORT_DFER register for PTA5.

5.3 DC electrical specifications at 3.3 V Range

NOTE

For details on the pad types defined in Table 13 and Table 14, see Reference Manual section *IO Signal Table* and IO Signal Description Input Multiplexing sheet(s) attached with Reference Manual.

Table 13. DC electrical specifications at 3.3 V Range for MCXE24x series

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	2.7	3.3	4	V	1
V_{ih}	Input Buffer High Voltage	0.7 × V_{DD}	—	V_{DD} + 0.3	V	2
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.3 × V_{DD}	V	3
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh} = (V_{DD} – 0.8 V)	3.5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	3	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = (V_{DD} – 0.8 V)	14	—	—	mA	4
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	12	—	—	mA	4
$Ioh_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{oh}=V_{DD}-0.8 V	9.5	—	—	mA	5
$Iol_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	10	—	—	mA	5
$Ioh_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{oh}=V_{DD}-0.8 V	16	—	—	mA	5
$Iol_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	15.5	—	—	mA	5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 3.3 V		5	500[6]	µA	7
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins [8]		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		60	kΩ	9
R_{PD}	Internal pulldown resistors	20		60	kΩ	10

1. MCXE247 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged MCXE247 is guaranteed to operate from 2.97 V. All other MCXE24x family devices operate from 2.7 V in all modes.
2. For reset pads, same V_{ih} levels are applicable

3. For reset pads, same V_{il} levels are applicable
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
5. For refernce only. Run simulations with the IBIS model and custom board for accurate results.
6. Typical leakage is given at room temperature. Maximum is given for 125°C. Leakage numbers increase with temperature, approximately every 12 – 14°C the value doubles. Leakage is tested at hot temperature. We ensure maximums are not exceeded. Please note that when the ADC module samples a pin, additional currents beyond the leakage number are drawn to charge the sample and hold capacitances and internal analog busses. These are difficult to predict
7. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details see IO Signal Description Input Multiplexing sheet(s) attached with the *Reference Manual*.
8. When using ENET and SAI on MCXE247, the overall device limits associated with high drive pin configurations must be respected i.e. On 144-pin LQFP the general purpose pins: PTA10, PTD0, and PTE4 must be set to low drive.
9. Measured at input V = V_{SS}
10. Measured at input V = V_{DD}

5.4 DC electrical specifications at 5.0 V Range

Table 14. DC electrical specifications at 5.0 V Range for MCXE24x series

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	0.65 x V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.35 x V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 x V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh}= (V_{DD} - 0.8 V)	5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	5	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = V_{DD} - 0.8 V	20	—	—	mA	3
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	20	—	—	mA	3
$Ioh_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{oh} = V_{DD} - 0.8 V	14.0	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	14.5	—	—	mA	4
$Ioh_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{oh} = V_{DD} - 0.8 V	21	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	20.5	—	—	mA	4
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 3.3 V		5	500[5]	µA	6
	All pins other than high drive port pins		0.005	0.5	µA	

Table continues on the next page...

Table 14. DC electrical specifications at 5.0 V Range for MCXE24x series (continued)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
	High drive port pins (excluding XTAL pin)		0.010	0.5	µA	
XTAL pin (PTB6) temperature ≤ 125° C		0.010	0.5	µA		
XTAL pin (PTB6) temperature ≥ 125° C			1.1	µA		
R_{PU}	Internal pullup resistors	20		50	kΩ	7
R_{PD}	Internal pulldown resistors	20		50	kΩ	8

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The strong pad I/O pin is capable of switching a 50 pF load up to 40 MHz.
4. For refernce only. Run simulations with the IBIS model and custom board for accurate results.
5. Typical leakage is given at room temperature. Maximum is given for 125°C. Leakage numbers increase with temperature, approximately every 12 – 14°C the value doubles. Leakage is tested at hot temperature. We ensure maximums are not exceeded. Please note that when the ADC module samples a pin, additional currents beyond the leakage number are drawn to charge the sample and hold capacitances and internal analog busses. These are difficult to predict
6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details see IO Signal Description Input Multiplexing sheet(s) attached with the *Reference Manual*.
7. Measured at input V = V_{SS}
8. Measured at input V = V_{DD}

5.5 AC electrical specifications at 3.3 V range

Table 15. AC electrical specifications at 3.3 V Range for MCXE24x series

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
tRF_{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
$tRF_{GPIO-HD}$	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200
$tRF_{GPIO-FAST}$	0	0.6	2.8	0.5	2.8	25
		3.0	7.1	2.6	7.5	50
		12.0	27.0	10.3	26.8	200
	1	0.4	1.3	0.38	1.3	25

Table continues on the next page...

Table 15. AC electrical specifications at 3.3 V Range for MCXE24x series (continued)

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
		1.5	3.8	1.4	3.9	50
		7.4	14.9	7.0	15.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 16. AC electrical specifications at 5 V Range for MCXE24x series

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
tRF_{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
$tRF_{GPIO-HD}$	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
	1	1.1	4.6	1.1	5.0	25
		2.0	5.7	2.0	5.8	50
		5.4	16.0	5.0	16.0	200
$tRF_{GPIO-FAST}$	0	0.42	2.2	0.37	2.2	25
		2.0	5.0	1.9	5.2	50
		9.3	18.8	8.5	19.3	200
	1	0.37	0.9	0.35	0.9	25
		1.2	2.7	1.2	2.9	50
		6.0	11.8	6.0	12.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.7 Standard input pin capacitance

Table 17. Standard input pin capacitance

Symbol	Description	Min.	Max.	Unit
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External System Oscillator electrical specifications for EXTAL/XTAL pins.

5.8 Device clock specifications

Table 18. Device clock specifications 1

Symbol	Description	Min.	Max.	Unit
High Speed run mode[2]				
f_{SYS}	System and core clock	—	112	MHz
f_{BUS}	Bus clock	—	56	MHz
f_{FLASH}	Flash clock	—	28	MHz
Normal run mode (MCXE24x series) [3]				
f_{SYS}	System and core clock	—	80	MHz
f_{BUS}	Bus clock	—	40[4]	MHz
f_{FLASH}	Flash clock	—	26.67	MHz
VLPR mode (MCXE24x series)[5]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	4	MHz
f_{FLASH}	Flash clock	—	1	MHz

1. Refer to the section Feature comparison for the availability of modes and other specifications.
2. Only available on some devices. See section Feature comparison.
3. With SPLL as system clock source.
4. 48 MHz when f_{SYS} is 48 MHz
5. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

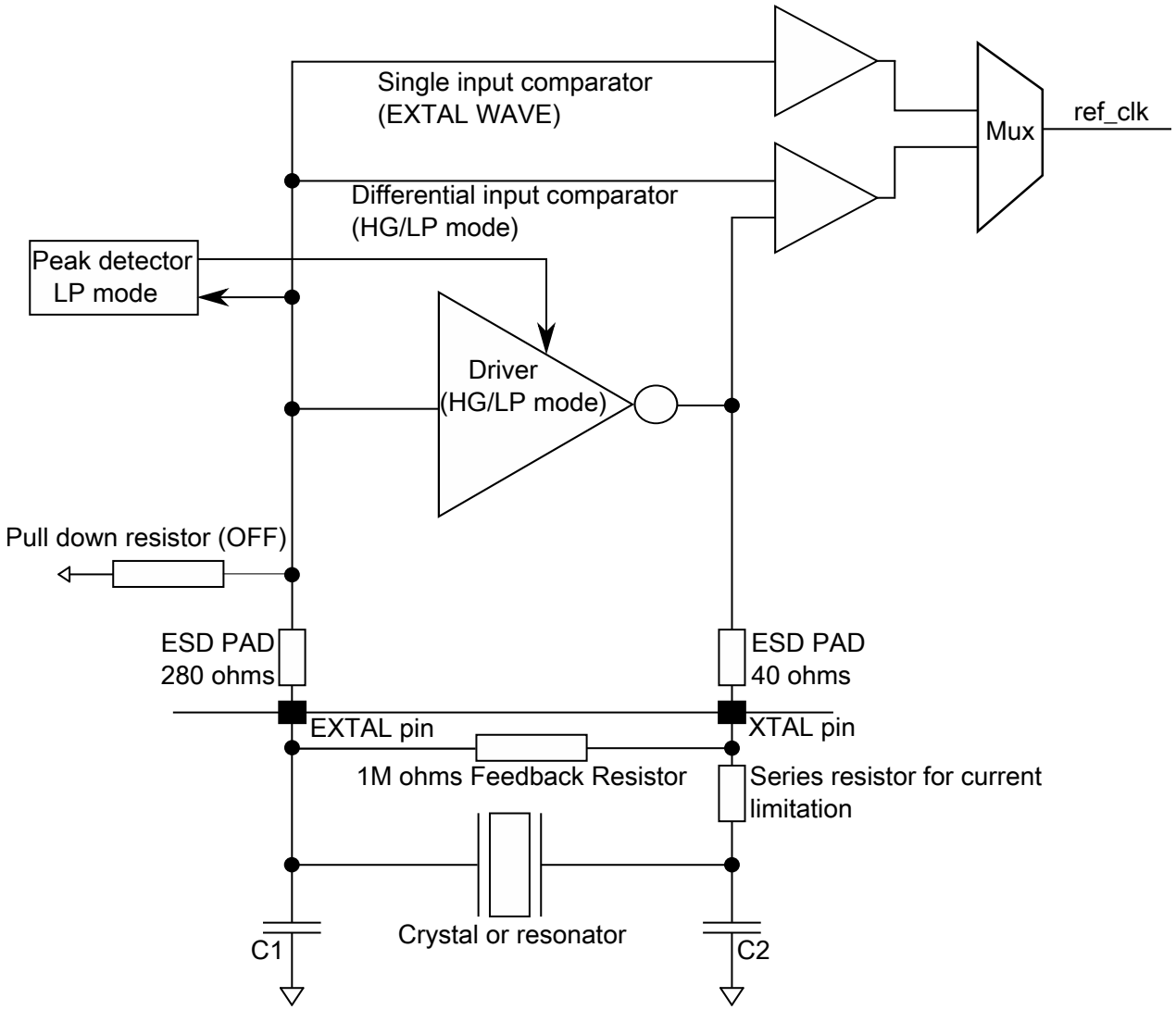


Figure 6. Oscillator connections scheme

Table 19. External System Oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
g_{mXOSC}	Crystal oscillator transconductance					
	SCG_SOSCCFG[RANGE]=2'b10 for 4-8 MHz	2.2	—	13.7	mA/V	
	SCG_SOSCCFG[RANGE]=2'b11 for 8-40 MHz	16	—	47	mA/V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	1.15	V	
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 * V_{DD}	—	V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		1
C_2	XTAL load capacitance	—	—	—		1
R_F	Feedback resistor					2
	Low-gain mode (HGO=0)	—	—	—	MΩ	

Table continues on the next page...

Table 19. External System Oscillator electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R_S, [3]	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp_XTAL}	Peak-to-peak amplitude of oscillation (oscillator mode) at XTAL					4
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	
V_{pp_EXTAL}	Peak-to-peak amplitude of oscillation (oscillator mode) at EXTAL					4, 5
	Low-gain mode (HGO=0)	0.8	—	—	V	
	High-gain mode (HGO=1), V_{DD}= 4.0 V to 5.5 V	1.7	—	—	V	
V_{SOSCOP}	Oscillation operating point					4
	High-gain mode (HGO=1)	1.15	—	—	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as:

   gm_crit = 4 * (ESR + R_S) * $(2\pi F)^2$ * $(C_0 + C_L)^2$

   where:

   - g_{mXOSC} is the transconductance of the internal oscillator circuit
   - ESR is the equivalent series resistance of the external crystal
   - R_S is the series resistance connected between XTAL pin and external crystal for current limitation
   - F is the external crystal oscillation frequency
   - C_0 is the shunt capacitance of the external crystal
   - C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2/(C_1+C_2)]$
   - C_s is stray or parasitic capacitance on the pin due to any PCB traces
   - C_1, C_2 external load capacitances on EXTAL and XTAL pins

   See manufacture datasheet for external crystal component values
2. - When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
   - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
3. R_S should be selected carefully to have appropriate oscillation amplitude for both protecting crystal or resonator device and satisfying proper oscillation startup condition.
4. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.
5. Minimum value is shown as a reference only, however the HW design needs to ensure it reaches the maximum value by following the guidelines given in above notes (notes 1, 2, and 3) and performs the required robustness testing at the application level. During testing, a low capacitance probe (< 5 pF) must be used to avoid any decrease in the V_{pp_EXTAL} value.

6.2.2 External System Oscillator frequency specifications

Table 20. External System Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_hi}	Oscillator crystal or resonator frequency	4	—	40 [1]	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	2
t_{dc_extal}	Input clock duty cycle (external clock mode)	48	50	52	%	2
t_{cst}	Crystal Start-up Time					
	8 MHz low-gain mode (HGO=0)	—	1.5	—	ms	3
	8 MHz high-gain mode (HGO=1)	—	2.5	—		
	40 MHz low-gain mode (HGO=0)	—	2	—		
	40 MHz high-gain mode (HGO=1)	—	2	—		

1. For an ideal clock of 40 MHz, if permitted by application requirements, an error of +/- 5% is supported with 50% duty cycle.
2. Frequencies below 40 MHz can be used for degraded duty cycle upto 40-60%. When using for ADC clock further restrictions apply. At 50 MHz to 45 MHz when sourcing for ADC clock please use divider ADCn.ADC_CFG1[ADICLK] to ½ or lower for the specific ADC instance. This will help achieve duty cycle requirement. for 45 MHz and 41 MHz 45-55% or higher duty cycle should be maintained.
3. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 System Clock Generation (SCG) specifications

6.2.3.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 21. Fast internal RC Oscillator electrical specifications for MCXE24x series

Symbol	Parameter[1]	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	FIRC target frequency	—	48	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	±0.5	±1	$\%F_{FIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	±0.5	±1.1	$\%F_{FIRC}$
$T_{Startup}$	Startup time		3.4	5	µs[2]
T_{JIT}, [3]	Cycle-to-Cycle jitter	—	300	500	ps
T_{JIT}[3]	Long term jitter over 1000 cycles	—	0.04	0.1	$\%F_{FIRC}$

1. With FIRC regulator enable
2. Startup time is defined as the time between clock enablement and clock availability for system use.
3. FIRC as system clock

NOTE

Fast internal RC oscillator is compliant with LIN when device is used as a slave node.

6.2.3.2 Slow internal RC oscillator (SIRC) electrical specifications

Table 22. Slow internal RC oscillator (SIRC) electrical specifications for MCXE24x series

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{SIRC}	SIRC target frequency	—	8	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	—	±3	$\%F_{SIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	—	±3.3	$\%F_{SIRC}$
$T_{Startup}$	Startup time	—	9	12.5	µs[1]

1. Startup time is defined as the time between clock enablement and clock availability for system use.

6.2.4 Low Power Oscillator (LPO) electrical specifications

Table 23. Low Power Oscillator (LPO) electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{LPO}	Internal low power oscillator frequency	113	128	139	kHz
$T_{startup}$	Startup Time	—	—	20	µs

6.2.5 SPLL electrical specifications

Table 24. SPLL electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SPLL_REF}[1]	PLL Reference Frequency Range	8	—	16	MHz
F_{SPLL_Input}[2]	PLL Input Frequency	8	—	40	MHz
F_{VCO_CLK}	VCO output frequency	180	—	320	MHz
F_{SPLL_CLK}	PLL output frequency	90	—	160	MHz
J_{CYC_SPLL}	PLL Period Jitter (RMS)[3]				
	at F_{VCO_CLK} 180 MHz	—	120	—	ps
	at F_{VCO_CLK} 320 MHz	—	75	—	ps
J_{ACC_SPLL}	PLL accumulated jitter over 1µs (RMS)[3]				
	at F_{VCO_CLK} 180 MHz	—	—	1350[4]	ps
	at F_{VCO_CLK} 320 MHz	—	—	600[4]	ps
D_{UNL}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%
T_{SPLL_LOCK}	Lock detector detection time[5]	—	—	$150 \times 10^{-6} + 1075(1/F_{SPLL\_REF})$	s

1. F_{SPLL_REF} is PLL reference frequency range after the PREDIV. For PREDIV and MULT settings refer SCG_SPLLCFG register of Reference Manual.
2. F_{SPLL_Input} is PLL input frequency range before the PREDIV must be limited to the range 8 MHz to 40 MHz. This input source could be derived from a crystal oscillator or some other external square wave clock source using OSC bypass mode. For external clock source settings refer SCG_SOSCCFG register of Reference Manual.
3. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary
4. The behavior of the accumulated PLL jitter saturates over 1us.
5. Lock detector detection time is defined as the time between PLL enablement and clock availability for system use.

6.3 Memory and memory interfaces

6.3.1 Flash memory module (FTFC/FTFM) electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.3.1.1 Flash timing specifications — commands

Table 25. Flash command timing specifications

Symbol	Description[1]		MCXE245		MCXE246		MCXE247			
			Typ	Max	Typ	Max	Typ	Max	Unit	Notes
t_{rd1blk}	Read 1 Block execution time	32 KB flash	—	—	—	—	—	—	ms	
		64 KB flash	—	0.5	—	0.5	—	—		
		128 KB flash	—	—	—	—	—	—		
		256 KB flash	—	—	—	—	—	—		
		512 KB flash	—	1.8	—	2	—	2		
t_{rd1sec}	Read 1 Section execution time	2 KB flash	—	75	—	75	—	75	µs	
		4 KB flash	—	100	—	100	—	100		
t_{pgmchk}	Program Check execution time	—	—	95	—	95	—	100	µs	
t_{pgm8}	Program Phrase execution time	—	90	225	90	225	90	225	µs	
t_{ersblk}	Erase Flash Block execution time	32 KB flash	—	—	—	—	—	—	ms	2
		64 KB flash	30	550	30	550	—	—		
		128 KB flash	—	—	—	—	—	—		
		256 KB flash	—	—	—	—	—	—		
		512 KB flash	250	4250	250	4250	250	4250		
t_{ersscr}	Erase Flash Sector execution time	—	12	130	12	130	12	130	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	5	—	5	—	5	—	ms	
t_{rd1all}	Read 1s All Block execution time	—	—	2.3	—	5.2	—	8.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	—	30	—	30	µs	
$t_{pgmonce}$	Program Once execution time	—	90	—	90	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	400	4900	700	10000	1400	17000	ms	2
$t_{pgmpart}$	Program Partition for EEPROM execution time	32 KB EEPROM backup	70	—	70	—	—	—	ms	3

Table continues on the next page...

Table 25. Flash command timing specifications (continued)

Symbol	Description[1]		MCXE245		MCXE246		MCXE247			
			Typ	Max	Typ	Max	Typ	Max	Unit	Notes
		64 KB EEPROM backup	71	—	71	—	150	—		
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2	—	—		
		48 KB EEPROM backup	1	1.5	1	1.5	—	—		
		64 KB EEPROM backup	1.3	1.9	1.3	1.9	1.3	1.9		
t_{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	—	—	µs	3,4
		48 KB EEPROM backup	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	4000		
$t_{eewr16b}$	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	—	—	µs	3,4
		48 KB EEPROM backup	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	4000		
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	360	2000	µs	
$t_{eewr32b}$	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	—	—	µs	3,4
		48 KB EEPROM backup	720	2125	720	2125	—	—		
		64 KB EEPROM backup	810	2250	810	2250	810	4500		
$t_{quickwr}$	32-bit Quick Write execution time: Time from CCIF	1st 32-bit write	200	550	200	550	200	1100	µs	4,5,6

Table continues on the next page...

Table 25. Flash command timing specifications (continued)

Symbol	Description[1]		MCXE245		MCXE246		MCXE247			
			Typ	Max	Typ	Max	Typ	Max	Unit	Notes
	clearing (start the write) until CCIF setting (32-bit write complete, ready for next 32-bit write)	2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550	150	550		
		Last (Nth) 32-bit write (time for write only, not cleanup)	200	550	200	550	200	550		
$t_{quickwrClnup}$	Quick Write Cleanup execution time	—	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	ms	7

1. All command times assumes 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2× the times shown.
5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write times may take up to 550 µs, as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

NOTE

Under certain circumstances FlexMEM maximum times may be exceeded. In this case the user or application may wait, or assert reset to the FTFC/FTFM macro to stop the operation.

6.3.1.2 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using as Program and Data Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	—	—	years	1
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	—	—	years	1
$n_{nvmcycp}$	Cycling endurance	10 K	—	—	cycles	2, 3
When using FlexMemory feature : FlexRAM as Emulated EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	—	—	years	1, 4

Table continues on the next page...

Table 26. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	—	—	years	1
$n_{nvmwree16}$ $n_{nvmwree256}$	Write endurance • EEPROM backup to FlexRAM ratio = 16 • EEPROM backup to FlexRAM ratio = 256	100 K 1.6 M	— —	— —	writes writes	5

1. Data retention period per block begins upon initial user factory programming or after each subsequent erase.
2. Program and Erase for PFlash and DFlash are supported across product temperature specification in Normal mode (not supported in HSRUN mode).
3. Cycling endurance is per DFlash or PFlash Sector.
4. Background maintenance operations during normal FlexRAM usage extend effective data retention life beyond 5 years.
5. FlexMemory write endurance specified for 16-bit and/or 32-bit writes to FlexRAM and is supported across product temperature specification in Normal Mode (not supported in HSRUN mode). Greater write endurance may be achieved with larger ratios of EEPROM backup to FlexRAM.

6.3.2 QuadSPI AC specifications

The following table describes the QuadSPI electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- Add 50 ohm series termination on board in QuadSPI SCK for Flash A to avoid loop back reflection when using in Internal DQS (PAD Loopback) mode.
- QuadSPI trace length should be 3 inches.
- For non-Quad mode of operation if external device doesn’t have pull-up feature, external pull-up needs to be added at board level for non-used pads.
- With external pull-up, performance of the interface may degrade based on load associated with external pull-up.

Table 27. QuadSPI electrical specifications

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN[1]						HSRUN[1]						RUN/HSRUN[2]			
QuadSPI Mode			SDR						SDR						SDR		DDR[3]	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		External DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Register Settings																		
MCR[DDR_EN]		-	0		0		0		0		0		0		0		1	
MCR[DQS_EN]		-	0		1		1		0		1		1		0		1	
MCR[SCLKCFG[0]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[1]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[2]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[3]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[5]]		-	0		0		0		0		0		0		0		1	
SMPR[FSPHS]		-	0		1		0		0		1		0		0		0	
SMPR[FSDLY]		-	0		0		0		0		0		0		0		0	
SOCCR [SOCCFG[7:0]]			-		0		23		-		0		30		-		-	
SOCCR[SOCCFG[15:8]]		-	-		-		-		-		-		-		-		30	
FLSHCR[TDH]		-	0x00		0x00		0x00		0x00		0x00		0x00		0x00		0x01	
Timing Parameters																		
SCK Clock Frequency	f_{SCK}	MHz	-	38	-	64	-	48	-	40	-	80	-	50	-	20	-	20[4]
SCK Clock Period	t_{SCK}	ns	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	50.0	-	50.0[4]	-

Table continues on the next page...

Table 27. QuadSPI electrical specifications (continued)

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN[1]						HSRUN[1]						RUN/HSRUN[2]			
QuadSPI Mode			SDR						SDR						SDR		DDR[3]	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		External DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
SCK Duty Cycle	t_{SDC}	ns	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 0.750	tSCK/2 - 0.750	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 2.5	tSCK/2 + 2.5	tSCK/2 - 2.5	tSCK/2 + 2.5
Data Input Setup Time	t_{IS}	ns	15	-	2.5	-	10	-	14	-	1.6	-	9	-	25	-	2	-
Data Input Hold Time	t_{IH}	ns	0	-	1	-	1	-	0	-	1	-	1	-	0	-	20	-
Data Output Valid Time	t_{OV}	ns	-	4.5	-	4.5	-	4.5	-	4	-	4	-	4	-	10	-	10
Data Output In-Valid Time	t_{IV}	ns	-	5	-	5	-	5	-	5	-	3[5]	-	5	-	5	5	-
CS to SCK Time [6]	t_{CSSCK}	ns	5	-	5	-	5	-	5	-	5	-	5	-	10	-	10	-
SCK to CS Time [7]	t_{SCKCS}	ns	5	-	5	-	5	-	5	-	5	-	5	-	5	-	5	-
Output Load		pf	25		25		25		25		25		25		25		25	

1. See Reference Manual for details on mode settings
2. See Reference Manual for details on mode settings
3. Valid for HyperRAM only
4. RWDS(External DQS CLK) frequency
5. For operating frequency ≤ 64 Mhz,Output invalid time is 5 ns.
6. Program register value QuadSPI_FLSHCR[TCSS] = 4`h2
7. Program register value QuadSPI_FLSHCR[TCSH] = 4`h1

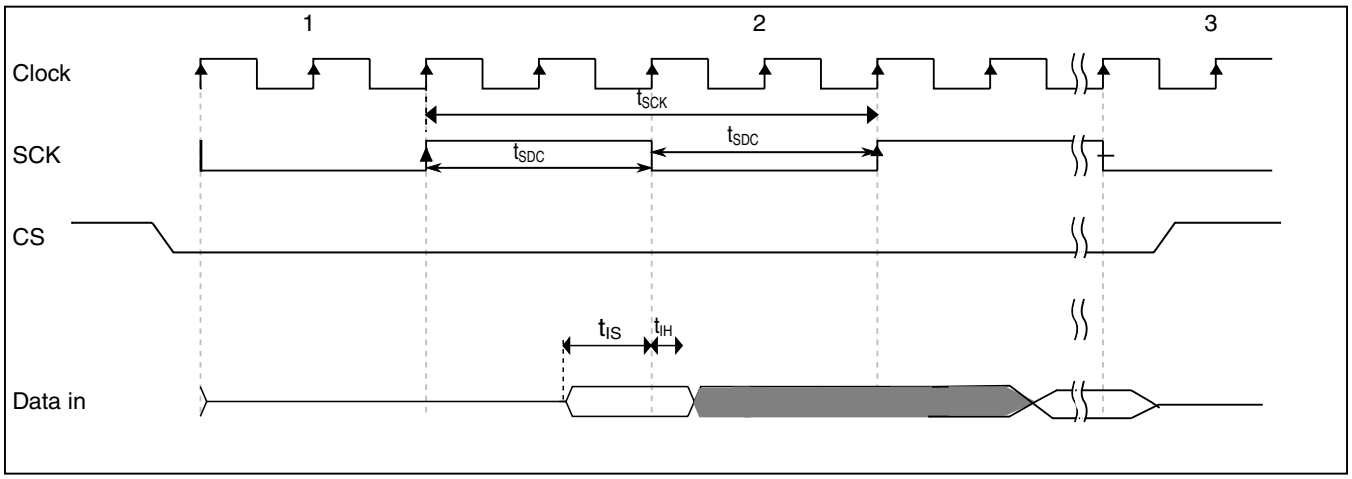


Figure 7. QuadSPI input timing (SDR mode) diagram

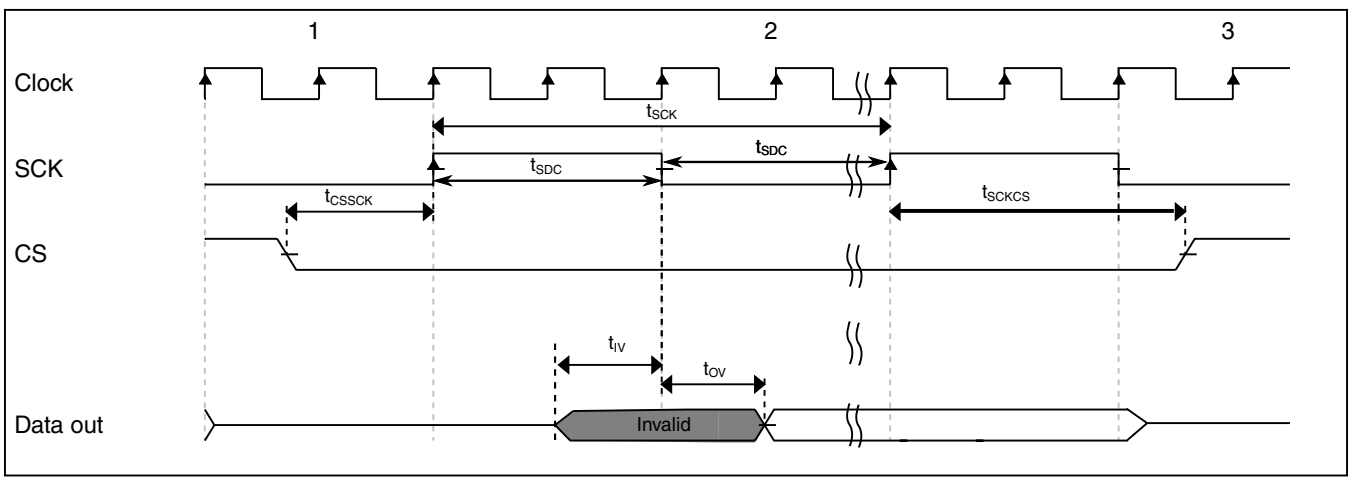
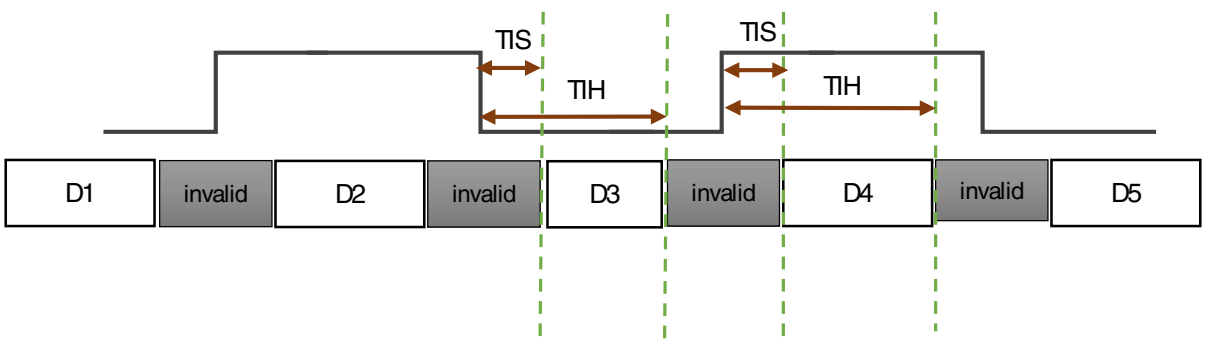


Figure 8. QuadSPI output timing (SDR mode) diagram



TIS – Setup Time
TIH – Hold Time

Figure 9. QuadSPI input timing (HyperRAM mode) diagram

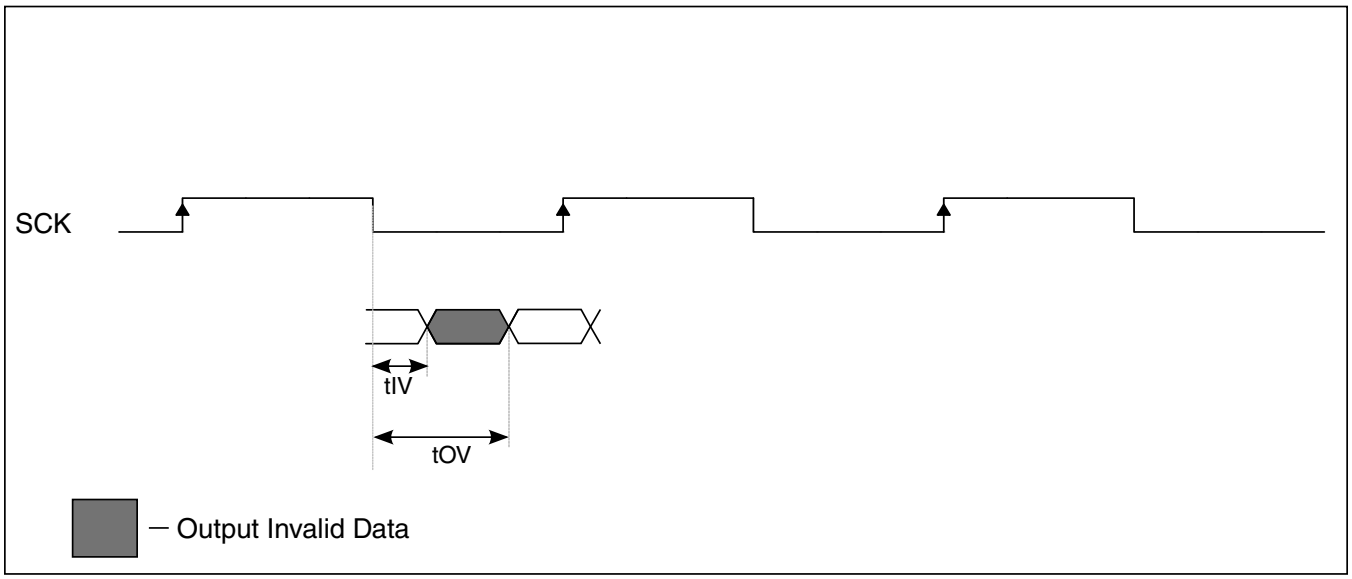


Figure 10. QuadSPI output timing (HyperRAM mode) diagram

6.4 Analog modules

6.4.1 ADC electrical specifications

6.4.1.1 12-bit ADC operating conditions

Table 28. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{REFH}	ADC reference voltage high		See Voltage and current operating requirements for values	V_{DDA}	See Voltage and current operating requirements for values	V	2
V_{REFL}	ADC reference voltage low		See Voltage and current operating requirements for values	0	See Voltage and current operating requirements for values	mV	2
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
R_S	Source impedendance	f_{ADCK} < 4 MHz	—	—	5	kΩ	
R_{SW1}	Channel Selection Switch Impedance		—	0.650	0.780	kΩ	
R_{AD}	Sampling Switch Impedance		—	0.155	1.0	kΩ	
C_{P1}	Pin Capacitance		—	2.1	2.5	pF	
C_{P2}	Analog Bus Capacitance		—	3 (MCXE245) 2	4	pF	
C_S	Sampling capacitance		—	5.1 (gain = 0)... 7.2 (gain = max)	6.36 (gain = 0)... 9.36 (gain = max)	pF	
f_{ADCK}	ADC conversion clock frequency	Normal usage	2	40	50	MHz	3, 4
f_{CONV}	ADC conversion frequency	No ADC hardware averaging.[5] Continuous conversions enabled, subsequent conversion time	46.4	928	1160	Ksps	6, 7
		ADC hardware averaging set to 32. [5] Continuous conversions enabled, subsequent conversion time	1.45	29	36.25	Ksps	6, 7
	ADC power consumption		—	1.0	1.1 [8]	pF	6, 7

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SS}. To get maximum performance, reference supply quality should be better than SAR ADC. See application note AN5032 for details.
3. Clock and compare cycle need to be set according to the guidelines mentioned in the *Reference Manual* .

4. ADC conversion will become less reliable above maximum frequency.
5. When using ADC hardware averaging, see the *Reference Manual* to determine the most appropriate setting for AVGS.
6. Numbers based on the minimum sampling time of 275 ns.
7. For guidelines and examples of conversion rate calculation, see the *Reference Manual* section 'Calibration function'
8. Configuration used during the test to obtain this value is:
    - VDD=VDDA=VREFH=2.5 V, 2.7 V, 3 V ,5.5 V, (externally forced)
    - BUS CLK=48 MHz, ADC CLK=48MHz (FIRC Used), Calibration CLK=24MHz, Sample Time =14 Cyc, Averaging=32
    - Resolution= 12 bit
    - Conversion Mode: Continuous Conversion
    - Channel: ADC0_SE1
    - Temperatures: -40 °C, 25 °C, 125 °C

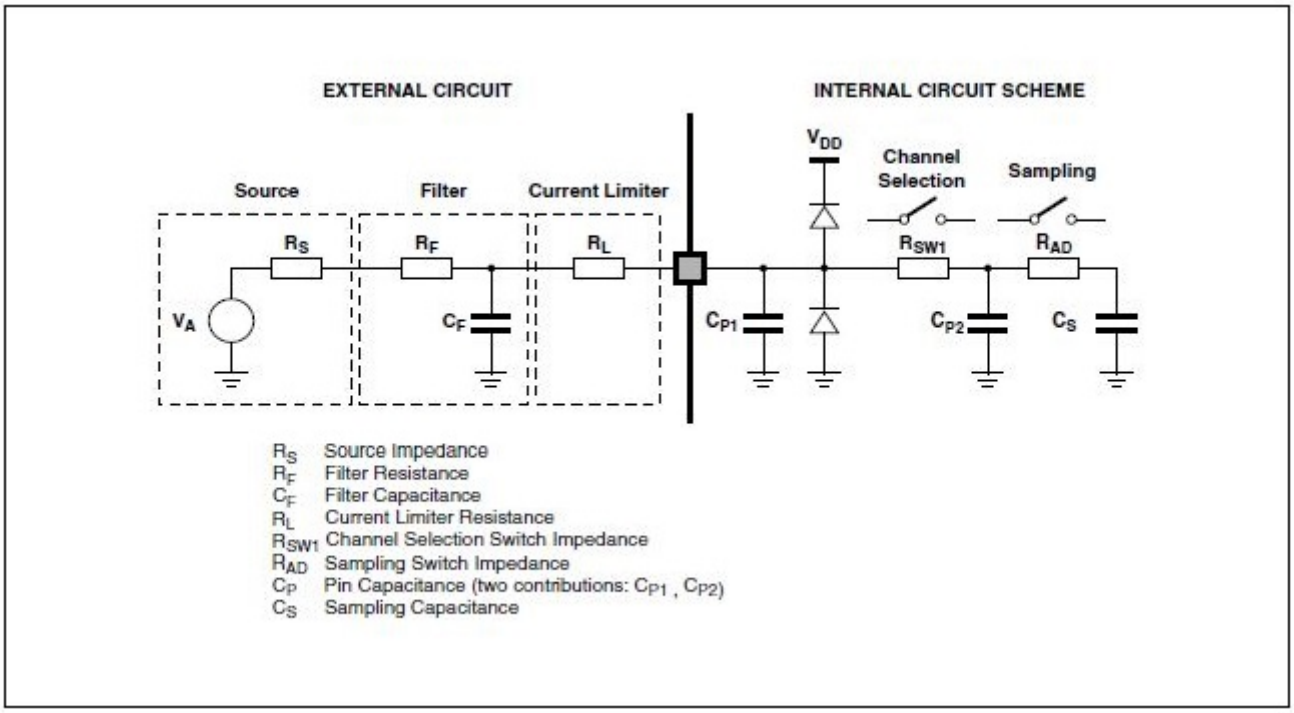


Figure 11. ADC input impedance equivalency diagram

6.4.1.2 12-bit ADC electrical characteristics

NOTE

- ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.
- On reduced pin packages where ADC reference pins are shared with supply pins, ADC analog performance characteristics may be impacted. The amount of variation will be directly impacted by the external PCB layout and hence care must be taken with PCB routing.
- All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.

Table 29. 12-bit ADC characteristics (2.7 V to 3 V) (V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	2.7	—	3	V	
I_{DDA_ADC}	Supply current per ADC	—	0.6	—	mA	2
SMPLTS	Sample Time	275	—	Refer to the *Reference Manual*	ns	
TUE[3]	Total unadjusted error	—	±4	±8	LSB[4]	5, 6, 7, 8
DNL	Differential non-linearity	—	±1.0	—	LSB[4]	5, 6, 7, 8
INL	Integral non-linearity	—	±2.0	—	LSB[4]	5, 6, 7, 8

1. Typical values assume V_{DDA} = 3 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF.
2. The ADC supply current depends on the ADC conversion rate.
3. Represents total static error, which includes offset and full scale error.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
6. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
7. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
8. All the parameters in the table are given assuming system clock as the clocking source for ADC.

Table 30. 12-bit ADC characteristics (3 V to 5.5 V)(V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	3	—	5.5	V	
I_{DDA_ADC}	Supply current per ADC	—	1	—	mA	2
SMPLTS	Sample Time	275	—	Refer to the *Reference Manual*	ns	
TUE[3]	Total unadjusted error	—	±4	±8	LSB[4]	5, 6, 7, 8
DNL	Differential non-linearity	—	±0.7	—	LSB[4]	5, 6, 7, 8
INL	Integral non-linearity	—	±1.0	—	LSB[4]	5, 6, 7, 8

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated.
2. The ADC supply current depends on the ADC conversion rate.
3. Represents total static error, which includes offset and full scale error.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
6. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
7. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
8. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

- Due to triple bonding in lower pin packages like 48-LQFP, and 64-LQFP degradation might be seen in ADC parameters.
- When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

6.4.2 CMP with 8-bit DAC electrical specifications

Table 32. Comparator with 8-bit DAC electrical specifications for MCXE24x series

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode[1]				µA
	-40 - 125 °C	—	230	300	
I_{DDLS}	Supply current, Low-speed mode[1]				µA
	-40 - 105 °C	—	6	11	
	-40 - 125 °C		6	13	
V_{AIN}	Analog input voltage	0	0 - V_{DDA}	V_{DDA}	V
V_{AIO}	Analog input offset voltage, High-speed mode				mV
	-40 - 125 °C	-25	±1	25	
V_{AIO}	Analog input offset voltage, Low-speed mode				mV
	-40 - 125 °C	-40	±4	40	
t_{DHSB}	Propagation delay, High-speed mode[2]				ns
	-40 - 105 °C	—	35	200	
	-40 - 125 °C		35	300	
t_{DLSB}	Propagation delay, Low-speed mode[2]				µs
	-40 - 105 °C	—	0.5	2	
	-40 - 125 °C	—	0.5	3	
t_{DHSS}	Propagation delay, High-speed mode[3]				ns
	-40 - 105 °C	—	70	400	

Table continues on the next page...

Table 32. Comparator with 8-bit DAC electrical specifications for MCXE24x series (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	-40 - 125 °C	—	70	500	
t_{DLSS}	Propagation delay, Low-speed mode[3]				µs
	-40 - 105 °C	—	1	5	
	-40 - 125 °C	—	1	5	
t_{IDHS}	Initialization delay, High-speed mode[4]				µs
	-40 - 125 °C	—	1.5	3	
t_{IDLS}	Initialization delay, Low-speed mode[4]				µs
	-40 - 125 °C	—	10	30	
V_{HYST0}	Analog comparator hysteresis, Hyst0				mV
	-40 - 125 °C	—	0	—	
V_{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	-40 - 125 °C	—	19	66	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	-40 - 125 °C	—	15	40	
V_{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	-40 - 125 °C	—	34	133	
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	-40 - 125 °C	—	23	80	
V_{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV
	-40 - 125 °C	—	46	200	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	-40 - 125 °C	—	32	120	
I_{DAC8b}	8-bit DAC current adder (enabled)				
	3.3V Reference Voltage	—	6	9	µA
	5V Reference Voltage	—	10	16	µA
INL[5]	8-bit DAC integral non-linearity	–0.75	—	0.75	LSB[6]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB[6]
t_{DDAC}	Initialization and switching settling time	—	—	30	µs

1. Difference at input > 200mV
2. Applied ± (100 mV + $V_{HYST0/1/2/3}$+ max. of V_{AIO}) around switch point.
3. Applied ± (30 mV + 2 × $V_{HYST0/1/2/3}$+ max. of V_{AIO}) around switch point.
4. Applied ± (100 mV + $V_{HYST0/1/2/3}$).
5. Calculation method used: Linear Regression Least Square Method
6. 1 LSB = $V_{reference}$/256

NOTE

For comparator IN signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired comparator performance. Additionally, an external capacitor (1nF) should be used to filter noise on input signal. Also, source drive should not be weak (Signal with < 50 K pull up/down is recommended).

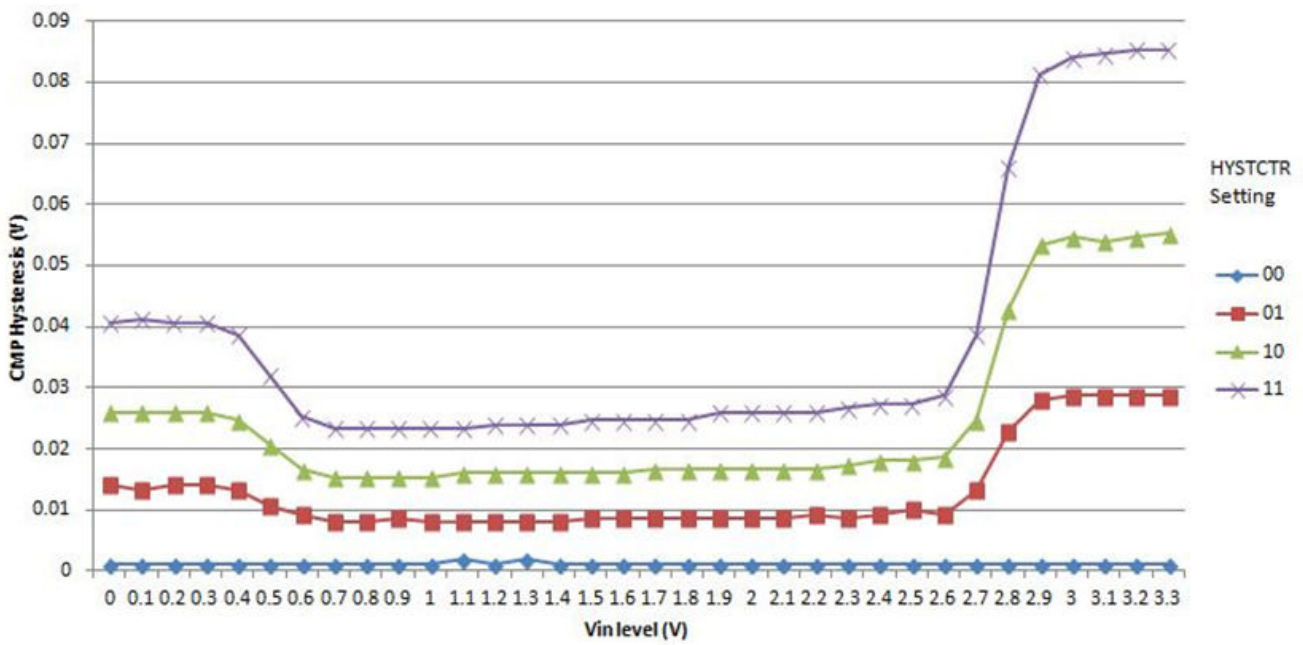


Figure 12. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 0)

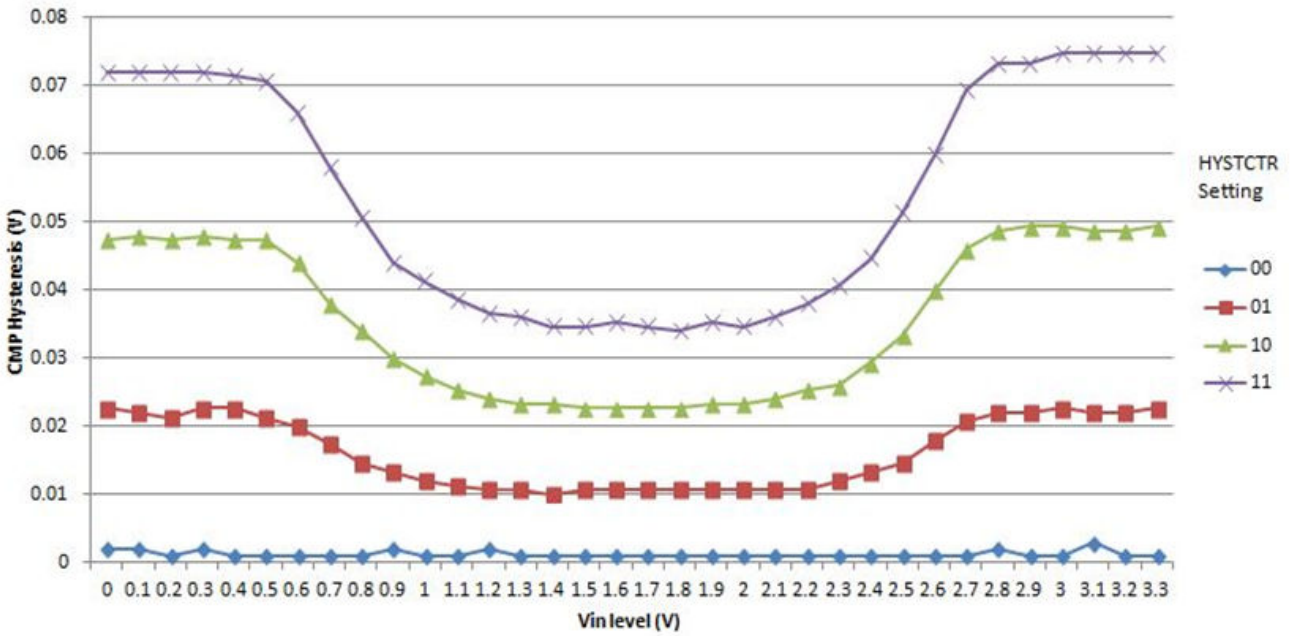


Figure 13. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 1)

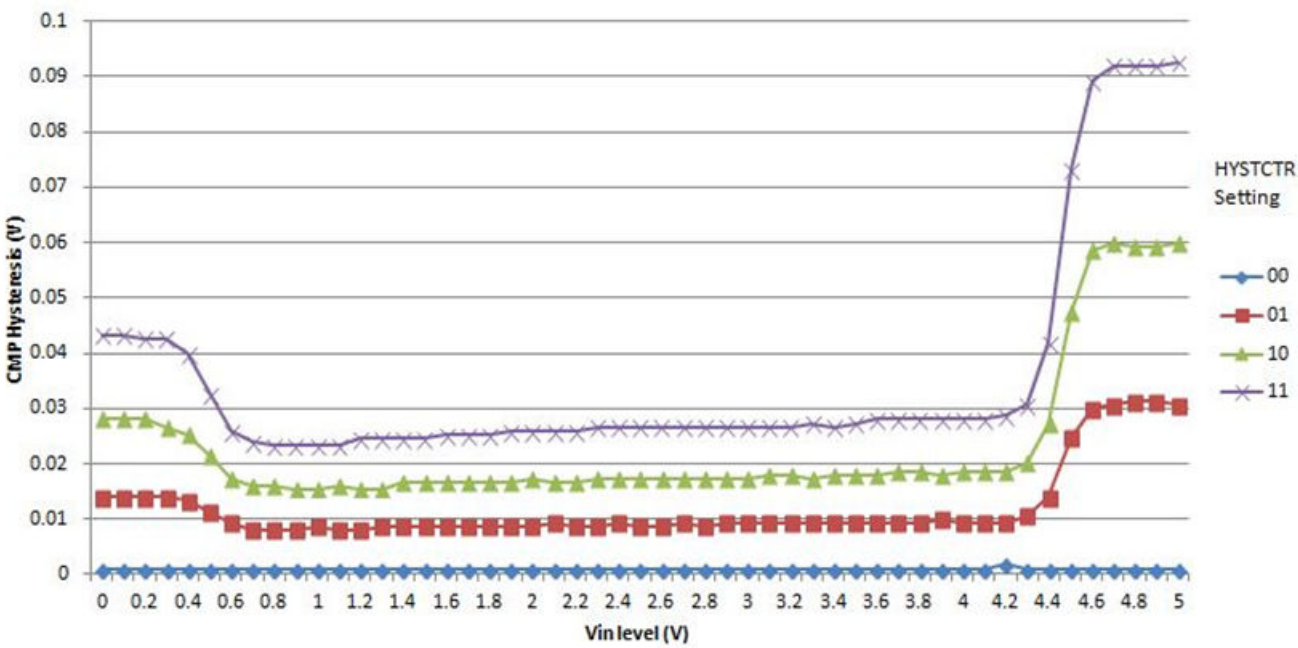


Figure 14. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 0)

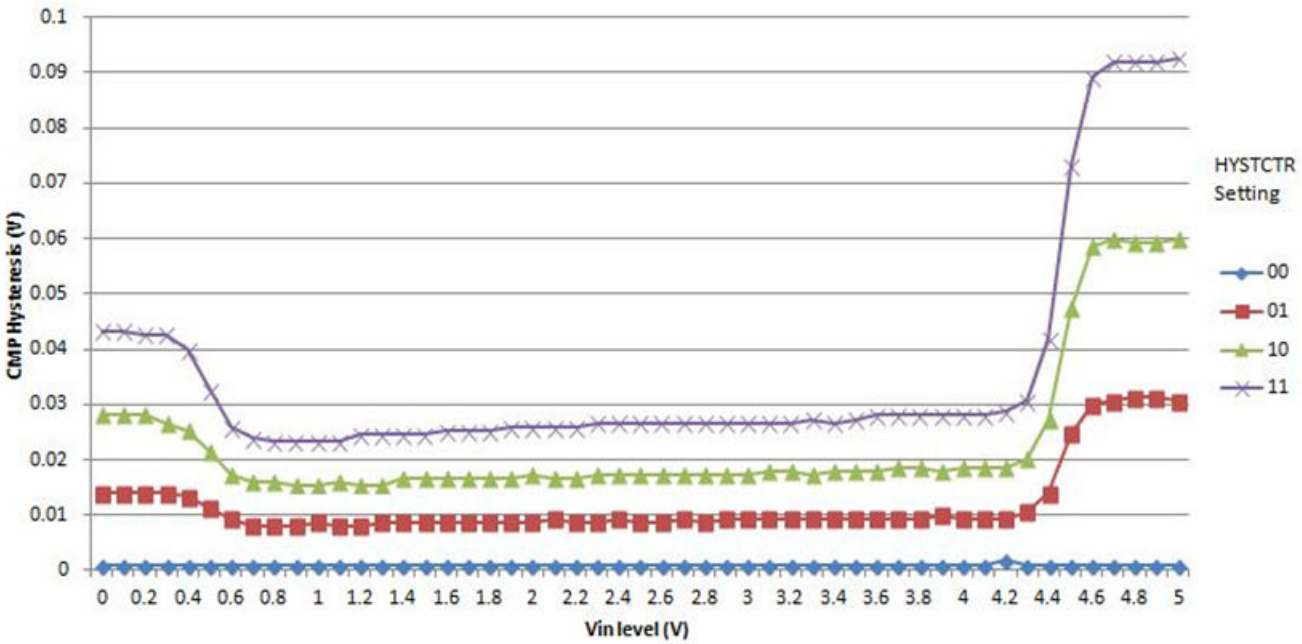


Figure 15. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 1)

6.5 Communication modules

6.5.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

6.5.1.1 Supported baud rate

Baud rate = Baud clock / ((OSR+1) * SBR).

For details, see section: 'Baud rate generation' of the *Reference Manual*.

6.5.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

- All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1).

Table 33. LPSPI electrical specifications[1]

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
	f_{periph}[3, 4]	Peripheral Frequency	Slave	-	40	-	40	-	56	-	56	-	4	-	4	MHz
			Master	-	40	-	40	-	56	-	56	-	4	-	4	
			Master Loopback[5]	-	40	-	48	-	48	-	48	-	4	-	4	
			Master Loopback(slow)[6]	-	48	-	48	-	48	-	48	-	4	-	4	
1	f_{op}	Frequency of operation	Slave	-	10	-	10	-	14	-	14[7]	-	2	-	2	MHz
			Master	-	10	-	10	-	14	-	14[7]	-	2	-	2	
			Master Loopback[5]	-	20	-	12	-	24	-	12	-	2	-	2	
			Master Loopback(slow)[6]	-	12	-	12	-	12	-	12	-	2	-	2	
2	t_{SPSCK}	SPSCK period	Slave	100	-	100	-	72	-	72	-	500	-	500	-	ns
			Master	100	-	100	-	72	-	72	-	500	-	500	-	
			Master Loopback[5]	50	-	83	-	42	-	83	-	500	-	500	-	
			Master Loopback(slow)[6]	83	-	83	-	83	-	83	-	500	-	500	-	
3	t_{Lead}[8]	Enable lead time (PCS to SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns

Table continues on the next page...

Table 33. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
			Master	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-50	-	(PCSSCK+1)*t_{periph}-50	-	
			Master Loopback[5]													
			Master Loopback(slow) [6]													
4	t_{Lag}[9]	Enable lag time (After SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 50	-	(SCKPCS+1)*t_{periph}- 50	-	
			Master Loopback[5]													
			Master Loopback(slow) [6]													
5	t_{WSPSCK}[10]	Clock(SPSCK) high or low time (SPSCK duty cycle)	Slave	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-5	t_{SPSCK}/2+5	t_{SPSCK}/2-5	t_{SPSCK}/2+5	ns
			Master													
			Master Loopback[5]													
			Master Loopback(slow) [6]													
6	t_{SU}	Data setup time(inputs)	Slave	3	-	5	-	3	-	5	-	18	-	18	-	ns
			Master	29	-	38	-	26	-	37[11] 32 [12]	-	72	-	78	-	

Table continues on the next page...

Table 33. LPSPI electrical specifications[1] (continued)

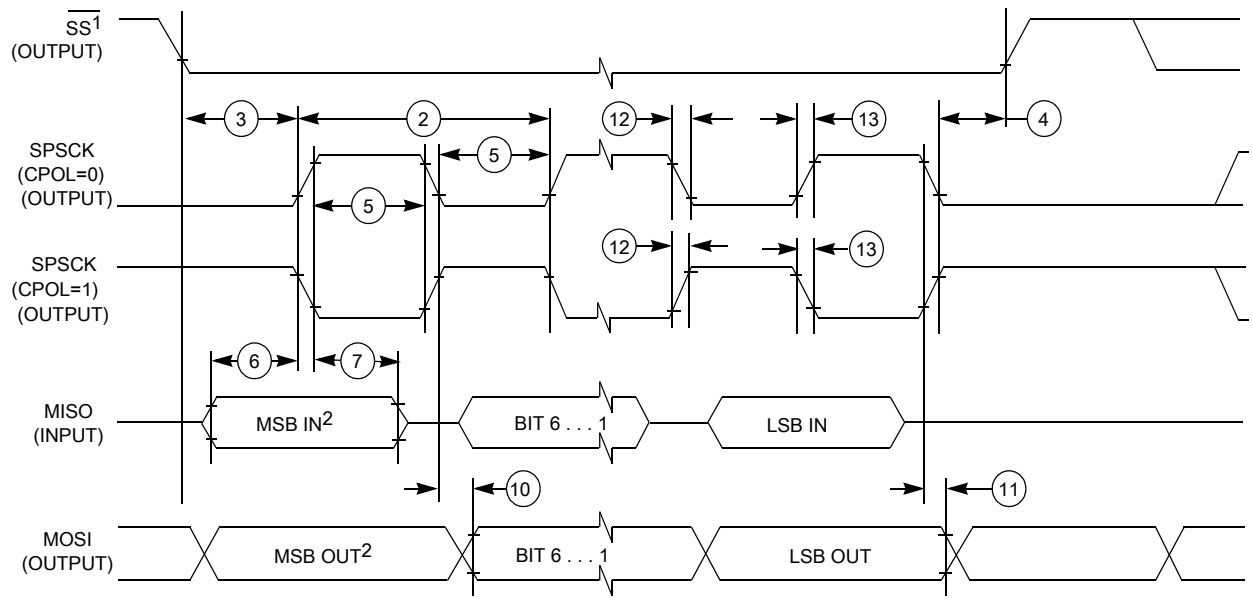
Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
			Master Loopback[5]	7	-	8	-	5	-	7	-	20	-	20	-	
			Master Loopback(slow) [6]	8	-	10	-	7	-	9	-	20	-	20	-	
7	t_{HI}	Data hold time(inputs)	Slave	3	-	3	-	3	-	3	-	14	-	14	-	ns
			Master	0	-	0	-	0	-	0	-	0	-	0	-	
			Master Loopback[5]	3	-	3	-	2	-	3	-	11	-	11	-	
			Master Loopback(slow) [6]	3	-	3	-	3	-	3	-	12	-	12	-	
8	t_a	Slave access time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns
9	t_{dis}	Slave MISO (SOUT) disable time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns
10	t_v	Data valid (after SPSCK edge)	Slave	-	30	-	39	-	26	-	36 [11] 31 [12]	-	92	-	96	ns
			Master	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback[5]	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback(slow) [6]	-	8	-	10	-	7	-	9	-	44	-	44	
11	t_{HO}	Data hold time(outputs)	Slave	4	-	4	-	4	-	4	-	4	-	4	-	ns
			Master	-15	-	-22	-	-15	-	-23	-	-22	-	-29	-	
			Master Loopback[5]	-10	-	-14	-	-10	-	-14	-	-14	-	-19	-	

Table continues on the next page...

Table 33. LPSPI electrical specifications[1] (continued)

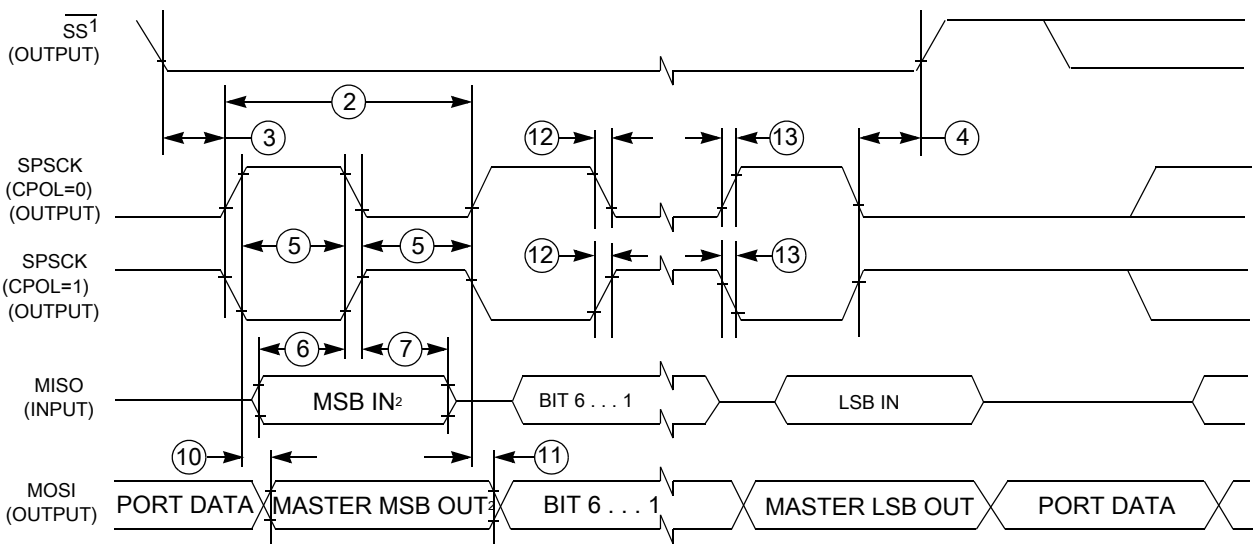
Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
			Master Loopback(slow) [6]	-15	-	-22	-	-15	-	-22	-	-21	-	-27	-	
12	$t_{RI/FI}$	Rise/Fall time input	Slave	-	1	-	1	-	1	-	1	-	1	-	1	ns
			Master	-		-		-		-		-		-		-
			Master Loopback[5]	-		-		-		-		-		-		-
			Master Loopback(slow) [6]	-		-		-		-		-		-		-
13	$t_{RO/FO}$	Rise/Fall time output	Slave	-	25	-	25	-	25	-	25	-	25	-	25	ns
			Master	-		-		-		-		-		-		-
			Master Loopback [5]	-		-		-		-		-		-		-
			Master Loopback(slow) [6]	-		-		-		-		-		-		-

1. Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
2. While transitioning from HSRUN mode to RUN mode, LPSPI output clock should not be more than 14 MHz.
3. f_{periph} = LPSPI peripheral clock
4. $t_{periph} = 1/f_{periph}$
5. Master Loopback mode - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pads used are PTD15 and PTE0. Applicable only for LPSPI0.
6. Master Loopback (slow) - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pad used is PTB2. Applicable only for LPSPI0.
7. This is the maximum operating frequency (f_{op}) for LPSPI0 with GPIO-HD PAD type only. Otherwise, the maximum operating frequency (f_{op}) is 12 Mhz.
8. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
9. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.
10. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.
11. Maximum operating frequency (f_{op}) is 12 MHz irrespective of PAD type and LPSPI instance.
12. Applicable for LPSPI0 only with GPIO-HD PAD type, with maximum operating frequency (f_{op}) as 14 MHz.



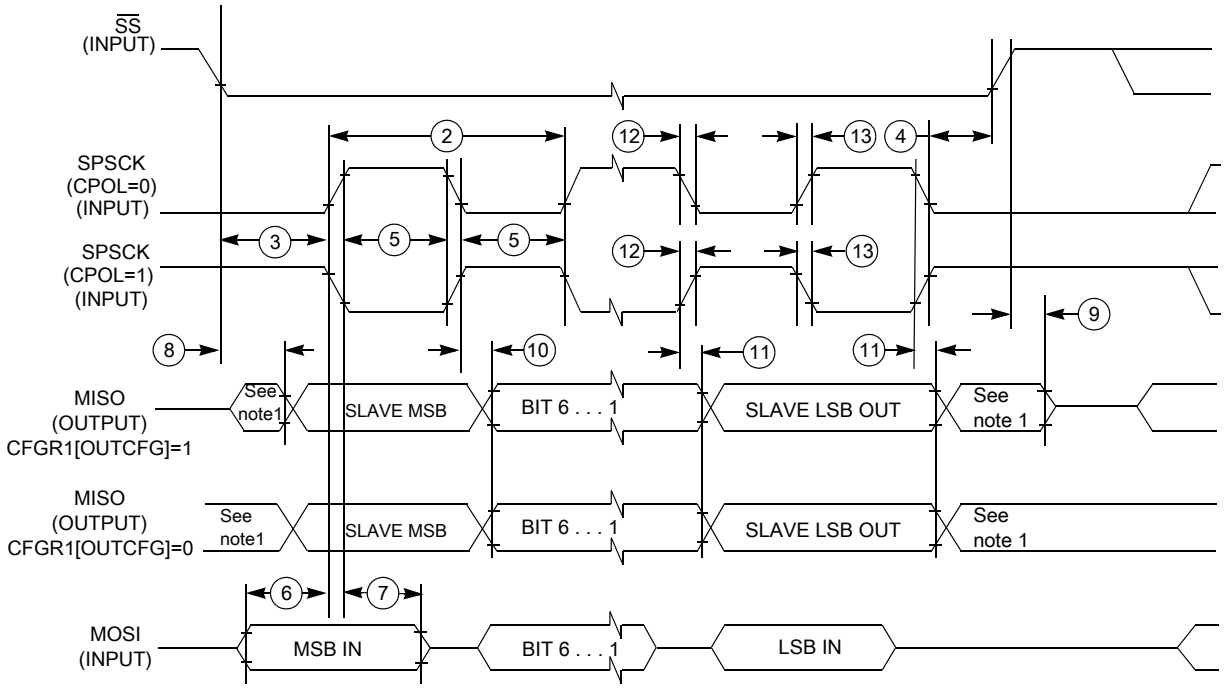
1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 16. LPSPI master mode timing (CPHA = 0)



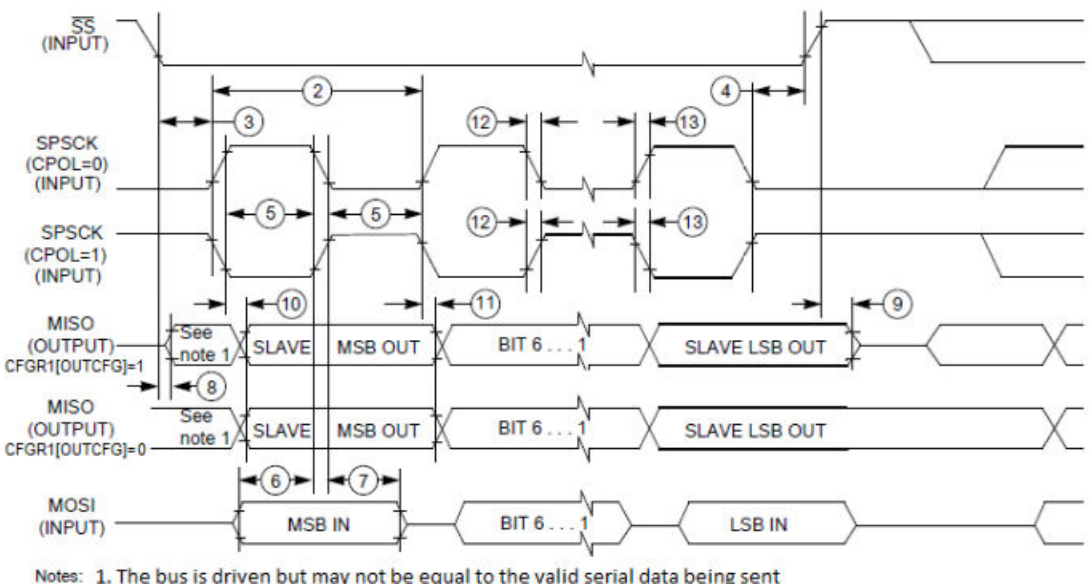
1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. LPSPI master mode timing (CPHA = 1)



Notes:
1.The bus is driven but may not be equal to the valid serial data being sent.

Figure 18. LPSPI slave mode timing (CPHA = 0)



Notes: 1. The bus is driven but may not be equal to the valid serial data being sent

Figure 19. LPSPI slave mode timing (CPHA = 1)

6.5.3 LPI2C electrical specifications

See General AC specifications for LPI2C specifications.

For supported baud rate see section 'Chip-specific LPI2C information' of the *Reference Manual.*

6.5.4 FlexCAN electical specifications

For supported baud rate, see section 'Protocol timing' of the *Reference Manual*.

6.5.5 SAI electrical specifications

The following table describes the SAI electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 34. Master mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S1	SAI_MCLK cycle time	40	—	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	—	ns
S4	SAI_BCLK pulse width high/low	45%	55%	BCLK period
S5	SAI_RXD input setup before SAI_BCLK	28	—	ns
S6	SAI_RXD input hold after SAI_BCLK	0	—	ns
S7	SAI_BCLK to SAI_TXD output valid	—	8	ns
S8	SAI_BCLK to SAI_TXD output invalid	-2	—	ns
S9	SAI_FS input setup before SAI_BCLK	28	—	ns
S10	SAI_FS input hold after SAI_BCLK	0	—	ns
S11	SAI_BCLK to SAI_FS output valid	—	8	ns
S12	SAI_BCLK to SAI_FS output invalid	-2	—	ns

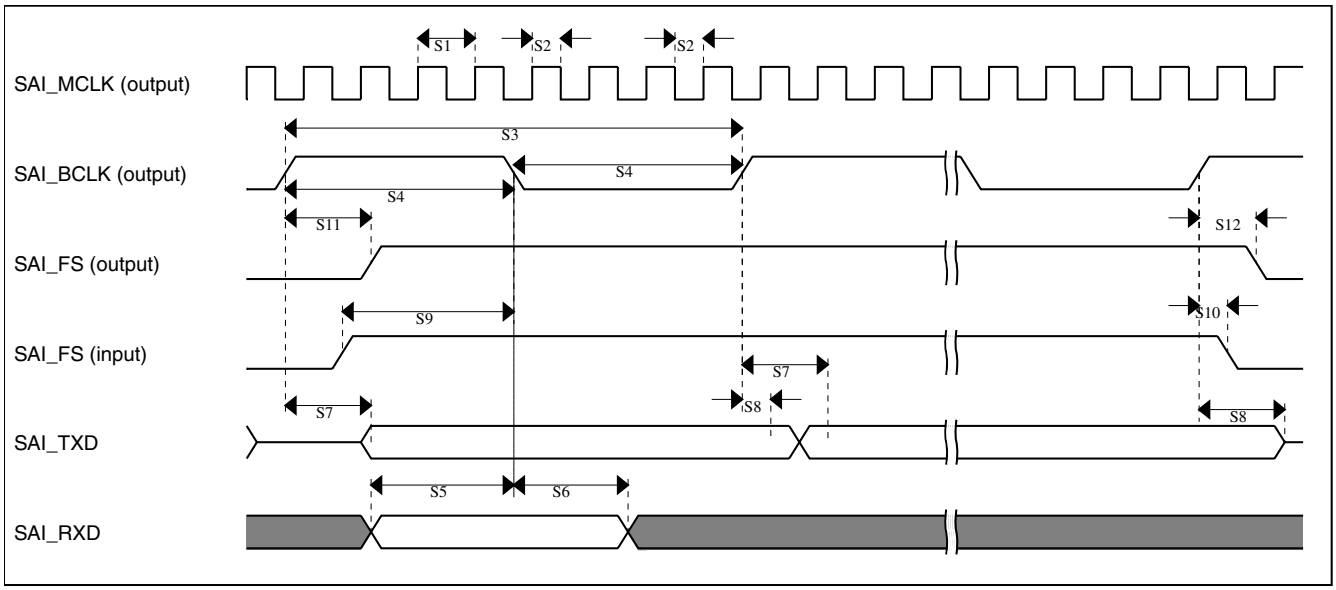


Figure 20. SAI Timing — Master modes

Table 35. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14[1]	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

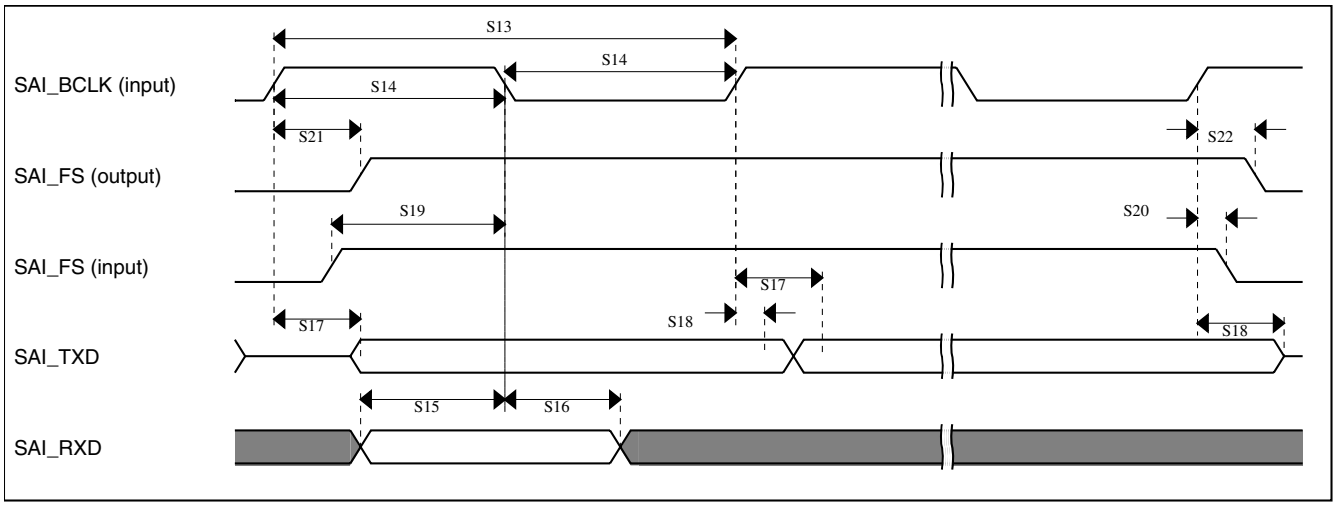


Figure 21. SAI Timing — Slave modes

6.5.6 Ethernet AC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

The following table describes the MII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 36. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

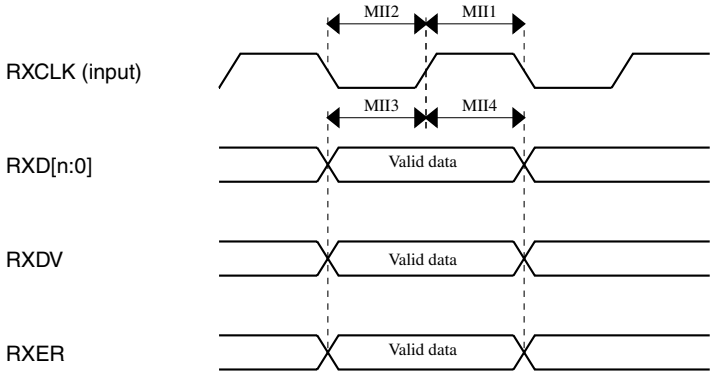


Figure 22. MII receive diagram

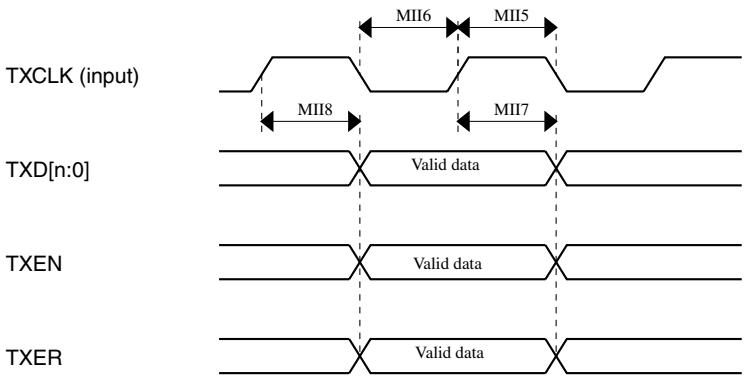


Figure 23. MII transmit signal diagram

The following table describes the RMII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 37. RMII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RMII input clock RMII_CLK Frequency	—	50	MHz
RMII1, RMII5	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2, RMII6	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

Table 37. RMII signal switching specifications (continued)

Symbol	Description	Min.	Max.	Unit
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	2	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

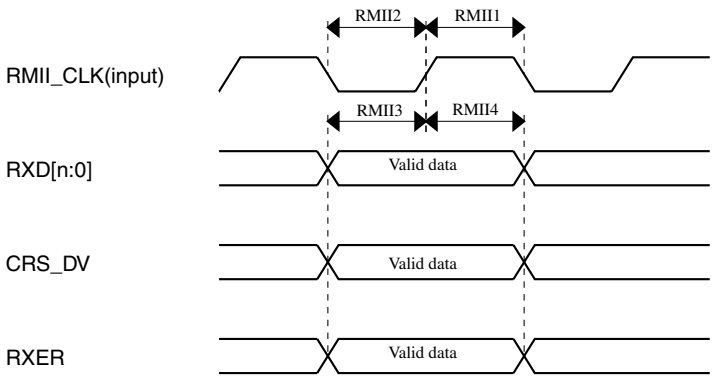


Figure 24. RMII receive diagram

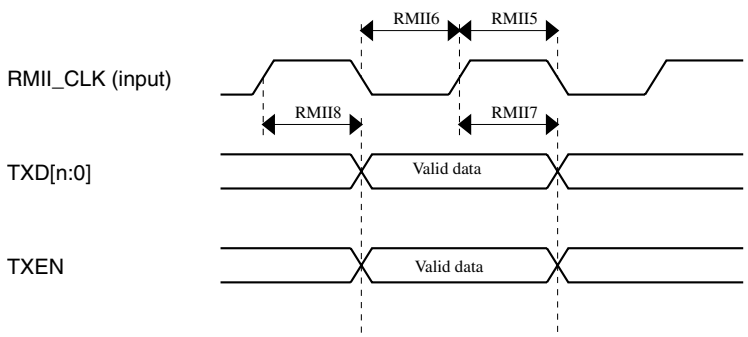


Figure 25. RMII transmit diagram

The following table describes the MDIO electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- MDIO pin must have external Pull-up.

Table 38. MDIO timing specifications

Symbol	Description	Min.	Max.	Unit
—	MDC Clock Frequency	—	2.5	MHz
MDC1	MDC pulse width high	40%	60%	MDC period

Table continues on the next page...

Table 38. MDIO timing specifications (continued)

Symbol	Description	Min.	Max.	Unit
MDC2	MDC pulse width low	40%	60%	MDC period
MDC3	MDIO (input) to MDC rising setup	25	—	ns
MDC4	MDIO (input) to MDC rising edge hold	0	—	ns
MDC5	MDC falling edge to MDIO output valid (maximum propagation delay)	—	25	ns
MDC6	MDC falling edge to MDIO output invalid (minimum propagation delay)	-10	—	ns

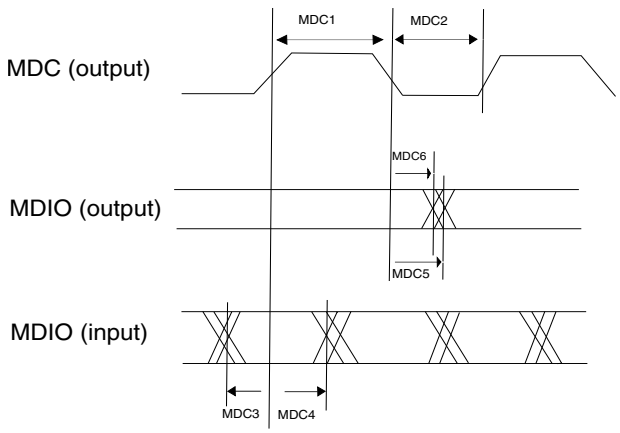


Figure 26. MII/RMII serial management channel timing diagram

6.5.7 Clockout frequency

Maximum supported clock out frequency for this device is 20 MHz

6.6 Debug modules

6.6.1 SWD electrical specofications

Table 39. SWD electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	25	-	25	-	25	-	25	-	10	-	10	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	4	-	4	-	4	-	4	-	16	-	16	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	3	-	3	-	3	-	3	-	10	-	10	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	28	-	38	-	28	-	38	-	70	-	77	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	28	-	38	-	28	-	38	-	70	-	77	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns

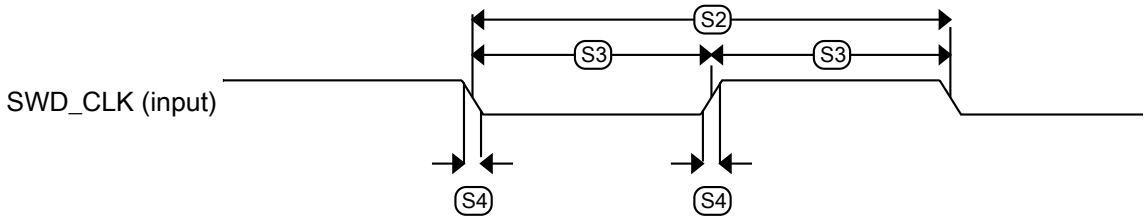


Figure 27. Serial wire clock input timing

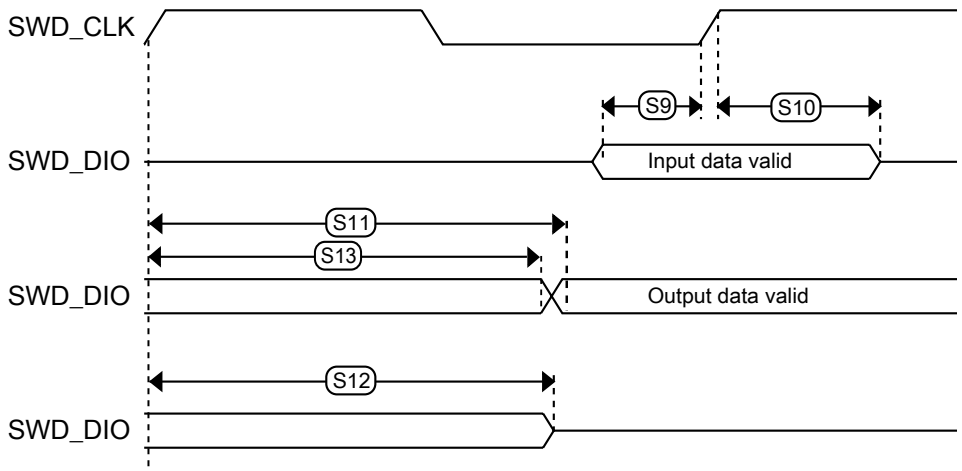


Figure 28. Serial wire data timing

6.6.2 Trace electrical specifications

The following table describes the ETM Trace electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

NOTE

ETM trace is supported only on MCXE247.

Table 40. ETM Trace specifications

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
—	Fsys	System frequency	80	48	40	112	80	4	MHz
Trace on fast pads	f_{TRACE}	Max Trace frequency	80	48	40	74.667	80	4	MHz
	t_{DVO}	Data Output Valid	4	4	4	4	4	20	ns
	t_{DIV}	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
Trace on slow pads	f_{TRACE}	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
	t_{DVO}	Data Output Valid	8	8	8	8	8	20	ns
	t_{DIV}	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

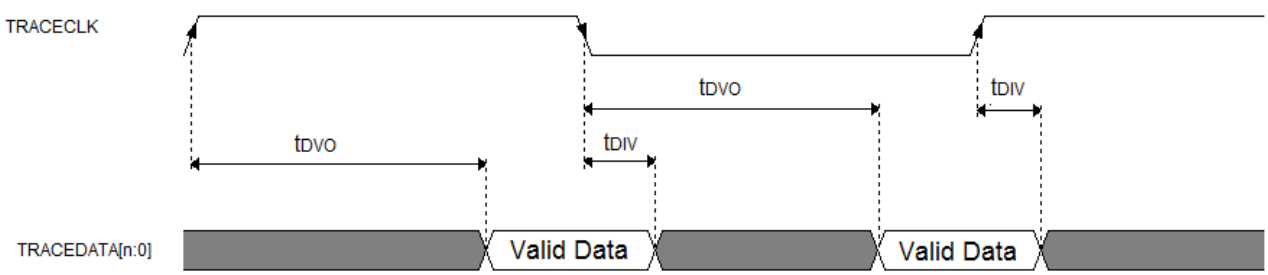


Figure 29. TRACE CLKOUT specifications

6.6.3 JTAG electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
JI	TCLK frequency of operation													MHz
	Boundary Scan	-	20	-	20	-	20	-	20	-	10	-	10	
	JTAG	-	20	-	20	-	20	-	20	-	10	-	10	
J2	TCLK cycle period	1/JI	-	1/JI	-	1/JI	-	1/JI	-	1/JI	-	1/JI	-	ns
J3	TCLK clock pulse width													ns

Table continues on the next page...

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG													
J4	TCLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	-	5	-	5	-	5	-	15	-	15	-	ns
J6	Boundary scan input data hold time after TCLK rise	5	-	5	-	5	-	5	-	8	-	8	-	ns
J7	TCLK low to boundary scan output data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J8	TCLK low to boundary scan output data invalid	0	-	0	-	0	-	0	-	0	-	0	-	
J9	TCLK low to boundary scan output high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns
J10	TMS, TDI input data setup time to TCLK rise	3	-	3	-	3	-	3	-	15	-	15	-	ns
J11	TMS, TDI input data hold time after TCLK rise	2	-	2	-	2	-	2	-	8	-	8	-	ns
J12	TCLK low to TDO data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J13	TCLK low to TDO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns
J14	TCLK low to TDO high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns

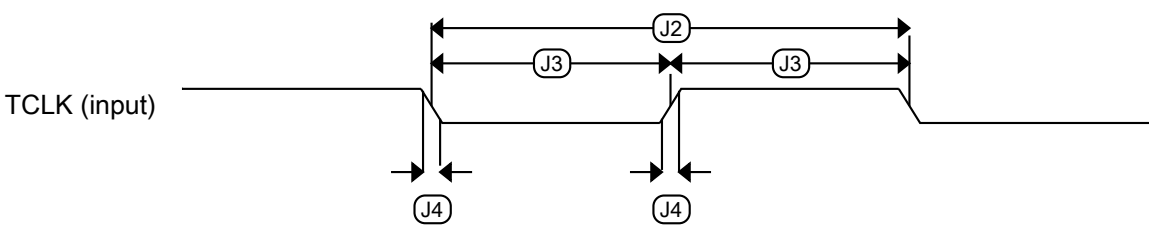


Figure 30. Test clock input timing

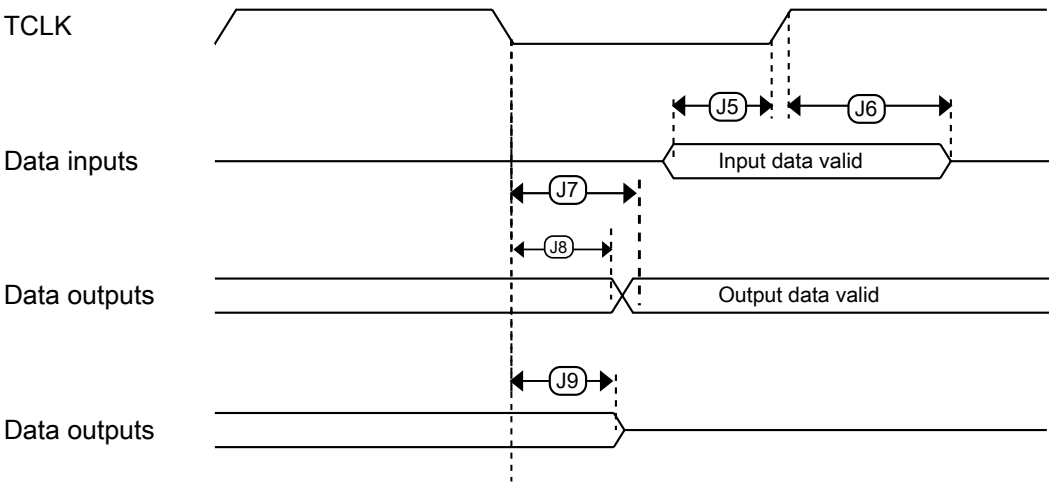


Figure 31. Boundary scan (JTAG) timing

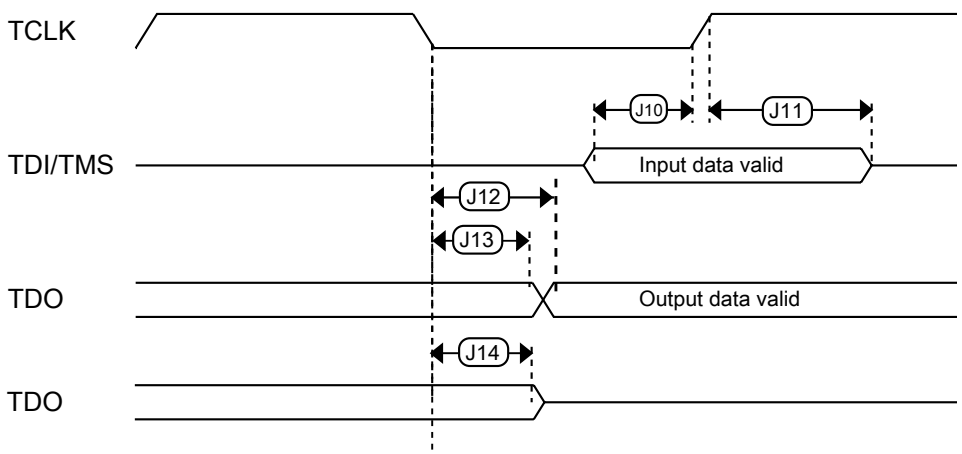


Figure 32. Test Access Port timing

7 Thermal attributes

7.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

7.2 Thermal characteristics

Table 41. Thermal characteristics for 48/64/100/144-pin LQFP package

Rating	Conditions	Symbol	Package	Values (in °C/W)		
				MCXE245	MCXE246	MCXE247
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	48	69	NA	NA
			64	61	59	NA
			100	52	51	46
			144	NA	51	44
Thermal resistance, Junction to Ambient (Natural Convection)[1]	Two layer board (1s1p)	$R_{\theta JA}$	48	48	NA	NA
			64	45	44	NA
			100	42	40	36
			144	NA	44	37
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	48	45	NA	NA
			64	43	41	NA
			100	40	39	34
			144	NA	42	36
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	48	57	NA	NA
			64	49	48	NA
			100	42	41	37
			144	NA	42	36
Thermal resistance, Junction to Ambient (@200 ft/min)[1]	Two layer board (1s1p)	$R_{\theta JMA}$	48	41	NA	NA
			64	38	37	NA
			100	35	34	30
			144	NA	37	31
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	48	39	NA	NA
			64	36	35	NA
			100	34	33	28
			144	NA	36	30
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	48	23	NA	NA
			64	25	23	NA
			100	25	24	19
			144	NA	30	24

Table continues on the next page...

Table 41. Thermal characteristics for 48/64/100/144-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values (in °C/W)		
				MCXE245	MCXE246	MCXE247
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	48	17	NA	NA
			64	12	11	NA
			100	12	11	9
			144	NA	12	9
Thermal resistance, Junction to Case (Bottom) [6]	—	$R_{\theta JCBottom}$	48	NA		
			64			
			100			
			144			
Thermal resistance, Junction to Package Top[7]	Natural Convection	Ψ_{JT}	48	2	NA	NA
			64	2	2	NA
			100	2	2	1
			144	NA	2	1

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in the package drawings.

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

Package option	Document Number	Manufacture Code
48-pin LQFP	SOT313-3	98ASH00962A
64-pin LQFP	SOT1699-1	98ASS23234W
100-pin LQFP	SOT407-3	98ASS23208W
144-pin LQFP	SOT486-2	98ASS23177W

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 42. Revision History

Rev. No.	Date	Substantial Changes
MCXEP144M112F70 v.2.0	15 July 2025	Initial release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

For more information, please visit: https://www.nxp.com

Date of release: July 2025 Document identifier: MCXEP144M112F70