19-2764; Rev 4; 7/05

EVALUATION KIT AVAILABLE

Low-Cost Multichemistry Battery Chargers

General Description

The MAX1908/MAX8724/MAX8765 highly integrated, multichemistry battery-charger control ICs simplify the construction of accurate and efficient chargers. These devices use analog inputs to control charge current and voltage, and can be programmed by the host or hardwired. The MAX1908/MAX8724/MAX8765 achieve high efficiency using a buck topology with synchronous rectification.

The MAX1908/MAX8724/MAX8765 feature input current limiting. This feature reduces battery charge current when the input current limit is reached to avoid overloading the AC adapter when supplying the load and the battery charger simultaneously. The MAX1908/MAX8724/MAX8765 provide outputs to monitor current drawn from the AC adapter (DC input source), battery-charging current, and the presence of an AC adapter. The MAX1908's conditioning charge feature provides 300mA to safely charge deeply discharged lithium-ion (Li+) battery packs.

The MAX1908 includes a conditioning charge feature while the MAX8724/MAX8765 do not.

The MAX1908/MAX8724/MAX8765 charge two to four series Li+ cells, providing more than 5A, and are available in a space-saving, 28-pin, thin QFN package (5mm × 5mm). An evaluation kit is available to speed designs.

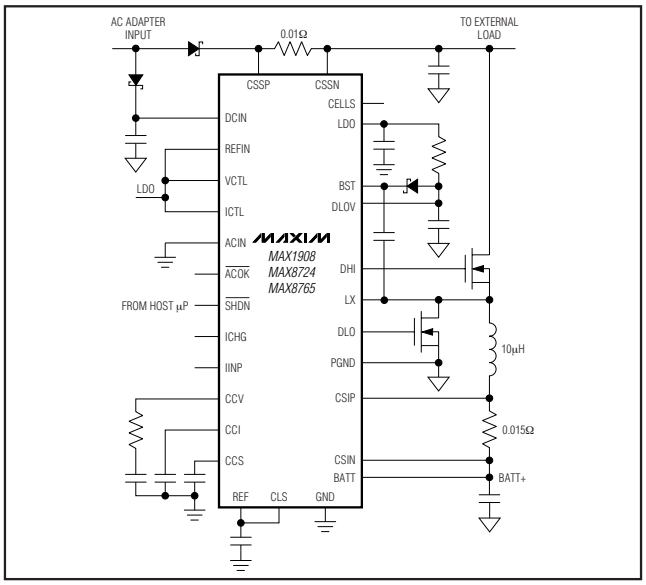
Applications

Notebook and Subnotebook Computers

Personal Digital Assistants

Handheld Terminals

Minimum Operating Circuit



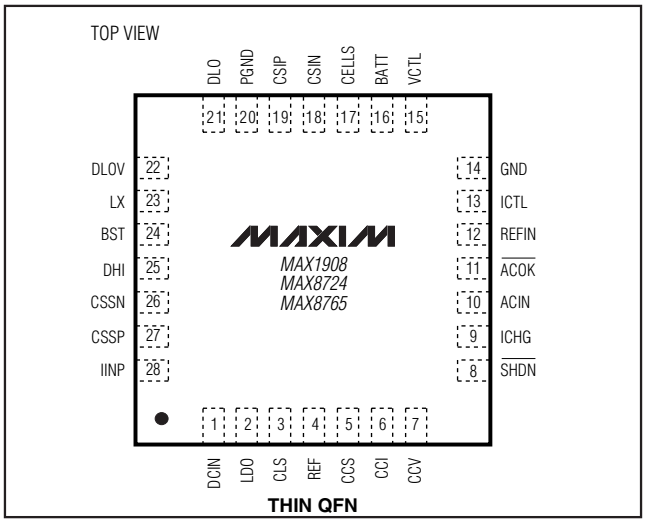
Features

- ±0.5% Output Voltage Accuracy Using Internal Reference (0°C to +85°C)
- ±4% Accurate Input Current Limiting
- ±5% Accurate Charge Current
- Analog Inputs Control Charge Current and Charge Voltage
- Outputs for Monitoring
  - Current Drawn from AC Adapter
  - Charging Current
  - AC Adapter Presence
- Up to 17.6V Battery-Voltage Set Point
- Maximum 28V Input Voltage
- > 95% Efficiency
- Shutdown Control Input
- Charge Any Battery Chemistry
  - Li+, NiCd, NiMH, Lead Acid, etc.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX1908ETI	-40°C to +85°C	28 Thin QFN	T2855-6
MAX8724ETI	-40°C to +85°C	28 Thin QFN	T2855-6
MAX8765ETI	-40°C to +85°C	28 Thin QFN	T2855-6

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

DCIN, CSSP, CSSN, $\overline{ACOK}$ to GND .....-0.3V to +30V
BST to GND .....-0.3V to +36V
BST to LX .....-0.3V to +6V
DHI to LX .....-0.3V to (V_{BST} + 0.3V)
LX to GND .....-6V to +30V
BATT, CSIP, CSIN to GND .....-0.3V to +20V
CSIP to CSIN or CSSP to CSSN or PGND to GND .....-0.3V to +0.3V
CCI, CCS, CCV, DLO, ICHG, IINP, ACIN, REF to GND .....-0.3V to (V_{LDO} + 0.3V)
DLOV, VCTL, ICTL, REFIN, CELLS, CLS, LDO, $\overline{SHDN}$ to GND .....-0.3V to +6V
DLOV to LDO .....-0.3V to +0.3V
DLO to PGND .....-0.3V to (V_{DLOV} + 0.3V)
LDO Short-Circuit Current 50mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN (5mm × 5mm)
(derate 20.8mW/°C above +70°C) 1666.7mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3V, V_{VCTL} = V_{ICTL} = 0.75 x V_{REFIN}, CELLS = float, CLS = REF, V_{BST} - V_{LX} = 4.5V, ACIN = GND = PGND = 0, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; CCI, CCS, and CCV are compensated per Figure 1a; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION						
Battery-Regulation Voltage Accuracy		V_{VCTL} = V_{REFIN} (2, 3, or 4 cells)	-0.5		+0.5	%
		V_{VCTL} = V_{REFIN} / 20 (2, 3, or 4 cells)	-0.5		+0.5	
		V_{VCTL} = V_{LDO} (2, 3, or 4 cells)	-0.5		+0.5	
VCTL Default Threshold		V_{VCTL} rising	4.0	4.1	4.2	V
REFIN Range		(Note 1)	2.5		3.6	V
REFIN Undervoltage Lockout		V_{REFIN} falling		1.20	1.92	V
CHARGE-CURRENT REGULATION						
CSIP-to-CSIN Full-Scale Current-Sense Voltage		V_{ICTL} = V_{REFIN}	71.25	75	78.75	mV
Charging-Current Accuracy		V_{ICTL} = V_{REFIN}	-5		+5	%
		V_{ICTL} = V_{REFIN} x 0.6	-5		+5	
		V_{ICTL} = V_{LDO}	-6		+6	
		MAX8765 only; V_{ICTL} = V_{REFIN} x 0.036	-45		+45	
		MAX8724 only; V_{ICTL} = V_{REFIN} x 0.058	-33		+33	
Charge-Current Gain Error (MAX8765 Only)			-2		+2	%
Charge-Current Offset (MAX8765 Only)			-2		+2	mV
ICTL Default Threshold		V_{ICTL} rising	4.0	4.1	4.2	V
BATT/CSIP/CSIN Input Voltage Range			0		19	V
CSIP/CSIN Input Current		V_{DCIN} = 0 or V_{ICTL} = 0 or $\overline{SHDN}$ = 0			1	µA
		Charging		400	650	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3V, V_{VCTL} = V_{ICTL} = 0.75 x V_{REFIN}, CELLS = float, CLS = REF, V_{BST} - V_{LX} = 4.5V, ACIN = GND = PGND = 0, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; CCI, CCS, and CCV are compensated per Figure 1a; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Cycle-by-Cycle Maximum Current Limit	I_{MAX}	RS2 = 0.015Ω		6.0	6.8	7.5	A
ICTL Power-Down Mode Threshold Voltage (MAX1908/MAX8724 Only)		V_{ICTL} rising		REFIN / 100	REFIN / 55	REFIN / 33	V
ICTL, VCTL Input Bias Current		V_{VCTL} = V_{ICTL} = 0 or 3V		-1		+1	µA
		V_{DCIN} = 0, V_{VCTL} = V_{ICTL} = V_{REFIN} = 5V		-1		+1	
REFIN Input Bias Current		V_{DCIN} = 5V, V_{REFIN} = 3V		-1		+1	µA
		V_{REFIN} = 5V		-1		+1	
ICHG Transconductance (MAX1908/MAX8724 Only)	G_{ICHG}	V_{CSIP} - V_{CSIN} = 45mV		2.7	3	3.3	µA/mV
ICHG Transconductance (MAX8765 Only)	G_{ICHG}	V_{CSIP} - V_{CSIN} = 45mV		2.85	3	3.15	µA/mV
ICHG Transconductance Error (MAX8765 Only)				-5		+5	%
ICHG Transconductance Offset (MAX8765 Only)				-5		+5	µA
ICHG Accuracy		V_{CSIP} - V_{CSIN} = 75mV		-6		+6	%
		V_{CSIP} - V_{CSIN} = 45mV		-5		+5	
		V_{CSIP} - V_{CSIN} = 5mV		-40		+40	
ICHG Output Current		V_{CSIP} - V_{CSIN} = 150mV, V_{ICHG} = 0		350			µA
ICHG Output Voltage		V_{CSIP} - V_{CSIN} = 150mV, ICHG = float		3.5			V
INPUT-CURRENT REGULATION							
CSSP-to-CSSN Full-Scale Current-Sense Voltage				72	75	78	mV
Input Current-Limit Accuracy		V_{CLS} = V_{REF}		-4		+4	%
		V_{CLS} = V_{REF} / 2		-7.5		+7.5	
		V_{CLS} = 1.1V (MAX8765 only)		-10		+10	
Input Current-Limit Gain Error (MAX8765 Only)				-2		+2	%
Input Current-Limit Offset (MAX8765 Only)				-2		+2	mV
CSSP, CSSN Input Voltage Range				8		28	V
CSSP, CSSN Input Current (MAX1908/MAX8724 Only)		V_{DCIN} = 0			0.1	1	µA
		V_{CSSP} = V_{CSSN} = V_{DCIN} > 8V			350	600	
CSSP Input Current (MAX8765 Only)		V_{CSSP} = V_{CSSN} = 28V	V_{DCIN} = 0V		0.1	1	µA
			V_{DCIN} = 28V		400	650	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3V, V_{VCTL} = V_{ICTL} = 0.75 x V_{REFIN}, CELLS = float, CLS = REF, V_{BST} - V_{LX} = 4.5V, ACIN = GND = PGND = 0, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; CCI, CCS, and CCV are compensated per Figure 1a; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CSSN Input Current (MAX8765 Only)		V_{CSSP} = V_{CSSN} = 28V	V_{DCIN} = 0		0.1	1	µA
			V_{DCIN} = 28V		0.1	1	
CLS Input Range (MAX1908/MAX8724 Only)				1.6		REF	V
CLS Input Range (MAX8765 Only)				1.1		REF	V
CLS Input Bias Current		V_{CLS} = 2V		-1		+1	µA
IINP Transconductance (MAX1908/MAX8724 Only)	G_{IINP}	V_{CSSP} - V_{CSSN} = 75mV		2.7	3	3.3	µA/mV
IINP Accuracy		V_{CSSP} - V_{CSSN} = 75mV		-5		+5	%
		V_{CSSP} - V_{CSSN} = 37.5mV		-7.5		+7.5	
IINP Transconductance (MAX8765 Only)	G_{IINP}	V_{CSSP} - V_{CCSN} = 75mV		2.82	3	3.18	µA/mV
IINP Transconductance Error (MAX8765 Only)				-6		+6	%
IINP Transconductance Offset (MAX8765 Only)				-10		+10	µA
IINP Output Current		V_{CSSP} - V_{CSSN} = 150mV, V_{IINP} = 0		350			µA
IINP Output Voltage		V_{CSSP} - V_{CSSN} = 150mV, V_{IINP} = float		3.5			V
SUPPLY AND LDO REGULATOR							
DCIN Input Voltage Range	V_{DCIN}			8		28	V
DCIN Undervoltage-Lockout Trip Point		V_{DCIN} falling		7	7.4		V
		V_{DCIN} rising			7.5	7.85	
DCIN Quiescent Current	I_{DCIN}	8.0V < V_{DCIN} < 28V			3.2	6	mA
BATT Input Current	I_{BATT}	V_{BATT} = 19V, V_{DCIN} = 0				1	µA
		V_{BATT} = 2V to 19V, V_{DCIN} = 19.3V			200	500	
LDO Output Voltage		8V < V_{DCIN} < 28V, no load		5.25	5.4	5.55	V
LDO Load Regulation		0 < I_{LDO} < 10mA			34	100	mV
LDO Undervoltage-Lockout Trip Point		V_{DCIN} = 8V		3.20	4	5.15	V
REFERENCE							
REF Output Voltage		0 < I_{REF} < 500µA		4.072	4.096	4.120	V
REF Undervoltage-Lockout Trip Point		V_{REF} falling			3.1	3.9	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3V, V_{VCTL} = V_{ICTL} = 0.75 x V_{REFIN}, CELLS = float, CLS = REF, V_{BST} - V_{LX} = 4.5V, ACIN = GND = PGND = 0, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; CCI, CCS, and CCV are compensated per Figure 1a; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRIP POINTS						
BATT Power-Fail Threshold		V_{DCIN} falling, referred to V_{CSIN} (MAX1908/MAX8724 only)	50	100	150	mV
		V_{CSSP} falling, referred to V_{CSIN} (MAX8765 only)	50	100	150	
BATT Power-Fail Threshold Hysteresis				200		mV
ACIN Threshold		ACIN rising (MAX8765 only)	2.028	2.048	2.068	V
		ACIN rising (MAX1908/MAX8724 only)	2.007	2.048	2.089	V
ACIN Threshold Hysteresis		0.5% of REF		20		mV
ACIN Input Bias Current		V_{ACIN} = 2.048V	-1		+1	µA
SWITCHING REGULATOR						
DHI Off-Time		V_{BATT} = 16V, V_{DCIN} = 19V, V_{CELLS} = V_{REFIN}	0.36	0.4	0.44	µs
DHI Minimum Off-Time		V_{BATT} = 16V, V_{DCIN} = 17V, V_{CELLS} = V_{REFIN}	0.24	0.28	0.33	µs
DHI Maximum On-Time			2.5	5	7.5	ms
DLOV Supply Current	I_{DLOV}	DLO low		5	10	µA
BST Supply Current	I_{BST}	DHI high		6	15	µA
BST Input Quiescent Current		V_{DCIN} = 0, V_{BST} = 24.5V, V_{BATT} = V_{LX} = 20V		0.3	1	µA
LX Input Bias Current		V_{DCIN} = 28V, V_{BATT} = V_{LX} = 20V		150	500	µA
LX Input Quiescent Current		V_{DCIN} = 0, V_{BATT} = V_{LX} = 20V		0.3	1	µA
DHI Maximum Duty Cycle			99	99.9		%
Minimum Discontinuous-Mode Ripple Current				0.5		A
Battery Undervoltage Charge Current		V_{BATT} = 3V per cell (RS2 = 15mΩ), MAX1908 only, V_{BATT} rising	150	300	450	mA
Battery Undervoltage Current Threshold		CELLS = GND, MAX1908 only, V_{BATT} rising	6.1	6.2	6.3	V
		CELLS = float, MAX1908 only, V_{BATT} rising	9.15	9.3	9.45	
		CELLS = V_{REFIN}, MAX1908 only, V_{BATT} rising	12.2	12.4	12.6	
DHI On-Resistance High		V_{BST} - V_{LX} = 4.5V, I_{DHI} = +100mA		4	7	Ω
DHI On-Resistance Low		V_{BST} - V_{LX} = 4.5V, I_{DHI} = -100mA		1	3.5	Ω
DLO On-Resistance High		V_{DLOV} = 4.5V, I_{DLO} = +100mA		4	7	Ω
DLO On-Resistance Low		V_{DLOV} = 4.5V, I_{DLO} = -100mA		1	3.5	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3V, V_{VCTL} = V_{ICTL} = 0.75 x V_{REFIN}, CELLS = float, CLS = REF, V_{BST} - V_{LX} = 4.5V, ACIN = GND = PGND = 0, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; CCI, CCS, and CCV are compensated per Figure 1a; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIERS						
GMV Amplifier Transconductance	GMV	V_{VCTL} = V_{LDO}, V_{BATT} = 16.8V, CELLS = V_{REFIN}	0.0625	0.125	0.2500	µA/mV
GMI Amplifier Transconductance	GMI	V_{ICTL} = V_{REFIN}, V_{CSIP} - V_{CSIN} = 75mV	0.5	1	2.0	µA/mV
GMS Amplifier Transconductance	GMS	V_{CLS} = V_{REF}, V_{CSSP} - V_{CSSN} = 75mV	0.5	1	2.0	µA/mV
CCI, CCS, CCV Clamp Voltage		0.25V < $V_{CCV,CCS,CCI}$ < 2V	150	300	600	mV
LOGIC LEVELS						
CELLS Input Low Voltage					0.4	V
CELLS Input Float Voltage		CELLS = float	(V_{REFIN} / 2) - 0.2V	V_{REFIN} / 2	(V_{REFIN} / 2) + 0.2V	V
CELLS Input High Voltage			V_{REFIN} - 0.4V			V
CELLS Input Bias Current		CELLS = 0 or V_{REFIN}	-2		+2	µA
$\overline{ACOK}$ AND $\overline{SHDN}$						
$\overline{ACOK}$ Input Voltage Range			0		28	V
$\overline{ACOK}$ Sink Current		$V_{\overline{ACOK}}$ = 0.4V, V_{ACIN} = 3V	1			mA
$\overline{ACOK}$ Leakage Current		$V_{\overline{ACOK}}$ = 28V, V_{ACIN} = 0			1	µA
$\overline{SHDN}$ Input Voltage Range			0		LDO	V
$\overline{SHDN}$ Input Bias Current		$V_{\overline{SHDN}}$ = 0 or V_{LDO}	-1		+1	µA
		V_{DCIN} = 0, $V_{\overline{SHDN}}$ = 5V	-1		+1	
$\overline{SHDN}$ Threshold		$V_{\overline{SHDN}}$ falling	22	23.5	25	% of V_{REFIN}
$\overline{SHDN}$ Threshold Hysteresis				1		% of V_{REFIN}

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3V, V_{VCTL} = V_{ICTL} = 0.75 x V_{REFIN}, CELLS = FLOAT, CLS = REF, V_{BST} - V_{LX} = 4.5V, ACIN = GND = PGND = 0, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; CCI, CCS, and CCV are compensated per Figure 1a; **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION						
Battery Regulation Voltage Accuracy		V_{VCTL} = V_{REFIN} (2, 3, or 4 cells)	-0.6		+0.6	%
		V_{VCTL} = V_{REFIN} / 20 (2, 3, or 4 cells)	-0.6		+0.6	
		V_{VCTL} = V_{LDO} (2, 3, or 4 cells)	-0.6		+0.6	
REFIN Range		(Note 1)	2.5		3.6	V
REFIN Undervoltage Lockout		V_{REFIN} falling			1.92	V
CHARGE CURRENT REGULATION						
CSIP-to-CSIN Full-Scale Current-Sense Voltage		V_{ICTL} = V_{REFIN}	70.5		79.5	mV
Charging-Current Accuracy		V_{ICTL} = V_{REFIN}	-6		+6	%
		V_{ICTL} = V_{REFIN} x 0.6	-7.5		+7.5	
		V_{ICTL} = V_{LDO}	-7.5		+7.5	
		MAX8765 only; V_{ICTL} = V_{REFIN} x 0.036	-50		+50	
		MAX8724 only; V_{ICTL} = V_{REFIN} x 0.058	-33		+33	
Charge-Current Gain Error (MAX8765 Only)			-2		+2	%
Charge-Current Offset (MAX8765 Only)			-2		+2	mV
BATT/CSIP/CSIN Input Voltage Range			0		19	V
CSIP/CSIN Input Current		V_{DCIN} = 0 or V_{ICTL} = 0 or $\overline{SHDN}$ = 0			1	µA
		Charging			650	
Cycle-by-Cycle Maximum Current Limit	I_{MAX}	RS2 = 0.015Ω	6.0		7.5	A
ICTL Power-Down Mode Threshold Voltage (MAX1908/MAX8724 Only)		V_{ICTL} rising	REFIN / 100		REFIN / 33	V
ICHG Transconductance (MAX1908/MAX8724 Only)	G_{ICHG}	V_{CSIP} - V_{CSIN} = 45mV	2.7		3.3	µA/mV
ICHG Transconductance (MAX8765 Only)	G_{ICHG}	V_{CSIP} - V_{CSIN} = 45mV	2.785		3.225	µA/mV
ICHG Transconductance Error (MAX8765 Only)			-7.5		+7.5	%
ICHG Transconductance Offset (MAX8765 Only)			-6.5		+6.5	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3V, V_{VCTL} = V_{ICTL} = 0.75 x V_{REFIN}, CELLS = FLOAT, CLS = REF, V_{BST} - V_{LX} = 4.5V, ACIN = GND = PGND = 0, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; CCI, CCS, and CCV are compensated per Figure 1a; **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ICHG Accuracy		V_{CSIP} - V_{CSIN} = 75mV		-7.5		+7.5	%
		V_{CSIP} - V_{CSIN} = 45mV		-7.5		+7.5	
		V_{CSIP} - V_{CSIN} = 5mV		-40		+40	
INPUT-CURRENT REGULATION							
CSSP-to-CSSN Full-Scale Current-Sense Voltage				71.25		78.75	mV
Input Current-Limit Accuracy		V_{CLS} = V_{REF}		-5		+5	%
		V_{CLS} = V_{REF} / 2		-7.5		+7.5	
		V_{CLS} = 1.1V (MAX8765 only)		-10		+10	
Input Current-Limit Gain Error (MAX8765 Only)				-2		+2	%
Input Current-Limit Offset (MAX8765 Only)				-2		+2	mV
CSSP, CSSN Input Voltage Range				8		28	V
CSSP, CSSN Input Current (MAX1908/MAX8724 Only)		V_{DCIN} = 0				1	µA
		V_{CSSP} = V_{CSSN} = V_{DCIN} > 8V				600	
CSSP Input Current (MAX8765 Only)		V_{CSSP} = V_{CSSN} = 28V	V_{DCIN} = 0V			1	µA
			V_{DCIN} = 28V			650	
CSSN Input Current (MAX8765 Only)		V_{CSSP} = V_{CSSN} = 28V	V_{DCIN} = 0V			1	µA
			V_{DCIN} = 28V			1	
CLS Input Range (MAX1908/MAX8724 Only)				1.6		REF	V
CLS Input Range (MAX8765 Only)				1.1		REF	V
IINP Transconductance (MAX1908/MAX8724 Only)	G_{IINP}	V_{CSSP} - V_{CSSN} = 75mV		2.7		3.3	µA/mV
IINP Transconductance (MAX8765 Only)	G_{IINP}	V_{CSSP} - V_{CCSN} = 75mV		2.785		3.225	µA/mV
IINP Transconductance Error (MAX8765 Only)				-7.5		+7.5	%
IINP Transconductance Offset (MAX8765 Only)				-12		+12	µA
IINP Accuracy		V_{CSSP} - V_{CSSN} = 75mV		-7.5		+7.5	%
		V_{CSSP} - V_{CSSN} = 37.5mV		-7.5		+7.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3V, V_{VCTL} = V_{ICTL} = 0.75 x V_{REFIN}, CELLS = FLOAT, CLS = REF, V_{BST} - V_{LX} = 4.5V, ACIN = GND = PGND = 0, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; CCI, CCS, and CCV are compensated per Figure 1a; **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND LDO REGULATOR						
DCIN Input Voltage Range	V_{DCIN}		8		28	V
DCIN Quiescent Current	I_{DCIN}	8V < V_{DCIN} < 28V			6	mA
BATT Input Current	I_{BATT}	V_{BATT} = 19V, V_{DCIN} = 0			1	µA
		V_{BATT} = 2V to 19V, V_{DCIN} = 19.3V			500	
LDO Output Voltage		8V < V_{DCIN} < 28V, no load	5.25		5.55	V
LDO Load Regulation		0 < I_{LDO} < 10mA			100	mV
REFERENCE						
REF Output Voltage		0 < I_{REF} < 500µA	4.065		4.120	V
TRIP POINTS						
BATT Power-Fail Threshold		V_{DCIN} falling, referred to V_{CSIN} (MAX1908/MAX8724 only)	50		150	mV
		V_{CSSP} falling, referred to V_{CSIN} (MAX8765 only)	50		150	
ACIN Threshold		ACIN rising (MAX8765 only)	2.028		2.068	V
		ACIN rising (MAX1908/MAX8724 only)	2.007		2.089	
SWITCHING REGULATOR						
DHI Off-Time		V_{BATT} = 16V, V_{DCIN} = 19V, V_{CELLS} = V_{REFIN}	0.35		0.45	µs
DHI Minimum Off-Time		V_{BATT} = 16V, V_{DCIN} = 17V, V_{CELLS} = V_{REFIN}	0.24		0.33	µs
DHI Maximum On-Time			2.5		7.5	ms
DHI Maximum Duty Cycle			99			%
Battery Undervoltage Charge Current		V_{BATT} = 3V per cell (RS2 = 15mΩ), MAX1908 only, V_{BATT} rising	150		450	mA
Battery Undervoltage Current Threshold		CELLS = GND, MAX1908 only, V_{BATT} rising	6.09		6.30	V
		CELLS = float, MAX1908 only, V_{BATT} rising	9.12		9.45	
		CELLS = V_{REFIN}, MAX1908 only, V_{BATT} rising	12.18		12.60	
DHI On-Resistance High		V_{BST} - V_{LX} = 4.5V, I_{DHI} = +100mA			7	Ω
DHI On-Resistance Low		V_{BST} - V_{LX} = 4.5V, I_{DHI} = -100mA			3.5	Ω
DLO On-Resistance High		V_{DLOV} = 4.5V, I_{DLO} = +100mA			7	Ω
DLO On-Resistance Low		V_{DLOV} = 4.5V, I_{DLO} = -100mA			3.5	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12V, V_{REFIN} = 3V, V_{VCTL} = V_{ICTL} = 0.75 x V_{REFIN}, CELLS = FLOAT, CLS = REF, V_{BST} - V_{LX} = 4.5V, ACIN = GND = PGND = 0, C_{LDO} = 1µF, LDO = DLOV, C_{REF} = 1µF; CCI, CCS, and CCV are compensated per Figure 1a; **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

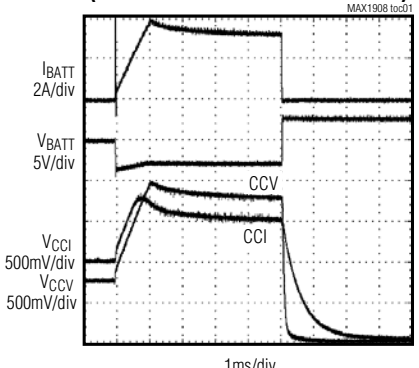
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIERS						
GMV Amplifier Transconductance	GMV	V_{VCTL} = V_{LDO}, V_{BATT} = 16.8V, CELLS = V_{REFIN}	0.0625		0.250	µA/mV
GMI Amplifier Transconductance	GMI	V_{ICTL} = V_{REFIN}, V_{CSIP} - V_{CSIN} = 75mV	0.5		2.0	µA/mV
GMS Amplifier Transconductance	GMS	V_{CLS} = V_{REF}, V_{CSSP} - V_{CSSN} = 75mV	0.5		2.0	µA/mV
CCI, CCS, CCV Clamp Voltage		0.25V < $V_{CCV,CCS,CCI}$ < 2V	150		600	mV
LOGIC LEVELS						
CELLS Input Low Voltage					0.4	V
CELLS Input Float Voltage		CELLS = float	(V_{REFIN} / 2) - 0.2V		(V_{REFIN} / 2) + 0.2V	V
CELLS Input High Voltage			V_{REFIN} - 0.4V			V
$\overline{ACOK}$ AND $\overline{SHDN}$						
$\overline{ACOK}$ Input Voltage Range			0		28	V
$\overline{ACOK}$ Sink Current		$V_{\overline{ACOK}}$ = 0.4V, V_{ACIN} = 3V	1			mA
$\overline{SHDN}$ Input Voltage Range			0		LDO	V
$\overline{SHDN}$ Threshold		$V_{\overline{SHDN}}$ falling	22		25	% of V_{REFIN}

Note 1: If both ICTL and VCTL use default mode (connected to LDO), REFIN is not used and can be connected to LDO.
Note 2: Specifications to -40°C are guaranteed by design and not production tested.

Typical Operating Characteristics

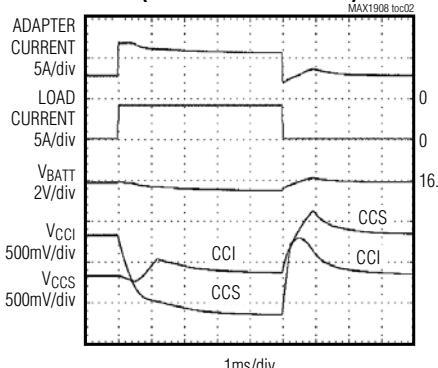
(Circuit of Figure 1, V_{DCIN} = 20V, T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE (BATTERY INSERTION AND REMOVAL)



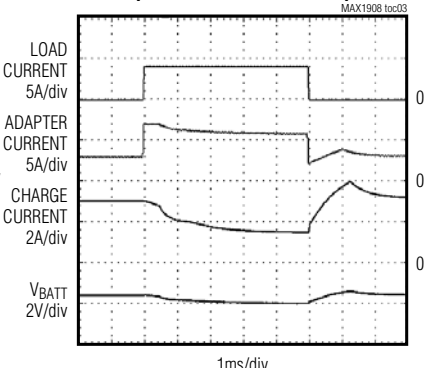
ICTL = LDO
VCTL = LDO

LOAD-TRANSIENT RESPONSE (STEP IN-LOAD CURRENT)



ICTL = LDO
CHARGING CURRENT = 3A
V_{BATT} = 16.8V
LOAD STEP = 0 TO 4A
I_{SOURCE} LIMIT = 5A

LOAD-TRANSIENT RESPONSE (STEP IN-LOAD CURRENT)

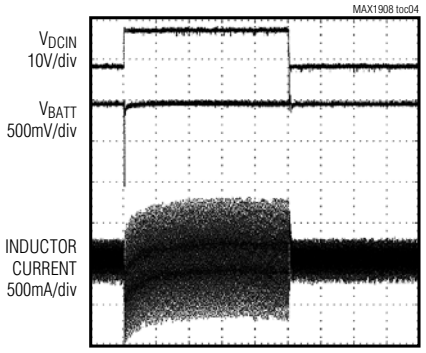


ICTL = LDO
CHARGING CURRENT = 3A
V_{BATT} = 16.8V
LOAD STEP = 0 TO 4A
I_{SOURCE} LIMIT = 5A

Typical Operating Characteristics (continued)

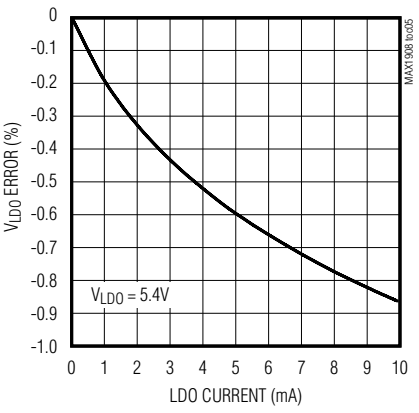
(Circuit of Figure 1, V_{DCIN} = 20V, T_A = +25°C, unless otherwise noted.)

LINE-TRANSIENT RESPONSE

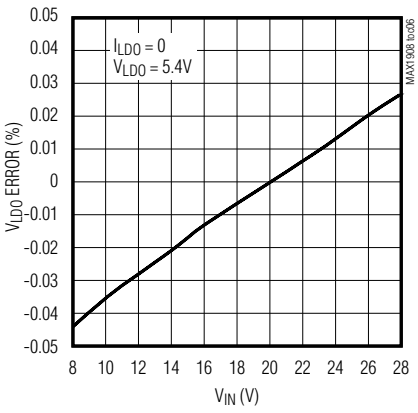


ICTL = LDO
VCTL = LDO
I_{CHARGE} = 3A
LINE STEP 18.5V TO 27.5V

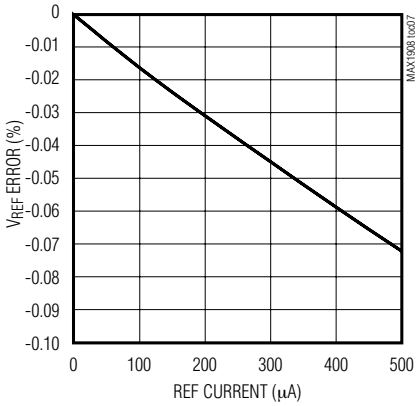
LDO LOAD REGULATION



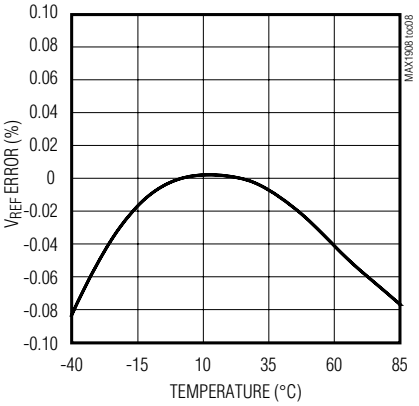
LDO LINE REGULATION



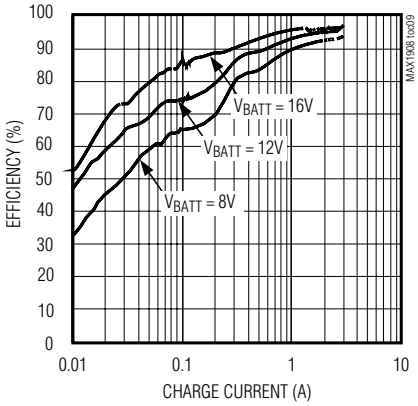
REF VOLTAGE LOAD REGULATION



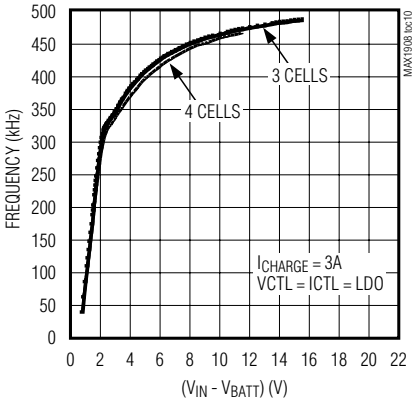
REF VOLTAGE ERROR vs. TEMPERATURE



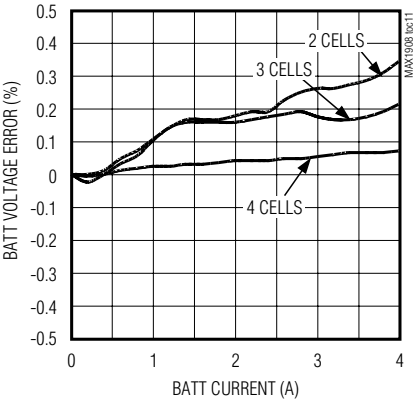
EFFICIENCY vs. CHARGE CURRENT



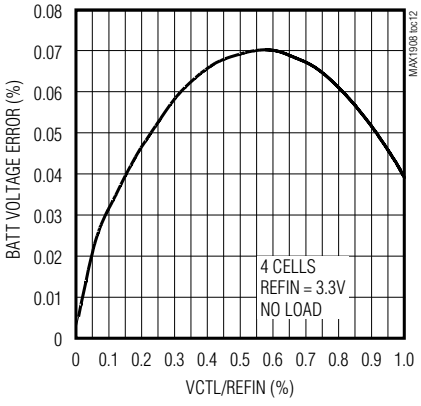
FREQUENCY vs. V_{IN} - V_{BATT}



OUTPUT V/I CHARACTERISTICS



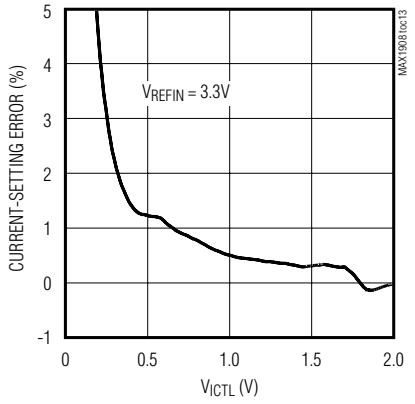
BATT VOLTAGE ERROR vs. VCTL



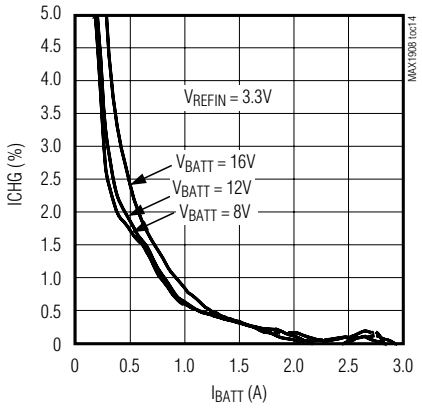
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DCIN} = 20V, T_A = +25°C, unless otherwise noted.)

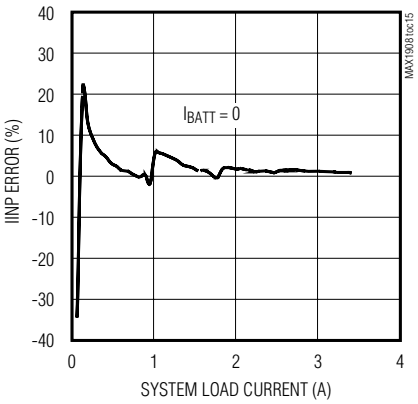
CURRENT-SETTING ERROR vs. ICTL



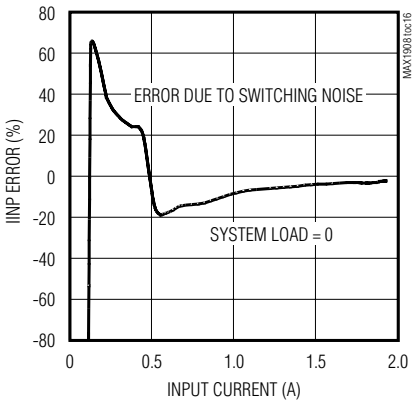
ICHG ERROR vs. CHARGE CURRENT



IINP ERROR vs. SYSTEM LOAD CURRENT



IINP ERROR vs. INPUT CURRENT



Pin Description

PIN	NAME	FUNCTION
1	DCIN	Charging Voltage Input. Bypass DCIN with a 1µF capacitor to PGND.
2	LDO	Device Power Supply. Output of the 5.4V linear regulator supplied from DCIN. Bypass with a 1µF capacitor to GND.
3	CLS	Source Current-Limit Input. Voltage input for setting the current limit of the input source.
4	REF	4.096V Voltage Reference. Bypass REF with a 1µF capacitor to GND.
5	CCS	Input-Current Regulation Loop-Compensation Point. Connect a 0.01µF capacitor to GND.
6	CCI	Output-Current Regulation Loop-Compensation Point. Connect a 0.01µF capacitor to GND.
7	CCV	Voltage Regulation Loop-Compensation Point. Connect 1kΩ in series with a 0.1µF capacitor to GND.
8	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ logic low to shut down the MAX1908/MAX8724/MAX8765. Use with a thermistor to detect a hot battery and suspend charging.
9	ICHG	Charge-Current Monitor Output. ICHG is a scaled-down replica of the charger output current. Use ICHG to monitor the charging current and detect when the chip changes from constant-current mode to constant-voltage mode. The transconductance of (CSIP - CSIN) to ICHG is 3µA/mV.
10	ACIN	AC Detect Input. Input to an uncommitted comparator. ACIN can be used to detect AC-adapter presence.
11	$\overline{ACOK}$	AC Detect Output. High-voltage open-drain output is high impedance when V_{ACIN} is less than V_{REF} / 2.
12	REFIN	Reference Input. Allows the ICTL and VCTL inputs to have ratiometric ranges for increased accuracy.
13	ICTL	Output Current-Limit Set Input. ICTL input voltage range is V_{REFIN} / 32 to V_{REFIN}. The MAX1908/MAX8724 shut down if ICTL is forced below V_{REFIN} / 100 while the MAX8765 does not. When ICTL is equal to LDO, the set point for CSIP - CSIN is 45mV.
14	GND	Analog Ground
15	VCTL	Output Voltage-Limit Set Input. VCTL input voltage range is 0 to V_{REFIN}. When VCTL is equal to LDO, the set point is (4.2 x CELLS)V.
16	BATT	Battery Voltage Input
17	CELLS	Cell Count Input. Tri-level input for setting number of cells. GND = 2 cells, float = 3 cells, REFIN = 4 cells.
18	CSIN	Output Current-Sense Negative Input
19	CSIP	Output Current-Sense Positive Input. Connect a current-sense resistor from CSIP to CSIN.
20	PGND	Power Ground
21	DLO	Low-Side Power MOSFET Driver Output. Connect to low-side nMOS gate.
22	DLOV	Low-Side Driver Supply. Bypass DLOV with a 1µF capacitor to GND.
23	LX	High-Side Power MOSFET Driver Power-Return Connection. Connect to the source of the high-side nMOS.
24	BST	High-Side Power MOSFET Driver Power-Supply Connection. Connect a 0.1µF capacitor from LX to BST.
25	DHI	High-Side Power MOSFET Driver Output. Connect to high-side nMOS gate.
26	CSSN	Input Current-Sense Negative Input
27	CSSP	Input Current-Sense Positive Input. Connect a current-sense resistor from CSSP to CSSN.
28	IINP	Input-Current Monitor Output. IINP is a scaled-down replica of the input current. IINP monitors the total system current. The transconductance of (CSSP - CSSN) to IINP is 3µA/mV.

Detailed Description

The MAX1908/MAX8724/MAX8765 include all the functions necessary to charge Li+ batteries. A high-efficiency synchronous-rectified step-down DC-DC converter controls charging voltage and current. The device also includes input-source current limiting and analog inputs for setting the charge current and charge voltage. Control charge current and voltage using the ICTL and VCTL inputs, respectively. Both ICTL and VCTL are ratiometric with respect to REFIN, allowing compatibility with DACs or microcontrollers (µCs). Ratiometric ICTL and VCTL improve the accuracy of the charge current and voltage set point by matching V_{REFIN} to the reference of the host. For standard applications, internal set points for ICTL and VCTL provide 3A charge current (with 0.015Ω sense resistor), and 4.2V (per cell) charge voltage. Connect ICTL and VCTL to LDO to select the internal set points. The MAX1908 safely conditions overdischarged cells with 300mA (with 0.015Ω sense resistor) until the battery-pack voltage exceeds 3.1V × number of series-connected cells. The $\overline{SHDN}$ input allows shutdown from a microcontroller or thermistor.

The DC-DC converter uses external n-channel MOSFETs as the buck switch and synchronous rectifier to convert the input voltage to the required charging current and voltage. The *Typical Application Circuit* shown in Figure 1 uses a µC to control charging current, while Figure 2 shows a typical application with charging voltage and current fixed to specific values for the application. The voltage at ICTL and the value of RS2 set the charging current. The DC-DC converter generates the control signals for the external MOSFETs to regulate the voltage and the current set by the VCTL, ICTL, and CELLS inputs.

The MAX1908/MAX8724/MAX8765 feature a voltage regulation loop (CCV) and two current regulation loops (CCI and CCS). The CCV voltage regulation loop monitors BATT to ensure that its voltage does not exceed the voltage set by VCTL. The CCI battery current regulation loop monitors current delivered to BATT to ensure that it does not exceed the current limit set by ICTL. A third loop (CCS) takes control and reduces the battery-charging current when the sum of the system load and the battery-charging input current exceeds the input current limit set by CLS.

Setting the Battery-Regulation Voltage

The MAX1908/MAX8724/MAX8765 use a high-accuracy voltage regulator for charging voltage. The VCTL input adjusts the charger output voltage. VCTL control voltage can vary from 0 to V_{REFIN}, providing a 10% adjustment range on the V_{BATT} regulation voltage. By limiting the adjust range to 10% of the regulation voltage, the external resistor mismatch error is reduced from 1% to 0.05% of the regulation voltage. Therefore, an overall voltage accuracy of better than 0.7% is maintained while using 1% resistors. The per-cell battery termination voltage is a function of the battery chemistry. Consult the battery manufacturer to determine this voltage. Connect VCTL to LDO to select the internal default setting V_{BATT} = 4.2V × number of cells, or program the battery voltage with the following equation:

$$V_{BATT} = CELLS \times \left(4V + \left(0.4 \times \frac{V_{VCTL}}{V_{REFIN}}\right)\right)$$

CELLS is the programming input for selecting cell count. Connect CELLS as shown in Table 2 to charge 2, 3, or 4 Li+ cells. When charging other cell chemistries, use CELLS to select an output voltage range for the charger.

The internal error amplifier (GMV) maintains voltage regulation (Figure 3). The voltage error amplifier is compensated at CCV. The component values shown in Figures 1 and 2 provide suitable performance for most applications. Individual compensation of the voltage regulation and current regulation loops allows for optimal compensation (see the *Compensation* section).

Table 1. Versions Comparison

DESCRIPTION	MAX1908	MAX8724	MAX8765
Conditioning Charge Feature	Yes	No	No
ICTL Shutdown Mode	Yes	Yes	No
$\overline{ACOK}$ Enable Condition	REFIN must be ready	REFIN must be ready	Independent of REFIN

Table 2. Cell-Count Programming

CELLS	CELL COUNT
GND	2
Float	3
V_{REFIN}	4

Typical Application Circuits

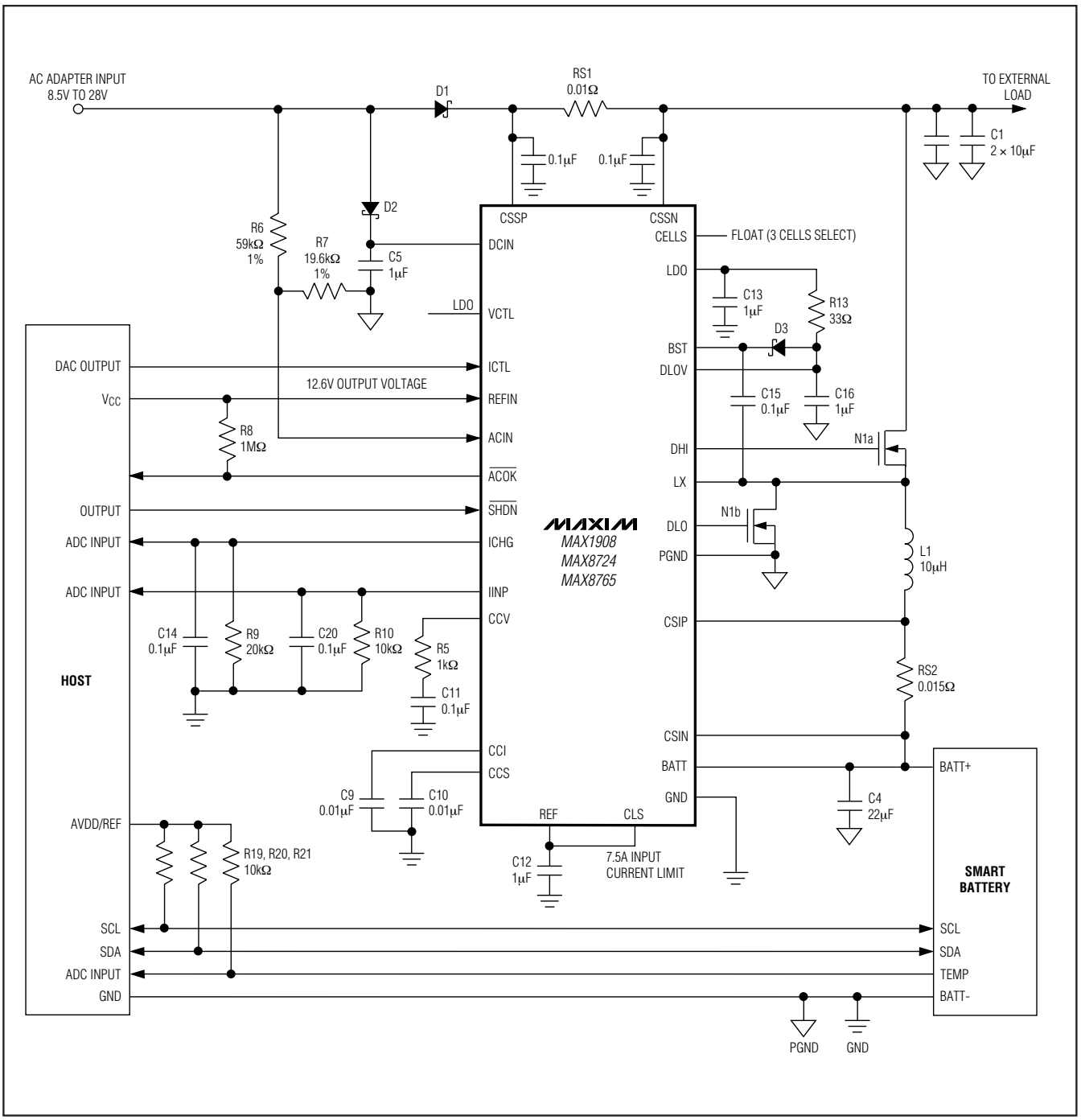


Figure 1. µC-Controlled Typical Application Circuit

Typical Application Circuits (continued)

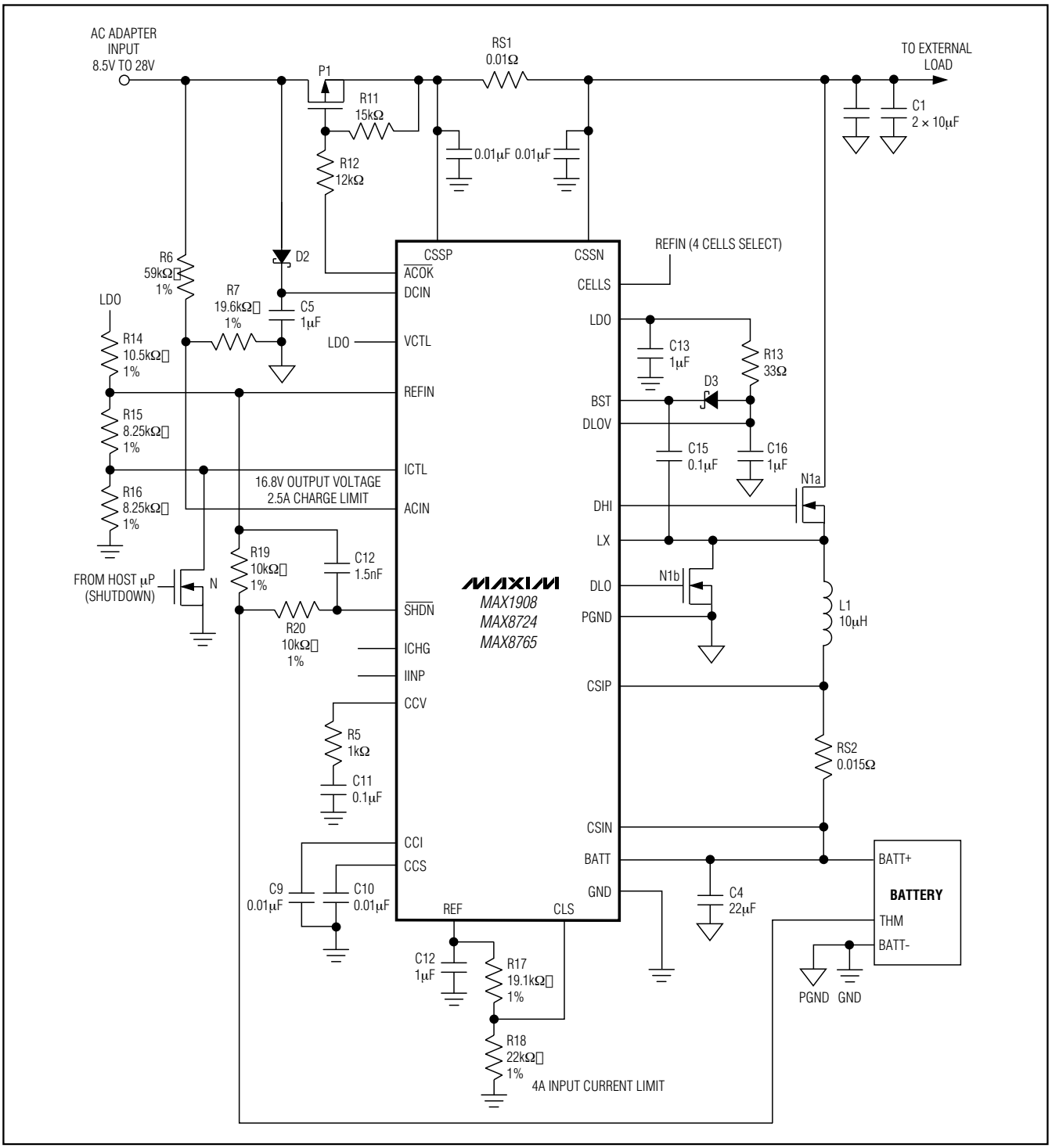


Figure 2. Typical Application Circuit with Fixed Charging Parameters

Functional Diagram

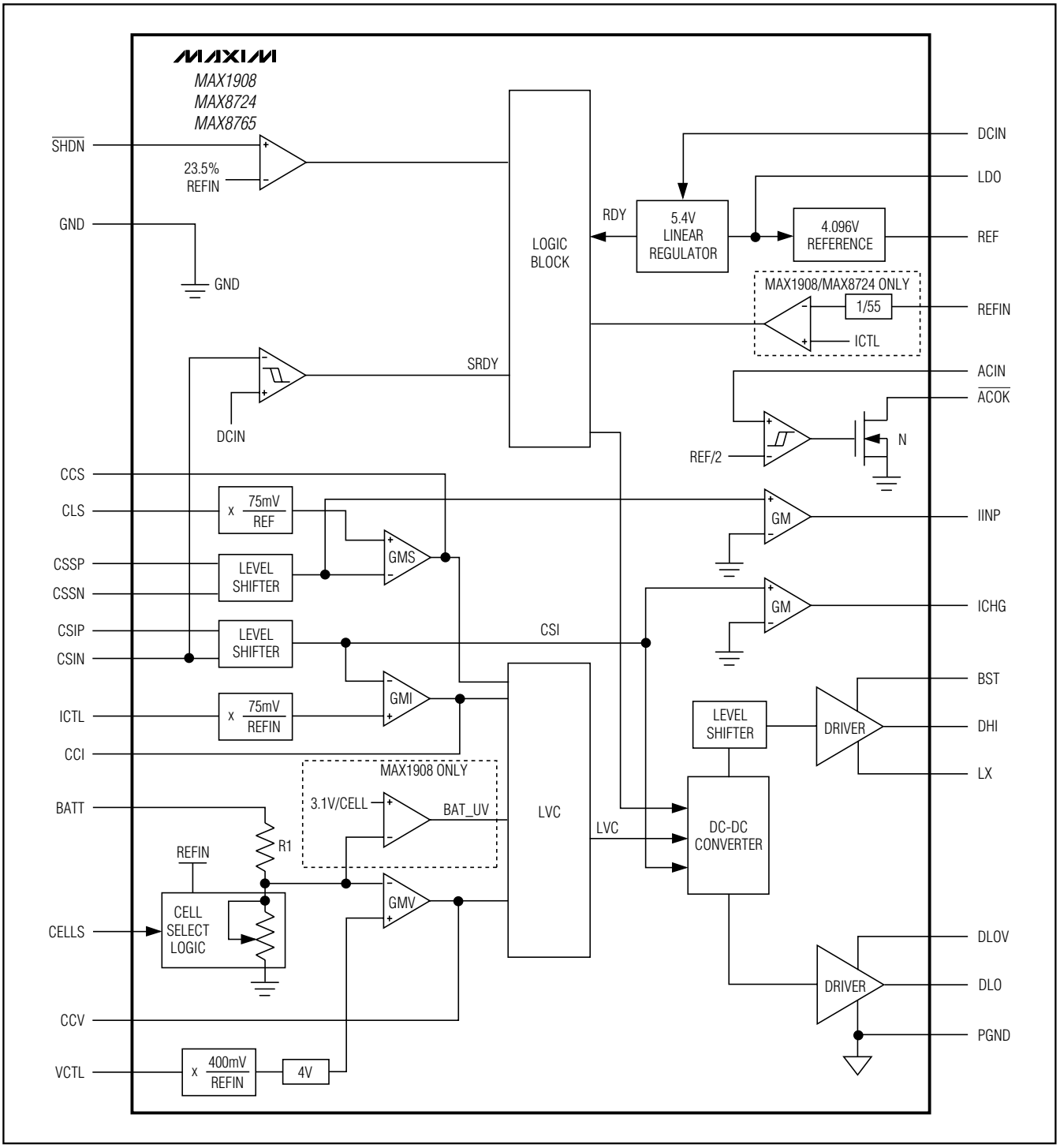


Figure 3. Functional Diagram

Setting the Charging-Current Limit

The ICTL input sets the maximum charging current. The current is set by current-sense resistor RS2, connected between CSIP and CSIN. The full-scale differential voltage between CSIP and CSIN is 75mV; thus, for a 0.015Ω sense resistor, the maximum charging current is 5A. Battery-charging current is programmed with ICTL using the equation:

$$I_{CHG} = \frac{V_{ICTL}}{V_{REFIN}} \times \frac{0.075}{RS2}$$

The input voltage range for ICTL is V_{REFIN} / 32 to V_{REFIN}. The MAX1908/MAX8724 shut down if ICTL is forced below V_{REFIN} / 100 (min), while the MAX8765 does not.

Connect ICTL to LDO to select the internal default full-scale, charge-current sense voltage of 45mV. The charge current when ICTL = LDO is:

$$I_{CHG} = \frac{0.045V}{RS2}$$

where RS2 is 0.015Ω, providing a charge-current set point of 3A.

The current at the ICHG output is a scaled-down replica of the battery output current being sensed across CSIP and CSIN (see the *Current Measurement* section).

When choosing the current-sense resistor, note that the voltage drop across this resistor causes further power loss, reducing efficiency. However, adjusting ICTL to reduce the voltage across the current-sense resistor can degrade accuracy due to the smaller signal to the input of the current-sense amplifier. The charging-current-error amplifier (GMI) is compensated at CCI (see the *Compensation* section).

Setting the Input Current Limit

The total input current (from an AC adapter or other DC source) is a function of the system supply current and the battery-charging current. The input current regulator limits the input current by reducing the charging current when the input current exceeds the input current-limit set point. System current normally fluctuates as portions of the system are powered up or down. Without input current regulation, the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using the input current limiter, the current capability of the AC adapter can be lowered, reducing system cost.

The MAX1908/MAX8724/MAX8765 limit the battery charge current when the input current-limit threshold is exceeded, ensuring the battery charger does not load down the AC adapter voltage. An internal amplifier compares the voltage between CSSP and CSSN to the voltage at CLS. V_{CLS} can be set by a resistive divider between REF and GND. Connect CLS to REF for the full-scale input current limit. The CLS voltage range for the MAX1908/MAX8724 is from 1.6V to REF, while the MAX8765 CLS voltage is from 1.1V to REF.

The input current is the sum of the device current, the charger input current, and the load current. The device current is minimal (3.8mA) in comparison to the charge and load currents. Determine the actual input current required as follows:

$$I_{INPUT} = I_{LOAD} + \left(\frac{I_{CHG} \times V_{BATT}}{V_{IN} \times \eta} \right)$$

where η is the efficiency of the DC-DC converter.

V_{CLS} determines the reference voltage of the GMS error amplifier. Sense resistor RS1 and V_{CLS} determine the maximum allowable input current. Calculate the input current limit as follows:

$$I_{INPUT} = \frac{V_{CLS}}{V_{REF}} \times \frac{0.075}{RS1}$$

Once the input current limit is reached, the charging current is reduced until the input current is at the desired threshold.

When choosing the current-sense resistor, note that the voltage drop across this resistor causes further power loss, reducing efficiency. Choose the smallest value for RS1 that achieves the accuracy requirement for the input current-limit set point.

Conditioning Charge

The MAX1908 includes a battery-voltage comparator that allows a conditioning charge of overdischarged Li+ battery packs. If the battery-pack voltage is less than 3.1V × number of cells programmed by CELLS, the MAX1908 charges the battery with 300mA current when using sense resistor RS2 = 0.015Ω. After the battery voltage exceeds the conditioning charge threshold, the MAX1908 resumes full-charge mode, charging to the programmed voltage and current limits. The MAX8724/MAX8765 do not offer this feature.

AC Adapter Detection

Connect the AC adapter voltage through a resistive divider to ACIN to detect when AC power is available, as shown in Figure 1. ACIN voltage rising trip point is V_{REF} / 2 with 20mV hysteresis. $\overline{ACOK}$ is an open-drain output and is high impedance when ACIN is less than V_{REF} / 2. Since $\overline{ACOK}$ can withstand 30V (max), $\overline{ACOK}$

can drive a p-channel MOSFET directly at the charger input, providing a lower dropout voltage than a Schottky diode (Figure 2). In the MAX1908/MAX8724 the $\overline{ACOK}$ comparator is enabled after REFIN is ready. In the MAX8765, the $\overline{ACOK}$ comparator is independent of REFIN.

Current Measurement

Use ICHG to monitor the battery-charging current being sensed across CSIP and CSIN. The ICHG voltage is proportional to the output current by the equation:

$$V_{ICHG} = ICHG \times RS2 \times G_{ICHG} \times R9$$

where I_{CHG} is the battery-charging current, G_{ICHG} is the transconductance of ICHG (3µA/mV typ), and R9 is the resistor connected between ICHG and ground. Leave ICHG unconnected if not used.

Use IINP to monitor the system input current being sensed across CSSP and CSSN. The voltage of IINP is proportional to the input current by the equation:

$$V_{IINP} = I_{INPUT} \times RS1 \times G_{IINP} \times R10$$

where I_{INPUT} is the DC current being supplied by the AC adapter power, G_{IINP} is the transconductance of IINP (3µA/mV typ), and R10 is the resistor connected between IINP and ground. ICHG and IINP have a 0 to 3.5V output voltage range. Leave IINP unconnected if not used.

LDO Regulator

LDO provides a 5.4V supply derived from DCIN and can deliver up to 10mA of load current. The MOSFET drivers are powered by DLOV and BST, which must be connected to LDO as shown in Figure 1. LDO supplies the 4.096V reference (REF) and most of the control circuitry. Bypass LDO with a 1µF capacitor to GND.

Shutdown

The MAX1908/MAX8724/MAX8765 feature a low-power shutdown mode. Driving $\overline{SHDN}$ low shuts down the MAX1908/MAX8724/MAX8765. In shutdown, the DC-DC converter is disabled and CCI, CCS, and CCV are pulled to ground. The IINP and $\overline{ACOK}$ outputs continue to function.

$\overline{SHDN}$ can be driven by a thermistor to allow automatic shutdown of the MAX1908/MAX8724/MAX8765 when the battery pack is hot. The shutdown falling threshold is 23.5% (typ) of V_{REFIN} with 1% V_{REFIN} hysteresis to provide smooth shutdown when driven by a thermistor.

DC-DC Converter

The MAX1908/MAX8724/MAX8765 employ a buck regulator with a bootstrapped nMOS high-side switch and a low-side nMOS synchronous rectifier.

CCV, CCI, CCS, and LVC Control Blocks

The MAX1908/MAX8724/MAX8765 control input current (CCS control loop), charge current (CCI control loop), or charge voltage (CCV control loop), depending on the operating condition.

The three control loops, CCV, CCI, and CCS are brought together internally at the LVC amplifier (lowest voltage clamp). The output of the LVC amplifier is the feedback control signal for the DC-DC controller. The output of the G_M amplifier that is the lowest sets the output of the LVC amplifier and also clamps the other two control loops to within 0.3V above the control point. Clamping the other two control loops close to the lowest control loop ensures fast transition with minimal overshoot when switching between different control loops.

DC-DC Controller

The MAX1908/MAX8724/MAX8765 feature a variable off-time, cycle-by-cycle current-mode control scheme. Depending upon the conditions, the MAX1908/MAX8724/MAX8765 work in continuous or discontinuous-conduction mode.

Continuous-Conduction Mode

With sufficient charger loading, the MAX1908/MAX8724/MAX8765 operate in continuous-conduction mode (inductor current never reaches zero) switching at 400kHz if the BATT voltage is within the following range:

$$3.1V \times (\text{number of cells}) < V_{BATT} < (0.88 \times V_{DCIN})$$

The operation of the DC-DC controller is controlled by the following four comparators as shown in Figure 4:

- **IMIN**—Compares the control point (LVC) against 0.15V (typ). If IMIN output is low, then a new cycle cannot begin.
- **CCMP**—Compares the control point (LVC) against the charging current (CSI). The high-side MOSFET on-time is terminated if the CCMP output is high.
- **IMAX**—Compares the charging current (CSI) to 6A (RS2 = 0.015Ω). The high-side MOSFET on-time is terminated if the IMAX output is high and a new cycle cannot begin until IMAX goes low.
- **ZCMP**—Compares the charging current (CSI) to 333mA (RS2 = 0.015Ω). If ZCMP output is high, then both MOSFETs are turned off.

DC-DC Functional Diagram

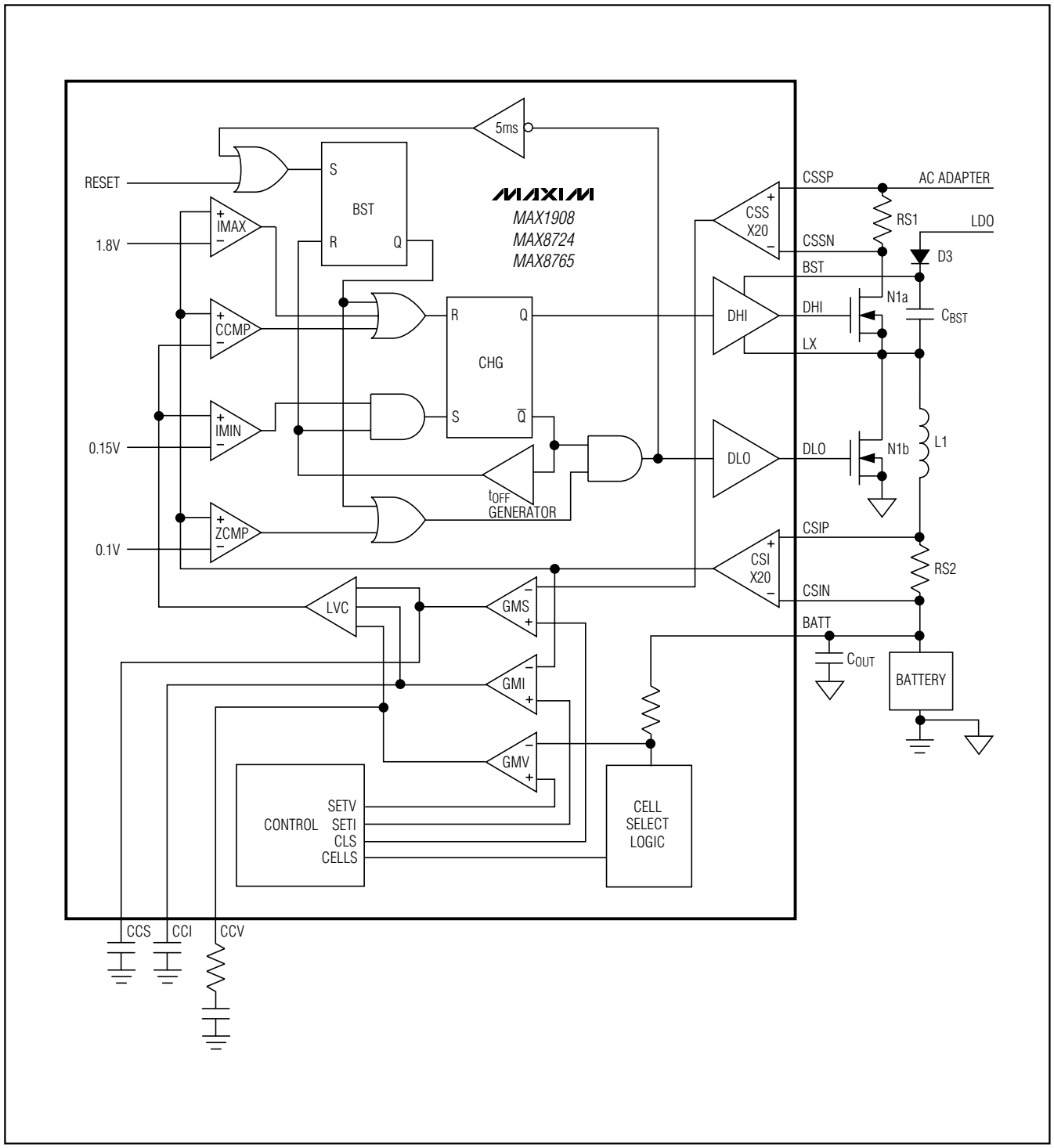


Figure 4. DC-DC Functional Diagram

In normal operation, the controller starts a new cycle by turning on the high-side n-channel MOSFET and turning off the low-side n-channel MOSFET. When the charge current is greater than the control point (LVC), CCMP goes high and the off-time is started. The off-time turns off the high-side n-channel MOSFET and turns on the low-side n-channel MOSFET. The operational frequency is governed by the off-time and is dependent upon V_{DCIN} and V_{BATT}. The off-time is set by the following equations:

$$t_{OFF} = 2.5\mu s \times \frac{V_{DCIN} - V_{BATT}}{V_{DCIN}}$$

$$t_{ON} = \frac{L \times I_{RIPPLE}}{V_{CSSN} - V_{BATT}}$$

where:

$$I_{RIPPLE} = \frac{V_{BATT} \times t_{OFF}}{L}$$

$$f = \frac{1}{t_{ON} + t_{OFF}}$$

These equations result in fixed-frequency operation over the most common operating conditions.

At the end of the fixed off-time, another cycle begins if the control point (LVC) is greater than 0.15V, IMIN = high, and the peak charge current is less than 6A (RS2 = 0.015Ω), IMAX = high. If the charge current exceeds IMAX, the on-time is terminated by the IMAX comparator. IMAX governs the maximum cycle-by-cycle current limit and is internally set to 6A (RS2 = 0.015Ω). IMAX protects against sudden overcurrent faults.

If, during the off-time, the inductor current goes to zero, ZCMP = high, both the high- and low-side MOSFETs are turned off until another cycle is ready to begin.

There is a minimum 0.3µs off-time when the (V_{DCIN} - V_{BATT}) differential becomes too small. If $V_{BATT} \geq 0.88 \times V_{DCIN}$, then the threshold for minimum off-time is reached and the t_{OFF} is fixed at 0.3µs. A maximum on-time of 5ms allows the controller to achieve > 99% duty cycle in continuous-conduction mode. The switching frequency in this mode varies according to the equation:

$$f = \frac{1}{\frac{L \times I_{RIPPLE}}{(V_{CSSN} - V_{BATT})} + 0.3\mu s}$$

Discontinuous Conduction

The MAX1908/MAX8724/MAX8765 enter discontinuous-conduction mode when the output of the LVC control point falls below 0.15V. For RS2 = 0.015Ω, this corresponds to 0.5A:

$$IMIN = \frac{0.15V}{20 \times RS2} = 0.5A$$

for RS2 = 0.015Ω.

In discontinuous mode, a new cycle is not started until the LVC voltage rises above 0.15V. Discontinuous-mode operation can occur during conditioning charge of overdischarged battery packs, when the charge current has been reduced sufficiently by the CCS control loop, or when the battery pack is near full charge (constant-voltage-charging mode).

MOSFET Drivers

The low-side driver output DLO switches between PGND and DLOV. DLOV is usually connected through a filter to LDO. The high-side driver output DHI is bootstrapped off LX and switches between V_{LX} and V_{BST}. When the low-side driver turns on, BST rises to one diode voltage below DLOV.

Filter DLOV with a lowpass filter whose cutoff frequency is approximately 5kHz (Figure 1):

$$f_C = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 33\Omega \times 1\mu F} = 4.8kHz$$

Dropout Operation

The MAX1908/MAX8724/MAX8765 have 99% duty-cycle capability with a 5ms (max) on-time and 0.3µs (min) off-time. This allows the charger to achieve dropout performance limited only by resistive losses in the DC-DC converter components (D1, N1, RS1, and RS2, Figure 1). Replacing diode D1 with a p-channel MOSFET driven by $\overline{ACOK}$ improves dropout performance (Figure 2). The dropout voltage is set by the difference between DCIN and CSIN. When the dropout voltage falls below 100mV, the charger is disabled; 200mV hysteresis ensures that the charger does not turn back on until the dropout voltage rises to 300mV.

Compensation

Each of the three regulation loops—input current limit, charging current limit, and charging voltage limit—are compensated separately using CCS, CCI, and CCV, respectively.

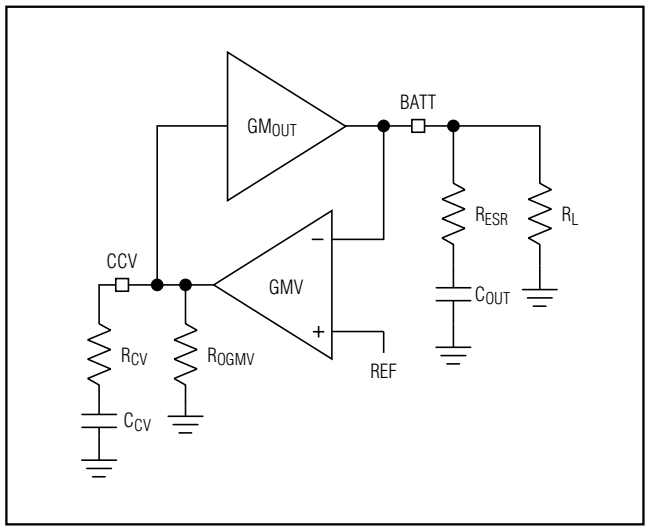


Figure 5. CCV Loop Diagram

CCV Loop Definitions

Compensation of the CCV loop depends on the parameters and components shown in Figure 5. C_{CV} and R_{CV} are the CCV loop compensation capacitor and series resistor. R_{ESR} is the equivalent series resistance (ESR) of the charger output capacitor (C_{OUT}). R_L is the equivalent charger output load, where $R_L = V_{BATT} / I_{CHG}$. The equivalent output impedance of the GMV amplifier, $R_{OGMV} \geq 10M\Omega$. The voltage amplifier transconductance, GMV = 0.125µA/mV. The DC-DC converter transconductance, GM_{OUT} = 3.33A/V:

$$GM_{OUT} = \frac{1}{A_{CSI} \times RS2}$$

where A_{CSI} = 20, and RS2 is the charging current-sense resistor in the *Typical Application Circuits*.

The compensation pole is given by:

$$f_{P\_CV} = \frac{1}{2\pi R_{OGMV} \times C_{CV}}$$

The compensation zero is given by:

$$f_{Z\_CV} = \frac{1}{2\pi R_{CV} \times C_{CV}}$$

The output pole is given by:

$$f_{P\_OUT} = \frac{1}{2\pi R_L \times C_{OUT}}$$

where R_L varies with load according to $R_L = V_{BATT} / I_{CHG}$.

Output zero due to output capacitor ESR:

$$f_{Z\_ESR} = \frac{1}{2\pi R_{ESR} \times C_{OUT}}$$

The loop transfer function is given by:

$$LTF = GM_{OUT} \times R_L \times GMV \times R_{OGMV} \times \frac{(1 + sC_{OUT} \times R_{ESR})(1 + sC_{CV} \times R_{CV})}{(1 + sC_{CV} \times R_{OGMV})(1 + sC_{OUT} \times R_L)}$$

Assuming the compensation pole is a very low frequency, and the output zero is a much higher frequency, the crossover frequency is given by:

$$f_{CO\_CV} = \frac{GMV \times R_{CV} \times GM_{OUT}}{2\pi C_{OUT}}$$

To calculate R_{CV} and C_{CV} values of the circuit of Figure 2:

Cells = 4

C_{OUT} = 22µF

V_{BATT} = 16.8V

I_{CHG} = 2.5A

GMV = 0.125µA/mV

GM_{OUT} = 3.33A/V

R_{OGMV} = 10MΩ

f = 400kHz

Choose crossover frequency to be 1/5th the MAX1908's 400kHz switching frequency:

$$f_{CO\_CV} = \frac{GMV \times R_{CV} \times GM_{OUT}}{2\pi C_{OUT}} = 80kHz$$

Solving yields R_{CV} = 26kΩ.

Conservatively set R_{CV} = 1kΩ, which sets the crossover frequency at:

$$f_{CO\_CV} = 3kHz$$

Choose the output-capacitor ESR so the output-capacitor zero is 10 times the crossover frequency:

$$R_{ESR} = \frac{1}{2\pi \times 10 \times f_{CO\_CV} \times C_{OUT}} = 0.24\Omega$$

$$f_{Z\_ESR} = \frac{1}{2\pi R_{ESR} \times C_{OUT}} = 2.412MHz$$

The 22µF ceramic capacitor has a typical ESR of 0.003Ω, which sets the output zero at 2.412MHz.

The output pole is set at:

$$f_{P\_OUT} = \frac{1}{2\pi R_L \times C_{OUT}} = 1.08kHz$$

where:

$$R_L = \frac{\Delta V_{BATT}}{\Delta I_{CHG}} = \text{Battery ESR}$$

Set the compensation zero (f_{Z_CV}) so it is equivalent to the output pole (f_{P_OUT} = 1.08kHz), effectively producing a pole-zero cancellation and maintaining a single-pole system response:

$$f_{Z\_CV} = \frac{1}{2\pi R_{CV} \times C_{CV}}$$

$$C_{CV} = \frac{1}{2\pi R_{CV} \times 1.08kHz} = 147nF$$

Choose C_{CV} = 100nF, which sets the compensation zero (f_{Z_CV}) at 1.6kHz. This sets the compensation pole:

$$f_{P\_CV} = \frac{1}{2\pi R_{OGMV} \times C_{CV}} = 0.16Hz$$

CCI Loop Definitions

Compensation of the CCI loop depends on the parameters and components shown in Figure 7. C_{CI} is the CCI loop compensation capacitor. A_{CSI} is the internal gain of the current-sense amplifier. RS2 is the charge current-sense resistor, RS2 = 15mΩ. R_{OGMI} is the equivalent output impedance of the GMI amplifier ≥ 10MΩ. GMI is the charge-current amplifier transconductance = 1µA/mV. GM_{OUT} is the DC-DC converter transconductance = 3.3A/V. The CCI loop is a single-pole system with a dominant pole compensation set by f_{P_CI}:

$$f_{P\_CI} = \frac{1}{2\pi R_{OGMI} \times C_{CI}}$$

The loop transfer function is given by:

$$LTF = GM_{OUT} \times A_{CSI} \times RS2 \times GMI \frac{R_{OGMI}}{1 + sR_{OGMI} \times C_{CI}}$$

Since:

$$GM_{OUT} = \frac{1}{A_{CSI} \times RS2}$$

The loop transfer function simplifies to:

$$LTF = GMI \times \frac{R_{OGMI}}{1 + sR_{OGMI} \times C_{CI}}$$

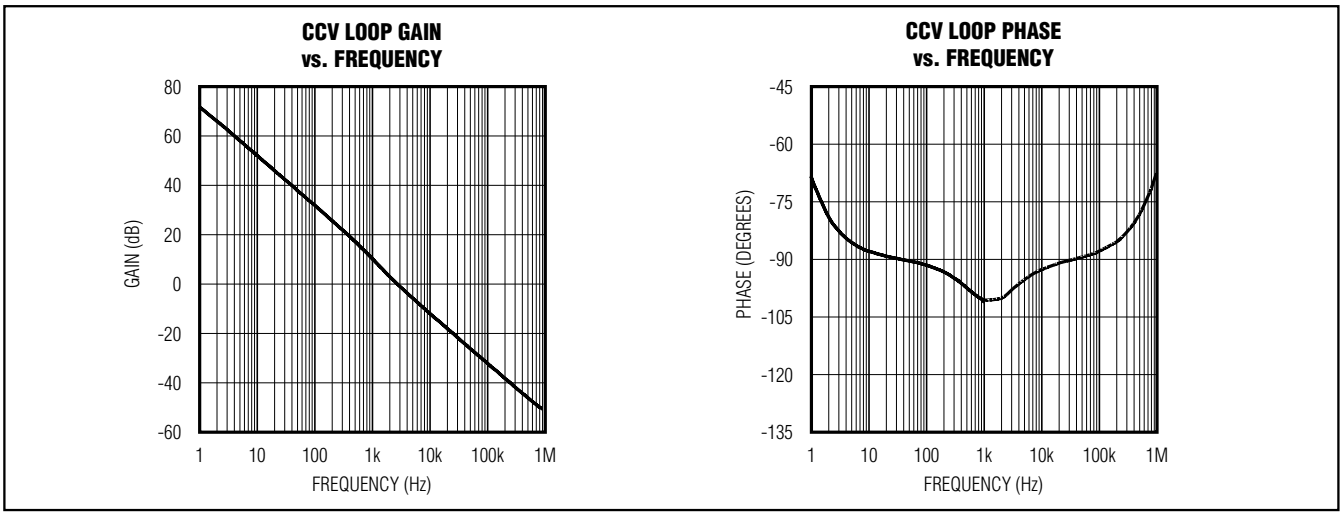


Figure 6. CCV Loop Gain/Phase vs. Frequency

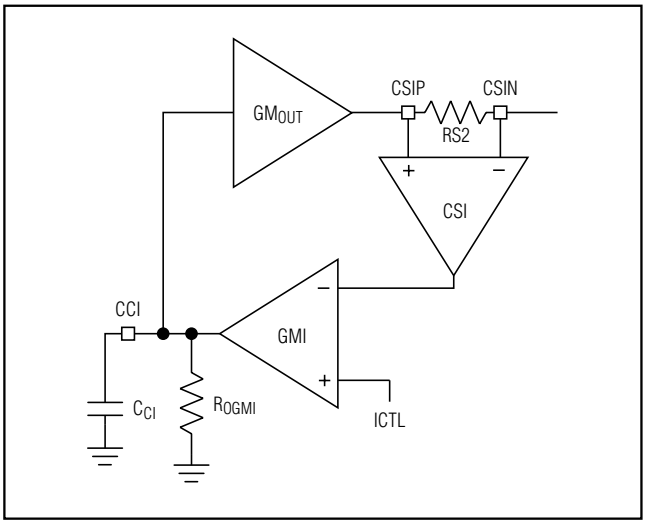


Figure 7. CCI Loop Diagram

The crossover frequency is given by:

$$f_{CO\_CI} = \frac{GMI}{2\pi C_{CI}}$$

The CCI loop dominant compensation pole:

$$f_{P\_CI} = \frac{1}{2\pi R_{OGMI} \times C_{CI}}$$

where the GMI amplifier output impedance, R_{OGMI} = 10MΩ.

To calculate the CCI loop compensation pole, C_{CI}:

GMI = 1µA/mV

GM_{OUT} = 3.33A/V

R_{OGMI} = 10MΩ

f = 400kHz

Choose crossover frequency f_{CO_CI} to be 1/5th the MAX1908/MAX8724/MAX8765 switching frequency:

$$f_{CO\_CI} = \frac{GMI}{2\pi C_{CI}} = 80kHz$$

Solving for C_{CI}, C_{CI} = 2nF.

To be conservative, set C_{CI} = 10nF, which sets the crossover frequency at:

$$f_{CO\_CI} = \frac{GMI}{2\pi 10nF} = 16kHz$$

The compensation pole, f_{P_CI} is set at:

$$f_{P\_CI} = \frac{GMI}{2\pi R_{OGMI} \times C_{CI}} = 0.0016Hz$$

CCS Loop Definitions

Compensation of the CCS loop depends on the parameters and components shown in Figure 9. C_{CS} is the CCS loop compensation capacitor. A_{CSS} is the internal gain of the current-sense amplifier. RS1 is the input current-sense resistor, RS1 = 10mΩ. R_{OGMS} is the equivalent output impedance of the GMS amplifier ≥ 10MΩ. GMS is

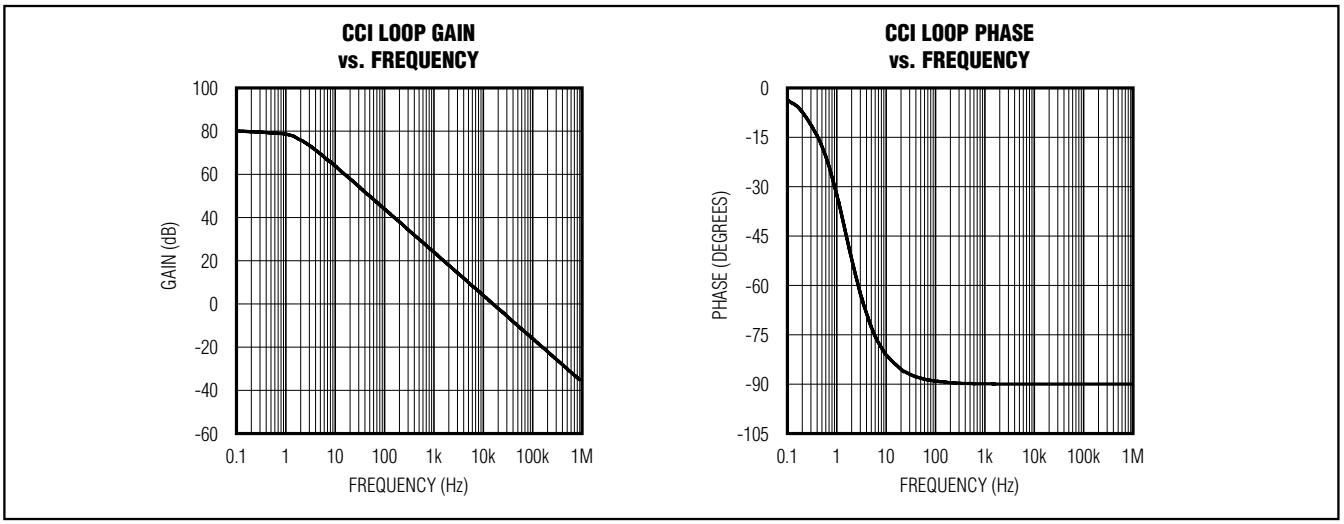


Figure 8. CCI Loop Gain/Phase vs. Frequency

the charge-current amplifier transconductance = 1µA/mV. GM_{IN} is the DC-DC converter transconductance = 3.3A/V. The CCS loop is a single-pole system with a dominant pole compensation set by f_{P_CS}:

$$f_{P\_CS} = \frac{1}{2\pi R_{OGMS} \times C_{CS}}$$

The loop transfer function is given by:

$$LTF = GM_{IN} \times A_{CSS} \times RS1 \times GMS \times \frac{R_{OGMS}}{1 + sR_{OGMS} \times C_{CS}}$$

Since:

$$GM_{IN} = \frac{1}{A_{CSS} \times RS1}$$

Then, the loop transfer function simplifies to:

$$LTF = GMS \times \frac{R_{OGMS}}{1 + sR_{OGMS} \times C_{CS}}$$

The crossover frequency is given by:

$$f_{CO\_CS} = \frac{GMS}{2\pi C_{CS}}$$

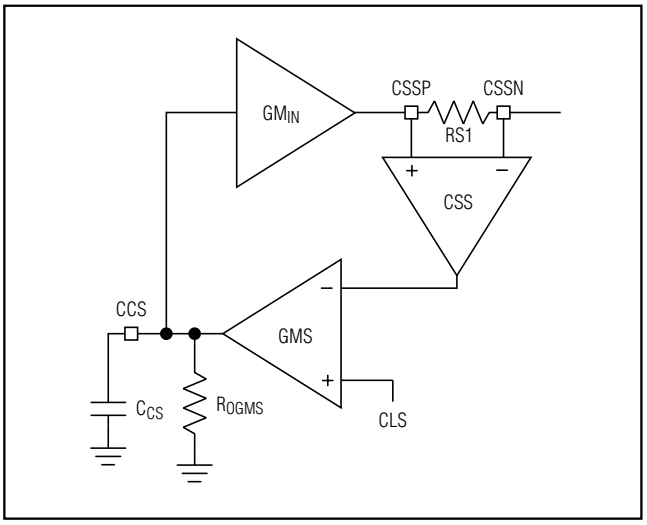


Figure 9. CCS Loop Diagram

The CCS loop dominant compensation pole:

$$f_{P\_CS} = \frac{1}{2\pi R_{OGMS} \times C_{CS}}$$

where the GMS amplifier output impedance, R_{OGMS} = 10MΩ.

To calculate the CCI loop compensation pole, C_{CS}:

GMS = 1µA/mV

GM_{IN} = 3.33A/V

R_{OGMS} = 10MΩ

f = 400kHz

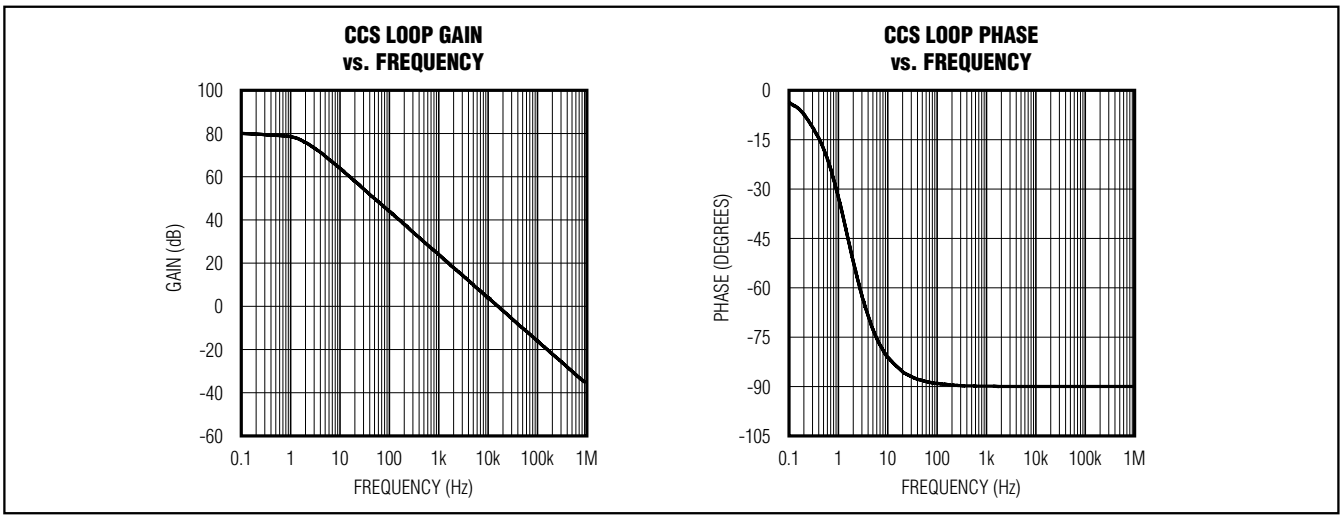


Figure 10. CCS Loop Gain/Phase vs. Frequency

Choose crossover frequency f_{CO_CS} to be 1/5th the MAX1908/MAX8724/MAX8765 switching frequency:

$$f_{CO\_CS} = \frac{GMS}{2\pi C_{CS}} = 80kHz$$

Solving for C_{CS}, C_{CS} = 2nF.

To be conservative, set C_{CS} = 10nF, which sets the crossover frequency at:

$$f_{CO\_CS} = \frac{GMS}{2\pi 10nF} = 16kHz$$

The compensation pole, f_{P_CS} is set at:

$$f_{P\_CS} = \frac{1}{2\pi R_{OGMS} \times C_{CS}} = 0.0016Hz$$

Component Selection

Table 3 lists the recommended components and refers to the circuit of Figure 2. The following sections describe how to select these components.

Inductor Selection

Inductor L1 provides power to the battery while it is being charged. It must have a saturation current of at least the charge current (I_{CHG}), plus 1/2 the current ripple I_{RIPPLE}:

$$I_{SAT} = I_{CHG} + (1/2)\ I_{RIPPLE}$$

Ripple current varies according to the equation:

$$I_{RIPPLE} = (V_{BATT}) \times t_{OFF} / L$$

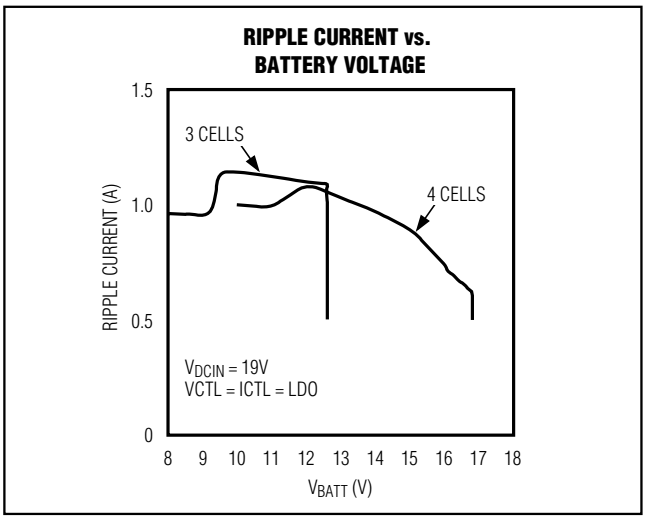


Figure 11. Ripple Current vs. Battery Voltage

where:

$$t_{OFF} = 2.5\mu s \times (V_{DCIN} - V_{BATT}) / V_{DCIN}$$

$$V_{BATT} < 0.88 \times V_{DCIN}$$

or:

$$t_{OFF} = 0.3\mu s$$

$$V_{BATT} > 0.88 \times V_{DCIN}$$

Figure 11 illustrates the variation of ripple current vs. battery voltage when charging at 3A with a fixed 19V input voltage.

Higher inductor values decrease the ripple current. Smaller inductor values require higher saturation current capabilities and degrade efficiency. Designs for ripple current, I_{RIPPLE} = 0.3 × I_{CHG} usually result in a good balance between inductor size and efficiency.

Input Capacitor

Input capacitor C1 must be able to handle the input ripple current. At high charging currents, the DC-DC converter operates in continuous conduction. In this case, the ripple current of the input capacitor can be approximated by the following equation:

$$I_{C1} = I_{CHG}\sqrt{D - D^2}$$

where:

I_{C1} = input capacitor ripple current.

D = DC-DC converter duty ratio.

I_{CHG} = battery-charging current.

Input capacitor C1 must be sized to handle the maximum ripple current that occurs during continuous conduction. The maximum input ripple current occurs at 50% duty cycle; thus, the worst-case input ripple current is 0.5 × I_{CHG}. If the input-to-output voltage ratio is such that the DC-DC converter does not operate at a 50% duty cycle, then the worst-case capacitor current occurs where the duty cycle is nearest 50%.

The input capacitor ESR times the input ripple current sets the ripple voltage at the input, and should not exceed 0.5V ripple. Choose the ESR of C1 according to:

$$ESR_{C1} < \frac{0.5V}{I_{C1}}$$

The input capacitor size should allow minimal output voltage sag at the highest switching frequency:

$$\frac{I_{C1}}{2} = C1\frac{dV}{dt}$$

where dV is the maximum voltage sag of 0.5V while delivering energy to the inductor during the high-side MOSFET on-time, and dt is the period at highest operating frequency (400kHz):

$$C1 > \frac{I_{C1}}{2} \times \frac{2.5\mu s}{0.5V}$$

Both tantalum and ceramic capacitors are suitable in most applications. For equivalent size and voltage rating, tantalum capacitors have higher capacitance, but also higher ESR than ceramic capacitors. This makes it more critical to consider ripple current and power-dissipation ratings when using tantalum capacitors. A single ceramic capacitor often can replace two tantalum capacitors in parallel.

Output Capacitor

The output capacitor absorbs the inductor ripple current. The output capacitor impedance must be significantly less than that of the battery to ensure that it absorbs the ripple current. Both the capacitance and ESR rating of the capacitor are important for its effectiveness as a filter and to ensure stability of the DC-DC converter (see the *Compensation* section). Either tantalum or ceramic capacitors can be used for the output filter capacitor.

MOSFETs and Diodes

Schottky diode D1 provides power to the load when the AC adapter is inserted. This diode must be able to deliver the maximum current as set by RS1. For reduced power dissipation and improved dropout performance, replace D1 with a p-channel MOSFET (P1) as shown in Figure 2. Take caution not to exceed the maximum V_{GS} of P1. Choose resistors R11 and R12 to limit the V_{GS}.

The n-channel MOSFETs (N1a, N1b) are the switching devices for the buck controller. High-side switch N1a should have a current rating of at least the maximum charge current plus one-half the ripple current and have an on-resistance ($R_{DS(ON)}$) that meets the power dissipation requirements of the MOSFET. The driver for N1a is powered by BST. The gate-drive requirement for N1a should be less than 10mA. Select a MOSFET with a low total gate charge (Q_{GATE}) and determine the required drive current by $I_{GATE} = Q_{GATE} \times f$ (where f is the DC-DC converter's maximum switching frequency).

The low-side switch (N1b) has the same current rating and power dissipation requirements as N1a, and should have a total gate charge less than 10nC. N2 is used to provide the starting charge to the BST capacitor (C15). During the dead time (50ns, typ) between N1a and N1b, the current is carried by the body diode of the MOSFET. Choose N1b with either an internal Schottky diode or body diode capable of carrying the maximum charging current during the dead time. The Schottky diode D3 provides the supply current to the high-side MOSFET driver.

Layout and Bypassing

Bypass DCIN with a 1µF capacitor to power ground (Figure 1). D2 protects the MAX1908/MAX8724/MAX8765 when the DC power source input is reversed. A signal diode for D2 is adequate because DCIN only powers the internal circuitry. Bypass LDO, REF, CCV, CCI, CCS, ICHG, and IINP to analog ground. Bypass DLOV to power ground.

Good PC board layout is required to achieve specified noise, efficiency, and stable performance. The PC board layout artist must be given explicit instructions—preferably, a pencil sketch showing the placement of the power-switching components and high-current routing. Refer to the PC board layout in the MAX1908 evaluation kit for examples. Separate analog and power grounds are essential for optimum performance.

Use the following step-by-step guide:

1) Place the high-power connections first, with their grounds adjacent:
   a) Minimize the current-sense resistor trace lengths, and ensure accurate current sensing with Kelvin connections.
   b) Minimize ground trace lengths in the high-current paths.
   c) Minimize other trace lengths in the high-current paths.
   d) Use > 5mm wide traces.
   e) Connect C1 to high-side MOSFET (10mm max length).
   f) LX node (MOSFETs, inductor (15mm max length)).

   Ideally, surface-mount power components are flush against one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper, so they do not go through vias.

   The resulting top-layer power ground plane is connected to the normal ground plane at the MAX1908/MAX8724/MAX8765s' backside exposed pad. Other high-current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates most PC board layout problems.

2) Place the IC and signal components. Keep the main switching node (LX node) away from sensitive analog components (current-sense traces and REF capacitor). **Important:** The IC must be no further than 10mm from the current-sense resistors.

   Keep the gate-drive traces (DHI, DLO, and BST) shorter than 20mm, and route them away from the current-sense lines and REF. Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away.

3) Use a single-point star ground placed directly below the part at the backside exposed pad of the MAX1908/MAX8724/MAX8765. Connect the power ground and normal ground to this node.

Table 3. Component List for Circuit of Figure 2

DESIGNATION	QTY	DESCRIPTION
C1	2	10µF, 50V 2220-size ceramic capacitors TDK C5750X7R1H106M
C4	1	22µF, 25V 2220-size ceramic capacitor TDK C5750X7R1E226M
C5	1	1µF, 25V X7R ceramic capacitor (1206) Murata GRM31MR71E105K Taiyo Yuden TMK316BJ105KL TDK C3216X7R1E105K
C9, C10	2	0.01µF, 16V ceramic capacitors (0402) Murata GRP155R71E103K Taiyo Yuden EMK105BJ103KV TDK C1005X7R1E103K
C11, C14, C15, C20	4	0.1µF, 25V X7R ceramic capacitors (0603) Murata GRM188R71E104K TDK C1608X7R1E104K
C12, C13, C16	3	1µF, 6.3V X5R ceramic capacitors (0603) Murata GRM188R60J105K Taiyo Yuden JMK107BJ105KA TDK C1608X5R1A105K
D1 (optional)	1	10A Schottky diode (D-PAK) Diodes, Inc. MBRD1035CTL ON Semiconductor MBRD1035CTL
D2	1	Schottky diode Central Semiconductor CMPSH1–4
D3	1	Schottky diode Central Semiconductor CMPSH1-4
L1	1	10µH, 4.4A inductor Sumida CDRH104R-100NC TOKO 919AS-100M
N1	1	Dual, n-channel, 8-pin SO MOSFET Fairchild FDS6990A or FDS6990S
P1	1	Single, p-channel, 8-pin SO MOSFET Fairchild FDS6675
R5	1	1kΩ ±5% resistor (0603)
R6	1	59kΩ ±1% resistor (0603)
R7	1	19.6kΩ ±1% resistor (0603)
R11	1	12kΩ ±5% resistor (0603)
R12	1	15kΩ ±5% resistor (0603)
R13	1	33Ω ±5% resistor (0603)
R14	1	10.5kΩ ±1% resistor (0603)
R15, R16	2	8.25kΩ ±1% resistors (0603)
R17	1	19.1kΩ ±1% resistor (0603)
R18	1	22kΩ ±1% resistor (0603)
R19, R20	2	10kΩ ±1% resistors (0603)
RS1	1	0.01Ω ±1%, 0.5W 2010 sense resistor Vishay Dale WSL2010 0.010 1.0% IRC LRC-LR2010-01-R010-F
RS2	1	0.015Ω ±1%, 0.5W 2010 sense resistor Vishay Dale WSL2010 0.015 1.0% IRC LRC-LR2010-01-R015-F
U1	1	MAX1908ETI, MAX8724ETI, or MAX8765ETI

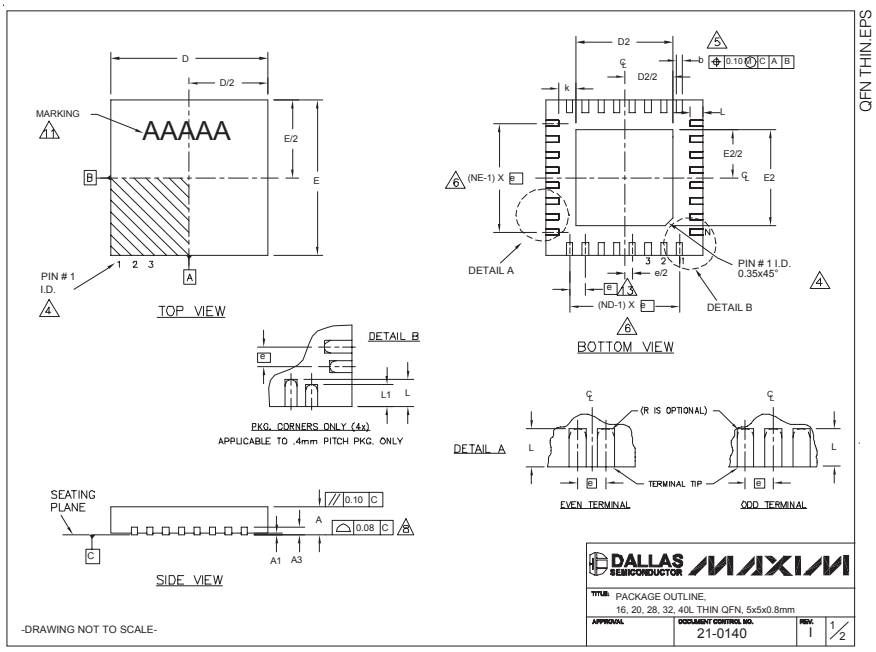
Chip Information

TRANSISTOR COUNT: 3772

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			L ±0.15	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	.20	**	NO
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm
21-0140
REV. I
2/2