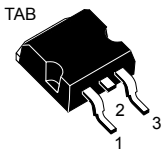
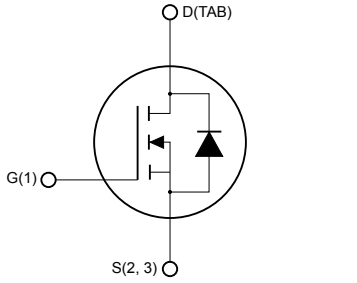
STH345N6F7-2

Datasheet

N-channel 60 V, 1.2 mΩ max., 397 A STripFET F7 Power MOSFET in an H²PAK-2 package



H²PAK-2



DTG1S23NZ

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STH345N6F7-2	60 V	1.2 mΩ	397 A

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Industrial motor control
- Industrial drives

Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status link
STH345N6F7-2

Product summary	
Order code	STH345N6F7-2
Marking(1)	345N6F7
Package	H²PAK-2
Packing	Tape and reel

1. *Engineering samples are clearly identified with a dedicated special symbol in the marking of each unit.*

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C(2)	397	A
	Drain current (continuous) at T_C = 25 °C(3)	240	
	Drain current (continuous) at T_C = 100 °C(2)	281	
I_{DM}(1)(2)(4)	Drain current (pulsed)	1588	A
P_{TOT}	Total power dissipation at T_C = 25 °C	341	W
I_{AS}	Single pulse avalanche current (pulse width limited by maximum junction temperature)	90	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_{AV} = 90 A, $R_{Gmin.}$ = 25 Ω)	1073	mJ
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		°C

1. *Specified by design, not tested in production.*
2. *This is the theoretical current value only related to the silicon.*
3. *This current value is limited by package.*
4. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.44	°C/W
R_{thJA}(1)	Thermal resistance, junction-to-ambient	14.8	°C/W

1. *Measured on 4 layer PCB according to Jedec 51.2 in natural convection (still air).*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 60 V			1	µA
		V_{GS} = 0 V, V_{DS} = 60 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 90 A		0.94	1.2	mΩ

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}(1)	Input capacitance	V_{DS} = 30 V, f = 1 MHz, V_{GS} = 0 V	-	12900	-	pF
C_{oss}(1)	Output capacitance		-	5600	-	pF
C_{rss}(1)	Reverse transfer capacitance		-	340	-	pF
Q_g(1)	Total gate charge	V_{DD} = 30 V, I_D = 90 A, V_{GS} = 0 to 10 V (see Figure 18. Test circuit for gate charge behavior)	-	230	-	nC
Q_{gs}(1)	Gate-source charge		-	65	-	nC
Q_{gd}(1)	Gate-drain charge		-	70	-	nC
R_g(1)	Intrinsic gate resistance		-	1.3	-	Ω
$Q_{g(sync)}$(1)	Total gate charge, sync. MOSFET	I_D = 90 A, V_{GS} = 0 to 10 V	-	180	-	nC
Q_{OSS}(1)	Output charge	V_{DD} = 30 V, V_{GS} = 0 V	-	255	-	nC

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(1)	Turn-on delay time	V_{DD} = 30 V, I_D = 90 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 17. Test circuit for resistive load switching times)	-	48.7	-	ns
t_r(1)	Rise time		-	87.3	-	ns
$t_{d(off)}$(1)	Turn-off delay time		-	107.4	-	ns
t_f(1)	Fall time		-	73.5	-	ns

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)(2)	Source-drain current		-		227	A
V_{SD}	Forward on voltage	V_{GS} = 0 V, I_{SD} = 90 A	-		1.2	V
t_{rr}(1)	Reverse recovery time	I_{SD} = 90 A, di/dt = 100 A/µs, V_{DD} = 48 V, T_J = 25 °C (see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	89.7		ns
Q_{rr}(1)	Reverse recovery charge		-	170.35		nC
I_{RRM}(1)	Reverse recovery current		-	3.8		A

1. *Specified by design and evaluated by characterization, not tested in production.*
2. *This is the theoretical current value only related to the silicon.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

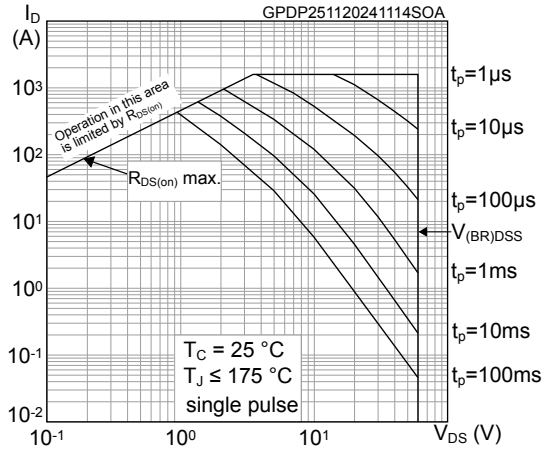


Figure 2. Normalized transient thermal impedance

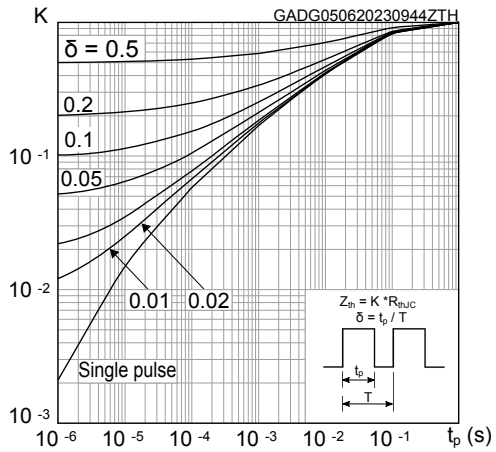


Figure 3. Typical output characteristics

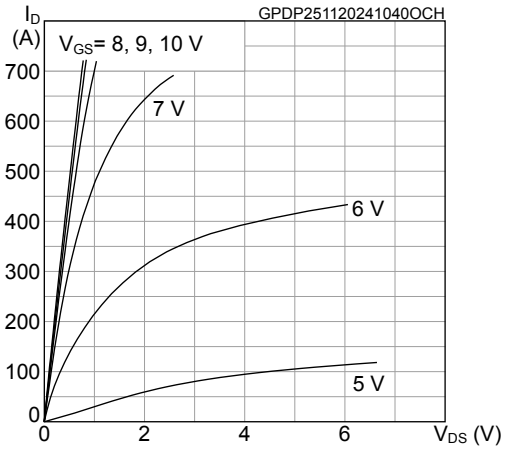


Figure 4. Typical transfer characteristics

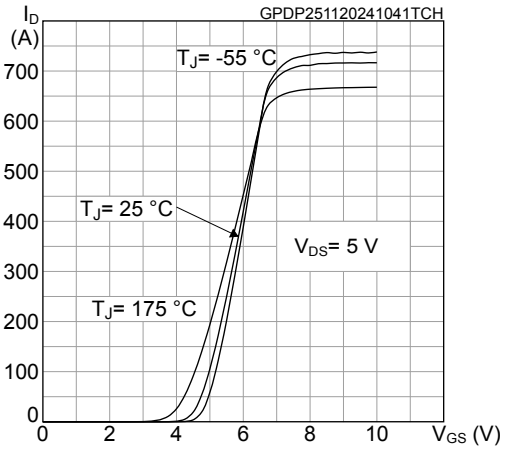


Figure 5. Typical drain-source on-resistance

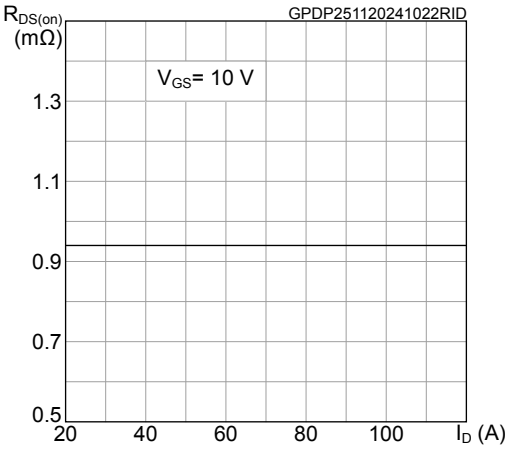


Figure 6. Typical on-resistance vs gate-source voltage

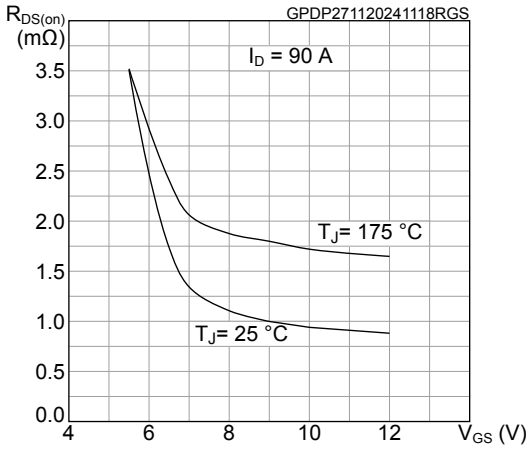


Figure 7. Typical gate charge characteristics

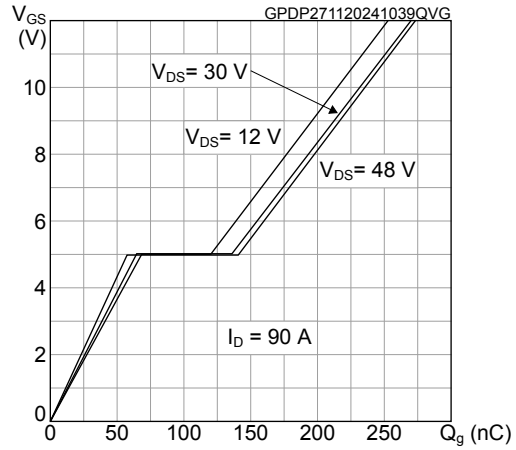


Figure 8. Typical capacitance characteristics

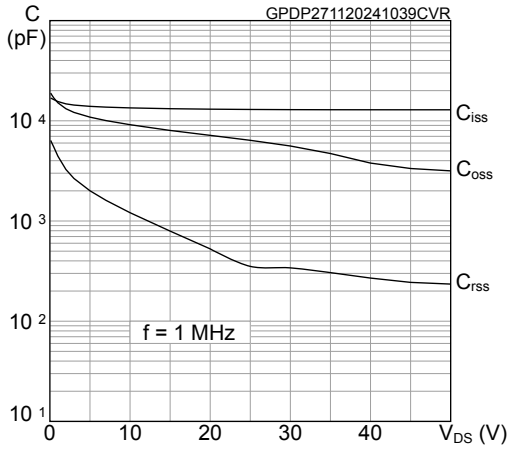


Figure 9. Avalanche characteristics

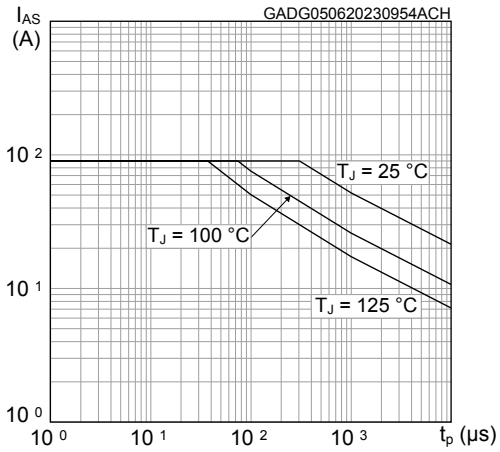


Figure 10. Avalanche energy

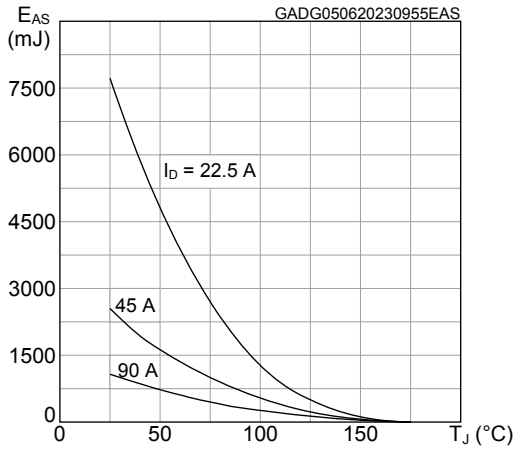


Figure 11. Typical reverse diode forward characteristics

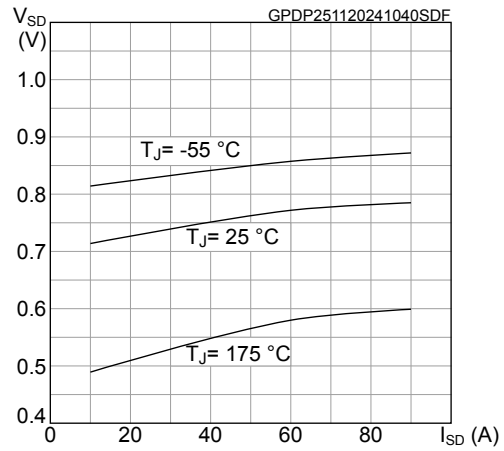


Figure 12. Normalized on-resistance vs temperature

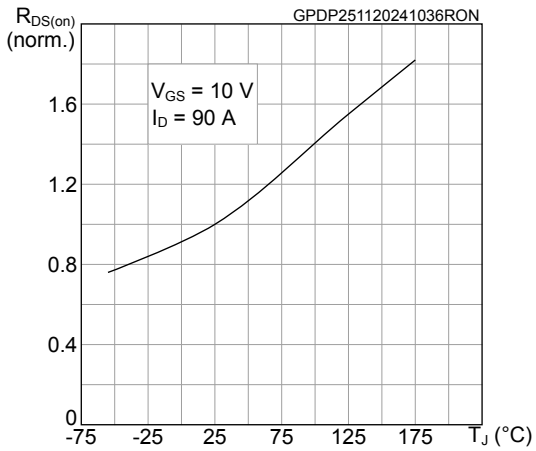


Figure 13. Normalized gate threshold voltage vs temperature

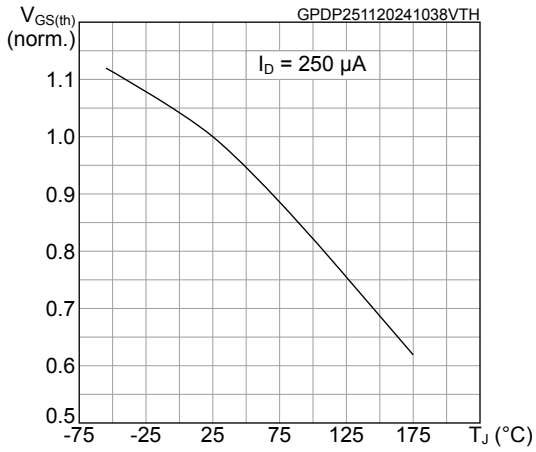


Figure 14. Normalized breakdown vs temperature

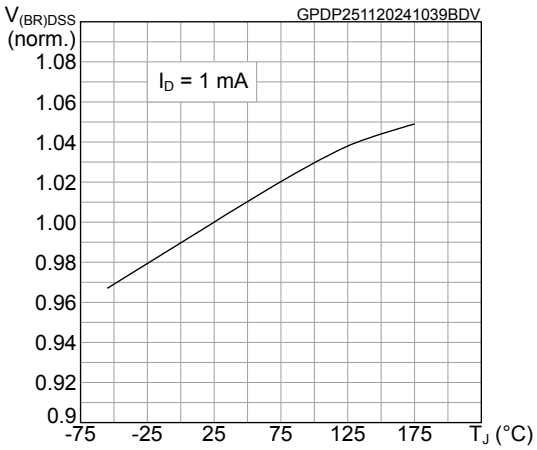


Figure 15. Total power dissipation

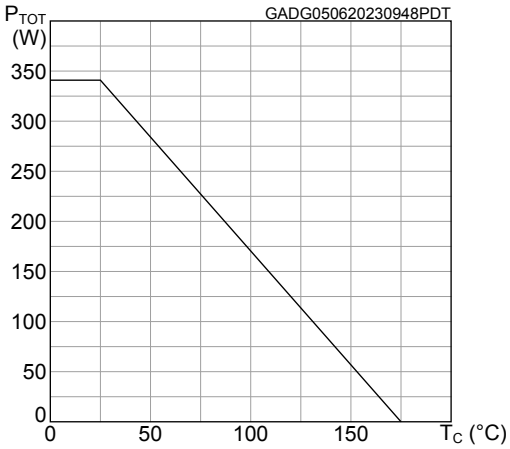
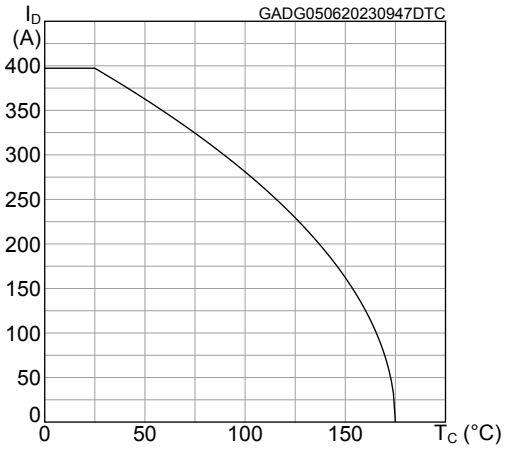


Figure 16. Drain current vs case temperature



3 Test circuits

Figure 17. Test circuit for resistive load switching times

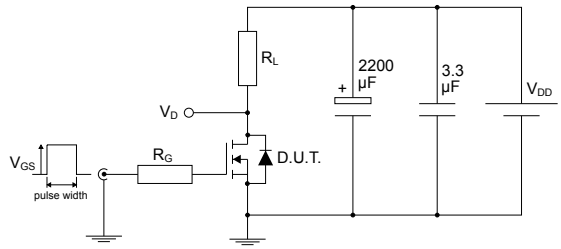


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Figure 18. Test circuit for gate charge behavior

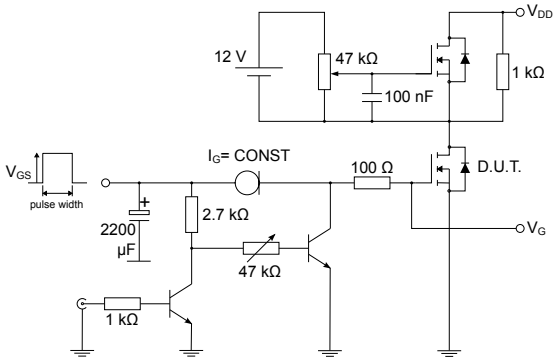

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Figure 19. Test circuit for inductive load switching and diode recovery times

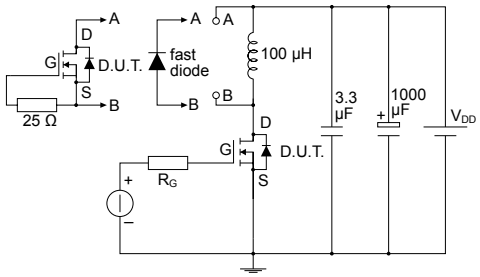

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Figure 20. Unclamped inductive load test circuit

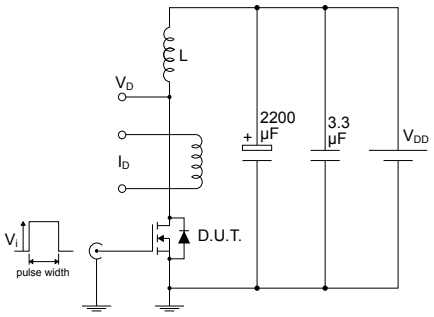

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Figure 21. Unclamped inductive waveform

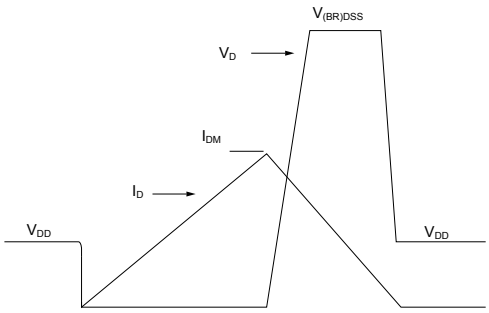

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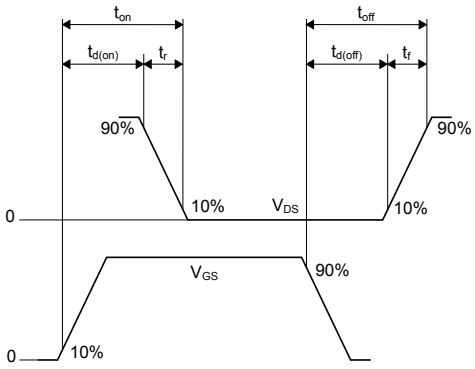
Figure 22. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-2 package information

Figure 23. H²PAK-2 package outline

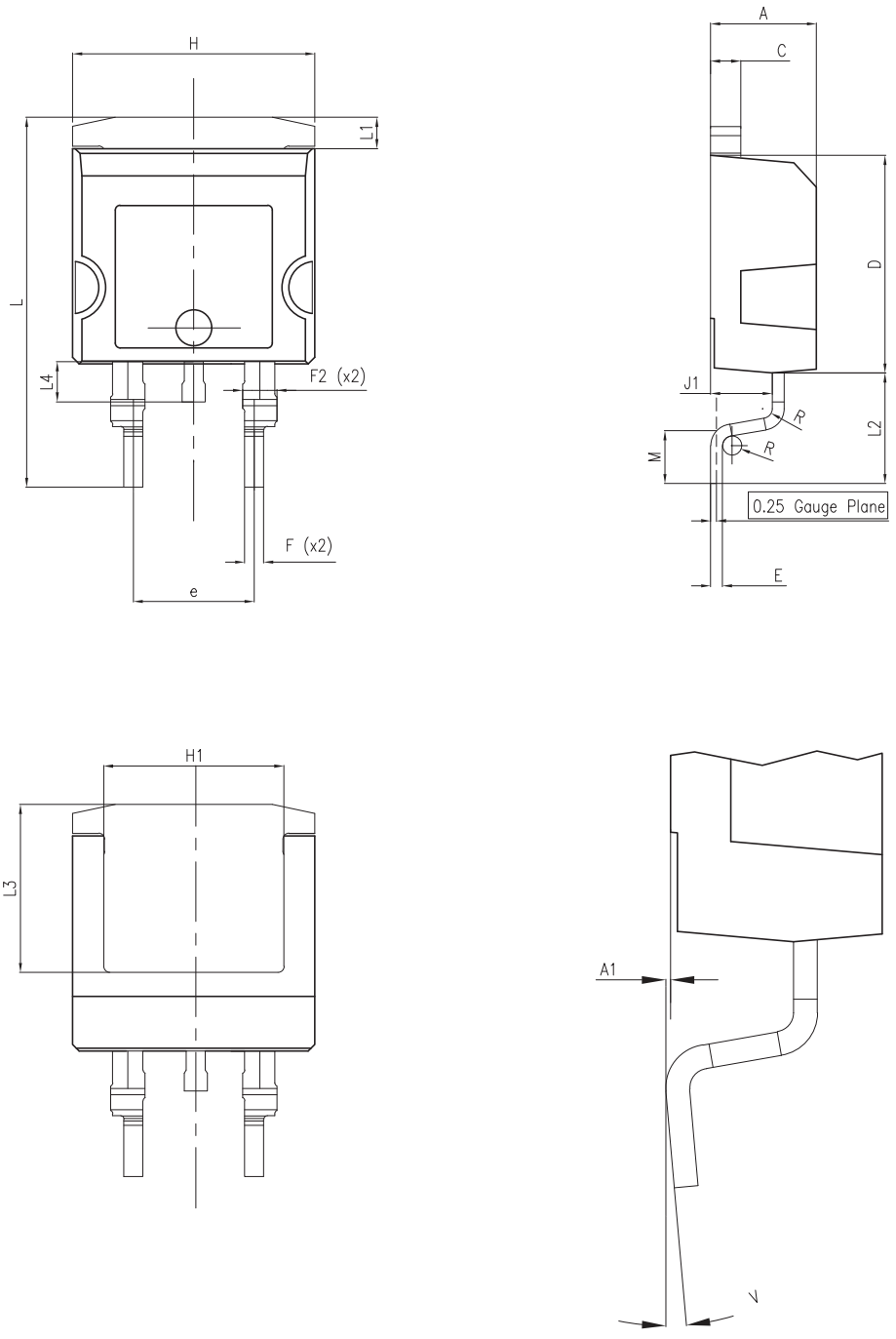
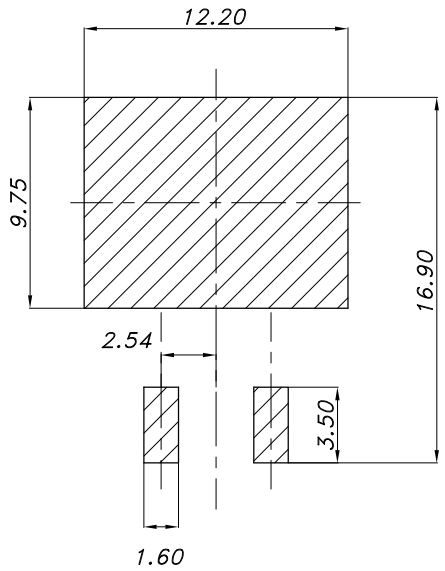


Table 7. **H²PAK-2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40	-	7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

Figure 24. **H²PAK-2 recommended footprint**



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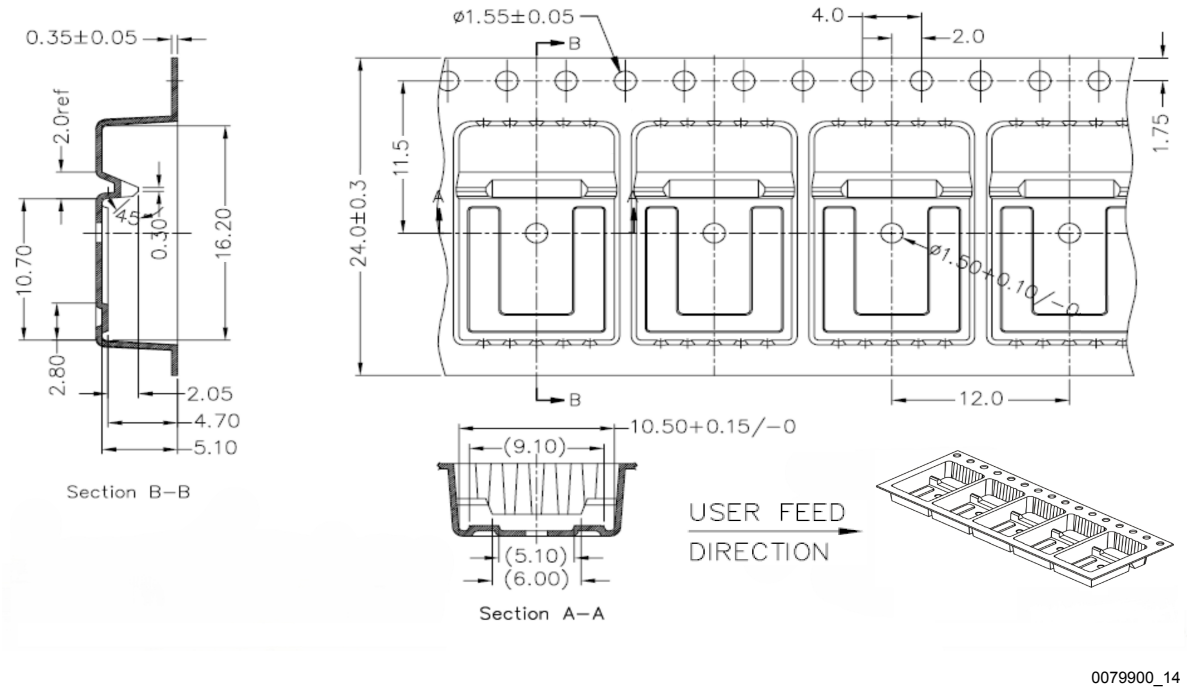
Note: Dimensions are in mm.

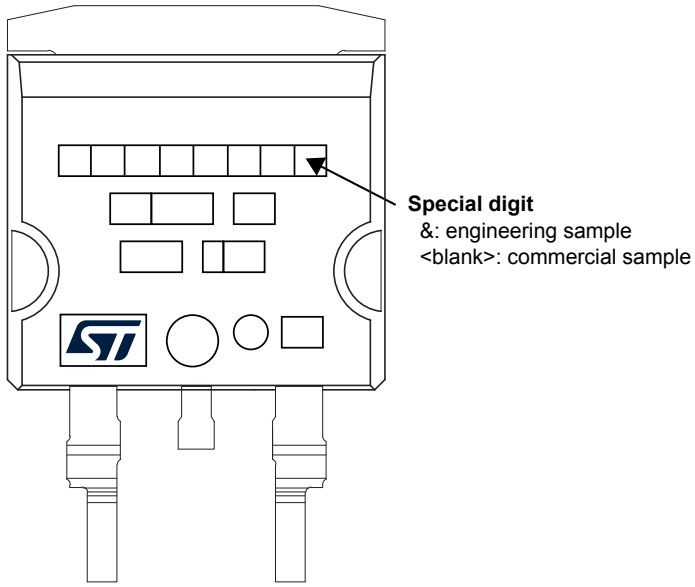
4.2 H²PAK-2 packing information

Figure 25. H²PAK-2 tape drawing (dimensions are in mm)



4.3 H²PAK-2 marking information

Figure 26. **H²PAK-2 marking information**



Note: Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
12-Jun-2023	1	First release.
20-Jun-2024	2	Updated *Table 1*, *Table 2*, *Table 4*, *Table 5*, and *Table 6*. Inserted *Section 4.3: H²PAK-2 marking information*.
09-Dec-2024	3	Updated *Table 2. Thermal data, Table 4. Dynamic, Table 5. Switching times,Table 6. Source-drain diode* and *Figure 1. Safe operating area.* Added *Figure 2. Normalized transient thermal impedance, Figure 3. Typical output characteristics, Figure 4. Typical transfer characteristics, Figure 5. Typical drain-source on-resistance, Figure 6. Typical on-resistance vs gate-source voltage, Figure 7. Typical gate charge characteristics, Figure 8. Typical capacitance characteristics, Figure 13. Normalized gate threshold voltage vs temperature, Figure 12. Normalized on-resistance vs temperature, Figure 14. Normalized breakdown vs temperature* and *Figure 11. Typical reverse diode forward characteristics.* Minor text changes.
28-May-2025	4	Updated Table 4. Dynamic. Minor text changes.

Contents