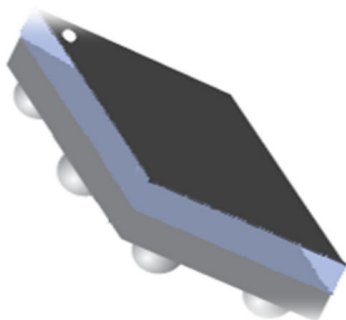
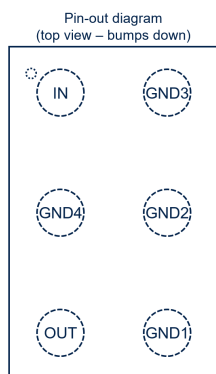


2.4 GHz low pass filter matched to STM32WBA CSP series



Chip scale package on glass 6 bumps



Features

- Integrated impedance matching to STM32WBA CSP series
- 50 Ω nominal impedance on antenna side
- Deep rejection harmonics filter
- Low insertion loss
- Small footprint
- Low profile $\leq 630 \mu\text{m}$ after reflow
- High RF performances
- RF BOM and area reduction
- **ECOPACK2** compliant component

Applications

- Bluetooth 5
- OpenThread
- Zigbee®
- IEEE 802.15.4
- Optimized for STM32WBA CSP series

Description

The MLPF-WB-05D3 integrates an impedance matching network and harmonics filter. The matching impedance network has been tailored to maximize the RF performances of STM32WBA CSP series. This device uses STMicroelectronics IPD technology on non-conductive glass substrate which optimizes RF performances.

Product status link

[MLPF-WB-05D3](#)

1 Characteristics

Table 1. Absolute ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Value	Unit
P_{IN}	Input power RF_{IN}	15	dBm
V_{ESD}	ESD ratings human body model (JESD22-A114-C), all I/O one at a time while others connected to GND	2000	V
T_{OP}	Maximum operating temperature	-40 to +105	$^{\circ}\text{C}$

Table 2. Impedances ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Z_{IN}	STM32WBA CSP single-ended impedance	-	Matched to STM32WBA CSP	-	Ω
Z_{OUT}	Antenna impedance	-	50	-	Ω

Table 3. Electrical characteristics and RF performances ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
f	Frequency range		2400		2500	MHz
IL	Insertion loss $ S_{21} $			0.9	1.1	dB
RL_{IN}	Input return loss $ S_{11} $		13	18		dB
RL_{OUT}	Output return loss $ S_{22} $		13	21		dB
Att	Harmonic rejection levels $ S_{21} $	Attenuation at 2fo (4800 – 5000) MHz	34	38		dB
		Attenuation at 3fo (7200 – 7500) MHz	37	39		dB
		Attenuation at 4fo (9600 – 10000) MHz	42	46		dB
		Attenuation at 5fo (12000 – 12500) MHz	35	37		dB

1.1 RF measurement

Figure 1. Transmission (dB)

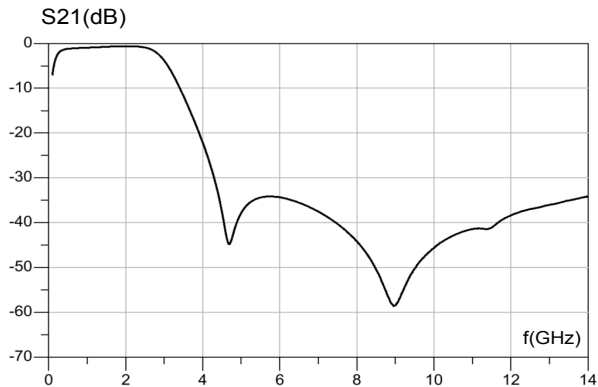


Figure 2. Insertion loss (dB)

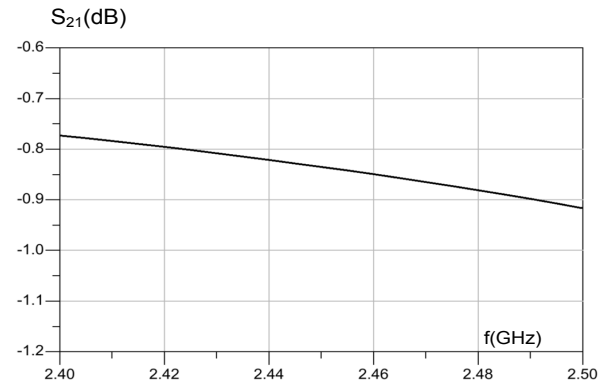


Figure 3. Input return loss (dB)

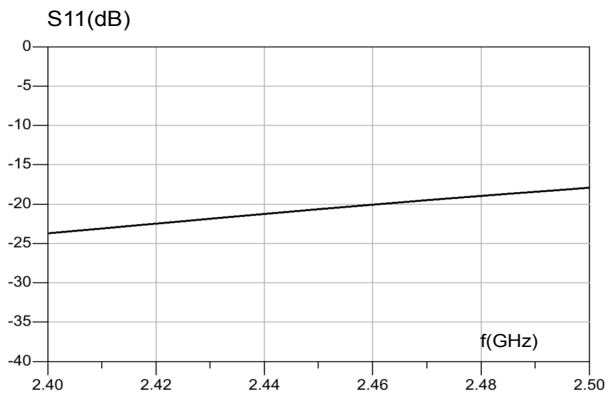


Figure 4. Output return loss (dB)

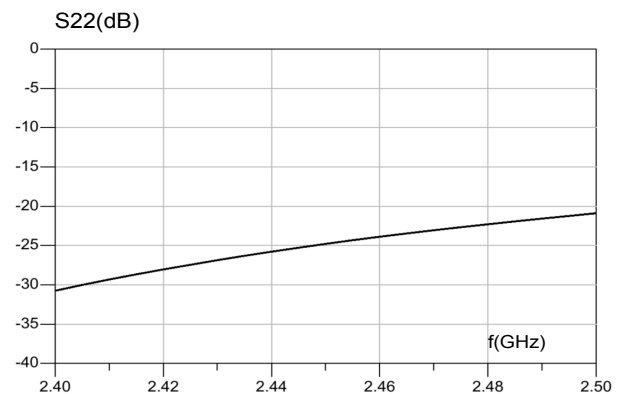


Figure 5. Attenuation 2f0 (dB)

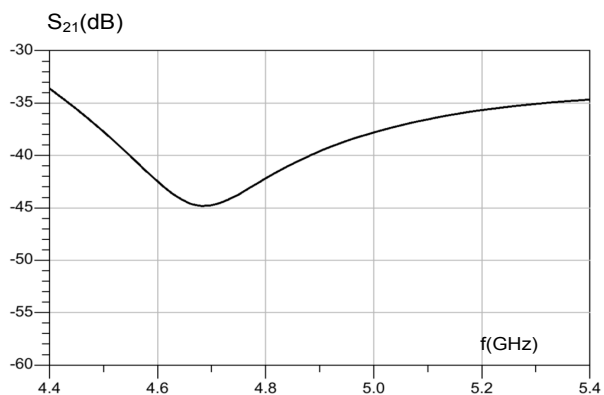


Figure 6. Attenuation 3f0 (dB)

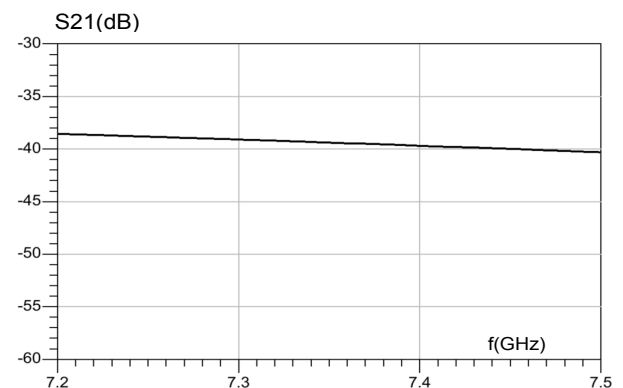


Figure 7. Attenuation 4f0 (dB)

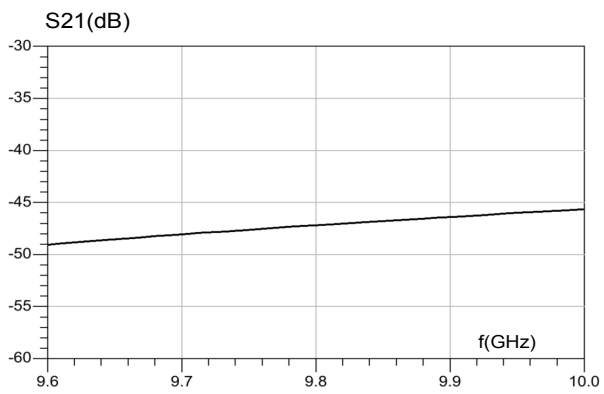
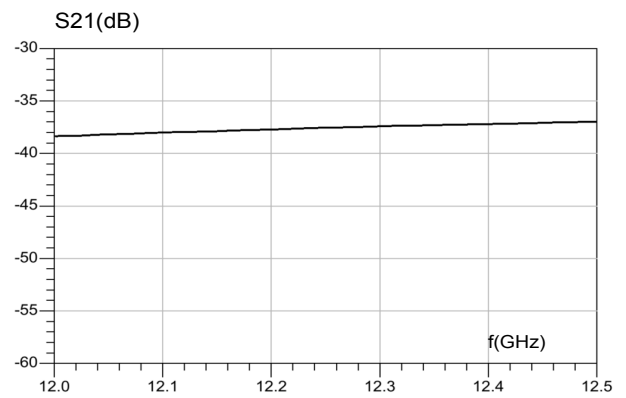


Figure 8. Attenuation 5f0 (dB)



2 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 CSPG package information

Figure 9. CSPG package outline (bottom view - bumps up)

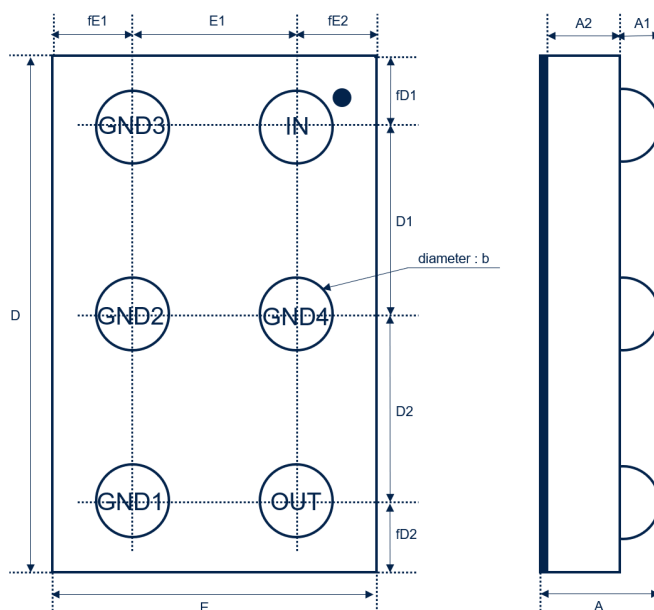
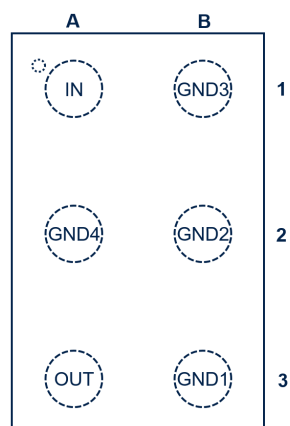


Table 4. CSPG 6 bumps mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.580	0.630	0.680
A1	0.180	0.205	0.230
A2	0.380	0.400	0.420
b	0.230	0.255	0.280
D	1.550	1.600	1.650
D1		0.577	
D2		0.577	
E	0.950	1.000	1.050
E1		0.500	
fD1		0.223	
fD2		0.223	
fE1		0.250	
fE2		0.250	

Figure 10. Marking

Dot, ST logo
 ■ ECOPACK® Grade
 xx = marking
 z = manufacturing location
 yww = datecode
 (y = year
 ww = week)


Figure 11. Top view

Table 5. Pad description top view (pads down)

Pad ref	Pad name	Description
A1	IN	STM32WBA CSP
A2	GND4	Ground
A3	OUT	Antenna
B1	GND3	Ground
B2	GND2	Ground
B3	GND1	Ground

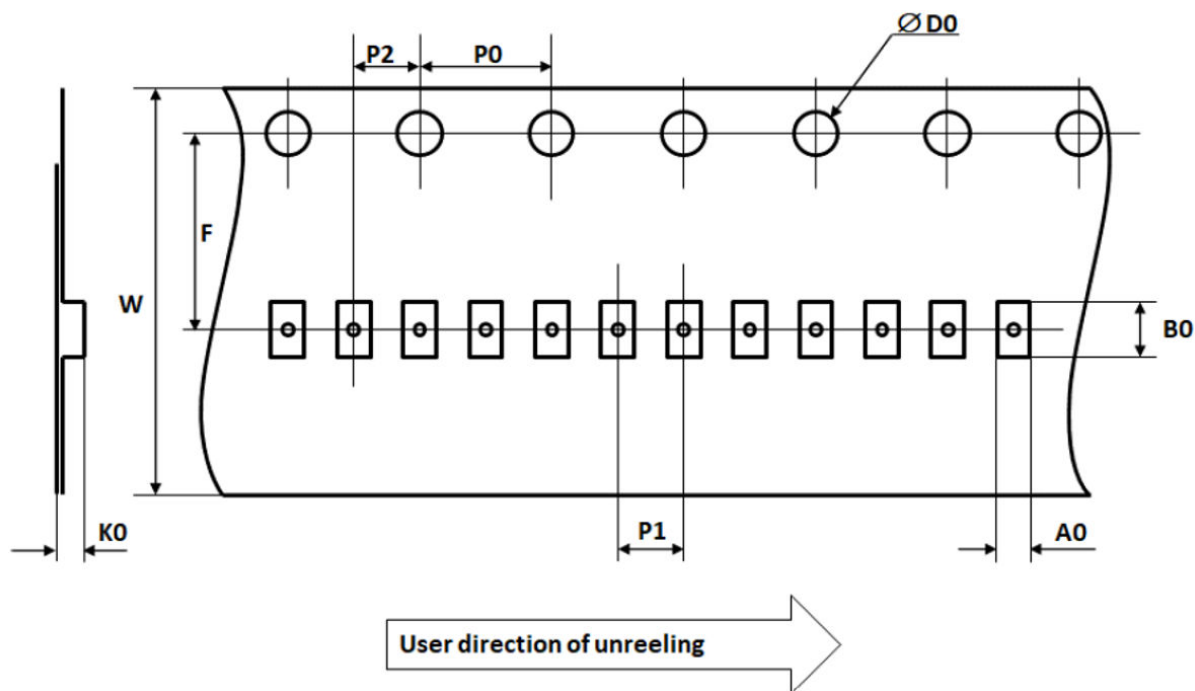
Figure 12. Tape and reel outline


Table 6. Tape and reel mechanical data

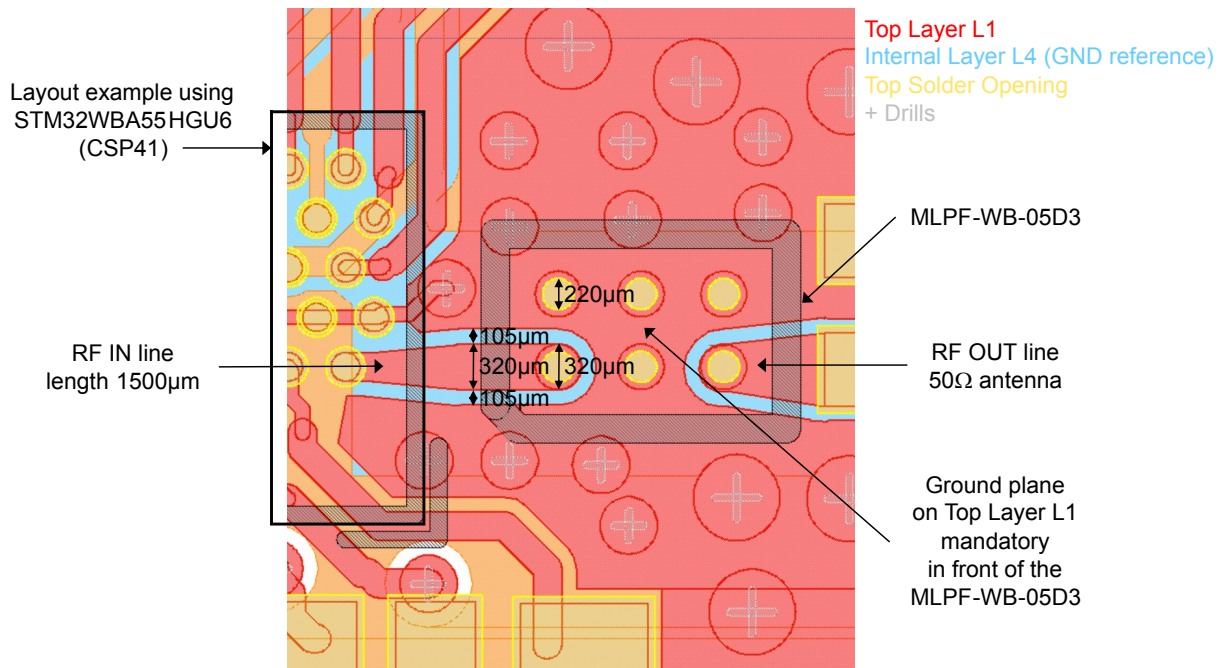
Ref	Dimensions		
	Millimeters		
	Min	Typ	Max
A0	1.06	1.09	1.12
B0	1.66	1.69	1.72
D0	1.40	1.50	1.60
F	3.45	3.50	3.55
K0	0.69	0.72	0.75
P0	3.90	4.00	4.10
P1	1.95	2.00	2.05
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

3 Recommendation on PCB assembly

3.1 Land pattern

Example of PCB land pattern using the evaluation board MB2147A (6-layers PCB).

Figure 13. PCB land pattern recommendations



The RF IN transmission line between STM32 and MLPF is dimensioned to 55 Ω characteristic impedance.

This characteristic impedance has to be followed as close as possible, within a tolerance of $\pm 15\%$.

The length of the RF IN line must be followed as precisely as possible.

The RF OUT transmission line between MLPF and antenna is dimensioned to 50 Ω characteristic impedance.

The ground plane on top layer is mandatory in front of the MLPF-WB-05D3, with its geometries which allow the best equipotentiality.

The drills density needs to be maximized near the MLPF-WB-05D3 area to ensure optimal RF performances.

Figure 14. PCB stack-up recommendations

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.01778mm	4.2	
1	Top Layer	Cu	Signal	1oz	0.03556mm		
	Dielectric 1-2	Prepreg	Prepreg		0.06858mm	3.9	0.02
2	Internal 2	Cu	Signal	1oz	0.03556mm		
	Dielectric 2-3	Prepreg	Prepreg		0.06858mm	3.9	0.02
3	Internal 3	Cu	Signal	1oz	0.03302mm		
	Dielectric 1	Core	Core		1.0668mm	4.7	0.02
4	Internal 4	Cu	Signal	1oz	0.03302mm		
	Dielectric 3	Prepreg	Prepreg		0.06858mm	3.9	0.02
5	Internal 5	Cu	Signal	1oz	0.03556mm		
	Dielectric 2	Prepreg	Prepreg		0.06858mm	3.9	0.02
6	Bottom Layer	Cu	Signal	1oz	0.03556mm		
	Bottom Solder	Solder Resist	Solder Mask		0.01778mm	4.2	
	Bottom Overlay		Overlay				

The Figure 14 is an example of PCB stack-up using the evaluation board MB2147A (6-layers PCB).

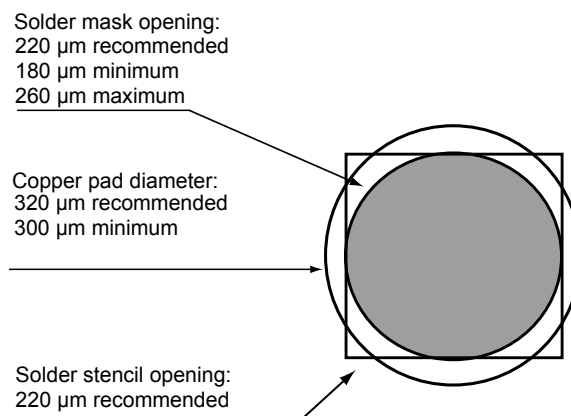
The number of PCB layers can be adjusted depending on the application.

As the ground plane on top layer is mandatory in front of the MLPF-WB-05D3, only the RF IN line is impacted by the thickness and the relative permittivity of the dielectric layers:

- The internal dielectric thickness can significantly vary with a low impact on the RF performances, provided that the RF IN line characteristic impedance is kept at the proper value
- For PCB relative permittivity in the conventional range [3.5-4.9], this MPLF is robust with a limited dispersion of the RF performances.

3.2 Stencil opening design

Figure 15. Footprint - 3 mils stencil - solder mask defined



3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38 μ m.

3.4 Placement

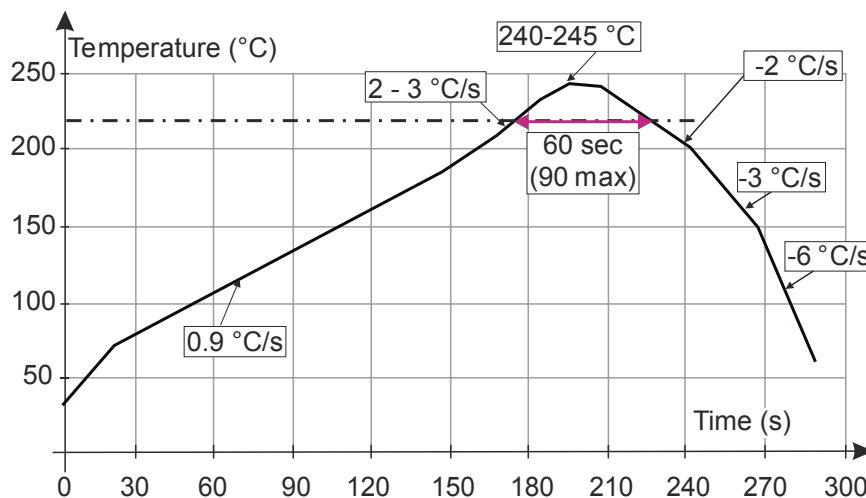
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

Figure 16. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Note: More information is available in the application note:

- [AN2348 Flip-Chip: "Package description and recommendations for use"](#)

4 Ordering information

Table 7. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
MLPF-WB-05D3	UR	CSPG	1.82 mg	5000	Tape and reel

Revision history

Table 8. Document revision history

Date	Revision	Changes
10-Jul-2025	1	Initial release.

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