

15 V / 50 W QR flyback converter based on VIPERGAN50W



Features

Universal input mains range: 90 – 265 V_{AC}

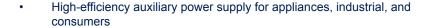
Frequency: 50-60 HzOutput voltage: 15 VOutput current: 3.35 A

Stand-by mains consumption: < 85 mW at 230 V_{AC}

• Average efficiency: > 90%

- Tight line and load regulation over the entire input and output range
- Meets IEC55022 Class B conducted EMI even with reduced EMI filter, thanks to the frequency jittering feature
- · RoHS compliant

Applications





Product status link

EVLVIPGAN50WF

Product label



Description

The EVLVIPGAN50WF evaluation board implements a 15 V / 50 W SSR isolated flyback converter developed for general-purpose applications, operating from 90 to 265 V_{AC} .

The reference design is built around the VIPERGAN50W, a new advanced offline high-voltage converter by STMicroelectronics with the following features:

- 700 V PowerGaN with embedded senseFET (Si) and HV startup;
- QR operation with dynamic blanking time and adjustable valley synchronization delay functions, to maximize efficiency at any input line and load conditions;
- Valley-lock to ensure constant valley skipping;
- Input voltage feedforward compensation for mains-independent OPP intervention;
- Adaptive burst mode for advanced power management in light load conditions;
- Frequency jittering for EMI suppression.

Enhanced system reliability is ensured by the built-in soft-start function and by the following set of protections:

- Input OVP (settable);
- Brown-in and brown-out (settable);
- Output OVP (settable);
- Output overload;
- OCP LEB:
- Embedded thermal shutdown.

The EVLVIPGAN50WF is composed of a main board and a daughter board, with schematics shown in Figure 1 and Figure 2 respectively.

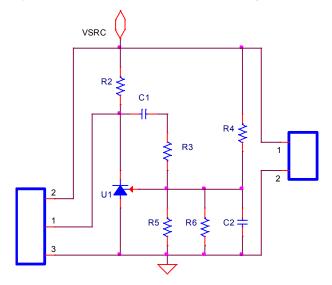
The main board contains a diode bridge for double wave rectification, an input pi filter for EMI, a flyback transformer, the VIPERGAN50W and all the related components needed for polarization and feature setting on the primary side. On the secondary side, it contains the output capacitors and the output rectifier, realized by a Power MOSFET driven by a synchronous rectifier for efficiency optimization.



Schematic diagram

Figure 1. EVLVIPGAN50WF schematic (main board)





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Revision history

Table 1. Document revision history

Date	Version	Changes
22-Sep-2025	1	Initial release.

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