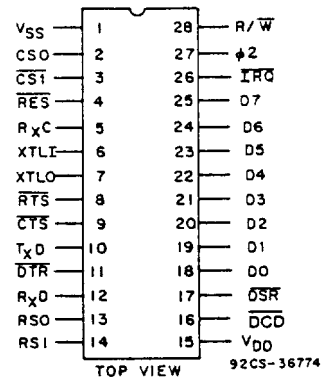
389-705

GE Solid State

GE/RCA Products

**Advance Information**

**TERMINAL ASSIGNMENT**




# CMOS Asynchronous Communications Interface Adapter (ACIA)

**Features:**

- *Compatible with 8-bit microprocessors*
- *Full duplex operation with buffered receiver and transmitter*
- *Data set/modem control functions*
- *Internal baud-rate generator with 15 programmable baud rates (50 to 19,200)*
- *Program-selectable internally or externally controlled receiver rate*
- *Operates at baud rates up to 250,000 via proper crystal or clock selection*
- *Programmable word lengths, number of stop bits, and parity-bit generation and detection*
- *Programmable interrupt control*
- *Program reset*
- *Program-selectable serial echo mode*
- *Two chip selects*
- *4-MHz, 2 MHz or 1 MHz operation (CDP65C51-4, CDP65C51-2, CDP65C51-1, respectively)*
- *Single 3 V to 6 V power supply*
- *Full TTL compatibility*

The RCA-CDP65C51 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program-controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The CDP65C51 has an internal baud-rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or 1/16 times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at 1/16 times an external clock rate. The CDP65C51 has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, 1½, or 2 stop bits.

The **Status Register** indicates the states of the $\overline{IRQ}$, $\overline{DSR}$, and $\overline{DCD}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

## CDP65C51 OPERATION (Cont'd)

### Overrun in Echo Mode (Fig. 14)

If Overrun occurs in Echo Mode, the Receiver is affected the same way as described in "Effect of Overrun on Receiver".

For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor.

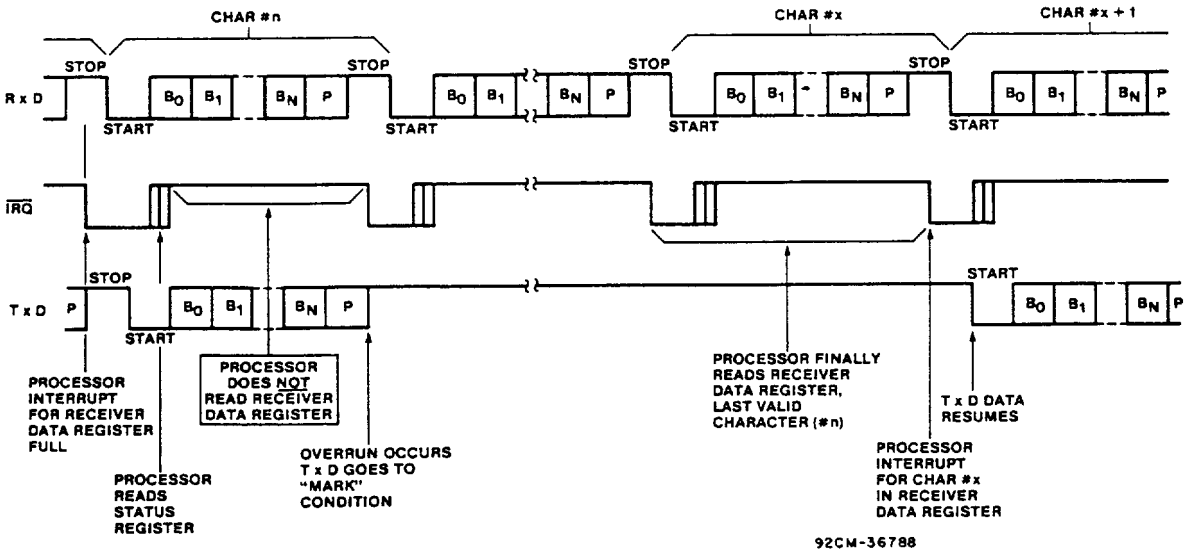



*Fig. 14 - Overrun in echo mode.*

### Framing Error (Fig. 15)

Framing Error is caused by the absence of Stop Bit(s) on received data. The status bit is set when the processor interrupt occurs. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received.

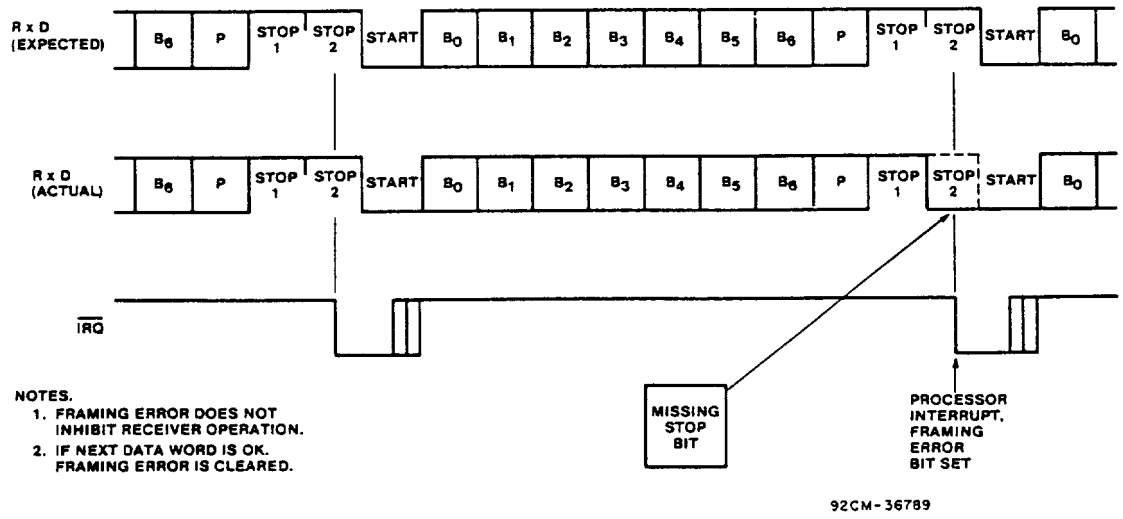



*Fig. 15 - Framing error.*

## CDP65C51 OPERATION (Cont'd)

### Effect of $\overline{DCD}$ on Receiver (Fig. 16)

$\overline{DCD}$ is a modem output used to indicate the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs,

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register

## CDP65C51 OPERATION (Cont'd)

### Receive Continuous "BREAK" (Fig. 19)

In the event the modem transmits continuous "BREAK" characters, the CDP65C51 will terminate receiving. Reception will resume only after a Stop Bit is encountered by the CDP65C51.

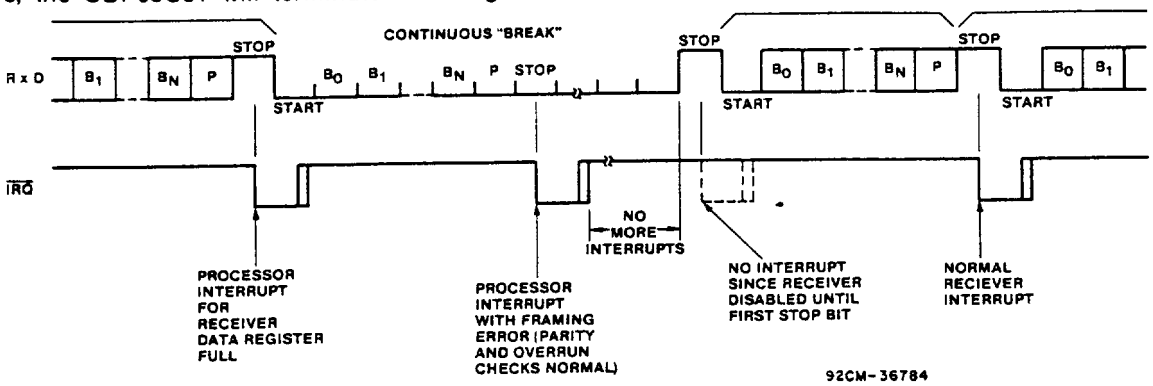



*Fig. 19 - Receive continuous "BREAK".*

### STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the CDP65C51 should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 (IRQ). Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.

2. Check IRQ Bit

   If not set, interrupt source is not the CDP65C51.

3. Check $\overline{DCD}$ and $\overline{DSR}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both "0" (modem "on-line") and they are unchanged then the remaining bits must be checked.

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2)

   Only if Receiver Data Register is Full.

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

7. If none of the above, then $\overline{CTS}$ must have gone to the False (high) state.

### PROGRAMMED RESET OPERATION

A program reset occurs when the processor performs a write operation to the CDP65C51 with RS0 high and RS1 low. The program reset operates somewhat different from the hardware reset ($\overline{RES}$ pin) and is described as follows:

1. Internal registers are not completely cleared. The data sheet indicates the effect of a program reset on internal registers.
2. The $\overline{DTR}$ line goes high immediately.
3. Receiver and transmitter interrupts are disabled immediately. If $\overline{IRQ}$ is low when the reset occurs, it stays low until serviced, unless interrupt was caused by $\overline{DCD}$ or $\overline{DSR}$ transition.
4. $\overline{DCD}$ and $\overline{DSR}$ interrupts disabled immediately. If $\overline{IRQ}$ is low and was caused by $\overline{DCD}$ or $\overline{DSR}$, then it goes high, also $\overline{DCD}$ and $\overline{DSR}$ status bits subsequently will follow the input lines, although no interrupt will occur.
5. Overrun cleared, if set.

### MISCELLANEOUS NOTES ON OPERATION

1. If Echo Mode is selected, $\overline{RTS}$ goes low.
2. If Bit 0 of Command Register is "0" (disabled), then:
   a) All interrupts disabled, including those caused by $\overline{DCD}$ and $\overline{DSR}$ transitions.
   b) Receiver disabled, but a character currently being received will be completed first.
   c) Transmitter is disabled after both the Transmit Data and Transmit Shift Registers have been emptied.
3. Odd parity occurs when the sum of all the "1" bits in the data word (including the parity bit) is odd.
4. In the Receive Mode, the received parity bit does not go into the Receiver Data Register, but is used to generate parity error for the Status Register.
5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.
6. If the RxD line inadvertently goes low and then high during the first 9 receiver clocks after a Stop Bit; a false Start Bit will result.

   For false Start Bit detection, the CDP65C51 does not begin to receive data, instead, only a true Start Bit initiates receiver operation.
7. A precaution to consider with the crystal oscillator circuit is:
   The XTLI input may be used as an external clock input. The XTLO pin must be floating and may not be used for any other function.
8. $\overline{DCD}$ and $\overline{DSR}$ transitions, although causing immediate processor interrupts, have no effect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be terminated either to Gnd or $V_{DD}$.

### GENERATION OF NON-STANDARD BAUD RATES

#### Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the CDP65C51 Control Register.

The divisors, then, are determined by bits 0-3 in the Control Register and their values are shown in Table II.

## CDP65C51 OPERATION (Cont'd)

**Table II - Divisor Selection for the CDP65C51**

| CONTROL REGISTER BITS | | | | DIVISOR SELECTED FOR THE INTERNAL COUNTER | BAUD RATE GENERATED WITH 1.8432 MHz | BAUD RATE GENERATED WITH FREQUENCY (F) |
|---|---|---|---|---|---|---|
| 3 | 2 | 1 | 0 | | | |
| 0 | 0 | 0 | 0 | No Divisor Selected | 1/16 of External Clock at Pin XTLI | 1/16 of External Clock at Pin XTLI |
| 0 | 0 | 0 | 1 | 36,864 | $\frac{1.8432 \times 10^6}{36,864} = 50$ | $\frac{F}{36,864}$ |
| 0 | 0 | 1 | 0 | 24,576 | $\frac{1.8432 \times 10^6}{24,576} = 75$ | $\frac{F}{24,576}$ |
| 0 | 0 | 1 | 1 | 16,768 | $\frac{1.8432 \times 10^6}{16,768} = 109.92$ | $\frac{F}{16,768}$ |
| 0 | 1 | 0 | 0 | 13,696 | $\frac{1.8432 \times 10^6}{13,696} = 134.58$ | $\frac{F}{13,696}$ |
| 0 | 1 | 0 | 1 | 12,288 | $\frac{1.8432 \times 10^6}{12,288} = 150$ | $\frac{F}{12,288}$ |
| 0 | 1 | 1 | 0 | 6,144 | $\frac{1.8432 \times 10^6}{6,144} = 300$ | $\frac{F}{6,144}$ |
| 0 | 1 | 1 | 1 | 3,072 | $\frac{1.8432 \times 10^6}{3,072} = 600$ | $\frac{F}{3,072}$ |
| 1 | 0 | 0 | 0 | 1,536 | $\frac{1.8432 \times 10^6}{1,536} = 1200$ | $\frac{F}{1,536}$ |
| 1 | 0 | 0 | 1 | 1,024 | $\frac{1.8432 \times 10^6}{1,024} = 1800$ | $\frac{F}{1,024}$ |
| 1 | 0 | 1 | 0 | 768 | $\frac{1.8432 \times 10^6}{768} = 2400$ | $\frac{F}{768}$ |
| 1 | 0 | 1 | 1 | 512 | $\frac{1.8432 \times 10^6}{512} = 3600$ | $\frac{F}{512}$ |
| 1 | 1 | 0 | 0 | 384 | $\frac{1.8432 \times 10^6}{384} = 4800$ | $\frac{F}{384}$ |
| 1 | 1 | 0 | 1 | 256 | $\frac{1.8432 \times 10^6}{256} = 7200$ | $\frac{F}{256}$ |
| 1 | 1 | 1 | 0 | 192 | $\frac{1.8432 \times 10^6}{192} = 9600$ | $\frac{F}{192}$ |
| 1 | 1 | 1 | 1 | 96 | $\frac{1.8432 \times 10^6}{96} = 19200$ | $\frac{F}{96}$ |

**Generating Other Baud Rates**

By using a different crystal, other baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the CDP65C51 with an off-chip oscillator to achieve the same thing. In this case, XTLI (pin 6) must be the clock input and XTLO (pin 7) must be a no-connect.

### DIAGNOSTIC LOOP—BACK OPERATING MODES

A simplified block diagram for a system incorporating a CDP65C51 ACIA is shown in Fig. 20.

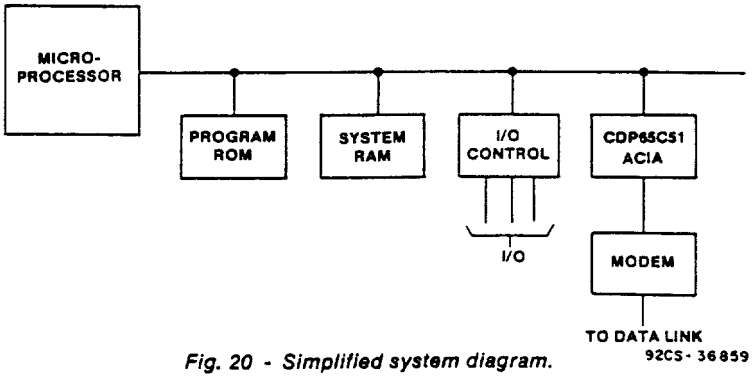



*Fig. 20 - Simplified system diagram.*

## CDP65C51 OPERATION (Cont'd)

Occasionally it may be desirable to include in the system a facility for "loop-back" diagnostic testing, of which there are two kinds.

1. Local Loop-Back

   Loop-back from the point of view of the processor. In this case, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

2. Remote Loop-Back

   Loop-back from the point of view of the Data Link and Modem. In this case, the processor, itself, is disconnected and all received data is immediately retransmitted, so the system on the other end of the Data Link may operate independent of the local system.

The CDP65C51 does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry.

Fig. 21 indicates the necessary logic to be used with the CDP65C51.

The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

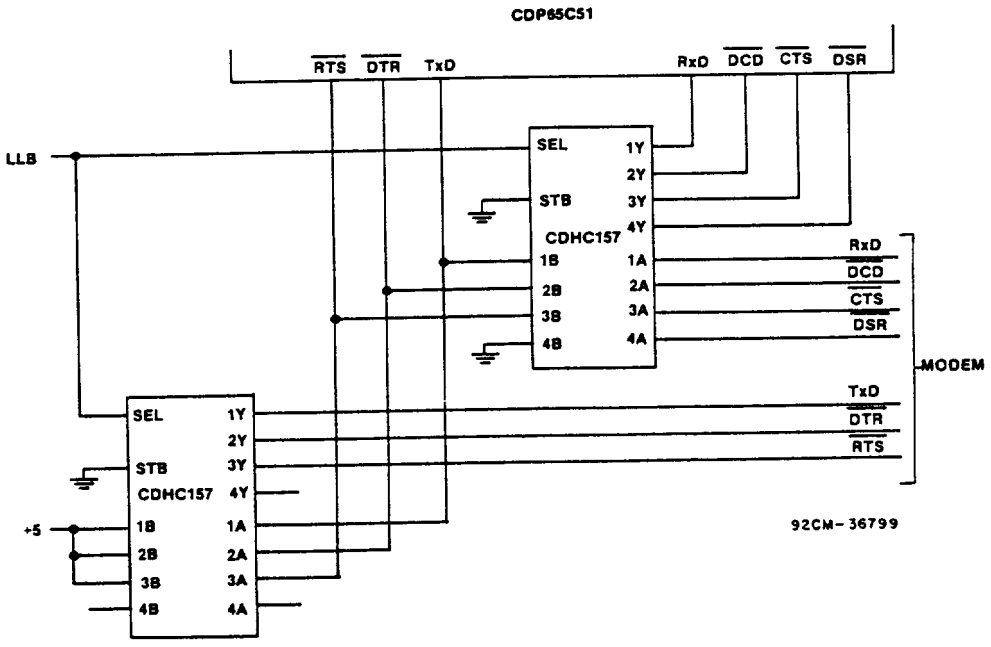
1. Disables outputs TxD, $\overline{DTR}$, and $\overline{RTS}$ (to Modem).
2. Disables inputs RxD, $\overline{DCD}$, $\overline{CTS}$, $\overline{DSR}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs:
   a) TxD to RxD
   b) $\overline{DTR}$ to $\overline{DCD}$
   c) $\overline{RTS}$ to $\overline{CTS}$

LLB may be tied to a peripheral control pin to provide processor control of local loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

Remote loop-back does not require this circuitry, so LLB must be set low. However, the processor must select the following:

1. Control Register bit 4 must be "1", so that the transmitter clock = receiver clock.
2. Command Register bit 4 must be "1" to select Echo Mode.
3. Command Register bits 3 and 2 must be "1" and "0", respectively, to disable transmitter interrupts.
4. Command Register bit 1 must be "0" to disable receiver interrupts.

In this way, the system retransmits received data without any effect on the local system.



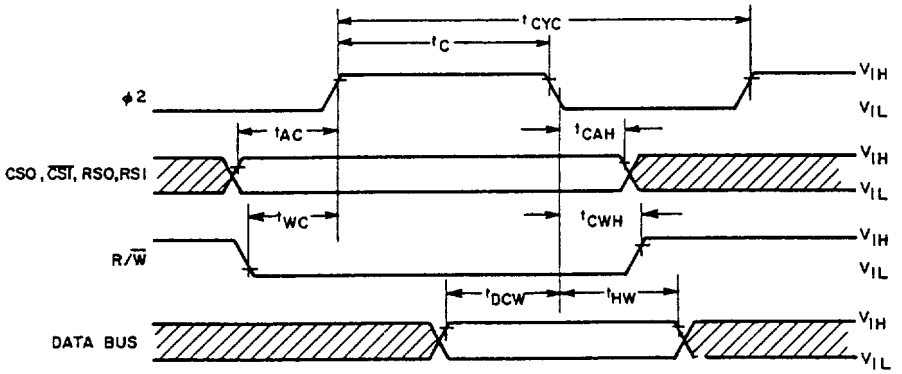

NOTES: 1. HIGH ON LLB SELECTS LOCAL LOOP-BACK MODE.
2. HIGH ON HC157 SELECT INPUT GATES "B" INPUTS TO "Y" OUTPUTS; LOW GATES "A" TO "Y".

*Fig. 21 - Loop-back circuit schematic.*

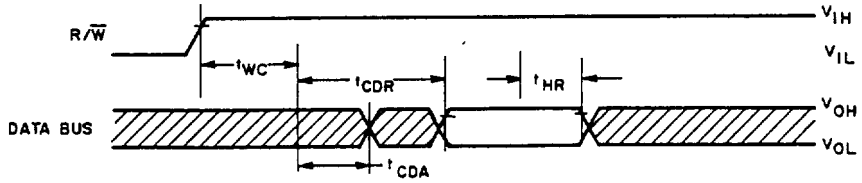
## DYNAMIC ELECTRICAL CHARACTERISTICS—READ/WRITE CYCLE

$V_{DD}$ = 5V ± 5%, $T_A$ = -40 to +85° C, $C_L$ = 75 pF

| CHARACTERISTIC | | LIMITS | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | CDP65C51-1 | | CDP65C51-2 | | CDP65C51-4 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Cycle Time | $t_{CYC}$ | 1 | — | 0.5 | — | 0.25 | — | μs |
| φ2 Pulse Width | $t_C$ | 400 | — | 200 | — | 100 | — | ns |
| Address Set-Up Time | $t_{AC}$ | 120 | — | 60 | — | 30 | — | ns |
| Address Hold Time | $t_{CAH}$ | 0 | — | 0 | — | 0 | — | ns |
| R/$\overline{W}$ Set-Up Time | $t_{WC}$ | 120 | — | 60 | — | 30 | — | ns |
| R/$\overline{W}$ Hold Time | $t_{CWH}$ | 0 | — | 0 | — | 0 | — | ns |
| Data Bus Set-Up Time | $t_{DCW}$ | 120 | — | 60 | — | 35 | — | ns |
| Data Bus Hold Time | $t_{HW}$ | 20 | — | 10 | — | 5 | — | ns |
| Read Access Time (Valid Data) | $t_{CDR}$ | — | 200 | — | 150 | — | 50 | ns |
| Read Hold Time | $t_{HR}$ | 20 | — | 10 | — | 10 | — | ns |
| Bus Active Time (Invalid Data) | $t_{CDA}$ | 40 | — | 20 | — | 10 | — | ns |




**Write-timing waveforms**




**Read-timing waveforms**

92CM-36775

*Fig. 22 - Timing waveforms.*

**DYNAMIC ELECTRICAL CHARACTERISTICS—TRANSMIT/RECEIVE, See Figs. 23, 24 and 25.**
**$V_{DD}$ = 5V ± 5%, $T_A$ = -40 to +85° C**

| CHARACTERISTIC | | LIMITS | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | CDP65C51-1 | | CDP65C51-2 | | CDP65C51-4 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Transmit/Receive Clock Rate | $t_{CCY}$ | 400* | — | 325 | — | 250 | — | ns |
| Transmit/Receive Clock High Time | $t_{CH}$ | 175 | — | 145 | — | 110 | — | |
| Transmit/Receive Clock Low Time | $t_{CL}$ | 175 | — | 145 | — | 110 | — | |
| XTLI to TxD Propagation Delay | $t_{DD}$ | — | 500* | — | 410 | — | 315 | |
| $\overline{RTS}$ Propagation Delay | $t_{DLY}$ | — | 500 | — | 410 | — | 315 | |
| $\overline{IRQ}$ Propagation Delay (Clear) | $t_{\overline{IRQ}}$ | — | 500 | — | 410 | — | 315 | |
| $\overline{RES}$ Pulse Width | $t_{\overline{RES}}$ | 400 | — | 300 | — | 200 | — | |

($t_r, t_f$ = 10 to 30 ns)

*The baud rate with external clocking is: $\text{Baud Rate} = \frac{1}{16 \times T_{CCY}}$

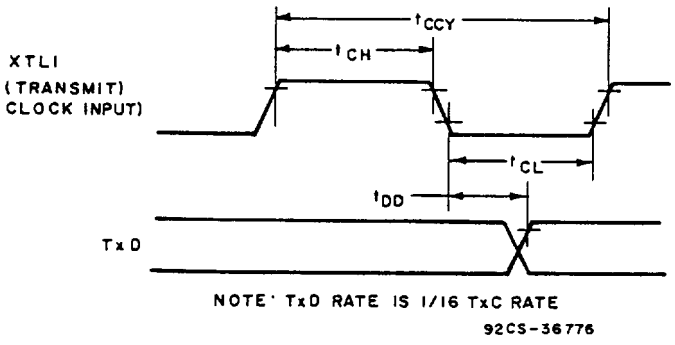



*Fig. 23 - Transmit-timing waveforms with external clock.*

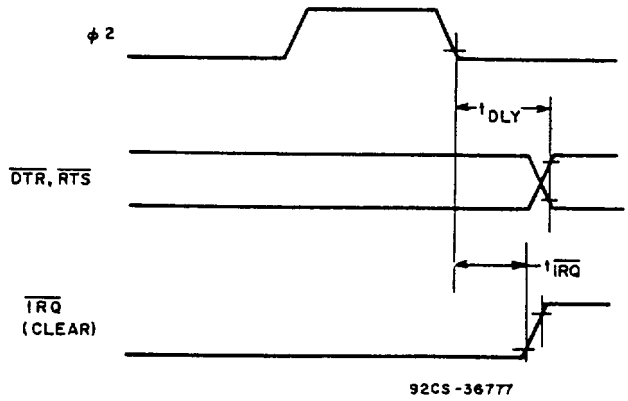



*Fig. 24 - Interrupt-and output-timing waveforms.*

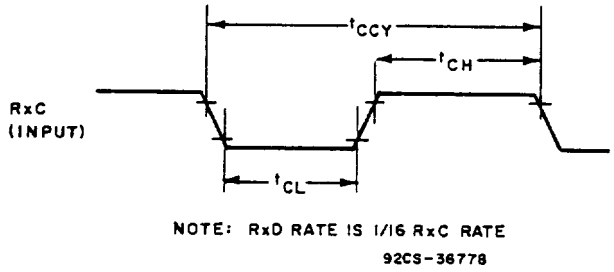



*Fig. 25 - Receive external clock timing waveforms.*

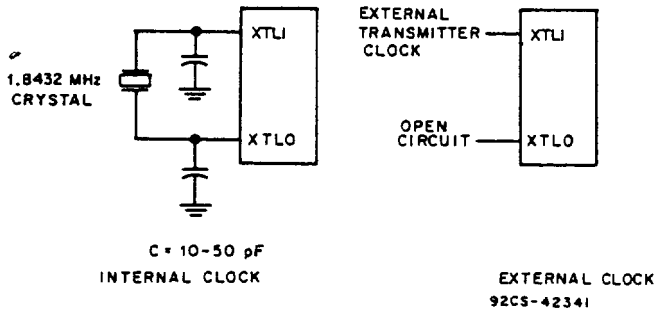



*Fig. 26 - Transmitter clock generation.*

## OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

**Operating Voltage**

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}$ - $V_{SS}$ to exceed the absolute maximum rating.

**Input Signals**

To prevent damage to the input protection circuit, input signals should never be greater than $V_{DD}$ nor less than $V_{SS}$.

**Unused Inputs**

Unless otherwise noted, all unused input terminals must be connected to either $V_{DD}$ or $V_{SS}$, whichever is appropriate.

**Output Short Circuits**

Shorting of outputs to $V_{DD}$ or $V_{SS}$ may damage CMOS devices by exceeding the maximum device dissipation.

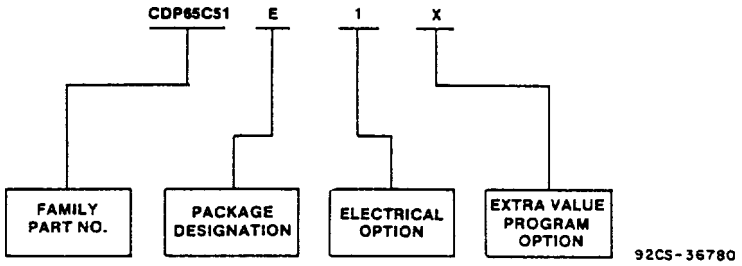
## ORDERING INFORMATION

The RCA-CDP65C51 family packages and electrical options are identified by suffix letters indicated in the following chart. When ordering a Memory/Microprocessor device, it is important that the appropriate suffix letter be affixed to the type number of the device.

| Package/Option | Suffix Letter |
|---|---|
| Dual-In-Line Side-Brazed Ceramic | D |
| Dual-In-Line Plastic | E |
| Small-Outline Plastic (SOP) | M |
| Chip (when applicable) | H |

| Package/Option | Suffix Letter |
|---|---|
| EVP Screening (Extra Value Program) i.e., Burn-In - optional for D, E package types | X |

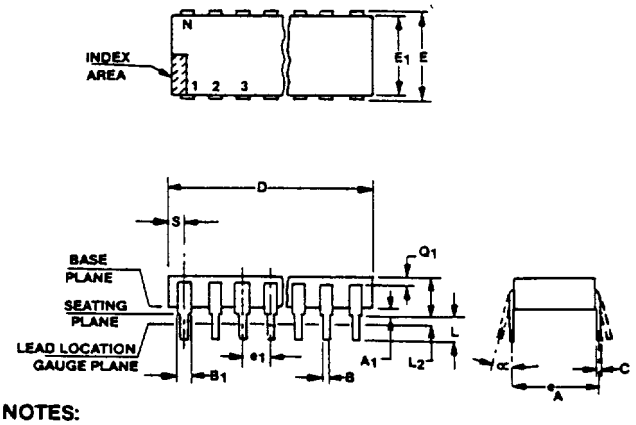
For example, a CDP65C51-1 in a dual-in-line plastic package will be identified as the CDP65C51E1. A CDP65C51E1 with EVP screening option will be identified as the CDP65C51E1X.




## DIMENSIONAL OUTLINES

### (D) Suffix (JEDEC MO-038-AB)

### 28-Lead Dual-In-Line Side-Brazed Ceramic Package




| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .085 | .190 | 2.2 | 4.8 | 9 |
| $A_1$ | .020 | .070 | .51 | 1.77 | 9 |
| B | .015 | .023 | .381 | .584 | |
| $B_1$ | .038 | .060 | .97 | 1.52 | |
| C | .008 | .012 | .204 | .304 | |
| D | 1.380 | 1.430 | 35.06 | 36.22 | |
| E | .595 | .625 | 15.12 | 15.87 | |
| $E_1$ | 0.580 | .610 | 14.74 | 15.49 | 8 |
| $e_1$ | .100 TP | | 2.54 TP | | 3, 4 |
| $e_A$ | .600 TP | | 15.24 TP | | 3, 4 |
| L | .125 | .175 | 3.18 | 4.44 | 9 |
| $L_2$ | .000 | .030 | .00 | .76 | |
| α | 0° | 15° | 0° | 15° | |
| N | 28 | | 28 | | |
| $Q_1$ | .010 | — | .25 | — | |
| S | .030 | .065 | .77 | 1.65 | |

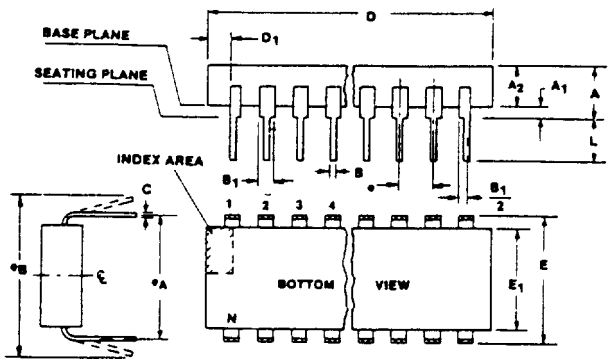
92CS-42884

NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5 1982.
3. Leads within .13mm (.005 in.) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
4. $e_1$ and $e_A$ applies in zone $L_2$ when unit installed.
5. α applies to spread leads prior to installation.
6. N is the number of terminal positions.
7. Outlines on which the seating plane is coincident with the base plane ($A_1$ = 0), terminals lead standoffs are not required, and $B_1$ may equal B along any part of the lead above the seating/base plane.
8. $E_1$ does not include particles of package materials.
9. This dimension shall be measured with the device seated in the seating plane gauge JEDEC Outline No. GS-3.
10. Controlling Dimension: INCH.

## DIMENSIONAL OUTLINES (Continued)

### (E) Suffix (JEDEC MS-011-AB)
### 28-Lead Dual-In-Line Plastic Package




| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | — | 0.250 | — | 6.35 | 9 |
| $A_1$ | 0.015 | — | 0.39 | — | 9 |
| $A_2$ | 0.125 | 0.195 | 3.18 | 4.95 | |
| B | 0.014 | 0.022 | 0.356 | 0.558 | |
| $B_1$ | 0.030 | 0.070 | 0.77 | 1.77 | 3 |
| C | 0.008 | 0.015 | 0.204 | 0.381 | |
| D | 1.380 | 1.565 | 35.1 | 39.7 | 4 |
| $D_1$ | 0.005 | — | 0.13 | — | 12 |
| E | 0.600 | 0.625 | 15.24 | 15.87 | 5 |
| $E_1$ | 0.485 | 0.580 | 12.32 | 14.73 | 6, 7 |
| e | 0.100 BSC | | 2.54 BSC | | 8 |
| $e_A$ | 0.600 BSC | | 15.24 BSC | | 9 |
| $e_B$ | — | 0.700 | — | 17.78 | 10 |
| L | 0.115 | 0.200 | 2.93 | 5.08 | 9 |
| N | 28 | | 28 | | 11 |

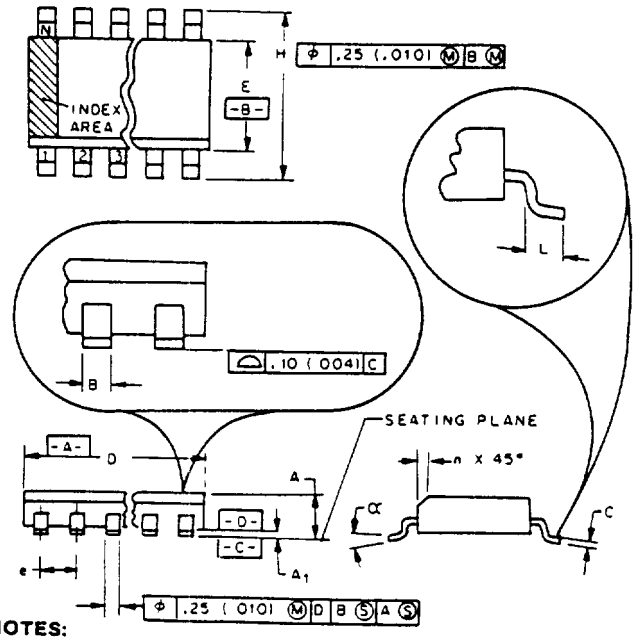
92CS-40001

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

   1, N, $\frac{N}{2}$ $\frac{N}{2}$+1.
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension $E_1$ does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension $e_A$.
10. $e_B$ is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension $D_1$ at the left end of the package must equal dimension $D_1$ at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

### M Suffix (JEDEC MS-013AE)
### 28-Lead Dual-In-Line Small-Outline (SO) Package




| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | 0.0926 | 0.1043 | 2.35 | 2.65 | |
| $A_1$ | 0.004 | 0.0118 | 0.1 | 0.3 | |
| B | 0.0138 | 0.02 | 0.35 | 0.508 | |
| C | 0.0091 | 0.0125 | 0.23 | 0.32 | |
| D | 0.6969 | 0.7125 | 17.7 | 18.1 | 4 |
| E | 0.2914 | 0.2992 | 7.4 | 7.6 | 4 |
| e | 0.05 BSC | | 1.27 BSC | | |
| H | 0.394 | 0.419 | 10.0 | 10.65 | |
| h | 0.01 | 0.029 | 0.25 | 0.75 | 5 |
| L | 0.016 | 0.05 | 0.4 | 1.27 | 6 |
| N | 28 | | 28 | | 7 |
| α | 0° | 8° | 0° | 8° | |

Notes: 1, 2, 3, 8, 9

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NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "D" is a reference datum.
4. "A" and "B" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

**GE Solid State**
*Somerville, NJ • Brussels • Paris • London • Munich • Hong Kong • Tokyo*
GE/RCA/Intersil Semiconductors

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltage referenced to $V_{SS}$ terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to $V_{DD}$ +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A$ = -55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For $T_A$ = +100 to +125°C (PACKAGE TYPE D) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A$ = -40 to +85°C (PACKAGE TYPE M)* ..... 425 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW

OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE D ..... -55 to +125°C
PACKAGE TYPE E and M ..... -40 to +85°C
STORAGE-TEMPERATURE RANGE ($T_{stg}$) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING).
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

**RECOMMENDED OPERATING CONDITIONS at $T_A$ = -40° to +85°C**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | Min. | Max. | |
| DC Operating Voltage Range | 3 | 6 | V |
| Input Voltage Range | $V_{SS}$ | $V_{DD}$ | |

**STATIC ELECTRICAL CHARACTERISTICS at $T_A$ = -40° to +85°C, $V_{DD}$ = 5V ± 5%**

| CHARACTERISTIC | | LIMITS | | | UNITS |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Quiescent Device Current | $I_{DD}$ | — | 50 | 200 | μA |
| Output Low Current (Sinking): $V_{OL}$ = 0.4 V (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$ | $I_{OL}$ | 1.6 | — | — | mA |
| Output High Current (Sourcing): $V_{OH}$ = 4.6 V (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$) | $I_{OH}$ | -1.6 | — | — | mA |
| Output Low Voltage: $I_{LOAD}$ = 1.6 mA (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$) | $V_{OL}$ | — | — | 0.4 | V |
| Output High Voltage: $I_{LOAD}$ = -1.6 mA (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$) | $V_{OH}$ | 4.6 | — | — | V |
| Input Low Voltage | $V_{IL}$ | $V_{SS}$ | — | 0.8 | V |
| Input High Voltage<br>(Except XTLI and XTLO)<br>(XTLI and XTLO) | $V_{IH}$ | <br>2<br>3 | <br>—<br>— | <br>$V_{DD}$<br>$V_{DD}$ | V |
| Input Leakage Current: $V_{IN}$ = 0 to 5 V ($\phi$2, R/$\overline{W}$, $\overline{RES}$, CS0, $\overline{CS1}$, RS0, RS1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$) | $I_{IN}$ | — | — | ±1 | μA |
| Input Leakage Current for High Impedance State (D0-D7) | $I_{TSI}$ | — | — | ±1.2 | μA |
| Output Leakage Current (off state): $V_{OUT}$ = 5 V ($\overline{IRQ}$) | $I_{OFF}$ | — | — | 2 | μA |
| Input Capacitance (except XTLI and XTLO) | $C_{IN}$ | — | — | 10 | pF |
| Output Capacitance | $C_{OUT}$ | — | — | 10 | pF |

## CDP65C51 INTERFACE REQUIREMENTS

This section describes the interface requirements for the CDP65C51 ACIA. Fig. 1 is the Interface Diagram and the Terminal Diagram shows the pin-out configuration for the CDP65C51.

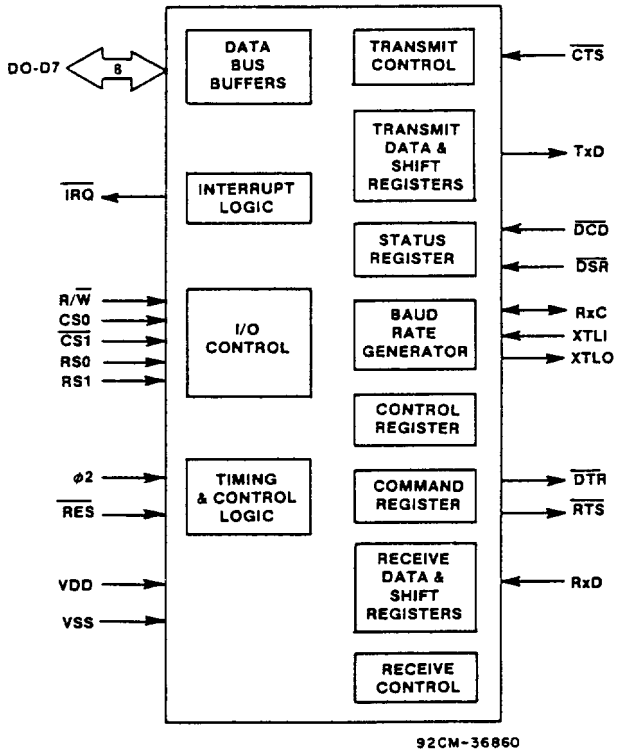



*Fig. 1 - CDP65C51 interface diagram.*

### MICROPROCESSOR INTERFACE SIGNAL DESCRIPTION

**$\overline{RES}$ (Reset) (4)**

During system initialization a low on the $\overline{RES}$ input will cause a hardware reset to occur. The Command Register and the Control Register will be cleared. The Status Register will be cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the $\overline{DSR}$ and $\overline{DCD}$ lines, and the transmitter Empty bit, which will be set. A hardware reset is required after power-up.

**$\phi$2 (Input Clock) (27)**

The input clock is the system $\phi$2 clock and is used to clock all data transfers between the system microprocessor and the CDP65C51.

**R/$\overline{W}$ (Read/$\overline{Write}$) (28)**

The R/$\overline{W}$ input, generated by the microprocessor, is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the CDP65C51, a low allows a write to the CDP65C51

**$\overline{IRQ}$ (Interrupt Request) (26)**

The $\overline{IRQ}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally at high level, $\overline{IRQ}$ goes low when an interrupt occurs.

**D0-D7 (Data Bus) (18-25)**

The D0-D7 pins are the eight data lines used to transfer data between the processor and the CDP65C51. These lines are bi-directional and are normally high-impedance except during Read cycles when the CDP65C51 is selected

**CS0, $\overline{CS1}$ (Chip Selects) (2, 3)**

The two chip-select inputs are normally connected to the processor address lines either directly or through decoders. The CDP65C51 is selected when CS0 is high and $\overline{CS1}$ is low.

**RS0, RS1 (Register Selects) (13, 14)**

The two register-select lines are normally connected to the processor address lines to allow the processor to select the various CDP65C51 internal registers. The following table shows the internal register-select coding.

**TABLE I**

| RS1 | RS0 | Write | Read |
|---|---|---|---|
| 0 | 0 | Transmit Data Register | Receiver Data Register |
| 0 | 1 | Programmed Reset (Data is "Don't Care") | Status Register |
| 1 | 0 | Command Register | |
| 1 | 1 | Control Register | |

Only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command Register and bit 2 in the Status Register. The Control Register is unchanged by a Programmed Reset. It should be noted that the Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$); these differences are shown in Figs. 3, 4 and 5.

### ACIA/MODEM INTERFACE SIGNAL DESCRIPTION

**XTLI, XTLO (Crystal Pins) (6, 7)**

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates (see "Generation of Non-Standard Baud Rates"). Alternatively, an externally generated clock may be used to drive the XTLI pin, in which case the XTLO pin must float XTLI is the input pin for the transmit clock.

**TxD (Transmit Data) (10)**

The TxD output line is used to transfer serial NRZ (nonreturn-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or under control of an external clock. This selection is made by programming the Control Register

**RxD (Receive Data) (12)**

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or under the control of an externally generated receiver clock. The selection is made by programming the Control Register.

## CDP65C51 INTERFACE REQUIREMENTS (Cont'd)

**RxC (Receive Clock) (5)**

The RxC is a bidirectional pin which serves as either the receiver 16X clock input or the receiver 16X clock output. The latter mode results if the internal baud-rate generator is selected for receiver data clocking.

**$\overline{RTS}$ (Request to Send) (8)**

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

**$\overline{CTS}$ (Clear to Send) (9)**

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

**$\overline{DTR}$ (Data Terminal Ready) (11)**

This output pin is used to indicate the status of the CDP65C51 to the modem. A low on $\overline{DTR}$ indicates the CDP65C51 is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

**$\overline{DSR}$ (Data Set Ready) (17)**

The $\overline{DSR}$ input pin is used to indicate to the CDP65C51 the status of the modem. A low indicates the "ready" state and a high, "not-ready".

**$\overline{DCD}$ (Data Carrier Detect) (16)**

The $\overline{DCD}$ input pin is used to indicate to the CDP65C51 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

## CDP65C51 INTERNAL ORGANIZATION

This section provides a functional description of the CDP65C51. A block diagram of the CDP65C51 is presented in Fig. 2.

### DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bidirectional. When the R/$\overline{W}$ line is high and the chip is selected, the Data Bus Buffer passes the data to the system data lines from the CDP65C51 internal data bus. When the R/$\overline{W}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the system data bus to the internal data bus.

### INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{IRQ}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{DCD}$) logic and the Data Set Ready ($\overline{DSR}$) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

### I/O CONTROL

The I/O Control Logic controls the selection of internal registers in preparation for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Register Select and Chip Select and Read/Write lines as described in Table I, previously.

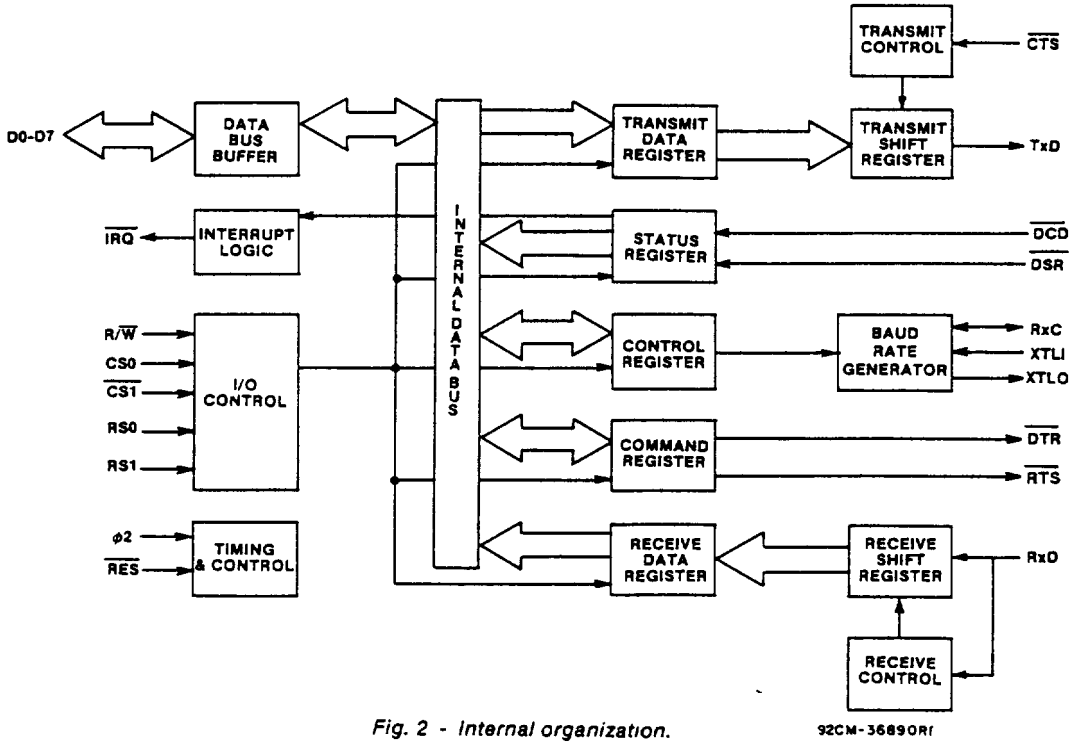



*Fig. 2 - Internal organization.* 92CM-36890R1

## CDP65C51 INTERNAL ORGANIZATION (Cont'd)

### TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus and the registers, the Data Bus Buffer, and the microprocessor data bus, and the hardware reset features.

Timing is controlled by the system $\phi 2$ clock input. The chip will perform data transfers to or from the microcomputer data bus during the $\phi 2$ high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{RES}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

### TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the CDP65C51 Transmit and Receive circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care"

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

### STATUS REGISTER

Fig. 3 indicates the format of the CDP65C51 Status Register. A description of each status bit follows.

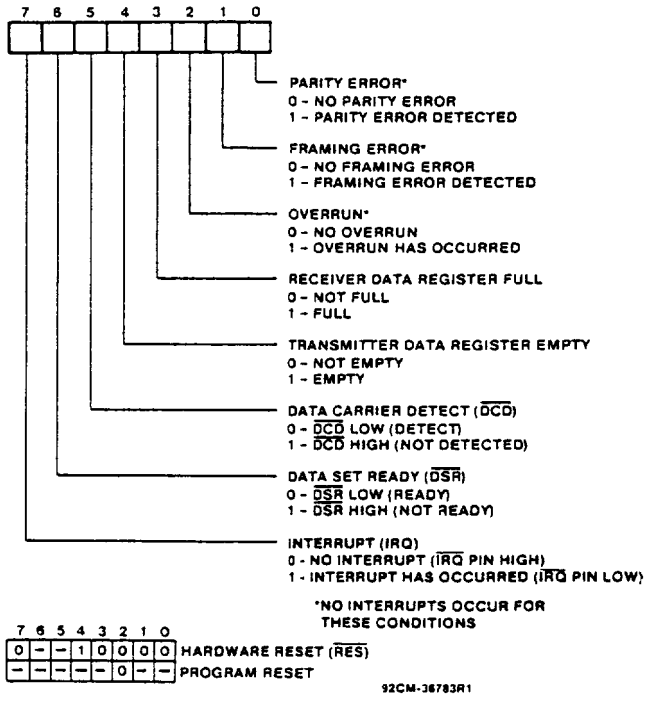



*Fig. 3 - Status register format.*

**Receiver Data Register Full (Bit 3)**

This bit goes to a "1" when the CDP65C51 transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a "0" when the processor reads the Receiver Data Register.

**Transmitter Data Register Empty (Bit 4)**

This bit goes to a "1" when the CDP65C51 transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a "0" when the processor writes new data onto the Transmitter Data Register.

**Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)**

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the CDP65C51. A "0" indicates a low level (true condition) and a "1" indicates a high (false). Whenever either of these inputs changes state, an immediate processor interrupt occurs, unless the CDP65C51 is disabled (bit 0 of the Command Register is a "0"). When the interrupt occurs, the status bits will indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until the Status Register is interrogated by the processor. At that time, another interrupt will immediately occur and the status bits will reflect the new input levels.

**Framing Error (Bit 1), Overrun (Bit 2), and Parity Error (Bit 0)**

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified.

**Interrupt (Bit 7)**

This bit goes to a "0" when the Status Register has been read by the processor, and goes to a "1" whenever any kind of interrupt occurs.

### CONTROL REGISTER

The Control Register selects the desired transmitter baud rate, receiver clock source, word length, and the number of stop bits.

**Selected Baud Rate (Bits 0, 1, 2, 3)**

These bits, set by the processor, select the Transmitter baud rate, which can be at 1/16 an external clock rate or one of 15 other rates controlled by the internal baud-rate generator as shown in Fig. 4.

**Receiver Clock Source (Bit 4)**

This bit controls the clock source to the Receiver. A "0" causes the Receiver to operate at a baud rate of 1/16 an external clock. A "1" causes the Receiver to operate at the same baud rate as is selected for the transmitter as shown in Fig. 4.

**Word Length (Bits 5, 6)**

These bits determine the word length to be used (5, 6, 7 or 8 bits). Fig. 4 shows the configuration for each number of bits desired.

**Stop Bit Number (Bit 7)**

This bit determines the number of stop bits used. A "0" always indicates one stop bit. A "1" indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, and 2 stop bits in all other configurations.

## CDP65C51 INTERNAL ORGANIZATION (Cont'd)

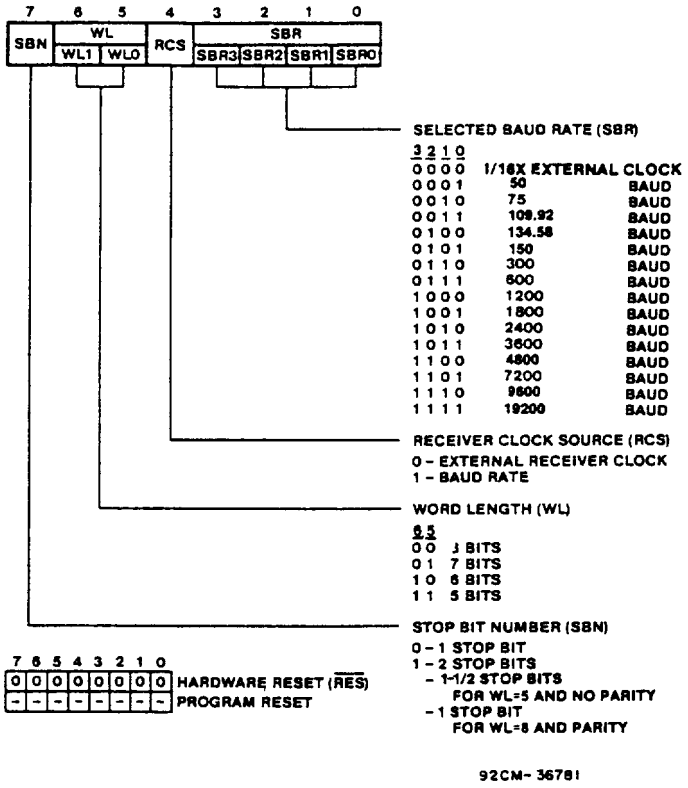



*Fig. 4 - CDP65C51 control register.*

### COMMAND REGISTER

The Command Register controls specific modes and functions (Fig. 5).

#### Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{DTR}$) line. A "0" indicates the microcomputer system is not ready by setting the $\overline{DTR}$ line high. A "1" indicates the microcomputer system is ready be setting the $\overline{DTR}$ line low. When the DTR bit is set to a "0", the receiver and transmitter are both disabled.

#### Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a "1". The Receiver interrupt is enabled when this bit is set to a "0" and Bit 0 is set to a "1".

#### Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{RTS}$) line and the Transmitter interrupt. Fig. 5 shows the various configurations of the $\overline{RTS}$ line and Transmit Interrupt bit settings.

#### Receiver Echo Mode (Bit 4)

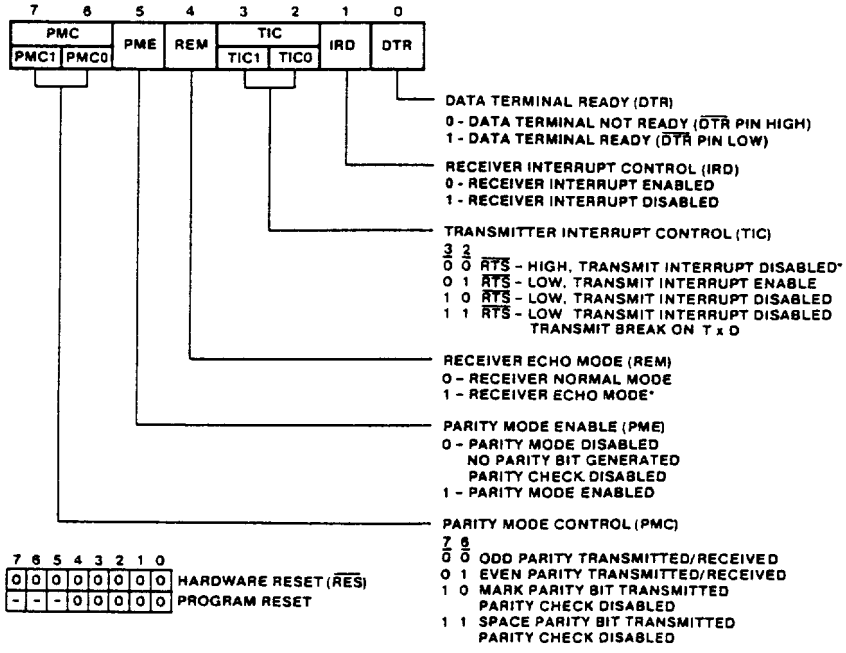
This bit enables the Receiver Echo Mode. Bits 2 and 3 must be zero. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by ½ bit time. A "1" enables the Receiver Echo Mode. A "0" bit disables the mode.

#### Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A "0" disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A "1" bit enables generation and checking of parity bits.

#### Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check). Fig. 5 shows the possible bit configurations for the Parity Mode Control bits.




*BITS 2 AND 3 MUST BE ZERO FOR RECEIVER ECHO MODE RTS WILL BE LOW

92CM-36790R1

*Fig. 5 - CDP65C51 command register.*

## CDP65C51 INTERNAL ORGANIZATION (Cont'd)

### TRANSMITTER AND RECEIVER

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the CDP65C51. Fig. 6 shows the Transmitter and Receiver layout.

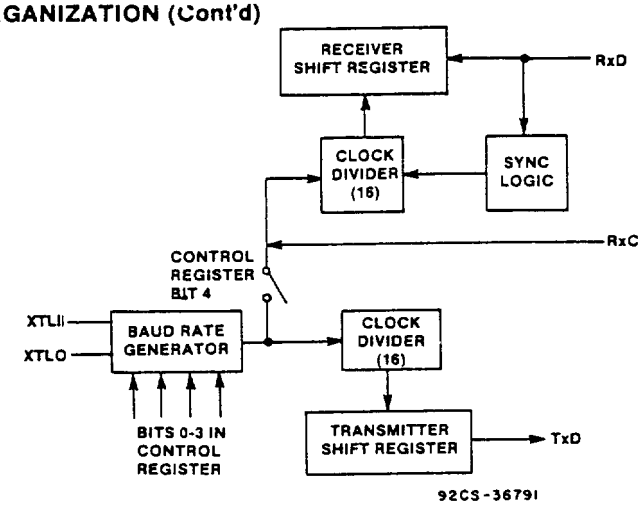



*Fig. 6 - Transmitter receiver clock circuits.*

## CDP65C51 OPERATION

### TRANSMITTER AND RECEIVER OPERATION

#### Continuous Data Transmit (Fig. 7)

In the normal operating mode, the processor interrupt ($\overline{IRQ}$) is used to signal when the CDP65C51 is ready to accept the next data word to be transmitted. This interrupt occurs at the beginnning of the Start Bit. When the processor reads the Status Register of the CDP65C51, the interrupt is cleared. The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted.

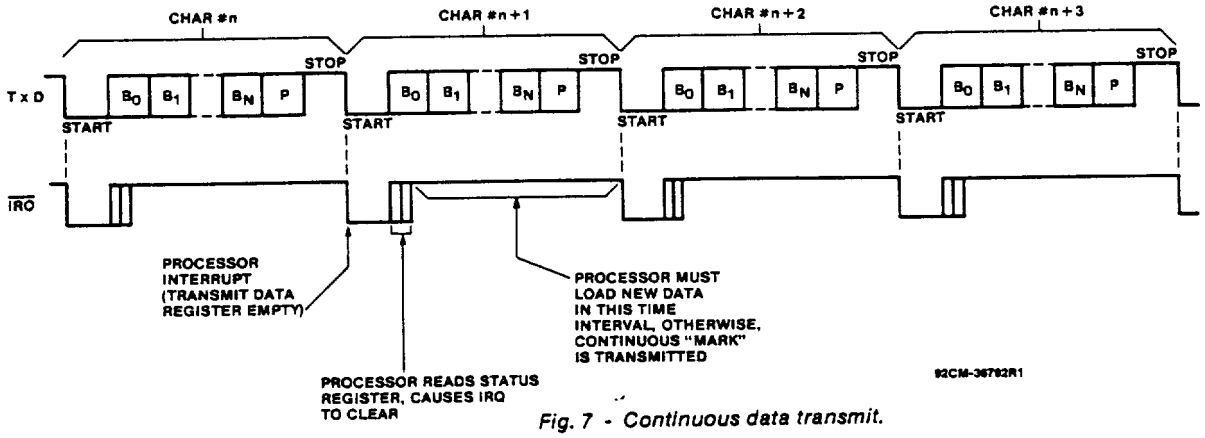



*Fig. 7 - Continuous data transmit.*

#### Continuous Data Receive (Fig. 8)

Similar to the above case, the normal mode is to generate a processor interrupt when the CDP65C51 has received a full data word. This occurs at about the 8/16 point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the Overrun condition occurs.

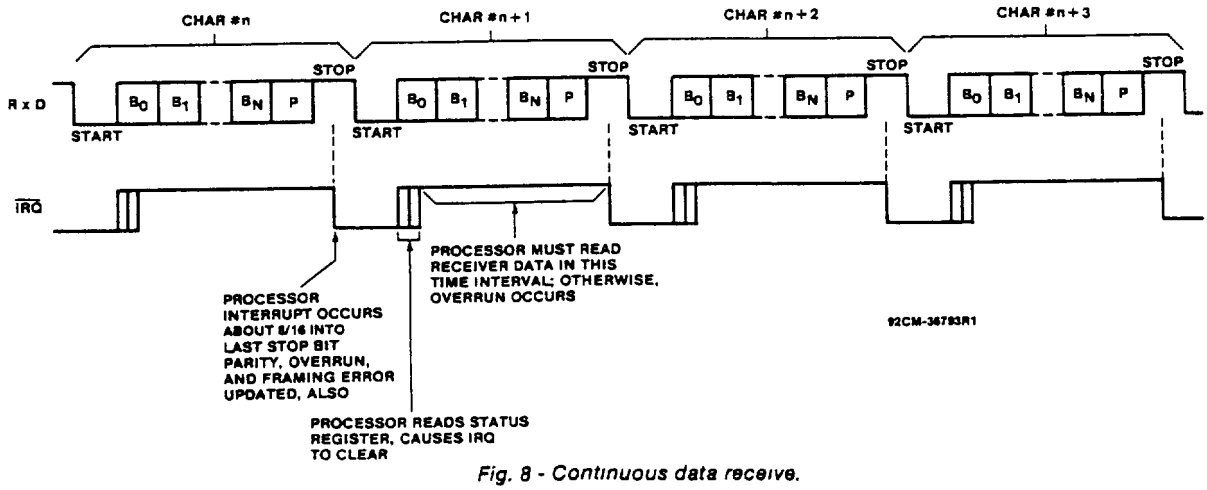



*Fig. 8 - Continuous data receive.*

## CDP65C51 OPERATION (Cont'd)

### Transmit Data Register Not Loaded By Processor (Fig. 9)

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line will go to the "MARK" condition until the data is loaded. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word.

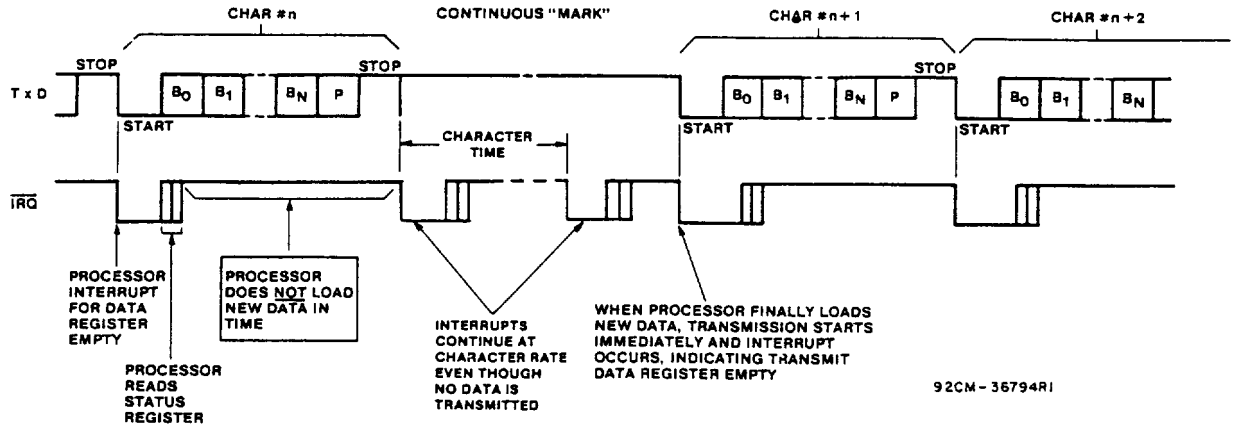



*Fig. 9 - Transmit data register not loaded by processor.*

### Effect of $\overline{CTS}$ on Transmitter (Fig. 10)

$\overline{CTS}$ is the Clear-to-Send signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line immediately goes to the "MARK" condition. Interrupts continue at the same rate, but the Status Register does not indicate that the Transmit Data Register is empty. Since there is no status bit for $\overline{CTS}$, the processor must deduce that $\overline{CTS}$ has gone to the False (high) state. This is covered later. $\overline{CTS}$ is a transmit control line only, and has no effect on the CDP65C51 Receiver Operation.

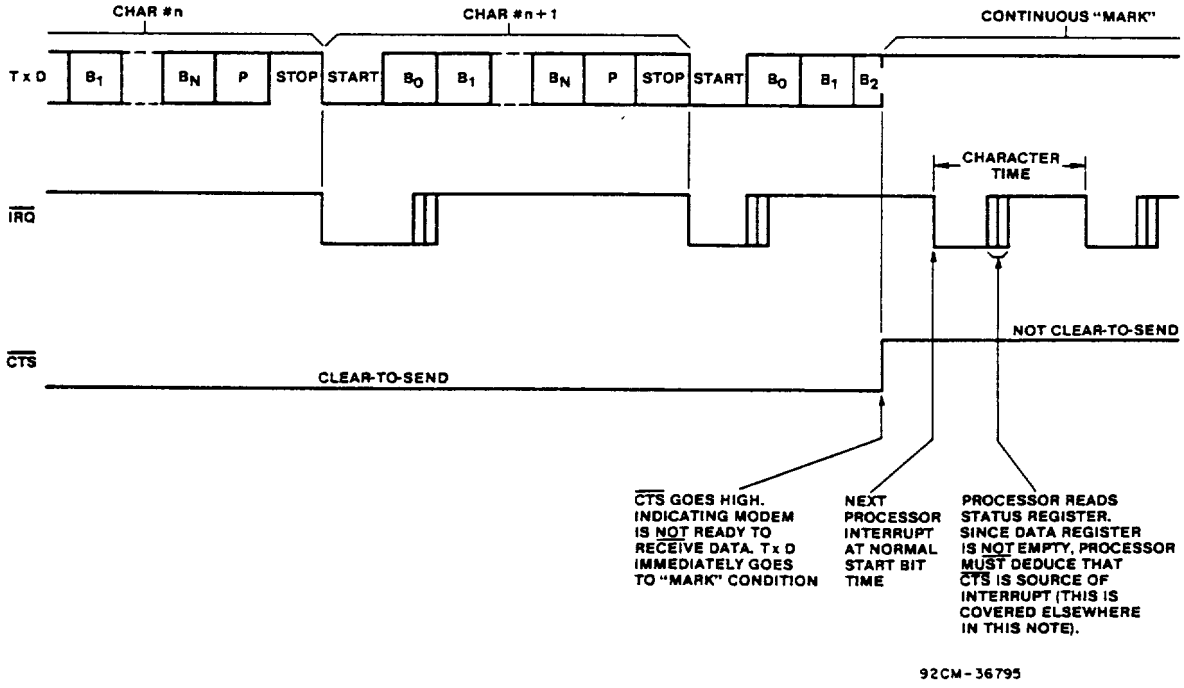



*Fig. 10 - Effect of $\overline{CTS}$ on transmitter.*

## CDP65C51 OPERATION (Cont'd)

### Effect of Overrun on Receiver (Fig. 11)

If the processor does not read the Receiver Data Register in the allocated time, then, when the following interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost.

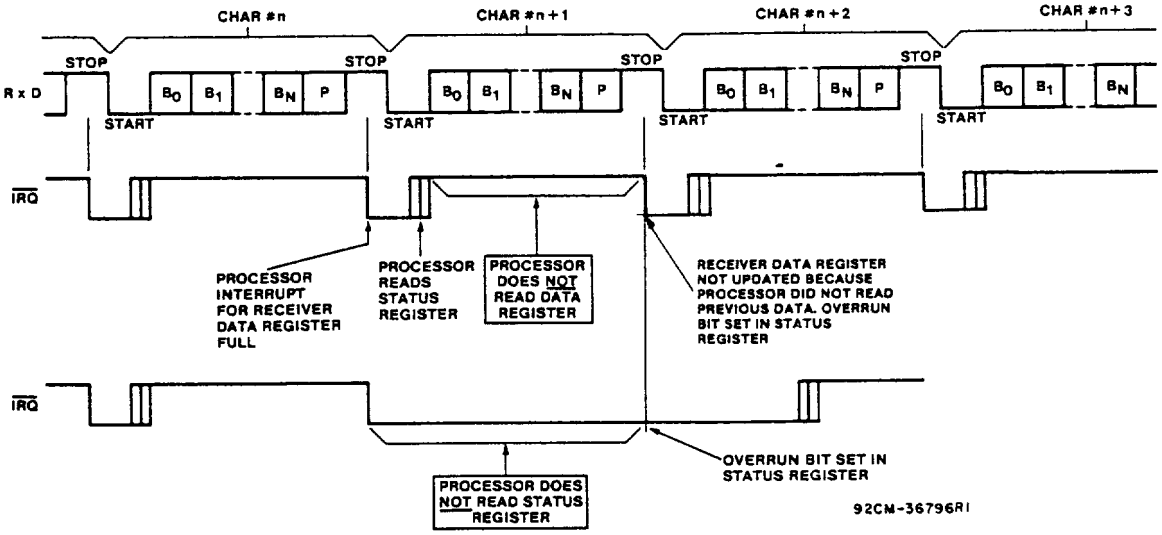



*Fig. 11 - Effect of overrun on receiver.*

### Echo Mode Timing (Fig. 12)

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by ½ of the bit time.

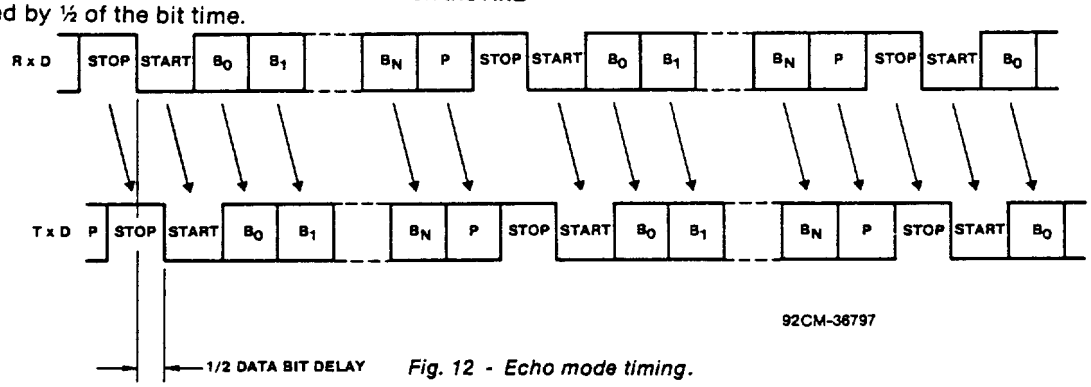



*Fig. 12 - Echo mode timing.*

### Effect of $\overline{CTS}$ on Echo Mode Operation (Fig. 13)

See "Effect of $\overline{CTS}$ on Transmitter" for the effect of $\overline{CTS}$ on the Transmitter. Receiver operation is unaffected by $\overline{CTS}$, so, in Echo Mode, the Transmitter is affected in the same way as "Effect of $\overline{CTS}$ on Transmitter". In this case however, the processor interrupts signify that the Receiver Data Register is full, so the processor has no way of knowing that the Transmitter has ceased to echo.

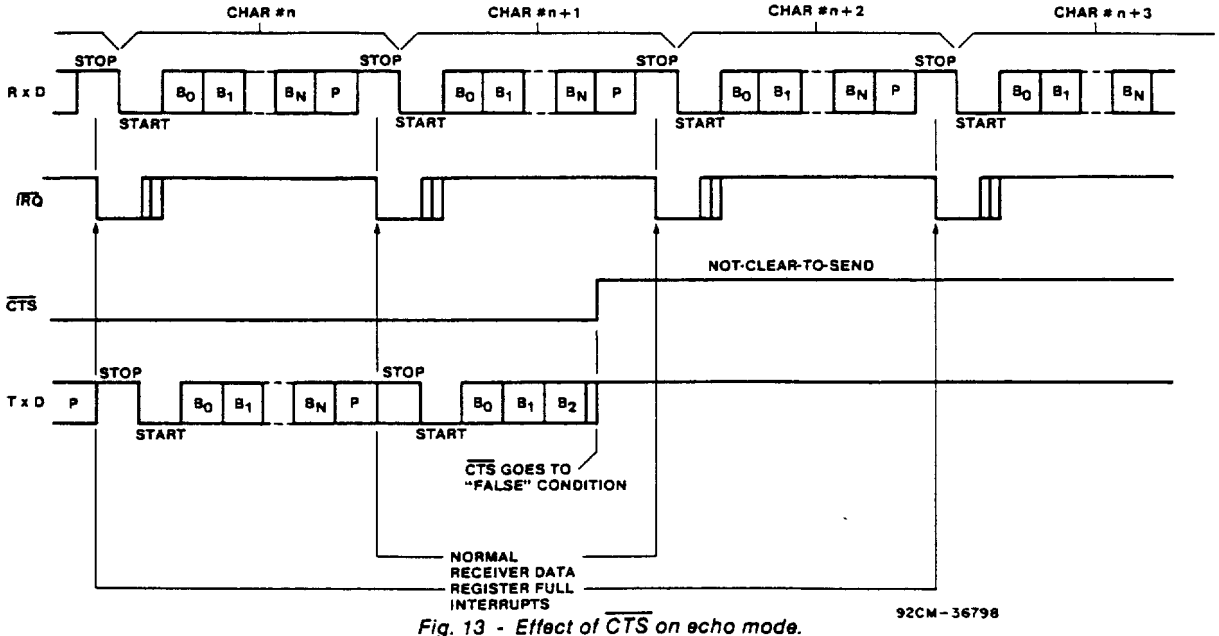



*Fig. 13 - Effect of $\overline{CTS}$ on echo mode.*