

MC74HC541A

Octal 3-State Non-Inverting Buffer/Line Driver/ Line Receiver High-Performance Silicon-Gate CMOS

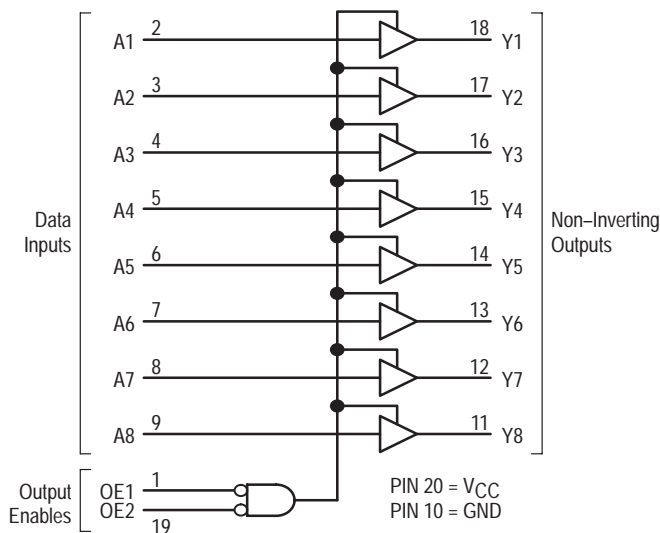
The MC74HC541A is identical in pinout to the LS541. The device inputs are compatible with Standard CMOS outputs. External pullup resistors make them compatible with LSTTL outputs.

The HC541A is an octal non-inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

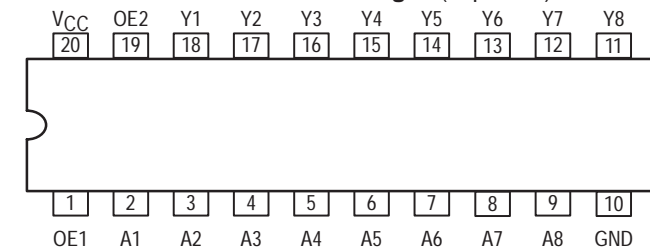
The HC541A is similar in function to the HC540A, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates

LOGIC DIAGRAM



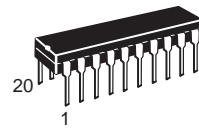
Pinout: 20-Lead Packages (Top View)



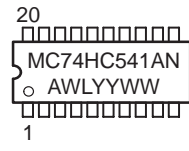
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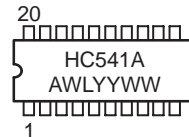
MARKING DIAGRAMS



PDIP-20
N SUFFIX
CASE 738



SOIC WIDE-20
DW SUFFIX
CASE 751D



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

FUNCTION TABLE

Inputs			Output Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = High Impedance
X = Don't Care

ORDERING INFORMATION

Device	Package	Shipping
MC74HC541AN	PDIP-20	1440 / Box
MC74HC541ADW	SOIC-WIDE	38 / Rail
MC74HC541ADWR2	SOIC-WIDE	1000 / Reel

MC74HC541A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
PD	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature Range	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP or SOIC Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature Range, All Package Types	- 55	+ 125	°C
t _r , t _f	Input Rise/Fall Time (Figure 1)	V _{CC} = 2.0 V 0 V _{CC} = 4.5 V 0 V _{CC} = 6.0 V 0	1000 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1V I _{out} ≤ 20μA	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = V _{CC} - 0.1V I _{out} ≤ 20μA	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IL} I _{out} ≤ 20μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} = V _{IL} I _{out} ≤ 3.6mA I _{out} ≤ 6.0mA I _{out} ≤ 7.8mA	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 20μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IH} I _{out} ≤ 3.6mA I _{out} ≤ 6.0mA I _{out} ≤ 7.8mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA

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DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
I _{OZ}	Maximum Three-State Leakage Current	Output in High Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0	80	100	120	ns
		3.0	30	40	55	
		4.5	18	23	28	
		6.0	15	20	25	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0	110	140	165	ns
		3.0	45	60	75	
		4.5	25	31	38	
		6.0	21	26	31	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0	110	140	165	ns
		3.0	45	60	75	
		4.5	25	31	38	
		6.0	21	26	31	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		3.0	22	28	34	
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance		10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High Impedance State)		15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Buffer)*	Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V	
			35

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

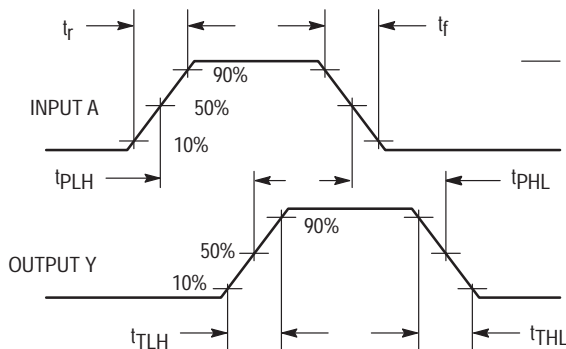


Figure 1.

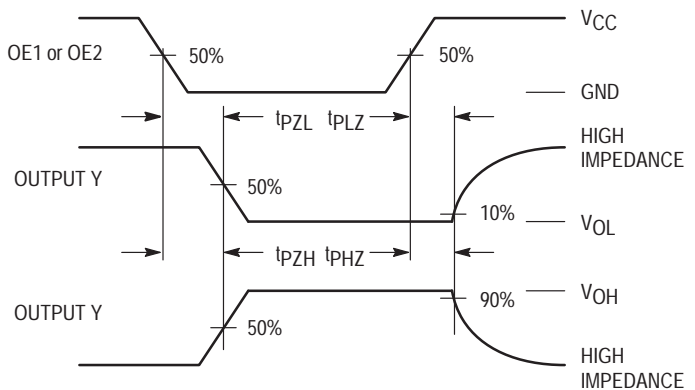
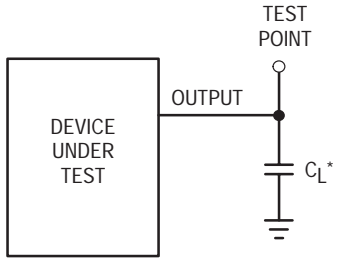


Figure 2.

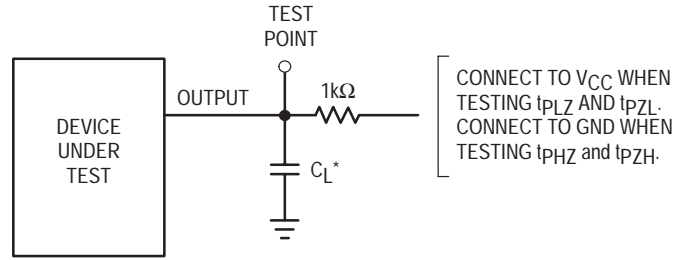
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TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 3.



*Includes all probe and jig capacitance

Figure 4.

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) — Data input pins. Data on these pins appear in non-inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

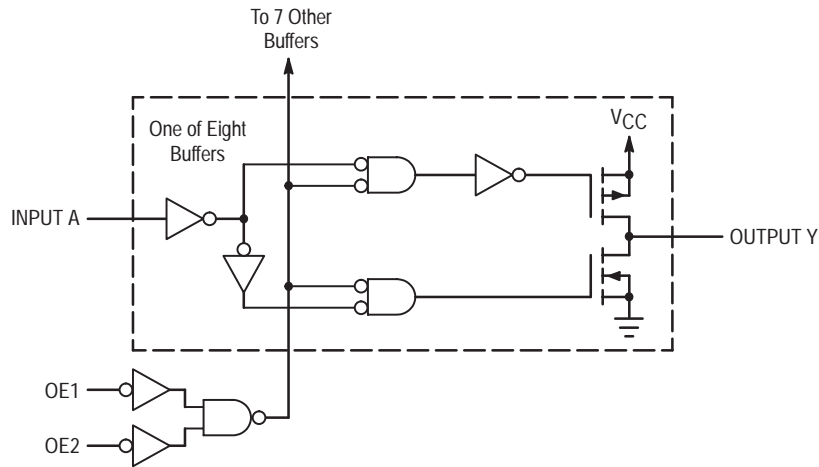
OE1, OE2 (PINS 1, 19) — Output enables (active-low). When a low voltage is applied to both of these pins, the

outputs are enabled and the device functions as a non-inverting buffer. When a high voltage is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output enable pins, these outputs are either non-inverting outputs or high-impedance outputs.

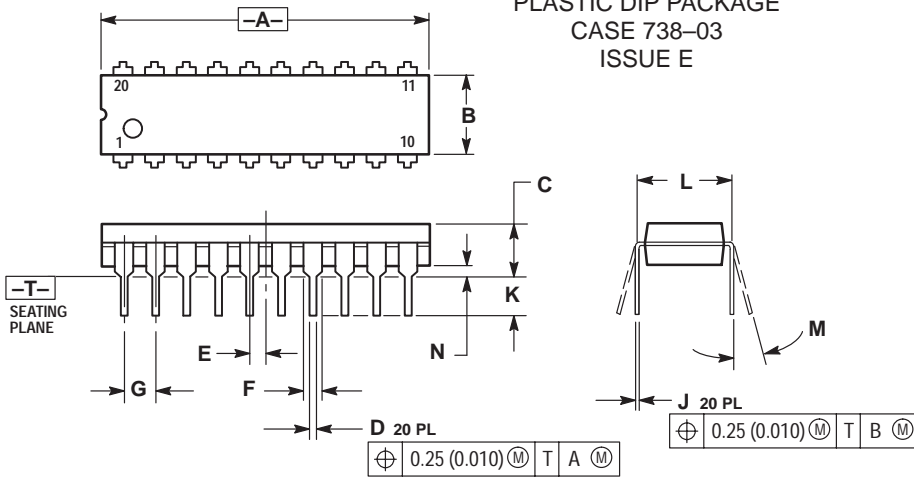
LOGIC DETAIL



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PACKAGE DIMENSIONS

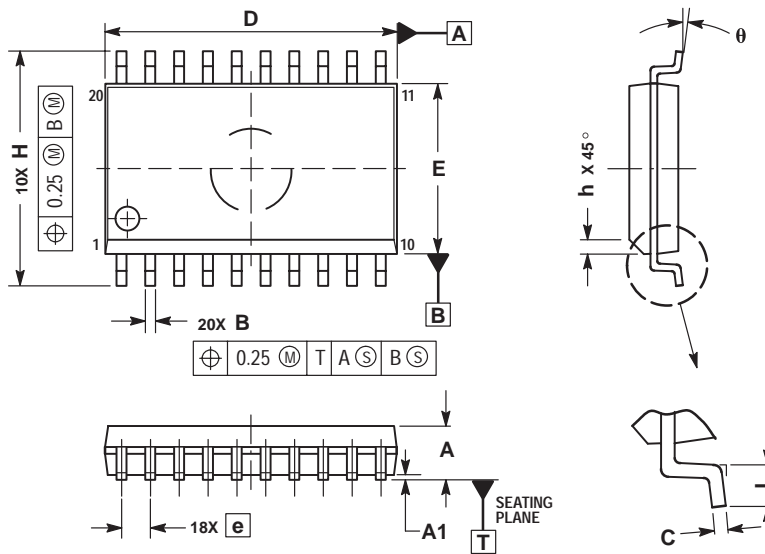
**PDIP-20
N SUFFIX**
PLASTIC DIP PACKAGE
CASE 738-03
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

**SO-20
DW SUFFIX**
CASE 751D-05
ISSUE F




- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

Notes

Notes

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