Micropower Single Supply Rail-to-Rail Input-Output (RRIO) Precision Op Amp

The EL8178 is a precision low power, operational amplifier. The device is optimized for single supply operation between 2.4V to 5V. This enables operation from one lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail.

For power sensitive applications, the EL8178 has and $\overline{EN}$ pin that will shut the device down and reduce the supply current to 3µA typ. In the active state, the EL8178 draws minimal supply current (55µA) while meeting excellent DC-accuracy, noise, and output drive specifications.

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-free)	PKG. DWG. #
EL8178FWZ-T7	BBWA	7” (3k pcs)	6 Ld SOT-23	MDP0038
EL8178FWZ-T7A	BBWA	7” (250 pcs)	6 Ld SOT-23	MDP0038
EL8178FSZ	8178FSZ	97/Tube	8 Ld SO	MDP0027
EL8178FSZ-T7	8178FSZ	7” (1k pcs)	8 Ld SO	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

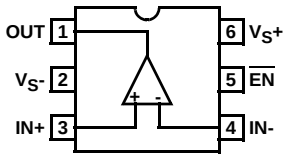
- Typical 55µA supply current
- 250µV max offset voltage
- Typical 1pA input bias current
- 266kHz gain-bandwidth product
- Single supply operation between 2.4V to 5.0V
- Rail-to-rail input and output
- Ground sensing
- Output sources and sinks 26mA load current
- Pb-free plus anneal available (RoHS compliant)

Applications

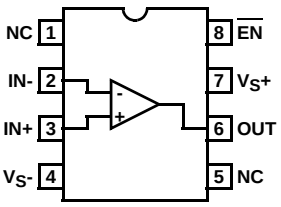
- Battery- or solar-powered systems
- 4mA to 20mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre-amps
- pH probe amplifiers

Pinouts

EL8178
(6 LD SOT-23)
TOP VIEW



EL8178
(8 LD SO)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_S) and Pwr-up Ramp Rate 5.5V, 1V/µs
Differential Input Voltage 0.5V
Current into IN+, IN-, and $\overline{EN}$. 5mA
Input Voltage . . . . . V_{S-} - 0.5V to V_{S+} + 0.5V
ESD Tolerance
Human Body Model 3kV
Machine Model 300V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
6 Ld SOT Package	230
8 Ld SO Package	110

Ambient Operating Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . +125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{S+} = 5V, V_{S-} = 0V, V_{CM} = 2.5V, V_O = 2.5V, T_A = +25°C unless otherwise specified. **Boldface limits** apply over the operating temperature range, **-40°C to +125°C**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage		-250	50	250	µV
			-450		**450**	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			3		µV/Mo
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drift vs Temperature			1.1		µV/°C
I_B	Input Bias Current	See Figures 18 and 19	-25	1	25	pA
			-600		**600**	pA
e_N	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz		2.8		μV_{P-P}
	Input Noise Voltage Density	f_O = 1kHz		48		$nV/\sqrt{Hz}$
i_N	Input Noise Current Density	f_O = 1kHz		0.15		$pA/\sqrt{Hz}$
CMIR	Input Voltage Range	Guaranteed by CMRR test	0		5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	80	100		dB
			75			dB
PSRR	Power Supply Rejection Ratio	V_S = 2.4V to 5V	80	100		dB
			80			dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ to $(V_{S+} + V_{S-})/2$	100	400		V/mV
			100			V/mV
V_{OUT}	Maximum Output Voltage Swing	V_{OL}; Output low, R_L = 100kΩ to $(V_{S+} + V_{S-})/2$		3	**10**	mV
		V_{OL}; Output low, R_L = 1kΩ to $(V_{S+} + V_{S-})/2$		130	250	mV
					350	mV
		V_{OH}; Output high, R_L = 100kΩ to $(V_{S+} + V_{S-})/2$	**4.994**	4.9975		V
		V_{OH}; Output high, R_L = 1kΩ to $(V_{S+} + V_{S-})/2$	4.750	4.875		V
			4.7			V
SR	Slew Rate		0.10	0.15	0.19	V/µs
			0.07		**0.25**	V/µs
GBWP	Gain Bandwidth Product	f_O = 100kHz		266		kHz

Electrical Specifications V_{S+} = 5V, V_{S-} = 0V, V_{CM} = 2.5V, V_O = 2.5V, T_A = +25°C unless otherwise specified. **Boldface limits** apply over the operating temperature range, **-40°C to +125°C (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{S(ON)}$	Supply Current, Enabled		35	55	75	µA
			30		**85**	µA
$I_{S(OFF)}$	Supply Current, Disabled			3	**5**	µA
I_{SC}^+	Short Circuit Output Sourcing Current	R_L = 10Ω to opposite supply	23	31		mA
			18			mA
I_{SC}^-	Short Circuit Output Sinking Current	R_L = 10Ω to opposite supply	20	26		mA
			15			mA
V_S	Minimum Supply Voltage	Guaranteed by PSRR		2.2	2.4	V
					2.4	V
V_{INH}	$\overline{EN}$ Pin High Level		2			V
V_{INL}	$\overline{EN}$ Pin Low Level				0.8	V
I_{ENH}	$\overline{EN}$ Pin Input Current	V_{EN} = 5V	**0.25**	0.8	**2.5**	µA
I_{ENL}	$\overline{EN}$ Pin Input Current	V_{EN} = 0V	**-0.5**		**+0.5**	µA

Typical Performance Curves V_S = ±2.5V, T_A = +25°C, Unless Otherwise Specified

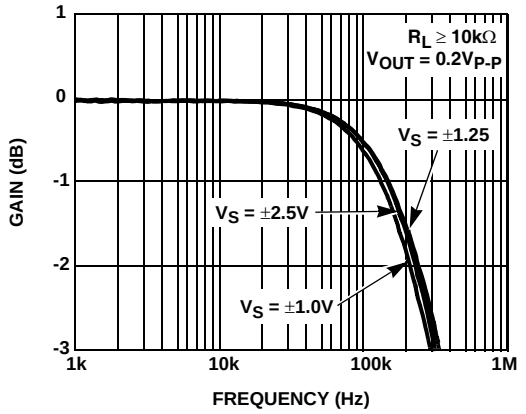


FIGURE 1. UNITY GAIN FREQUENCY RESPONSE at VARIOUS SUPPLY VOLTAGES

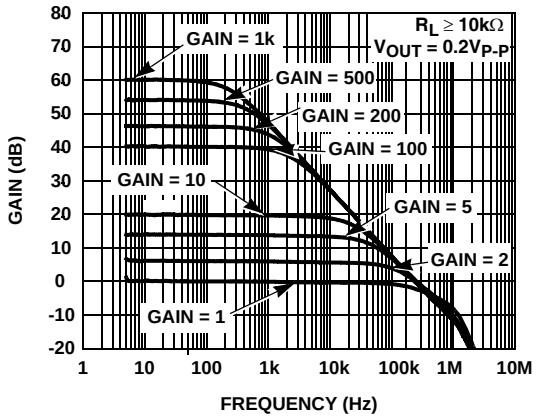


FIGURE 2. FREQUENCY RESPONSE at VARIOUS CLOSED LOOP GAINS

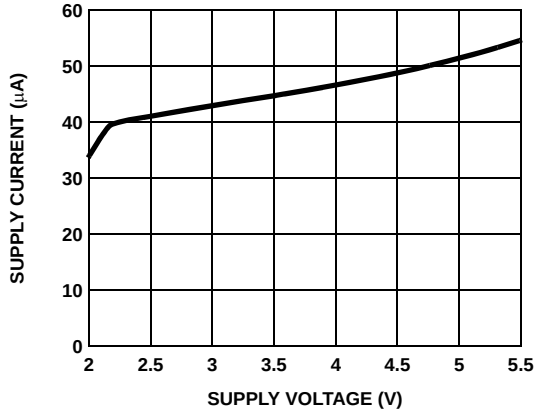


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

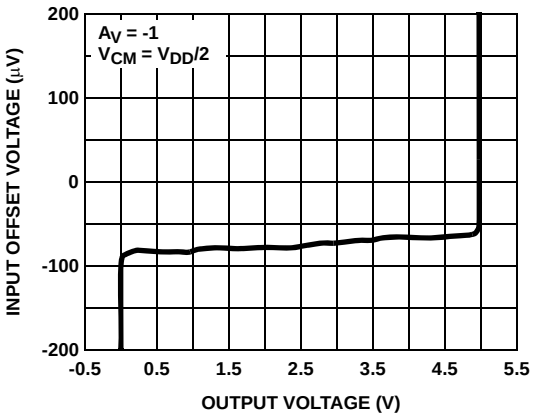


FIGURE 4. INPUT OFFSET VOLTAGE vs OUTPUT VOLTAGE

Typical Performance Curves (Continued) V_S = ±2.5V, T_A = +25°C, Unless Otherwise Specified (Continued)

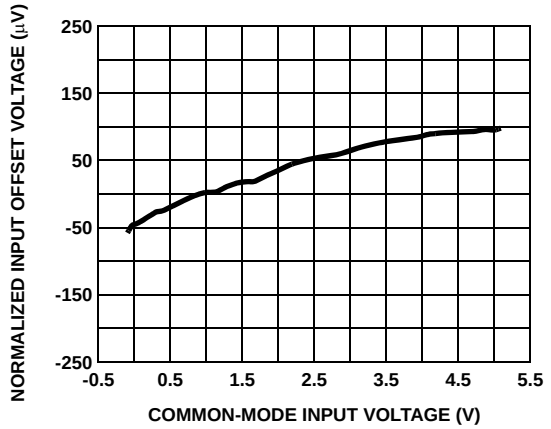


FIGURE 5. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

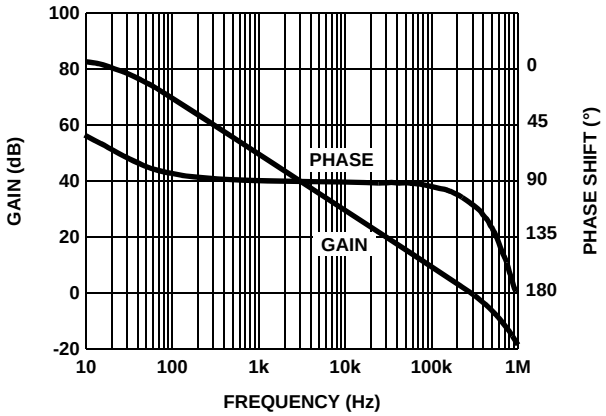


FIGURE 6. OPEN LOOP GAIN AND PHASE vs FREQUENCY (R_L = 1kΩ)

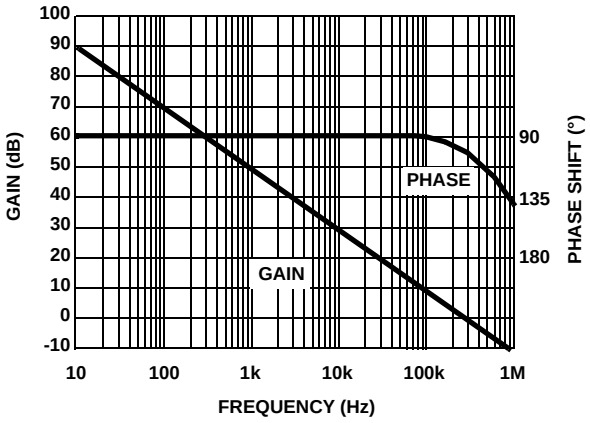


FIGURE 7. OPEN LOOP GAIN AND PHASE vs FREQUENCY (R_L = 100kΩ)

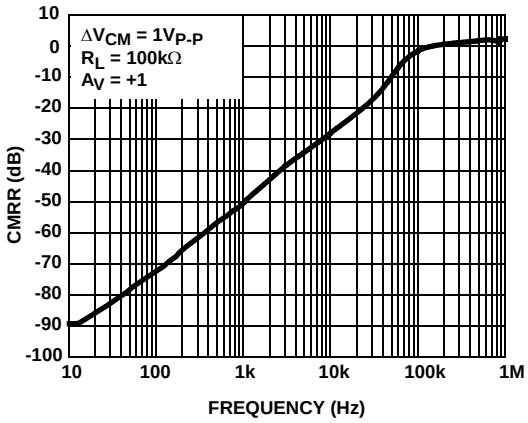


FIGURE 8. CMRR vs FREQUENCY

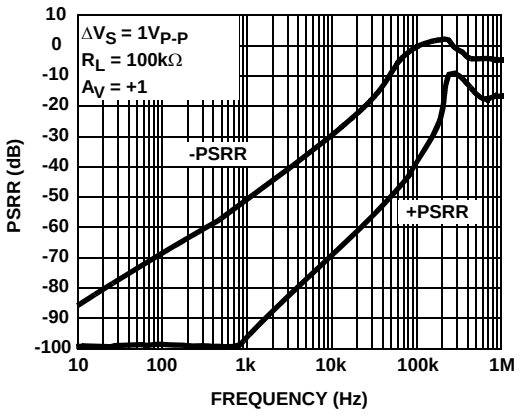


FIGURE 9. PSRR vs FREQUENCY

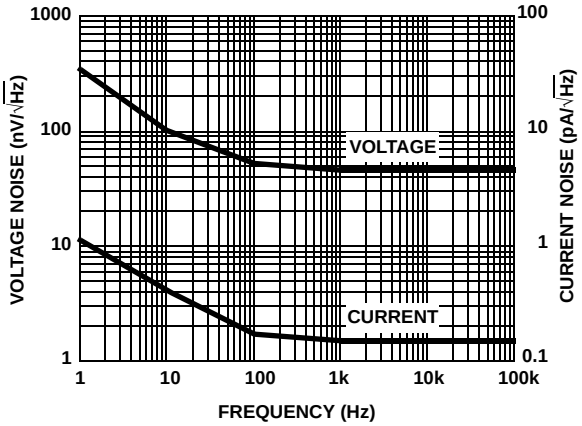


FIGURE 10. INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY

Typical Performance Curves (Continued) V_S = ±2.5V, T_A = +25°C, Unless Otherwise Specified (Continued)

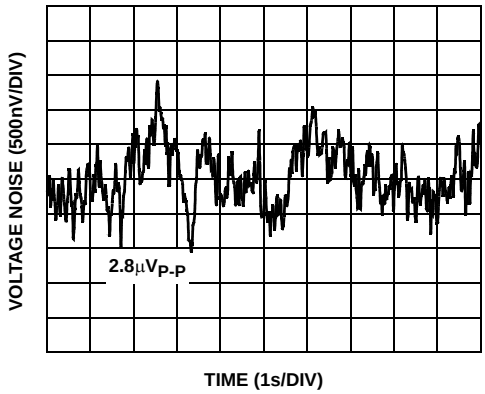


FIGURE 11. 0.1Hz TO 10Hz INPUT VOLTAGE NOISE

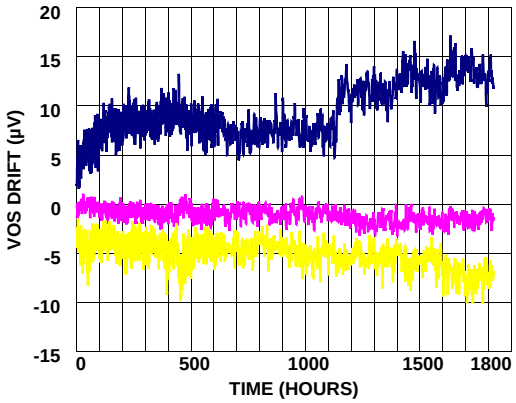


FIGURE 12. IVOS DRIFT (SOT-23 PACKAGE) vs TIME

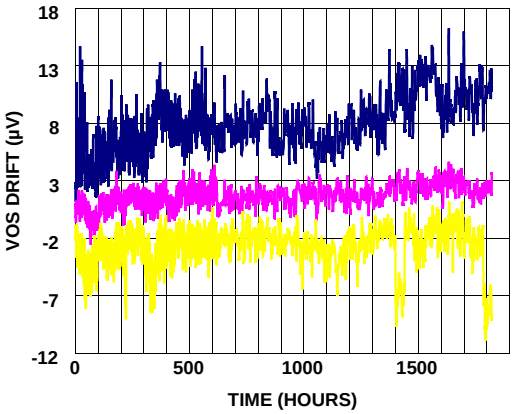


FIGURE 13. IVOS DRIFT (SOIC PACKAGE) vs TIME

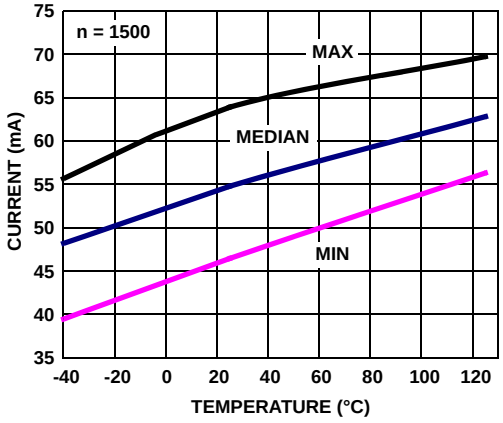


FIGURE 14. ENABLED SUPPLY CURRENT vs TEMPERATURE, V_S = ±2.5V

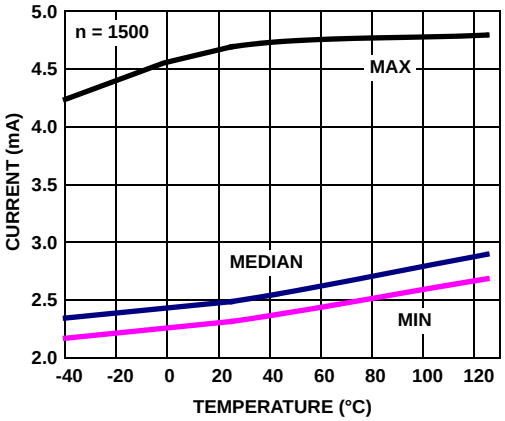


FIGURE 15. DISABLED SUPPLY CURRENT vs TEMPERATURE, V_S = ±2.5V

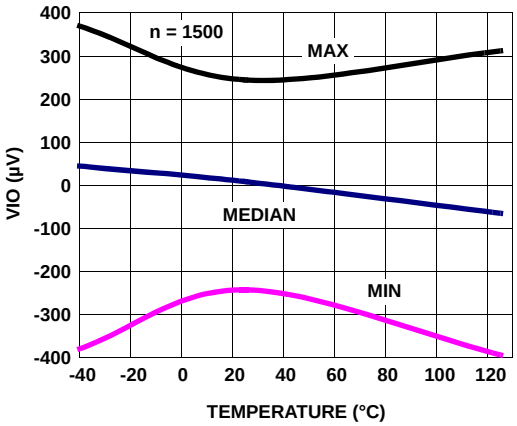


FIGURE 16. V_{OS} vs TEMPERATURE, V_S = ±2.5V

Typical Performance Curves (Continued) V_S = ±2.5V, T_A = +25°C, Unless Otherwise Specified (Continued)

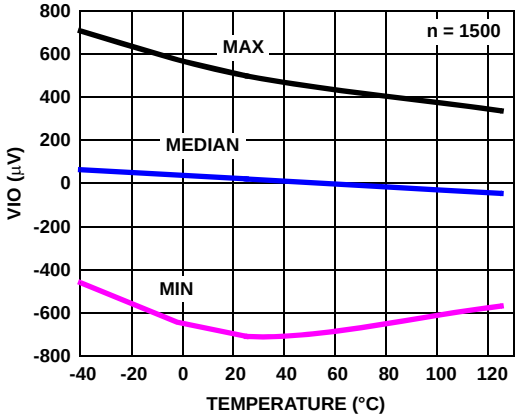


FIGURE 17. V_{OS} vs TEMPERATURE, V_S = ±1.2V

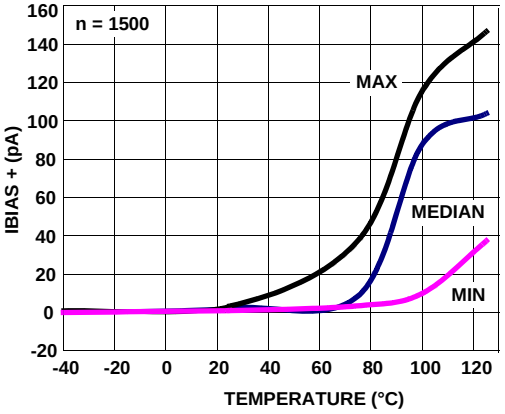


FIGURE 18. I_{BIAS+} vs TEMPERATURE, V_S = ±2.5V

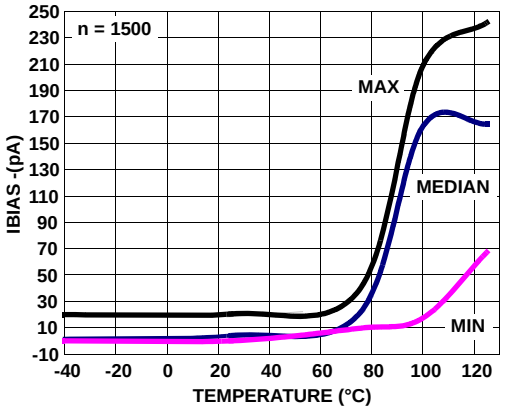


FIGURE 19. I_{BIAS-} vs TEMPERATURE, V_S = ±2.5V

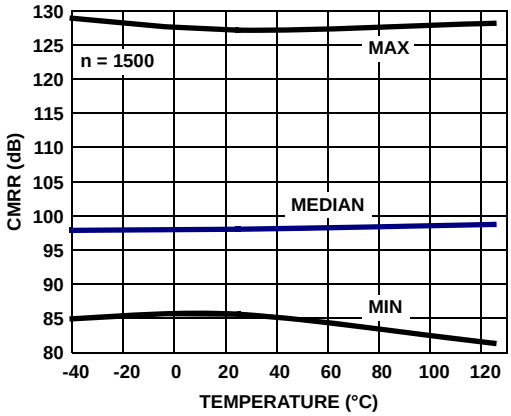


FIGURE 20. CMRR vs TEMPERATURE, V+ = ±2.5V, ±1.5V

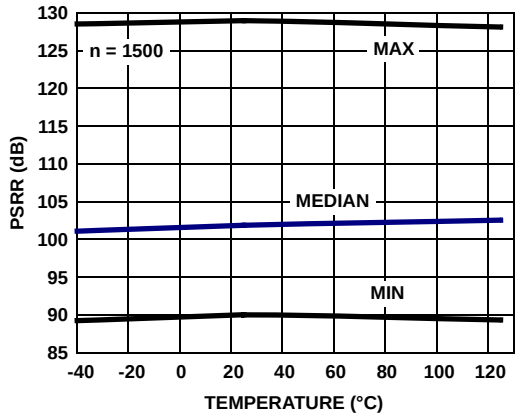


FIGURE 21. PSRR vs TEMPERATURE ±1.5V TO ±2.5V

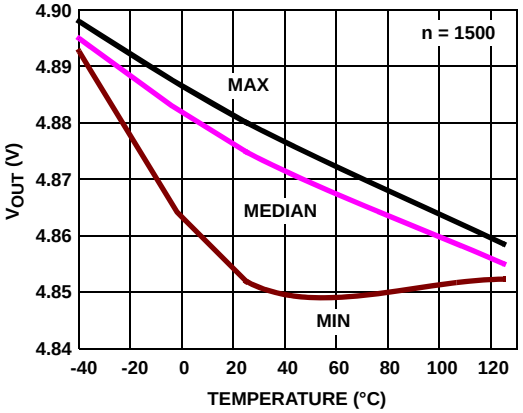


FIGURE 22. V_{OUT} HIGH vs TEMPERATURE, V_S = ±2.5V, R_L = 1k

Typical Performance Curves (Continued) V_S = ±2.5V, T_A = +25°C, Unless Otherwise Specified (Continued)

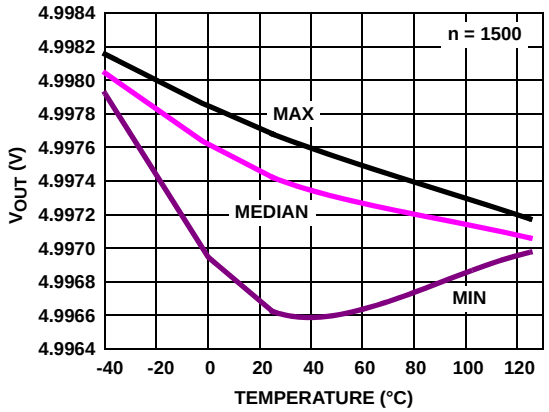


FIGURE 23. V_{OUT} HIGH vs TEMPERATURE, V_S = ±2.5V, R_L = 100k

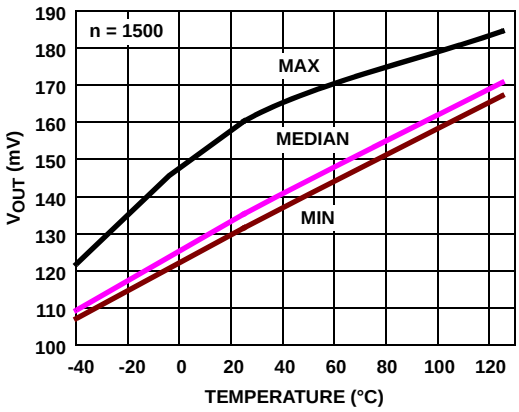


FIGURE 24. V_{OUT} LOW vs TEMPERATURE, V_S = ±2.5V, R_L = 1k

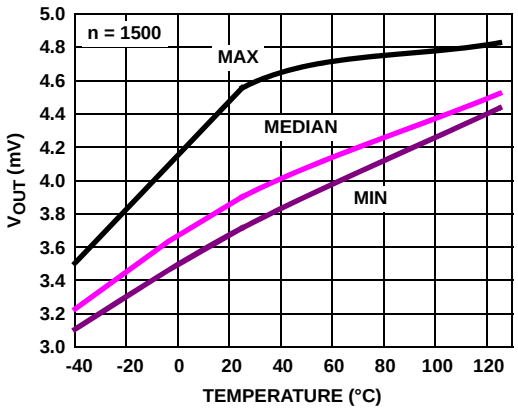


FIGURE 25. V_{OUT} LOW vs TEMPERATURE, V_S = ±2.5V, R_L = 100k

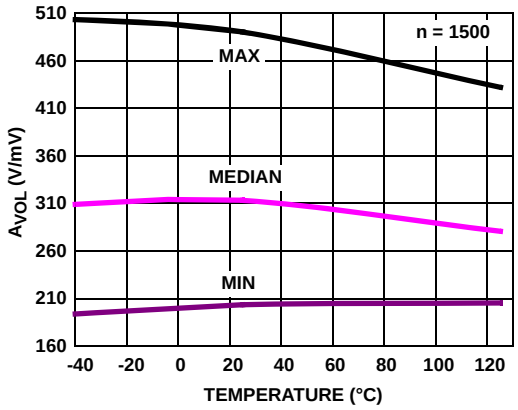
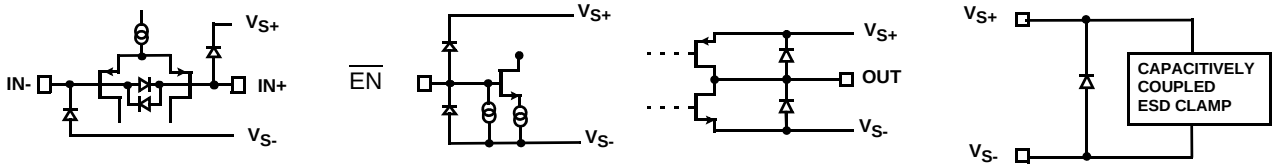


FIGURE 26. A_{VOL} vs TEMPERATURE, R_L = 100k, V_O = ±2V @ V_S = ±2.5V

Pin Descriptions

SO PIN NUMBER	SOT-23 PIN NUMBER	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1		NC		No internal connection
2	4	IN-	Circuit 1	Amplifier's inverting input
3	3	IN+	Circuit 1	Amplifier's non-inverting input
4	2	V_{S-}	Circuit 4	Negative power supply
5		NC		No internal connection
6	1	OUT	Circuit 3	Amplifier's output
7	6	V_{S+}	Circuit 4	Positive power supply
8	5	$\overline{EN}$	Circuit 2	Amplifier's enable pin with internal pull-down; Logic "1" selects the disabled state; Logic "0" selects the enabled state.



CIRCUIT 1 CIRCUIT 2 CIRCUIT 3 CIRCUIT 4

Application Information

Introduction

The EL8178 is a rail-to-rail input and output (RRIO), micro-power, precision, single supply op amp with an enable feature. This amplifier is designed to operate from single supply (2.4V to 5.0V) or dual supply (±1.2V to ±2.5V) while drawing only 55µA of supply current.The device achieves rail-to-rail input and output operation while eliminating the drawbacks of many conventional RRIO op amps.

Rail-to-Rail Input

The PFET input stage of the EL8178 has an input common-mode voltage range that includes the negative and positive supplies without introducing offset errors or degrading performance like some existing rail-to-rail input op amps. Many rail-to-rail input stages use two differential input pairs: a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties result from using this topology. As the input signal moves from one supply rail to the other, the op amp switches from one input pair to the other causing changes in input offset voltage and an undesired change in the input offset current's magnitude and polarity.

The EL8178 achieves rail-to-rail input performance without sacrificing important precision specifications and without degrading distortion performance. The EL8178's input offset voltage exhibits a smooth behavior throughout the entire common-mode input range.

Rail-to-Rail Output

A pair of complementary MOSFET devices achieves rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction, while the PMOS sources current to swing the output in the positive direction. The EL8178 with a 100kΩ load swings to within 3mV of the supply rails.

Results of Over-Driving the Output

Caution should be used when over-driving the output for long periods of time. Over-driving the output can occur in three ways:

1. The input voltage times the gain of the amplifier exceeds the supply voltage by a large value.
2. The output current required is higher than the output stage can deliver.
3. Operating the device in Slew Rate Limit. These conditions can result in a shift in the Input Offset Voltage (VOS) as much as 1µV/hr of exposer under these condition.

Enable/Disable Feature

The EL8178 features an active low $\overline{EN}$ pin that when pulled up to at least 2V, disables the output and drops the I_{CC} to a 3µA. The $\overline{EN}$ pin has an internal pull down, so an undriven pin pulls to the negative rail, thereby enabling the op amp by default. For applications where the $\overline{EN}$ pin is not being used, it is recommended that the $\overline{EN}$ pin be permanently tie to ground.

The high impedance output during disable allows for connecting multiple EL8178s together to implement a Mux Amp. The outputs are connected together and activating the appropriate $\overline{EN}$ pin selects the desired channel. If utilizing

non-unity gain op amp configurations, then the loading effects of the disabled amplifiers' feedback networks must be considered when evaluating the active amplifier's performance in Mux Amp configurations.

Note that feed through from the IN+ to IN- pins occurs on any Mux Amp disabled channel where the input differential voltage exceeds 0.5V (e.g., active channel V_{OUT} = 1V, while disabled channel V_{IN} = GND), so the mux implementation is best suited for small signal applications. In any application where two or more amplifier outputs are muxed, use series IN+ resistors, or large value R_Fs in each amplifier to keep the feed through current low enough to minimize the impact on the active channel. See "Usage Implications" on page 9 for more details.

IN+ and IN- Input Protection

In addition to ESD protection diodes to each supply rail, the EL8178 has additional back-to-back protection diodes across the differential input terminals (see "Circuit 1" diagram on page 8). If the magnitude of the differential input voltage exceeds the diode's V_F, then one of these diodes will conduct. For elevated temperatures, the leakage of the protection diodes (Circuit 1 pin description table) increases, resulting in the increase in Ibias as seen in Figures 18 and 19.

Usage Implications

If the input differential voltage is expected to exceed 0.5V, an external current limiting resistor must be used to ensure the input current never exceeds 5mA. For noninverting unity gain applications the current limiting can be via a series IN+ resistor, or via a feedback resistor of appropriate value. For other gain configurations, the series IN+ resistor is the best choice, unless the feedback (R_F) and gain setting (R_G) resistors are both sufficiently large to limit the input current to 5mA.

Large differential input voltages can arise from several sources:

1) During open loop (comparator) operation. The IN+ and IN- input voltages don't track.

2) When the amplifier is disabled but an input signal is still present. An R_L or R_G to GND keeps the IN- at GND, while the varying IN+ signal creates a differential voltage. Mux Amp applications are similar, except that the active channel V_{OUT} determines the voltage on the IN- terminal.

3) When the slew rate of the input pulse is considerably faster than the op amp's slew rate. If the V_{OUT} can't keep up with the IN+ signal, a differential voltage results, and visible distortion occurs on the input and output signals. To avoid this issue, keep the input slew rate below 0.2V/µs, or use appropriate current limiting resistors.

Large (>2V) differential input voltages can also cause an increase in disabled I_{CC}.

$\overline{EN}$ Input Protection

The $\overline{EN}$ input has internal ESD protection diodes to both the positive and negative supply rails, limiting the input voltage range to within one diode beyond the supply rails (see "Circuit 2" diagram on page 8). If the input voltage is expected to exceed V_{S+} or V_{S-}, then an external series resistor should be added to limit the current to 5mA.

Output Current Limiting

The EL8178 has no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the "Absolute Maximum Rating" for "operating junction temperature", potentially resulting in the destruction of the device.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperature (T_{JMAX}) under certain load and power-supply conditions. It is therefore important to calculate T_{JMAX} for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} \times PD_{MAX}) \quad \text{(EQ. 1)}$$

where PD_{MAX} is calculated using:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of the amplifier
- V_S = Supply voltage
- I_{MAX} = Maximum supply current of the amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Proper Layout Maximizes Precision

To achieve the optimum levels of high input impedance (i.e., low input currents) and low offset voltage, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. When input leakage current is a paramount concern, the use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 27 shows a guard ring example for a unity gain amplifier that uses the low impedance amplifier output at the same voltage as the high impedance input to eliminate surface leakage. The guard ring does not need to be a

specific width, but it should form a continuous loop around both inputs. For further reduction of leakage currents, mount components to the PC board using PTFE standoffs.

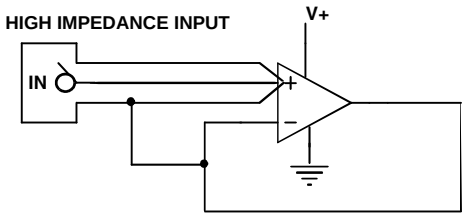


FIGURE 27. GUARD RING EXAMPLE FOR UNITY GAIN AMPLIFIER

Typical Applications

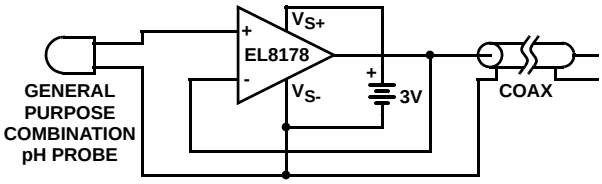


FIGURE 28. pH PROBE AMPLIFIER

A general-purpose combination pH probe has extremely high output impedance typically in the range of 10GΩ to 12GΩ. Low loss and expensive PTFE cables are often used to connect the pH probe to the meter electronics. Figure 28 details a low-cost alternative solution using the EL8178 and a low-cost coax cable. The EL8178 PMOS high impedance input senses the pH probe output signal and buffers it to drive the coax cable. Its rail-to-rail input nature also eliminates the need for a bias resistor network required by other amplifiers in the same application.

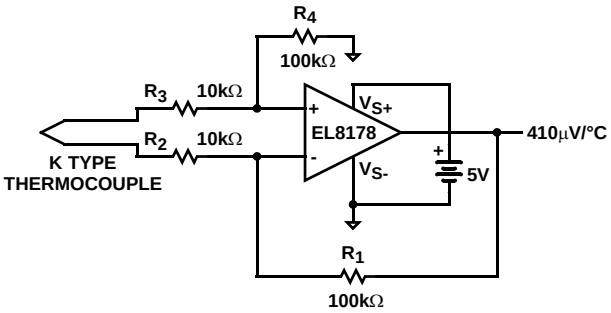
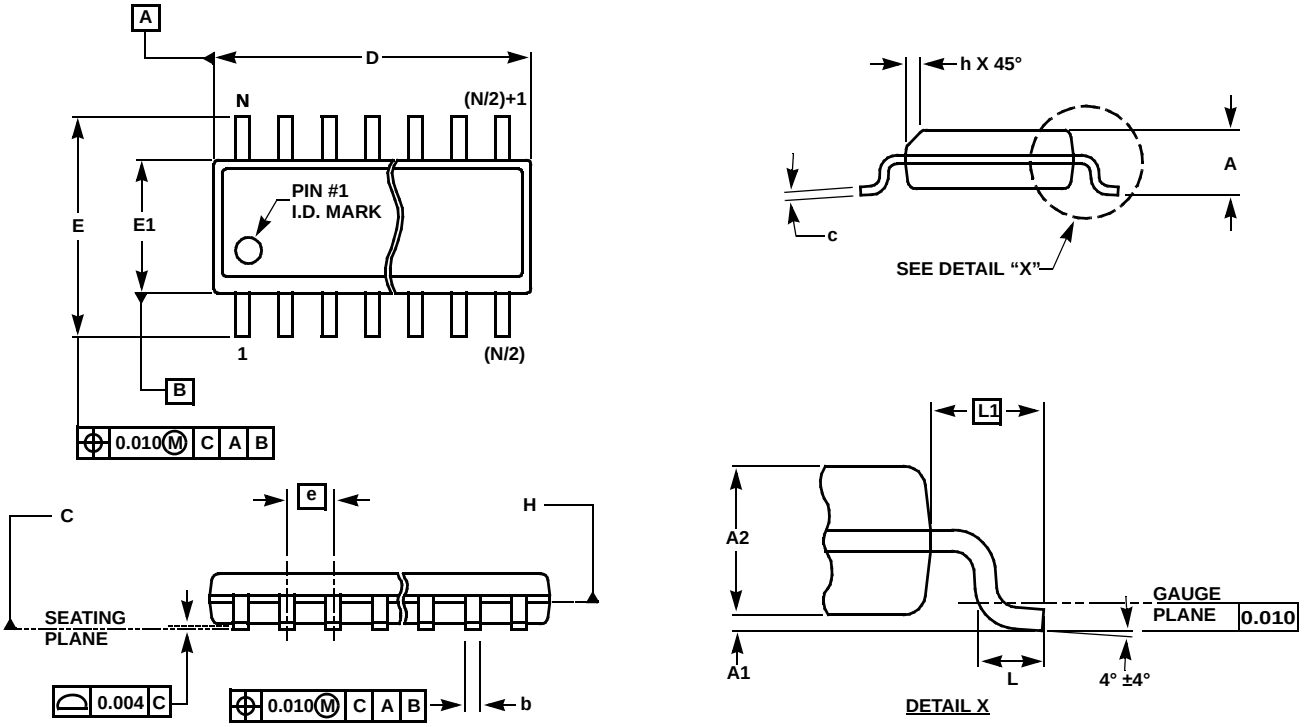


FIGURE 29. THERMOCOUPLE AMPLIFIER

Thermocouples are the most popular temperature sensing devices because of their low cost, interchangeability, and ability to measure a wide range of temperatures. In Figure 29, the EL8178 converts the differential thermocouple voltage into single-ended signal with 10X gain. The EL8178's rail-to-rail input characteristic allows the thermocouple to be biased at ground and permits the op amp to operate from a single 5V supply.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

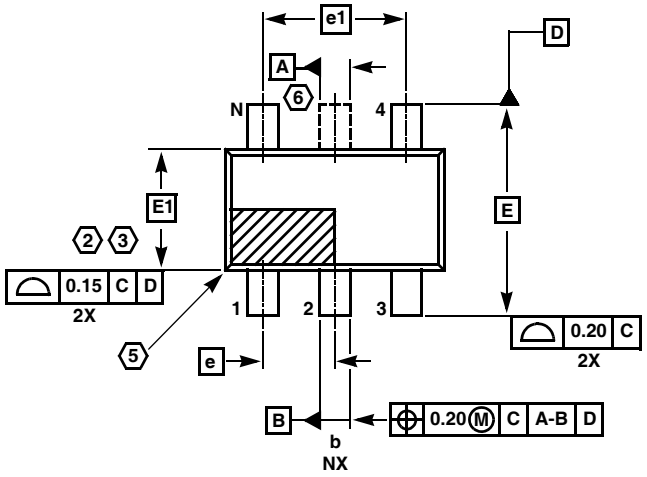
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

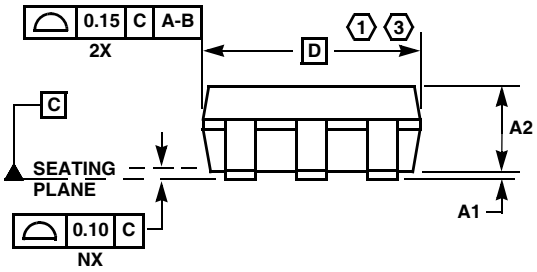
Rev. M 2/07

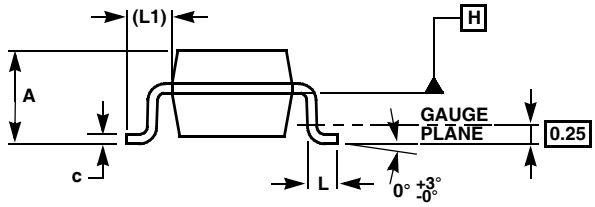
NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

SOT-23 Package Family







MDP0038

SOT-23 PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).