



Cyclone IV GX Transceiver Starter Board

Reference Manual



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Introduction

This document describes the hardware features of the Cyclone® IV GX Transceiver starter board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Cyclone IV GX transceiver starter board provides a hardware platform for developing and prototyping low-power, high-volume, feature-rich designs as well as to demonstrate the Cyclone IV GX device's on-chip memory, embedded multipliers, and the Nios® II embedded soft processor. The board provides peripherals and memory interfaces to facilitate the development of the Cyclone IV GX transceiver designs.

The Cyclone IV GX transceiver starter board is especially suitable for cost-sensitive applications that require high-speed transceivers and power integrity solutions.

 For more information on the Cyclone IV device family, refer to the *Cyclone IV Device Handbook*.

Board Component Blocks

The board features the following major component blocks:

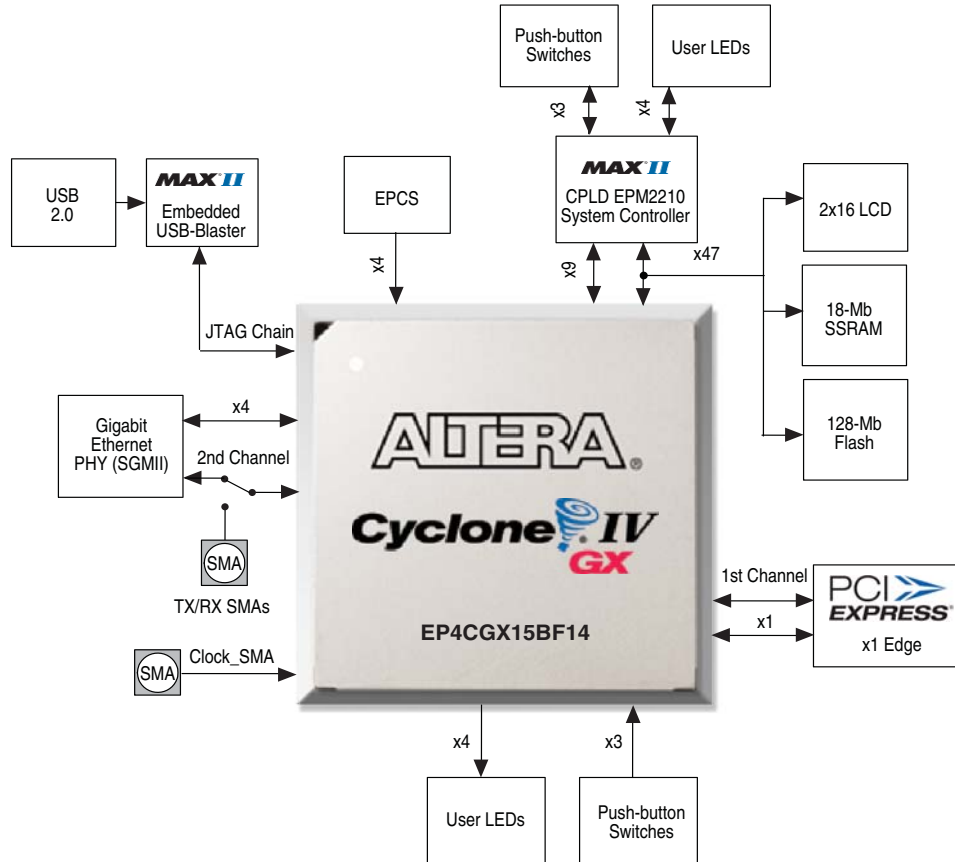
- Cyclone IV GX EP4CGX15BF14 FPGA in the 169-pin FineLine BGA (FBGA) package
 - 14,400 LEs
 - 540-kilobit (Kb) on-die memory
 - 20 global clocks
 - 72 user I/Os
 - 3 phase locked loops (PLLs)
 - 1 PCI Express hard IP block
 - 1.2-V core power
- MAX[®] II EPM2210F256 CPLD in the 256-pin FBGA package
 - 2.5-V core power
- MAX II EPM240M100 CPLD in the 100-pin Micro FBGA (MBGA) package
- FPGA configuration circuitry
 - MAXII CPLD EPM2210 System Controller and flash passive serial (PS) configuration
 - On-board USB-Blaster[™] for use with the Quartus[®] II Programmer
 - JTAG header for external USB-Blaster with the Quartus II Programmer
 - Erasable programmable configurable serial (EPCS) device
- On-Board ports
 - USB 2.0
 - One gigabit Ethernet port
- Transceiver interfaces
 - PCI Express x1 edge connector
 - 10/100/1000BASE-T Ethernet PHY with RJ-45 connector
 - One optional TX/RX transceiver to SMA connectors (requires a minor modification on the board)
- On-Board memory
 - 18-megabit (Mb) Synchronous Static Random Access Memory (SSRAM)
 - 128-Mb flash
- On-Board clocking circuitry
 - 6-MHz, 24-MHz, 25-MHz, and 50-MHz oscillators
 - 125-MHz LVDS oscillator
 - SMA clock input

- General user I/O
 - LEDs and display
 - Four FPGA user LEDs
 - One configuration done LED
 - One max error LED
 - Five Ethernet status LEDs
 - One USB status LED
 - One power status LED
 - Two PGM LEDs
 - A two-line character LCD display
 - Push-Button switches
 - One CPU reset push-button switch
 - One MAX II configuration reset push-button switch
 - One PGM configure push-button switch (configure the FPGA from flash memory)
 - One PGM select push-button switch (select image to load from flash memory)
 - Two general user push-button switches
 - DIP switches
 - Board setting DIP switch
 - Configuration setting DIP switch
- Power supply
 - 9-V – 16-V DC input
 - 2.5-mm barrel jack for DC power input
 - On/Off slide power switch
 - On-Board power measurement circuitry
- Mechanical
 - 6.6" x 2.713" board
 - PCI Express chassis or bench-top operation

Starter Board Block Diagram

Figure 1-1 shows the block diagram of the Cyclone IV GX transceiver starter board.

Figure 1-1. Cyclone IV GX transceiver Starter Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:



Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Introduction

This chapter introduces the major components on the Cyclone IV GX Transceiver starter board. [Figure 2-1](#) illustrates major component locations and [Table 2-1](#) provides a brief description of all component features of the board.



A complete set of schematics, a physical layout database, and GERBER files for the starter board reside in the Cyclone IV GX Transceiver starter kit documents directory.



For information about powering up the board and installing the demonstration software, refer to the [Cyclone IV GX Transceiver Starter Kit User Guide](#).

This chapter consists of the following sections:

- “Board Overview”
- “Featured Device: Cyclone IV GX Device” on page 2-4
- “MAX II CPLD EPM2210 System Controller” on page 2-6
- “Configuration, Status, and Setup Elements” on page 2-9
- “Clock Circuitry” on page 2-16
- “General User Input/Output” on page 2-17
- “Components and Transceiver Interfaces” on page 2-19
- “Memory” on page 2-22
- “Power Supply” on page 2-26
- “Statement of China-RoHS Compliance” on page 2-29

Board Overview

This section provides an overview of the Cyclone IV GX Transceiver starter board, including an annotated board image and component descriptions. [Figure 2-1](#) provides an overview of the starter board features.

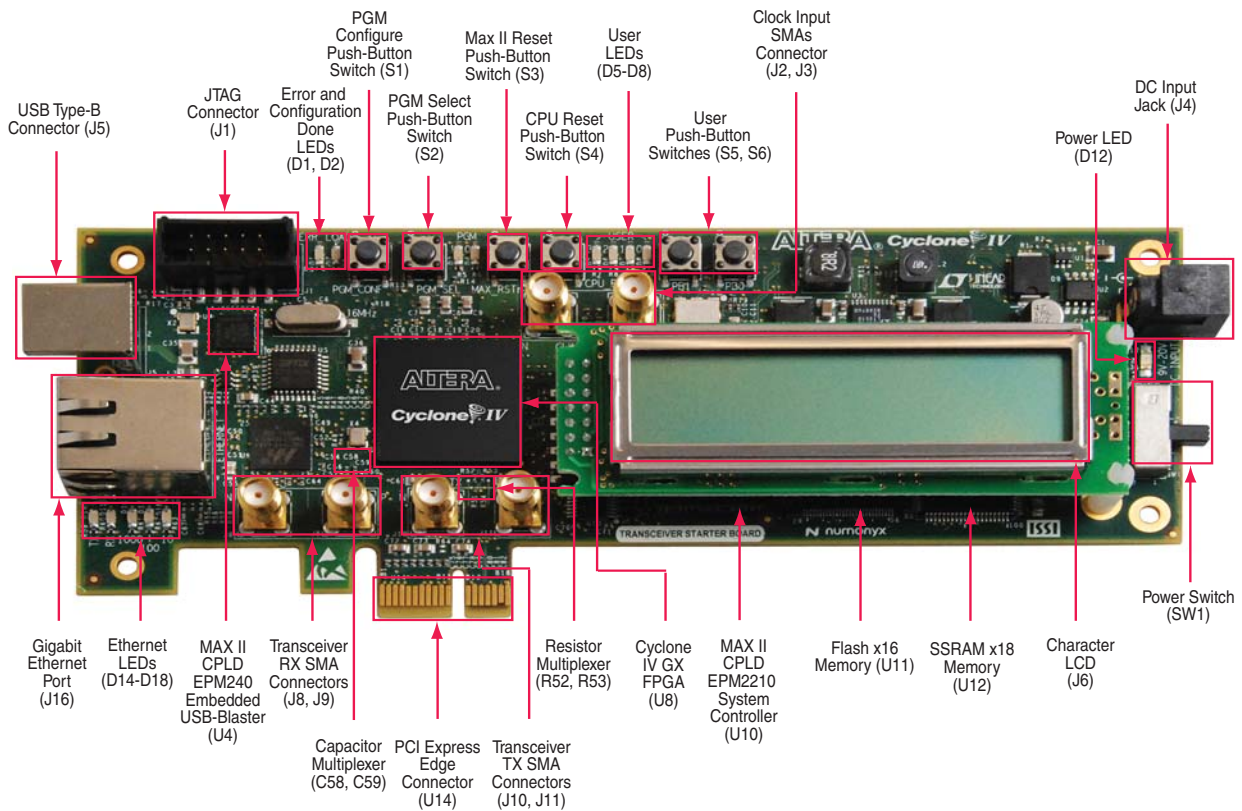
Figure 2–1. Overview of the Cyclone IV GX Transceiver Starter Board Features

Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Cyclone IV GX Transceiver Starter Board Components (Part 1 of 3)

Board Reference	Type	Description
Featured Devices		
U8	FPGA	EP4CGX15BF14, 169-pin FBGA.
U10	CPLD	EPM2210F256, 256-pin FBGA.
Configuration, Status, and Setup Elements		
J5	USB Type-B connector	Connects to the computer to enable embedded USB-Blaster JTAG.
J13	JTAG chain header	Enables and disables devices in the JTAG chain.
S8	Board settings DIP switch	Controls the MAX II CPLD EPM2210 System Controller functions such as clock select, SMA clock input control, and which image to load from flash memory at power-up. This switch is located at the bottom of the board.
J1	JTAG connector	Disables embedded blaster (for use with external USB-Blasters).
U15	EPCS128 serial configuration device	Flash memory device with a serial interface which stores configuration data for FPGA device that supports active serial configuration and reloads the data to the FPGA upon power-up or reconfiguration.

Table 2-1. Cyclone IV GX Transceiver Starter Board Components (Part 2 of 3)

Board Reference	Type	Description
D2	Load LED	Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA.
D1	Error LED	Illuminates when the FPGA configuration from flash memory fails.
D14, D15, D16, D17, D18	Ethernet LEDs	Shows the connection speed as well as transmit or receive activity.
D12	Power LED	Illuminates when 9-V – 16-V DC power is present.
S7	Configuration settings DIP switch	Sets the configuration mode to either passive serial (flash) or active serial (EPCS). This switch is located at the bottom of the board.
S4	CPU reset push-button switch	Press to reset the FPGA logic.
S3	MAX II reset push-button switch	Press to reset the MAX II CPLD EPM2210 System Controller.
S2	PGM select push-button switch	Toggles the PGM LEDs which selects the program image that loads from flash memory to the FPGA.
S1	PGM configure push-button switch	Configure the FGPA from flash memory based on the PGM LEDs setting.
Clock Circuitry		
X1	125-MHz oscillator	125-MHz crystal oscillator for PCI Express or general use such as memories. Multiplexed with CLKIN_SMA_P/N signals based on CLK_SEL switch value.
X5	50-MHz oscillator	50-MHz crystal oscillator for configuration purpose. This oscillator is located at the bottom of the board.
J2, J3	Clock input SMAs	Drive LVPECL-compatible clock inputs into the clock multiplexer buffer (U6).
General User Input/Output		
D5, D6, D7, D8	User LEDs	Four user LEDs. Illuminates when driven low.
S5, S6	User push-button switches	Two user push-button switches. Driven low when pressed.
J6	Character LCD	Connector which interfaces to the provided 16 character × 2 line LCD module.
Memory Devices		
U12	SSRAM x18 memory	Standard synchronous RAM which provides a 2-MB SSRAM port.
U11	Flash x16 memory	Synchronous burst mode flash device which provides a 16-MB non-volatile memory port.
Components and Transceiver Interfaces		
J7	RJ-45 connector	Provides 10/100/1000 BASE-T Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Altera Triple Speed Ethernet MegaCore function in SGMII mode.
U9	Gigabit Ethernet	A Marvell 88E1111 PHY device for 10/100/1000 BASE-T Ethernet connection. The device is an auto-negotiating Ethernet PHY with an SGMII interface to the FPGA.
U14	PCI Express edge connector	Interfaces to a PCI Express root port such as an appropriate PC motherboard. Made of gold-plated edge fingers for up to ×1 signaling in Gen1 mode.

Table 2-1. Cyclone IV GX Transceiver Starter Board Components (Part 3 of 3)

Board Reference	Type	Description
J8, J9	Transceiver RX SMA connectors	Two input SMAs (optional) to the high-speed positive and negative differential receiver channel. These connectors cannot be used together with the Gigabit Ethernet port.
J10, J11	Transceiver TX SMA connectors	Two output SMAs (optional) from the high-speed positive and negative differential transmitter channel. These connectors cannot be used together with the Gigabit Ethernet port.
C57, C58, C59, C60	Transceiver RX capacitor multiplexer	Capacitor multiplexer which requires a minor modification on the board if the optional transceiver RX SMA connectors (J8, J9) are used.
R51, R52, R53, R54	Transceiver TX resistor multiplexer	Resistor multiplexer which requires a minor modification on the board if the optional transceiver TX SMA connectors (J11, J10) are used.
Power Supply		
J4	DC input jack	Accepts a 9-V – 16-V DC power supply. Do not use this input jack while the board is plugged into a PCI Express slot.
SW1	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

Featured Device: Cyclone IV GX Device

The Cyclone IV GX Transceiver starter board features the Cyclone IV GX EP4CGX15BF14 device (U8) in a 169-pin FBGA package.



For more information about Cyclone IV device family, refer to the [Cyclone IV Device Handbook](#).

[Table 2-2](#) describes the features of the Cyclone IV GX EP4CGX15BF14 device.

Table 2-2. Cyclone IV GX EP4CGX15BF14 Device Features

Equivalent LEs	M9K RAM Blocks (Kbits)	Embedded Memory (Kbits)	18-bit × 18-bit Multipliers	Transceivers (2.5 Gbps)	PLLs	Package Type
14,400	9	540	0	2	3	169-pin FBGA

[Table 2-3](#) lists the Cyclone IV GX device component reference and manufacturing information.

Table 2-3. Cyclone IV GX Device Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U8	FPGA, Cyclone IV GX, 169-pin FBGA package, 14K LEs, lead-free	Altera Corporation	EP4CGX15BF14	www.altera.com

I/O Resources

Figure 2–2 illustrates the bank organization and I/O count for the EP4CGX15BF14 device in the 169-pin FBGA package.

Figure 2–2. EP4CGX15BF14 Device I/O Bank Diagram

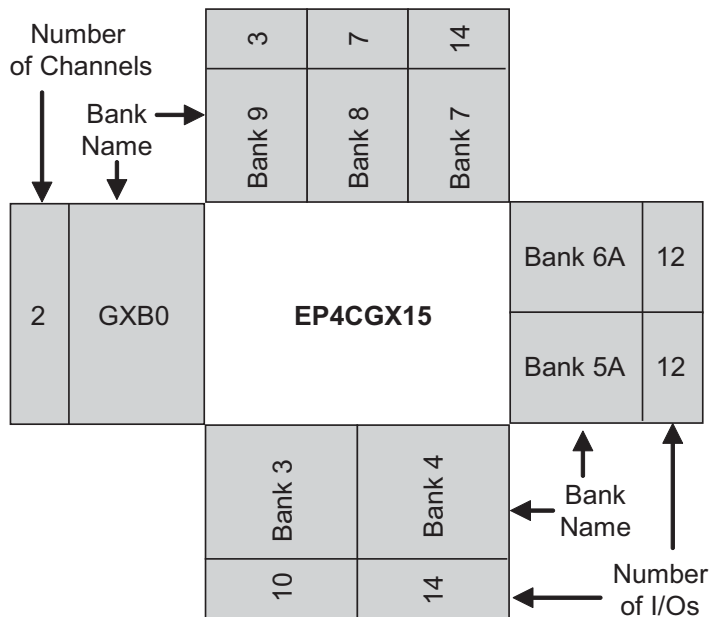


Table 2–4 lists the Cyclone IV GX device pin count and usage by function on the starter board.

Table 2–4. Cyclone IV GX Device I/O Pin Count and Usage (Note 1)

Function	I/O Standard	I/O Count	Special Pins
Flash, SSRAM, FSML Bus	2.5-V CMOS	47	1 DEV_OE
Gigabit Ethernet		4	—
Buttons		3	1 DEV_CLRn
LCD		1	—
LEDs		4	1 INIT_DONE, 1 nCEO
Clocks or Oscillators	2.5-V CMOS + LVDS	7	3 differential clock input pair, 1 clock input
PCI Express	2.5-V CMOS	1	—
Passive serial and active serial configuration		4	—
Device I/O Total:		71/72 (2)	
Notes to Table 2–4:			
(1) 60 out of 72 user I/Os are bidirectional I/O pins while the other 12 pins are for clock inputs only.			
(2) The total I/O count excludes the transceiver bank.			

MAX II CPLD EPM2210 System Controller

The board utilizes the EPM2210 System Controller, an Altera MAXII CPLD, for the following purposes:

- FPGA configuration from flash memory
- Power consumption monitoring
- Virtual JTAG interface for PC-based GUI
- Control registers for clocks
- Control registers for remote system update

Figure 2-3 illustrates the MAX II CPLD EPM2210 System Controller's functionality and external circuit connections as a block diagram.

Figure 2-3. MAX II CPLD EPM2210 System Controller Block Diagram

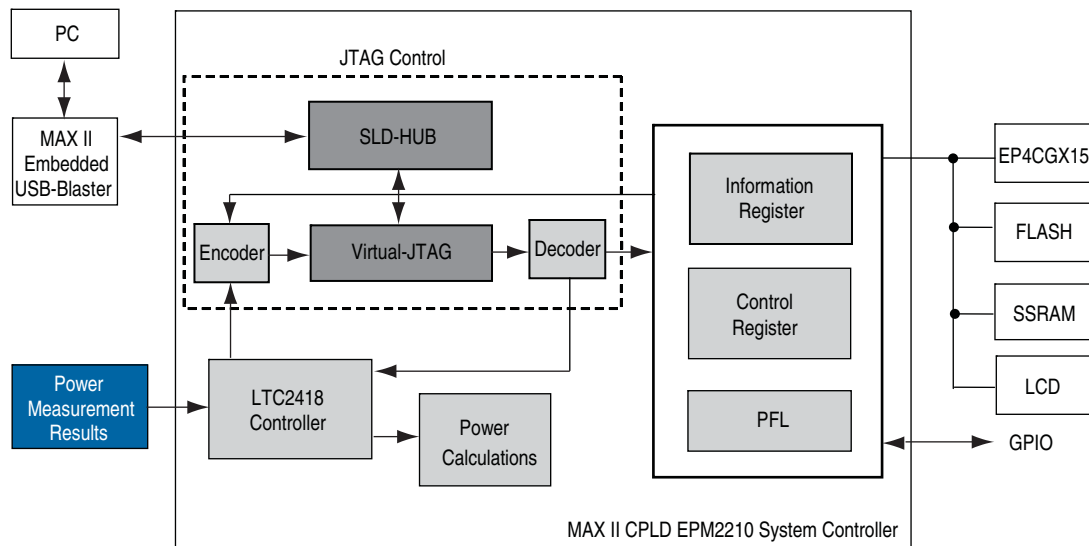


Table 2-5 lists the I/O signals present on the MAX II CPLD EPM2210 System Controller. The signal names and functions are relative to the MAX II device (U10).

Table 2-5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 1 of 3)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP4CGX15BF14 Pin Number	Description
CLK125_EN	2.5-V	R1	—	125-MHz oscillator enable
CLK125_SDA		T2	—	125-MHz programming data
CLK125_SCK		R3	—	125-MHz programming clock
CLK_SEL		R4	—	DIP - clock select SMA or oscillator
CLK_MAXII		J5	—	MAX II clock input
EPCS_nCS		B13	C5	EPCS memory chip enable
FLASH_CEn		A2	B8	FSML bus flash memory chip enable
FSML_OEn		B1	B13	FSML bus flash memory output enable

Table 2-5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 2 of 3)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP4CGX15BF14 Pin Number	Description
FSML_WEn	2.5-V	C5	A13	FSML bus flash memory write enable
FPGA_CONF_DONE		M2	J5	FPGA configuration done
FPGA_CONFIG_D0		N2	A5	FPGA configuration data
FPGA_nCONFIG		M1	D5	FPGA configuration active
FPGA_nSTATUS		L2	K6	FPGA configuration ready
FPGA_DCLK		L1	A4	FPGA configuration clock
JTAG_TCK		P3	B3	FPGA JTAG TCK
JTAG_TMS		N4	A2	FPGA JTAG TMS
JTAG_FPGA_TDO		L6	A1	FPGA JTAG TDO
JTAG_EPM2210_TDO		M5	—	MAX II JTAG TDO
FPGA_MSEL0		B16	K5	FPGA MSEL0 configuration mode select
FPGA_MSEL1		A15	N3	FPGA MSEL1 configuration mode select
FPGA_MSEL2		B14	L3	FPGA MSEL2 configuration mode select
FSML_A1		P15	A6	FSML bus address
FSML_A2		N15	B6	FSML bus address
FSML_A3		N16	C6	FSML bus address
FSML_A4		M15	A8	FSML bus address
FSML_A5		M16	A7	FSML bus address
FSML_A6		L15	M11	FSML bus address
FSML_A7		L16	N12	FSML bus address
FSML_A8		K15	K10	FSML bus address
FSML_A9		K16	L11	FSML bus address
FSML_A10		J15	M9	FSML bus address
FSML_A11		J16	N10	FSML bus address
FSML_A12		H16	N11	FSML bus address
FSML_A13		H15	H10	FSML bus address
FSML_A14		G16	H12	FSML bus address
FSML_A15		G15	N13	FSML bus address
FSML_A16		F16	M13	FSML bus address
FSML_A17		F15	J13	FSML bus address
FSML_A18		E16	K13	FSML bus address
FSML_A19		E15	L12	FSML bus address
FSML_A20		D16	L13	FSML bus address
FSML_A21		D15	K11	FSML bus address
FSML_A22		C15	K12	FSML bus address
FSML_A23		C14	D13	FSML bus address
FSML_D0		A9	D11	FSML bus data
FSML_D1		A8	D12	FSML bus data
FSML_D2		B8	E10	FSML bus data

Table 2-5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 3 of 3)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP4CGX15BF14 Pin Number	Description
FSML_D3	2.5-V	A7	F9	FSML bus data
FSML_D4		B7	E13	FSML bus data
FSML_D5		C8	F10	FSML bus data
FSML_D6		A6	F11	FSML bus data
FSML_D7		B6	G9	FSML bus data
FSML_D8		A5	G10	FSML bus data
FSML_D9		B5	A12	FSML bus data
FSML_D10		C7	A11	FSML bus data
FSML_D11		A4	B11	FSML bus data
FSML_D12		B4	B10	FSML bus data
FSML_D13		C4	C11	FSML bus data
FSML_D14		C6	C12	FSML bus data
FSML_D15		B3	C8	FSML bus data
CONF_DONE_LED		T11	—	FPGA configuration done LED
MAX_ERROR		T8	—	FPGA configuration error LED
MAX_RESETE _n		M9	—	MAX II reset push-button switch
MAX_CS _n		T12	L5	MAX II chip select
PGM_CONFIG		R10	—	Loads flash memory image identified by the PGM LEDs
PGM_LED0		T9	—	Flash memory PGM select indicator 0
PGM_LED1		R9	—	Flash memory PGM select indicator 1
PGM_SEL		T10	—	Toggles the PGM_LED[0:1] sequence
SENSE_CS _n		J3	—	Power monitor chip select
SENSE_SCK		J1	—	Power monitor serial peripheral interface (SPI) clock
SENSE_SDI		J2	—	Power monitor SPI data in
SENSE_SDO		K1	—	Power monitor SPI data out
SRAM_BW _{an}		C2	L4	FSML bus SSRAM byte write enable
SRAM_BW _{bn}		D2	M4	FSML bus SSRAM byte write enable
SRAM_CEn		E2	N6	FSML bus SSRAM chip enable
SRAM_ADSC _n		F2	—	FSML bus SSRAM address status controller
SRAM_ADSP _n		F1	—	FSML bus SSRAM address status processor
SRAM_ADV _n		G2	—	FSML bus SSRAM address valid
SRAM_CLK		G1	L7	FSML bus SSRAM clock

Table 2-6 lists the MAX II CPLD EPM2210 System Controller component reference and manufacturing information.

Table 2-6. MAX II CPLD EPM2210 System Controller Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U10	IC - MAX II CPLD EPM2210 256FBGA -3 LF 2.5 V VCCINT	Altera Corporation	EPM2210F256C3N	www.altera.com

Configuration, Status, and Setup Elements

This section describes the board's configuration, status, and setup elements.

Configuration

This section describes the FPGA, flash memory, and MAX II CPLD EPM2210 System Controller device configuration methods supported by the Cyclone IV GX Transceiver starter board. The Cyclone IV GX Transceiver starter board supports the following configuration methods:

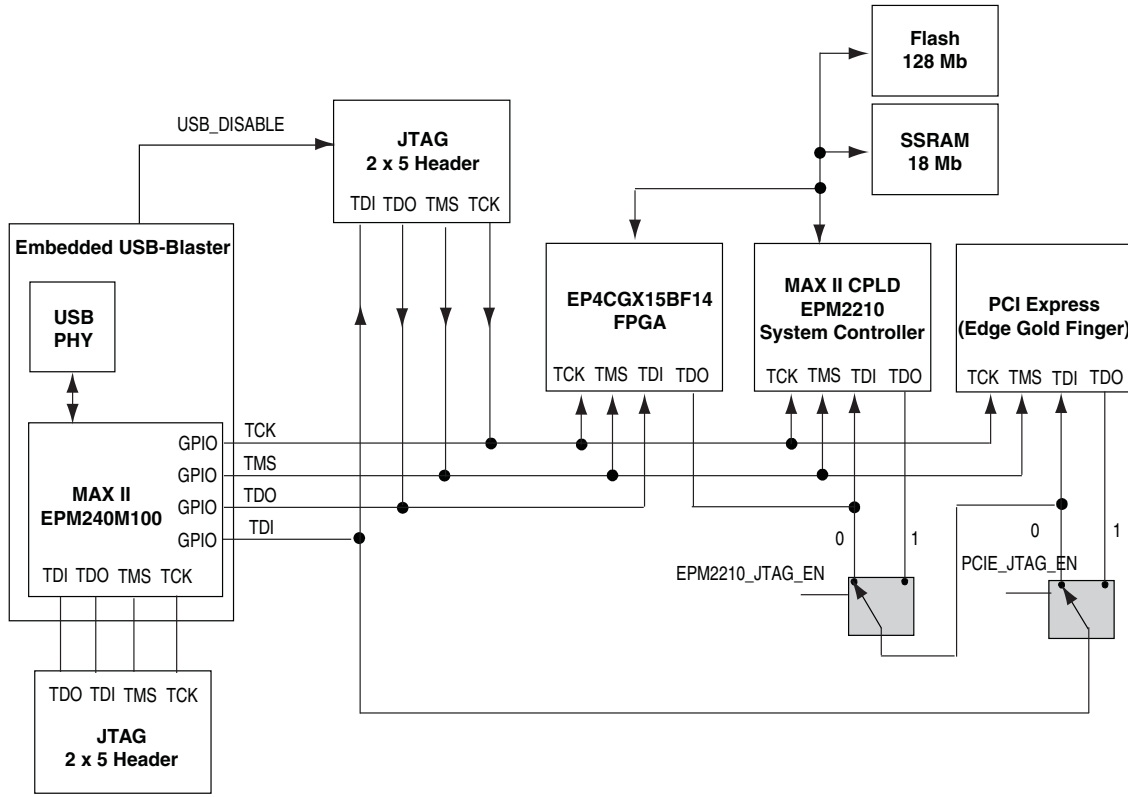
- Embedded USB-Blaster is the default method for configuring the FPGA at any time using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- Flash memory download is used for storing FPGA images which the MAX II CPLD EPM2210 System Controller uses to configure the Cyclone IV GX device either on board power-up or after the PGM configure push-button switch (S8) is pressed.
- External USB-Blaster for configuring the FPGA using an external USB-Blaster.
- Serial configuration (EPCS) device (U15) is used to store configuration data for FPGA device that supports active serial (AS) configuration and reloads the data to the FPGA upon power-up or reconfiguration.

FPGA Configuration over Embedded USB-Blaster

The USB-Blaster is implemented using a USB Type-B connector (J5), a FTDI USB 2.0 PHY device (U5), and an Altera MAX II CPLD (U4). This allows the configuration of the FPGA using a USB cable directly connected between the USB port on the board (J5) and a USB port of a PC running the Quartus II software. The JTAG chain is normally mastered by the embedded USB-Blaster found in the MAX II CPLD EPM240M100.

The embedded USB-Blaster is automatically disabled when an external USB-Blaster is connected to the JTAG chain. [Figure 2-4](#) illustrates the JTAG chain.

Figure 2-4. JTAG Chain



The Cyclone IV GX FPGA is configured via JTAG using the MAX II configuration controller design (embedded blaster) as the primary configuration mode. The board includes a MAX II CPLD EPM2210 System Controller which interfaces directly to the Cyclone IV GX FPGA for configuration, LCD control, power monitor control, and other purposes. The MAX II CPLD EPM2210 System Controller contains the required state machine and control logic to determine the configuration source for the Cyclone IV GX FPGA.

Table 2-7 lists the Cyclone IV GX configuration modes.

Table 2-7. Cyclone IV GX Configuration Modes

Configuration Mode	Device			
	Flash	MAX II	EPCS	JTAG
Passive Serial (PS)	✓	✓		
Active Serial (AS)			✓	
Flash Source	Numonyx			
JTAG		✓		✓

Flash Memory Programming

Flash memory programming is possible through a variety of methods using the Cyclone IV GX device.

The default method is to use the factory design called the Board Update Portal. This design is an embedded webserver, which serves the Board Update Portal web page. The web page allows you to select new FPGA designs including hardware, software, or both in an industry-standard S-Record File (.flash) and write the design to the user hardware page (page 1) of the flash memory over the network.

The secondary method is to use the pre-built parallel flash loader (PFL) design included in the starter kit. The starter board implements the Altera PFL megafunction for flash memory programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash memory device. This pre-built design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash memory over the USB interface using the Quartus II software. This method is used to restore the starter board to its factory default settings.

Other methods to program the flash memory can be used as well, including the Nios® II processor.



For more information on the Nios II processor, refer to the [Nios II Processor](#) page of the Altera website.

FPGA Configuration from Flash Memory

On either power-up or by pressing the PGM configure push-button switch (S1), the MAXII CPLD EPM2210 System Controller's PFL configures the FPGA from the flash memory hardware page 0 or 1 based on whether PGM_LED0 or PGM_LED1 is illuminated. [Table 2-8](#) defines the hardware page that loads when the PGM configure push-button switch (S1) is pressed. The PFL megafunction reads 16-bit data from the flash memory and converts the data to PS format. This 1-bit data is then written to the FPGA's dedicated configuration pins during configuration.

There are two pages reserved for the FPGA configuration data. The factory hardware page is considered page 0 and is loaded upon power-up if the USER_PGM DIP switch (S8) is set to '0'. Otherwise, the user hardware page 1 is loaded. Pressing the PGM configure push-button switch (S1) loads the FPGA with a hardware page based on which PGM_LED [1 : 0] (D3, D4) LED is illuminated. [Table 2-8](#) defines the hardware page that loads when the PGM configure push-button switch (S1) is pressed.

Table 2-8. PGM Configure Push-Button Switch (S1) LED Settings *(Note 1)*

PGM_LED0	PGM_LED1	Design
ON	ON	Factory hardware
ON	OFF	User hardware 1
OFF	ON	User hardware 2

Note to [Table 2-8](#):

(1) ON indicates that the LED is illuminated while OFF indicates that the LED is not illuminated.

FPGA Configuration using External USB-Blaster

The JTAG programming header provides another method for configuring the FPGA using an external USB-Blaster device with the Quartus II Programmer running on a PC. The external USB-Blaster is connected to the board through the JTAG connector (J1). [Figure 2-4 on page 2-10](#) illustrates the JTAG chain.

By default, the FPGA is the first device in the JTAG chain. To add the MAX II CPLD EPM2210 System Controller into the JTAG chain, set the board settings DIP switch (S8.3) to '0'. When the starter board is plugged into a PCI Express slot, you can add the PCI Express card into the JTAG chain by setting the board settings DIP switch (S8.4) to '1'. [Table 2-11 on page 2-14](#) summarizes the board settings DIP switch controls.

FPGA Configuration using EPCS Device

Active serial configuration can be performed using an Altera® EPCS device. During configuration, the FPGA is the master and the EPCS128 device is the slave. The configuration data is transferred to the FPGA on the DATA0 pin at a rate of one bit per clock cycle. This configuration data is synchronized to the DCLK input.



Before you program the EPCS device, set the configuration DIP switch (S7) to select the AS configuration scheme as shown in [Table 2-13 on page 2-14](#). After programming the EPCS device, the design is loaded from the EPCS device to the FPGA when you power up the board.

EPCS Programming

EPCS programming is possible through a variety of methods. One method to program the EPCS device is to use the Serial FlashLoader (SFL), a JTAG-based in-system programming solution for Altera serial configuration devices. The SFL is a bridge design for the FPGA that uses the JTAG connector (J1) to access the JTAG Indirect Configuration Device Programming File (.jic) and then uses the AS interface to program the EPCS device. Both the JTAG and AS interfaces are bridged together inside the SFL design.

Another method to program the EPCS device is to perform in-system programming through the AS programming header (J12).

Other methods to program the EPCS can be used as well, including the Nios II processor.



For more information on the following topics, refer to the respective documents:

Topic	Reference
Board Update Portal	Cyclone IV GX Transceiver Starter Kit User Guide
PFL Design	Cyclone IV GX Transceiver Starter Kit User Guide
PFL Megafunction	AN 386: Using the Parallel Flash Loader with the Quartus II Software
SFL Megafunction	AN 370: Using the Serial FlashLoader with the Quartus II Software
Managing and programming EPCS memory contents	Nios II Flash Programmer User Guide

Status Elements

The starter board includes status LEDs. This section describes the status elements.

Table 2–9 lists the LED board references, names, and functional descriptions.

Table 2–9. Board-Specific LEDs

Board Reference	LED Name	Description
D1	MAX_ERROR	Red LED. Illuminates when the MAX II CPLD EPM2210 System Controller fails to configure the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.
D2	CONF_DONE_LED	Green LED. Illuminates when the FPGA is successfully configured. Driven by the MAX II CPLD EPM2210 System Controller.
D3, D4	PROGRAM (PGM_LED1, PGM_LED0)	Green LEDs. Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when PGM select push-button switch is pressed. Driven by the MAX II CPLD EPM2210 System Controller.
D12	Power	Blue LED. Illuminates when 9-V – 16-V power is active.
D13	USB_LED	Green LED. Illuminates when the embedded USB-Blaster is in use to program the FPGA. Driven by the MAX II CPLD EPM2210 System Controller and MAX IIZ.
D14	ENET_LEDR_TX	Green LED. Illuminates to indicate Ethernet PHY transmit activity. Driven by the Marvell 88E1111 PHY.
D15	ENET_LEDR_RX	Green LED. Illuminates to indicate Ethernet PHY receive activity. Driven by the Marvell 88E1111 PHY.
D16	ENET_LEDR_LINK1000	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D17	ENET_LEDR_LINK100	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D18	ENET_LEDR_LINK10	Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed. Driven by the Marvell 88E1111 PHY.

Table 2–10 lists the board-specific LEDs component references and manufacturing information.

Table 2–10. Board-Specific LEDs Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D1	Red LED	Lumex, Inc.	SML-LXT0805IW-TR	www.lumex.com
D2-D4, D13-D18	Green LEDs	Lumex, Inc.	SML-LX1206GC-TR	www.lumex.com
D12	Blue LED	Lumex, Inc.	SML-LX1206USBC-TR	www.lumex.com

Setup Elements

The starter board includes several different kinds of setup elements. This section describes the following setup elements:

- Board settings DIP switch
- Configuration settings DIP switch
- Configuration push-button switches

Board Settings DIP Switch

The board settings DIP switch (S8) controls various features specific to the board and the MAX II CPLD EPM2210 System Controller logic design. Table 2-11 shows the switch controls and descriptions.

Table 2-11. Board Settings DIP Switch Controls

Board Reference	Schematic Signal Name	Description	Default (1)
S8.1	CLK_SEL	ON : On-board 125-MHz LVDS oscillator clock select OFF : SMA input clock select	ON
S8.2	USER_PGM	ON: Load user hardware page 1 from flash memory upon power-up OFF: Load factory design from flash memory upon power-up	OFF
S8.3	EPM2210_JTAG_EN	ON : Bypass Max II CPLD EPM2210 System Controller OFF : Max II CPLD EPM2210 System Controller in-chain	OFF
S8.4	PCIE_JTAG_EN	ON : Bypass PCI Express OFF : PCI Express in-chain	ON

Note to Table 2-11:

(1) ON indicates a setting of '0' while OFF indicates a setting of '1'.

Table 2-12 lists the board settings DIP switch component reference and manufacturing information.

Table 2-12. Board Settings DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S8	Four-position slide DIP switch	C & K Components	TDA04H0SB1	www.ck-components.com

Configuration Settings DIP Switch

The configuration settings DIP switch (S7) controls the configuration scheme selection. A configuration scheme with different configuration voltage standards is selected by driving the MSEL pins either high or low, as shown in Table 2-11.

Table 2-13. Configuration Settings DIP Switch Controls (Part 1 of 2) (Note 1)

Configuration Scheme	Setting				POR Delay
	EPCS_nCS (S7.4)	FPGA_MSEL2 (S7.3)	FPGA_MSEL1 (S7.2)	FPGA_MSEL0 (S7.1)	
Active Serial – Enables active serial configuration with fast or standard power-on-reset delay.	1	0	1	1	Fast
	1	0	1	0	Standard
Passive Serial – Enables passive serial configuration with fast or standard power-on-reset delay.	0	1	0	0	Fast
	0	0	0	0	Standard

Table 2-13. Configuration Settings DIP Switch Controls (Part 2 of 2) (Note 1)

Configuration Scheme	Setting				POR Delay
	EPCS_nCS (S7.4)	FPGA_MSEL2 (S7.3)	FPGA_MSEL1 (S7.2)	FPGA_MSEL0 (S7.1)	
JTAG – JTAG-based configuration	X (2)				—

Notes to Table 2-13:

- (1) ON indicates a setting of '0' while OFF indicates a setting of '1'.
- (2) X indicates does not care. The JTAG-based configuration takes precedence over other configuration schemes and therefore, the FPGA_MSEL pin settings are ignored.

Table 2-12 lists the configuration settings DIP switch component reference and manufacturing information.

Table 2-14. Configuration Settings DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S8	Four-position slide DIP switch	C & K Components	TDA04H0SB1	www.ck-components.com

Configuration Push-Button Switches

The PGM configure push-button switch, PGM_CONFIG (S1), is an input to the MAX II CPLD EPM2210 System Controller. The push-button switch forces a reconfiguration of the FPGA from flash memory. The location in the flash memory is based on the PGM_LED [1 : 0] setting when the button is released. Valid settings include PGM_LED0 or PGM_LED1.

The PGM select push-button switch, PGM_SEL (S2), toggles the program LEDs (D3, D4) sequence. Refer to Table 2-8 on page 2-11 for the PGM_LED [1 : 0] sequence definitions.

The MAX II reset push-button switch, MAX_RESETn (S3), resets the MAX II CPLD EPM2210 System Controller.

Table 2-15 lists the configuration push-button switches component reference and manufacturing information.

Table 2-15. Configuration Push-button Switches Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S1-S3	Push-button switches	Panasonic	EVQPAC07K	www.panasonic.com/industrial/

Clock Circuitry

This section describes the board's clock inputs.

Cyclone IV GX Transceiver Clock Inputs

Figure 2-5 shows the Cyclone IV GX Transceiver starter board clock inputs.

Figure 2-5. Cyclone IV GX Transceiver Starter Board Clock Inputs

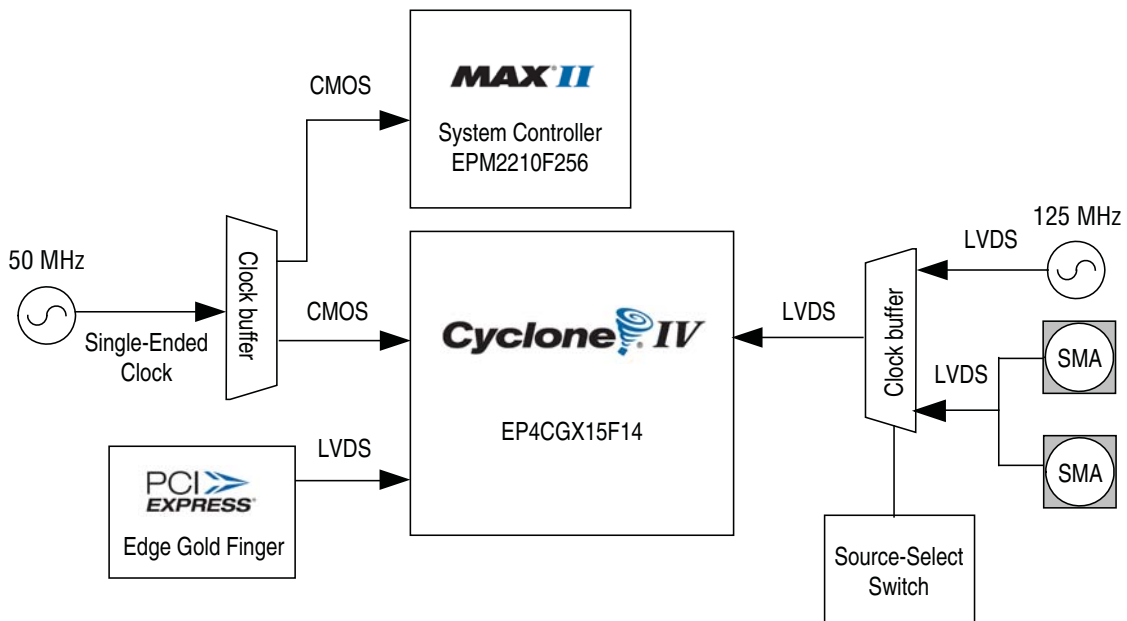


Table 2-16 shows the clock inputs for the Cyclone IV GX Transceiver starter board.

Table 2-16. Cyclone IV GX Transceiver Starter Board Clock Inputs

Source Component Board Reference	Source	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number	Description
J3	SMA or 125 MHz	CLKIN_SMA_P	LVPECL	M7 or E7 depending on CLK_SEL	Positive and negative differential LVPECL clock inputs from SMAs.
J2		CLKIN_SMA_N		N7 or E6 depending on CLK_SEL	
X1.4	125 MHz	125M_OCS_P	LVDS	M7 or E7 depending on CLK_SEL	Positive and negative differential LVDS clock inputs from 125-MHz crystal oscillator.
X1.5		125M_OCS_N		N7 or E6 depending on CLK_SEL	
U14.A13	100 MHz	PCIE_REFCLK_P	HCSL	J6	Positive and negative differential HCSL clock inputs from PCI Express edge connector.
U14.A14		PCIE_REFCLK_N		J7	

General User Input/Output

This section describes the user I/O interface to the FPGA, including the push-buttons, DIP switches, status LEDs, and character LCD.

User-Defined Push-Button Switches

The starter board includes three user-defined push-button switches: two general user and one CPU reset push-button switches. For information on the system and safe reset push-button switches, refer to “[Configuration Push-Button Switches](#)” on [page 2-15](#).

Board references S5 and S6 are push-button switches that allow you to interact with the Cyclone IV GX device. When the switch is pressed and held down, the device pin is set to logic 0; when the switch is released, the device pin is set to logic 1. There is no board-specific function for these general user push-button switches.

Board reference S4 is the CPU reset push-button switch, CPU_RESETh, which is an input to the Cyclone IV GX device and the MAX II CPLD EPM2210 System Controller. CPU_RESETh is intended to be the master reset signal for the FPGA design loaded into the Cyclone IV GX device. This switch also acts as a regular I/O pin.

[Table 2-17](#) lists the user-defined push-button switch schematic signal names and their corresponding Cyclone IV GX device pin numbers.

Table 2-17. User-Defined Push-Button Switch Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
S6	User-defined push-button switch. When the switch is pressed, a logic 0 is selected. When the switch is released, a logic 1 is selected.	USER_PB0	2.5-V	H13
S5		USER_PB1		G13
S4		CPU_RESETh		D10

[Table 2-18](#) lists the user-defined push-button switch component reference and the manufacturing information.

Table 2-18. User-Defined Push-Button Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S4 to S6	Push-button switches	Panasonic	EVQPAC07K	www.panasonic.com/industrial/

User-Defined LEDs

The starter board includes four general purpose LEDs. This section describes all user-defined LEDs. For information on board-specific or status LEDs, refer to “[Status Elements](#)” on [page 2-13](#).

Board references D5 through D8 are four user-defined LEDs which allow status and debugging signals to be driven to the LEDs from the FPGA designs loaded into the Cyclone IV GX device. The LEDs illuminate when a logic 0 is driven, and turns off when a logic 1 is driven. There is no board-specific function for these LEDs.

[Table 2-19](#) lists the user-defined LED schematic signal names and their corresponding Cyclone IV GX pin numbers.

Table 2-19. User-Defined LED Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
D8	User-defined LEDs. Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	USER_LED0	2.5-V	N8
D7		USER_LED1		C13
D6		USER_LED2		N5
D5		USER_LED3		M6

Table 2-20 lists the user-defined LED component reference and the manufacturing information.

Table 2-20. User-Defined LED Component Reference and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D5 to D8	Green LEDs	Lumex, Inc.	SML-LX1206GC-TR	www.lumex.com

LCD

The starter board contains a single 14-pin 0.1" pitch dual-row header that interfaces to a 16 character × 2 line Lumex LCD display. The LCD has a 14-pin receptacle that mounts directly to the board's 14-pin header, so it can be easily removed for access to components under the display. You can also use the header for debugging or other purposes.

Table 2-21 summarizes the LCD pin assignments. The signal names and directions are relative to the Cyclone IV GX Transceiver.

Table 2-21. LCD Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
J6.5	LCD read or write	FSML_A0	2.5-V	N4
J6.4	LCD register select	FSML_A1		A6
J6.7	LCD data bus	FSML_D0		D11
J6.8	LCD data bus	FSML_D1		D12
J6.9	LCD data bus	FSML_D2		E10
J6.10	LCD data bus	FSML_D3		F9
J6.11	LCD data bus	FSML_D4		E13
J6.12	LCD data bus	FSML_D5		F10
J6.13	LCD data bus	FSML_D6		F11
J6.14	LCD data bus	FSML_D7		G9
J6.6	LCD chip select	LCD_CS _n		L9

Table 2-22 shows the LCD pin definitions, and is an excerpt from the Lumex data sheet.



For more information such as timing, character maps, interface guidelines, and other related documentation, visit www.lumex.com.

Table 2-22. LCD Pin Definitions and Functions

Pin Number	Symbol	Level	Function	
1	V _{DD}	—	Power supply	5 V
2	V _{SS}	—		GND (0 V)
3	V ₀	—		For LCD drive
4	RS	H/L	Register select signal H: Data input L: Instruction input	
5	R/W	H/L	H: Data read (module to MPU) L: Data write (MPU to module)	
6	E	H, H to L	Enable	
7-14	DB0-DB7	H/L	Data bus, software selectable 4-bit or 8-bit mode	



The particular model used does not have a backlight and the LCD drive pin is not connected.

Table 2-23 lists the LCD component references and the manufacturing information.

Table 2-23. LCD Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J6	2×7 pin, 100 mil, vertical header	Samtec	TSM-107-07-G-D	www.samtec.com
	2×16 character display, 5×8 dot matrix	Lumex Inc.	LCM-S01602DSR/C	www.lumex.com

Components and Transceiver Interfaces

This section describes the starter board's communication ports and interface cards relative to the Cyclone IV GX device. The starter board supports the following communication ports:

- PCI Express
- 10/100/1000 Ethernet
- Transceiver SMA connectors (optional)

PCI Express

The Cyclone IV GX Transceiver starter board fits entirely into a PC motherboard with a ×1 PCI Express slot which can accommodate a half height low-profile PCI Express add-in card. The starter board comes with a full height I/O bracket for its low profile form factor card. This interface uses the Cyclone IV GX device's PCI Express hard IP block, saving logic resources for the user logic application.



For more information on using the PCI Express hard IP block, refer to the *PCI Express Compiler User Guide*.

The PCI Express interface supports a channel width of ×1 as well as the connection speed of Gen1 at 2.5 Gbps/lane.

The board's power can be sourced entirely from the PCI Express edge connector when installed into a PC motherboard. Turn the power switch (SW1) to ON position when you install the board into a PC motherboard. Although the board can also be powered by a laptop power supply for use on a lab bench, it is not recommended to use from both supplies at the same time. Ideal diode power sharing devices have been designed into this board to prevent damages or back-current from one supply to the other.

The PCIE_REFCLK_P and PCIE_REFCLK_N signals are a 100-MHz differential input that is driven from the PC motherboard on this board through the PCI Express edge connector. This signal connects directly to a Cyclone IV GX REFCLK input pin pair. This clock is terminated on the motherboard and therefore, no on-board termination is required. This clock can have spread-spectrum properties that change its period between 9.847 ps to 10.203 ps. The I/O standard is High-Speed Current Steering Logic (HCSL).

By default, the GXB_RX0 channel of the FPGA is connected to the PCIE_RX_P and PCIE_RX_N signals, while the GXB_TX0 channel is connected to the PCIE_TX_P and PCIE_TX_N signals.

Table 2-24 summarizes the PCI Express pin assignments. The signal names and directions are relative to the Cyclone IV GX FPGA.

Table 2-24. PCI Express Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U14.A16	Add-in card transmit bus	PCIE_TX_P	1.4-V PCML	G2
U14.A17	Add-in card transmit bus	PCIE_TX_N		G1
U14.B14	Add-in card receive bus	PCIE_RX_P		J2
U14.B15	Add-in card receive bus	PCIE_RX_N		J1
U14.A13	Motherboard reference clock	PCIE_REFCLK_P	HCSL	J6
U14.A14	Motherboard reference clock	PCIE_REFCLK_N		J7
U14.A11	Reset	PCIE_PERSTn	LVTTTL	A10
U14.A1	Present	PCIE_PRSENTn_x1	—	—
U14.B17	x1 Present	PCIE_PRSENTn_x1	—	—
U14.A5	Motherboard TCK	PCIE_JTAG_TCK	3.3-V	—
U14.A6	Motherboard TDI	PCIE_JTAG_TDI		—
U14.A7	Motherboard TDO	PCIE_JTAG_TDO		—
U14.A8	Motherboard TMS	PCIE_JTAG_TMS		—

10/100/1000 Ethernet

A Marvell 88E1111 PHY device is used for 10/100/1000 BASE-T Ethernet connection. The device is an auto-negotiating Ethernet PHY with an SGMII interface to the FPGA. The MAC function must be provided in the FPGA for typical networking applications such as the Altera Triple Speed Ethernet MegaCore design. The Marvell 88E1111 PHY uses 2.5-V and 1.2-V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator. The device interfaces to a Halo Electronics HFJ11-1G02E model RJ45 with internal magnetics that can be used for driving copper lines with Ethernet traffic.

By default, the GXB_RX1 and GXB_TX1 channels of the FPGA are connected to the Ethernet PHY as shown in Table 2-27 on page 2-22.

Figure 2-6 shows the SGMII interface between the FPGA (MAC) and Marvell 88E1111 PHY.

Figure 2-6. SGMII Interface between FPGA (MAC) and Marvell 88E1111 PHY

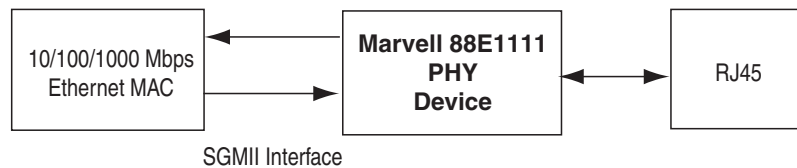


Table 2-25 lists the Ethernet PHY interface pin assignments.

Table 2-25. Ethernet PHY Pin Assignments, Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U9.82	SGMII TX data	ENET_TX_P	1.4-V PCML	C2
U9.81	SGMII TX data	ENET_TX_N		C1
U9.77	SGMII RX data	ENET_RX_P		E2
U9.75	SGMII RX data	ENET_RX_N		E1
U9.25	Management bus control	ENET_MDC	2.5-V	N9
U9.24	Management bus data	ENET_MDIO		K8
U9.23	Management bus interrupt	ENET_INTn		F12
U9.28	Device reset	ENET_RESETn		K9

Table 2-26 lists the Ethernet PHY interface component reference and manufacturing information.

Table 2-26. Ethernet PHY Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U9	Ethernet PHY BASE-T device	Marvell Semiconductor	88E1111-B2-CAAIC000	www.marvell.com

Transceiver SMA Connectors (Optional)

Board references J9 and J8 are two optional input SMAs to the high-speed positive and negative differential receiver channel while J11 and J10 are two optional output SMAs from the high-speed positive and negative differential transmitter channel. By default, the `GXB_RX1` channel of the FPGA is connected to the Ethernet PHY through capacitor multiplexer C59 and C58, while the `GXB_TX1` channel is connected to the Ethernet PHY through resistor multiplexer R53 and R52. You need to perform a solder modification on the board if you intend to use the optional transceiver SMA connectors. You can use these SMAs to connect to external circuit boards or daughtercards for transceiver applications.

Table 2-27 shows the capacitor and resistor multiplexer locations to enable either the default Ethernet PHY connection or the optional transceiver SMA connectors. The capacitors multiplexer are 0.1- μ F capacitors and the multiplexer resistors are 0- Ω resistors.

Table 2-27. Multiplexer Locations for the Ethernet PHY Connection and Transceiver SMAs Connectors

Board Reference	Description	Multiplexer Location
C59, C58, C60, C57	Ethernet PHY RX enable	<ul style="list-style-type: none"> ■ Populate C59 and C58 ■ Unpopulate C60 and C57 (default)
R53, R52, R54, R51	Ethernet PHY TX enable	<ul style="list-style-type: none"> ■ Populate R53 and R52 ■ Unpopulate R54 and R51 (default)
C59, C58, C60, C57	Transceiver SMA RX enable	<ul style="list-style-type: none"> ■ Populate C60 and C57 ■ Unpopulate C59 and C58
R53, R52, R54, R51	Transceiver SMA TX enable	<ul style="list-style-type: none"> ■ Populate R54 and R51 ■ Unpopulate R53 and R52

Memory

This section describes the board's memory interface support and also their signal names, types, and connectivity relative to the Cyclone IV GX device. The board has the following memory interfaces:

- SSRAM
- Flash

SSRAM

The SSRAM device consists of a single standard synchronous SRAM, providing 18-Mb of memory with a 16-bit data bus. This device is part of the shared FSML bus which connects to the flash memory, SRAM, and MAX II CPLD EPM2210 System Controller.

Table 2-28 lists the SSRAM pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone IV GX device in terms of I/O setting and direction.

Table 2-28. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U12.37	Address bus	FSML_A1	2.5-V	A6
U12.36	Address bus	FSML_A2		B6
U12.32	Address bus	FSML_A3		C6
U12.33	Address bus	FSML_A4		A8
U12.34	Address bus	FSML_A5		A7
U12.35	Address bus	FSML_A6		M11
U12.42	Address bus	FSML_A7		N12
U12.43	Address bus	FSML_A8		K10
U12.44	Address bus	FSML_A9		L11
U12.45	Address bus	FSML_A10		M9
U12.46	Address bus	FSML_A11		N10
U12.47	Address bus	FSML_A12		N11
U12.48	Address bus	FSML_A13		H10
U12.49	Address bus	FSML_A14		H12
U12.50	Address bus	FSML_A15		N13
U12.80	Address bus	FSML_A16		M13
U12.81	Address bus	FSML_A17		J13
U12.82	Address bus	FSML_A18		K13
U12.99	Address bus	FSML_A19		L12
U12.100	Address bus	FSML_A20		L13
U12.39	Address bus	FSML_A21		K11
U12.58	Data bus	FSML_D0		D11
U12.59	Data bus	FSML_D1		D12
U12.62	Data bus	FSML_D2		E10
U12.63	Data bus	FSML_D3		F9
U12.68	Data bus	FSML_D4		E13
U12.69	Data bus	FSML_D5		F10
U12.72	Data bus	FSML_D6		F11
U12.73	Data bus	FSML_D7		G9
U12.8	Data bus	FSML_D8		G10
U12.9	Data bus	FSML_D9		A12
U12.12	Data bus	FSML_D10		A11
U12.13	Data bus	FSML_D11		B11
U12.18	Data bus	FSML_D12		B10
U12.19	Data bus	FSML_D13		C11
U12.22	Data bus	FSML_D14		C12
U12.23	Data bus	FSML_D15	C8	
U12.86	Output enable	FSML_OEn	B13	

Table 2-28. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U12.85	Address status controller	SRAM_ADSCn	2.5-V	—
U12.84	Address status processor	SRAM_ADSPn		—
U12.83	Burst address advance	SRAM_ADVn		—
U12.93	Byte lane a write enable	SRAM_BWan		L4
U12.94	Byte lane b write enable	SRAM_BWbn		M4
U12.98	Chip enable	SRAM_CEn		N6
U12.89	Clock	SRAM_CLK		L7
U12.97	Chip enable	SRAM_CE2		—
U12.92	Chip enable	SRAM_CE3n		—
U12.88	Global write enable	SRAM_GWn		—
U12.31	Burst sequence mode selection	SRAM_MODE		—
U12.64	Sleep enable	SRAM_ZZ		—

Table 2-29 lists the SSRAM component reference and manufacturing information.

Table 2-29. SSRAM Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U12	Standard Synchronous Pipelined SCD, 1024 K × 18, 250 MHz	ISSI Inc.	IS61VPS102418A-250TQL	www.issi.com

Flash

The flash interface consists of a single synchronous flash memory device, providing 128-Mb of memory with a 16-bit data bus. This device is part of the shared FSML bus which connects to the flash memory, SRAM, LCD, and MAX II CPLD EPM2210 System Controller.



For more information about the flash memory map storage, refer to the *Cyclone IV GX Transceiver Starter Kit User Guide*.

Table 2-30 lists the flash pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone IV GX device in terms of I/O setting and direction.

Table 2-30. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U11.30	Chip enable	FLASH_CEn	2.5-V	B8
U11.32	Output enable	FSML_OEn		B13
U11.44	Reset	FLASH_RESEtN		—
U11.14	Write enable	FSML_WEn		A13
U11.15	Write protect	FLASH_WPn		—
U11.29	Address bus	FSML_A1		A6
U11.25	Address bus	FSML_A2		B6
U11.24	Address bus	FSML_A3		C6
U11.23	Address bus	FSML_A4		A8
U11.22	Address bus	FSML_A5		A7
U11.21	Address bus	FSML_A6		M11
U11.20	Address bus	FSML_A7		N12
U11.19	Address bus	FSML_A8		K10
U11.8	Address bus	FSML_A9		L11
U11.7	Address bus	FSML_A10		M9
U11.6	Address bus	FSML_A11		N10
U11.5	Address bus	FSML_A12		N11
U11.4	Address bus	FSML_A13		H10
U11.3	Address bus	FSML_A14		H12
U11.2	Address bus	FSML_A15		N13
U11.1	Address bus	FSML_A16		M13
U11.55	Address bus	FSML_A17		J13
U11.18	Address bus	FSML_A18		K13
U11.17	Address bus	FSML_A19		L12
U11.16	Address bus	FSML_A20		L13
U11.11	Address bus	FSML_A21		K11
U11.10	Address bus	FSML_A22		K12
U11.9	Address bus	FSML_A23		D13
U11.34	Data bus	FSML_D0		D11
U11.36	Data bus	FSML_D1		D12
U11.39	Data bus	FSML_D2		E10
U11.41	Data bus	FSML_D3		F9
U11.47	Data bus	FSML_D4	E13	
U11.49	Data bus	FSML_D5	F10	
U11.51	Data bus	FSML_D6	F11	
U11.53	Data bus	FSML_D7	G9	
U11.35	Data bus	FSML_D8	G10	
U11.37	Data bus	FSML_D9	A12	

Table 2-30. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U11.40	Data bus	FSML_D10	2.5-V	A11
U11.42	Data bus	FSML_D11		B11
U11.48	Data bus	FSML_D12		B10
U11.50	Data bus	FSML_D13		C11
U11.52	Data bus	FSML_D14		C12
U11.54	Data bus	FSML_D15		C8

Table 2-31 lists the flash component reference and manufacturing information.

Table 2-31. Flash Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U11	128-Mb synchronous flash	Numonyx	JS28F128P33BF	www.numonyx.com

Power Supply

The starter board's power is provided through a laptop-style DC power input. The input voltage must be in the range of 9 V to 16 V. The DC voltage is then stepped down to various power rails used by the components on the board.

An on-board multi-channel analog-to-digital converter (ADC) measures both the voltage and current for several specific board rails. The power utilization is displayed using a GUI that can graph power consumption versus time.

Power Distribution System

Figure 2-7 shows the power distribution system on the starter board. The currents shown are conservative absolute maximum levels and reflect the regulator inefficiencies and sharing.

Figure 2-7. Power Distribution System

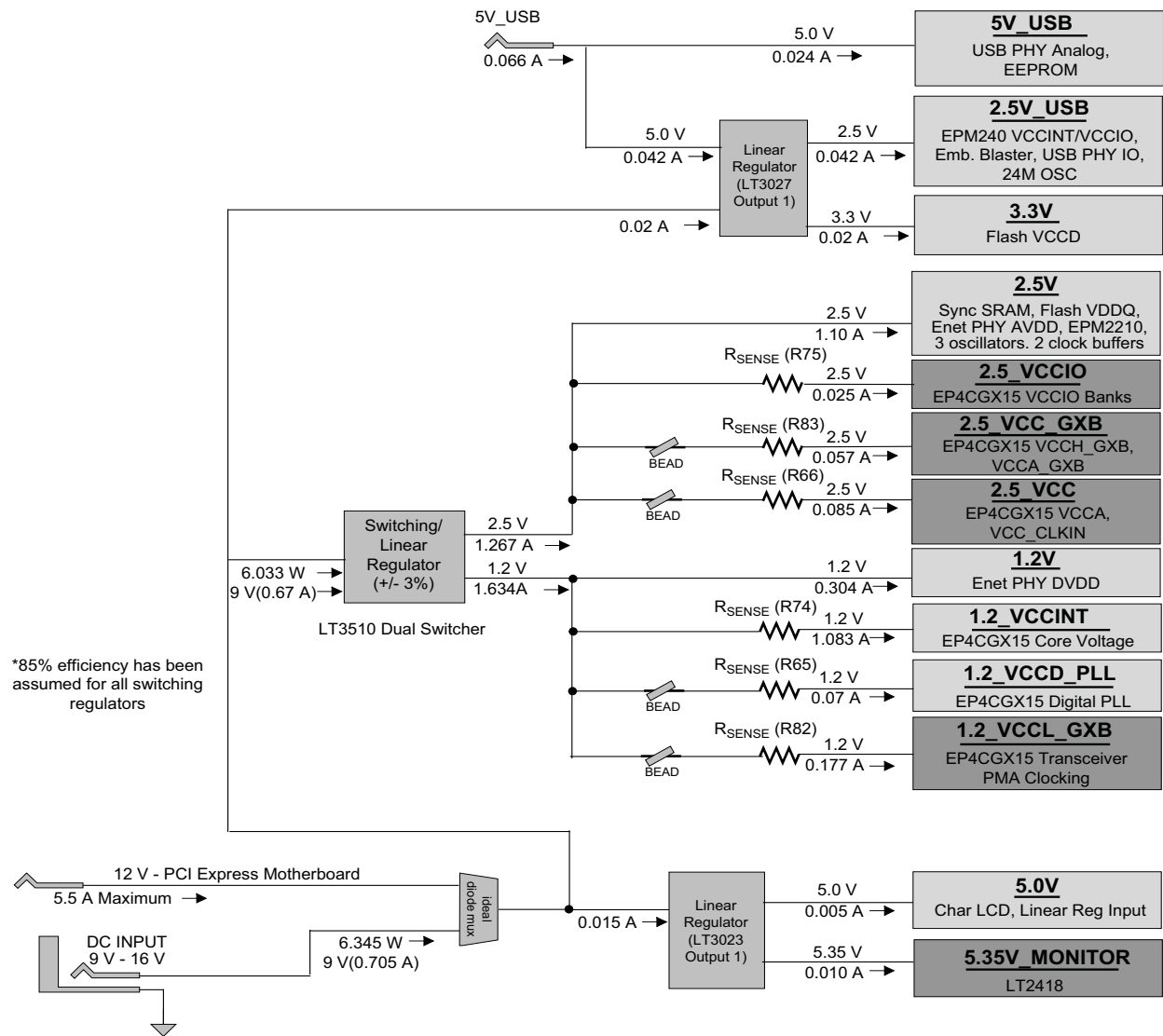


Table 2-32 lists the power supply component reference and manufacturing information.

Table 2-32. Power Supply Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
—	16-V power supply	EDAC Power Electronics	EA1060A	www.edac.com.tw

Power Measurement

There are six power supply rails which have on-board voltage and current sense capabilities. The power supply rails are split from the primary supply plane by a low-value sense resistor for the 8-channel differential input 24-bit ADC device to measure voltage and current. A SPI bus connects the ADC device to the MAX II CPLD EPM2210 System Controller as well as the Cyclone IV GX Transceiver.

Figure 2-8 shows the block diagram for the power measurement circuitry.

Figure 2-8. Power Measurement Circuit

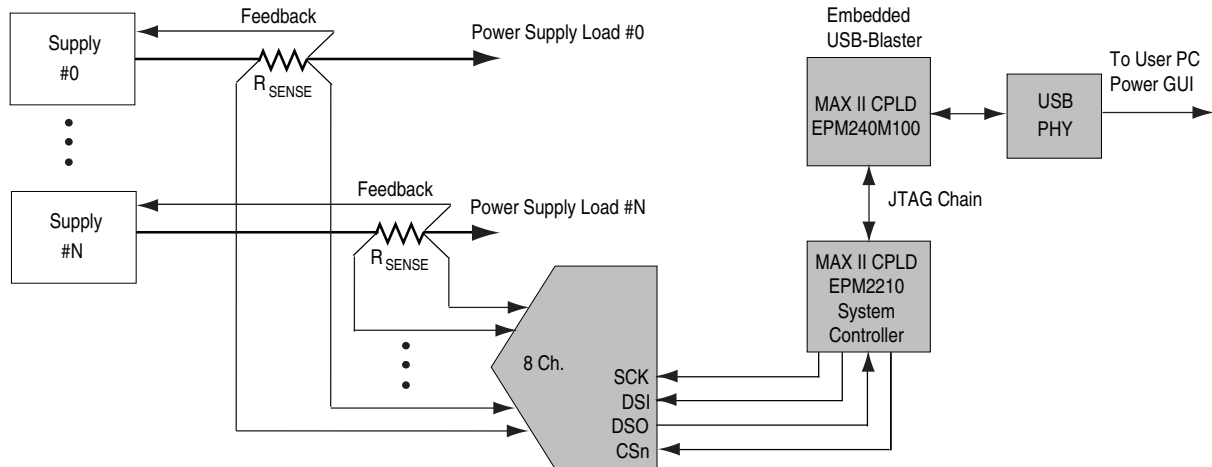


Table 2-33 lists the targeted rails. The schematic signal name column specifies the name of the rail being measured and the device pin column specifies the devices attached to the rail. If no subnet is named, the power is the total output power for that voltage.

Table 2-33. Power Rails Measurement Based on the Rail Selected in the Power GUI

Rail	Schematic Signal Name	Voltage (V)	Device Pin	Description
1	2.5_VCC	2.5	VCCA	FPGA PLL analog power
		2.5	VCC_CLKIN	V _{IO} clock input pins
2	1.2_VCCL_GXB	1.2	VCCL_GXB	Transceiver physical medium attachment (PMA) and auxiliary power
3	2.5_VCC_GXB	2.5	VCCH_GXB	Transceiver output buffer power
		2.5	VCCA_GXB	Transceiver PMA power
4	2.5_VCCIO	2.5	VCCIO	FPGA I/O bank power
5	1.2_VCCINT	1.2	VCCINT	FPGA core voltage and PCI Express hard IP block power
6	1.2_VCCD_PLL	1.2	VCCD_PLL	FPGA PLL digital power

Table 2-34 lists the power measurement ADC component reference and manufacturing information.

Table 2-34. Power Measurement ADC Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U19	8-channel differential input 24-bit ADC	Linear Technology	LTC2418	www.linear.com



Statement of China-RoHS Compliance

Table 2-35 lists hazardous substances included with the kit.

Table 2-35. Table of Hazardous Substances' Name and Concentration *Notes (1), (2)*

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Cyclone IV GX Transceiver starter board	X*	0	0	0	0	0
16-V power supply	0	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 2-35:

- (1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.
- (2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

Revision History

The following table displays the revision history for this reference manual.

Date and Document Version	Changes Made	Summary of Changes
March 2010 v1.0	Initial release.	—

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.






Contact <i>(Note 1)</i>	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General) (Software Licensing)	Email	nacomp@altera.com
	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown in the following table.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicates command names, dialog box titles, dialog box options, and other GUI labels. For example, Save As dialog box.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, and software utility names. For example, qdesigns directory, d: drive, and chiptrip.gdf file.
<i>Italic Type with Initial Capital Letters</i>	Indicates document titles. For example, <i>AN 519: Design Guidelines</i> .
<i>Italic type</i>	Indicates variables. For example, $n + 1$. Variable names are enclosed in angle brackets (< >). For example, <file name> and <project name>.pdf file.
Initial Capital Letters	Indicates keyboard keys and menu names. For example, Delete key and the Options menu.
“Subheading Title”	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, “Typographic Conventions.”
Courier type	Indicates signal, port, register, bit, block, and primitive names. For example, data1, tdi, and input. Active-low signals are denoted by suffix n. For example, resetn. Indicates command line commands and anything that must be typed exactly as it appears. For example, c:\qdesigns\tutorial\chiptrip.gdf. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword SUBDESIGN), and logic function names (for example, TRI).
1., 2., 3., and a., b., c., and so on.	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The angled arrow instructs you to press Enter.
	The feet direct you to more information about a particular topic.