## DESCRIPTION

The GR12883 is a 131072 word by 8 bits (128K x 8) non-volatile CMOS Static Ram, fabricated from advanced silicon gate CMOS technology and a high reliability lithium power cell.

The power down circuit is fully automatic and is referenced at 4.5 volts. At this point the GR12883 is write protected by an internal inhibit function for Data Protection and the memory contents are retained by the lithium power source.

Power down is very fast, this being essential for data integrity, taking a maximum of 15 µS (15 microseconds) to power down from 5 volts to 0 volts. This is much faster than system power failure conditions. Therefore there are no special conditions required when installing the GR12883.

The GR12883 can, without external power, retain data almost indefinitely. The limiting factor will be the shelf life of the lithium cell, which is typically ten years. It is possible that this figure may be extended in view of the extremely light duty imposed upon the cell.

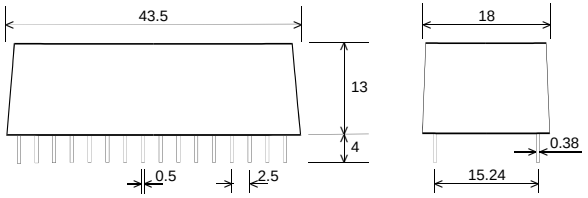
## APPLICATION

When powered down, the GR12883 is transportable and data can be moved from system to system, this makes it ideal for program development, data collection in data loggers, program changes in process control, automation and robotics and user definable lookup tables, etc.

## DISPOSAL INSTRUCTIONS

Do not dispose of non-volatile memory devices by incineration or crushing. Devices may be returned carriage paid to Greenwich Instruments Ltd., for disposal.

## DIMENSIONS (mm)

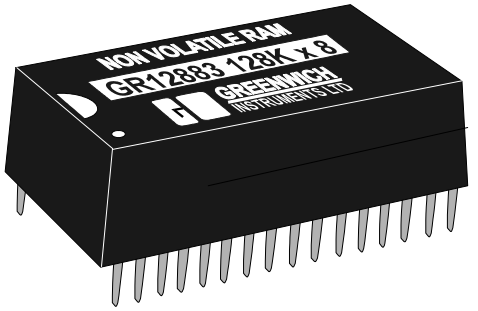



UK

Greenwich Instruments Ltd.,
Meridian House, Park Road,
Swanley, Kent. BR8 8AH
Tele: 08700 505 404
Fax: 08700 505 405



# *GR12883 (128K x 8) NON-VOLATILE RAM*




**http://www.greenwichinst.co.uk**

ISSUE 3 JAN 2006

# GR12883 NON-VOLATILE RAM

GREENWICH INSTRUMENTS LTD

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Min | Max | Units |
|---|---|---|---|
| Vdd | – 0.3 | 7.0 | Volts |
| Vi/o | – 0.3 | Vdd + 0.3 | Volts |
| Temp | – 20 | + 70 | deg. C |

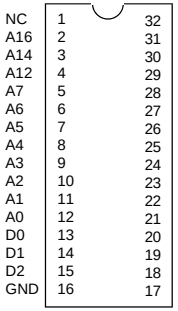
### OPERATING CONDITIONS

| Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Vdd | 4.75 | 5.0 | 5.5 | Volts |
| VTH | | 4.5 | | Volts |
| Vin (1) | 2.2 | | | Volts |
| Vin (0) | | | 0.8 | Volts |
| Iin (CE) | | | 1.0 | LSTTL Load |
| Iin (any other pin) | – 1.0 | | + 1.0 | µA. |
| Vout (1)(Iout = –1mA) | 2.4 | | | Volts |
| Vout (0)(Iout = +2mA) | | | 0.4 | Volts |
| Idd (Active) | | 30 | | mA. |
| Idd (Deselected) | | 1.0 | | mA. |
| Tcycle | | | 100 | nS. |
| Cin (any pin) | | 10 | | pF |

### OPERATING MODE

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WR}$ | MODE | D0 - D7 | Idd |
|---|---|---|---|---|---|
| H | X | X | Unsel. | Hi-Z | Deselected |
| L | H | H | Unsel. | Hi-Z | Active |
| L | L | H | Read | Dout | Active |
| L | X | L | Write | Din | Active |

### PIN CONNECTIONS



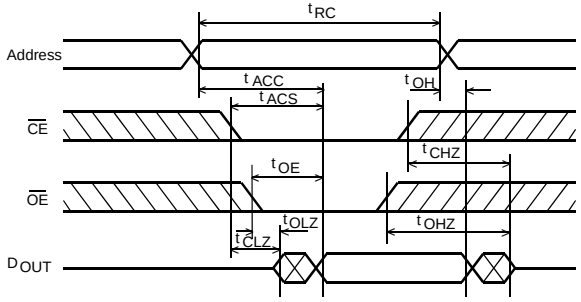

### PIN DESIGNATIONS

| Pin | Function |
|---|---|
| A0-A16 | Address I/P`s |
| D0-D7 | Data in/out |
| $\overline{OE}$ | Output Enable |
| $\overline{CE}_1$ $CE_2$ | Chip Enable |
| $\overline{WR}$ | Write Enable |
| Vdd | +5Volt Power |
| GND | Ground |
| NC | No Connect |

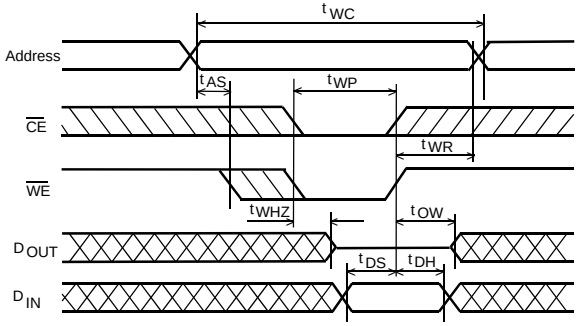
### REPLACES

HM628128., M5M51008.

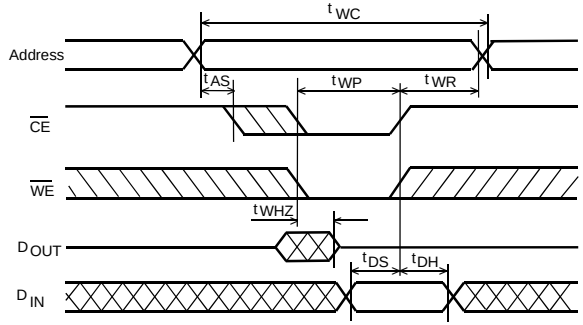
### READ CYCLE




### WRITE CYCLE 1




### WRITE CYCLE 2




### TIMING (nS-nano seconds)

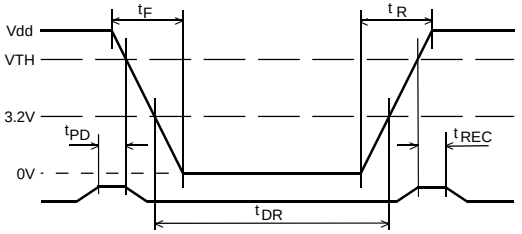
| | Read Cycle | 100nS | |
|---|---|---|---|
| Symbol | Parameter | Min | Max |
| $t_{RC}$ | Read cycle time | 100 | |
| $t_{ACC}$ | Access time | | 100 |
| $t_{ACS}$ | $\overline{CE}$ to output valid | | 100 |
| $t_{OE}$ | $\overline{OE}$ to output valid | | 50 |
| $t_{CLZ}$ | $\overline{CE}$ to output active | 5 | |
| $t_{OLZ}$ | $\overline{OE}$ to output active | 5 | |
| $t_{OH}$ | Output hold time | 10 | |
| $t_{CHZ}$ | $\overline{CE}$ to output disable | | 35 |
| $t_{OHZ}$ | $\overline{OE}$ to output disable | | 35 |

| | Write Cycle | 100nS | |
|---|---|---|---|
| Symbol | Parameter | Min | Max |
| $t_{WC}$ | Write cycle time | 100 | |
| $t_{WP}$ | Write pulse width | 75 | |
| $t_{AS}$ | Address setup time | 0 | |
| $t_{WR}$ | Write recovery time | 0 | |
| $t_{WHZ}$ | $\overline{WR}$ to output disable | | 35 |
| $t_{OW}$ | Output active from $\overline{WR}$ | 5 | |
| $t_{DS}$ | Data setup time | 40 | |
| $t_{DH}$ | Data HOLD TIME | 0 | |

Notes

1. $\overline{WE}$ must be high during address transitions.
2. A Write occurs during the overlap of a low $\overline{CE}_1$, a high $CE_2$ and a low $\overline{WE}$.
3. $\overline{WE}$ is high for a read cycle.

### DATA RETENTION OPERATING CONDITIONS




| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Vdd | Operating supply voltage | 4.75 | 5.0 | 5.50 | Volts |
| VTH | Data retention voltage | | 4.5 | | Volts |
| $t_F$ | Vdd slew to 0V | 15 | | | µS |
| $t_R$ | Vdd slew 0V to 5.0V | 15 | | | µS |
| $t_{REC}$ | CE to O/P valid from power up | | | 15 | µS |
| $t_{DR}$ | Data retention time | | 10 | | Years |
| $t_{PD}$ | CE at Vin(1) before power down | 0 | | | µS |