

## IRS2184/IRS21844(S)PbF HALF-BRIDGE DRIVER

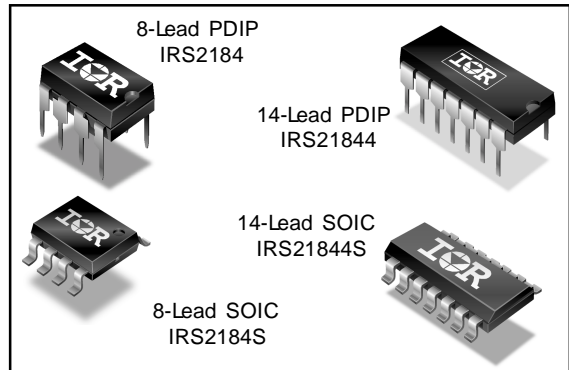
### Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V and 5 V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset.
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4 A/1.8 A

### Description

The IRS2184/IRS21844 are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V.

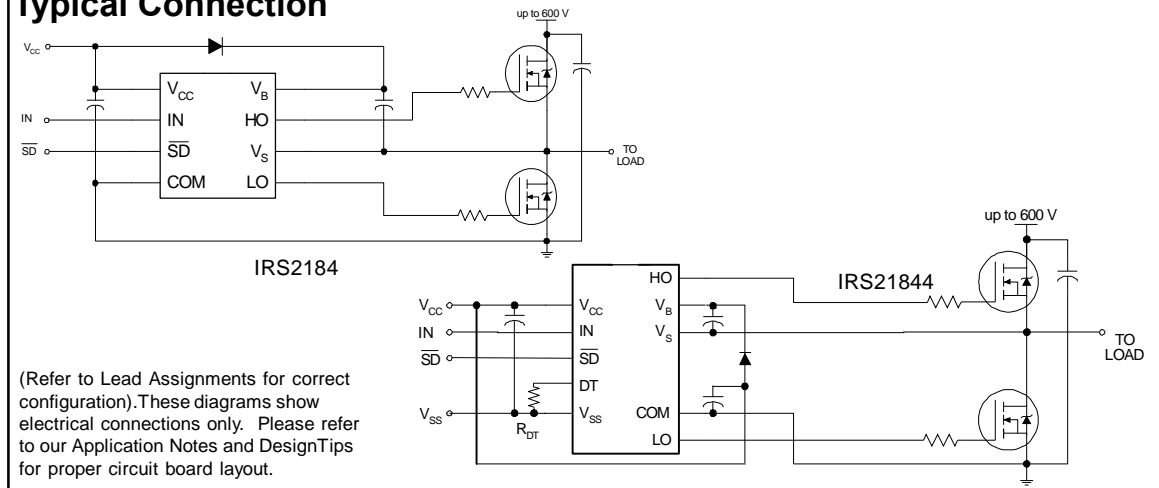
### Packages



### Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Deadtime (ns)	Ground Pins	Ton/Toff (ns)
2181	HIN/LIN	no	none	COM	180/220
21814				Vss/COM	
2183	HIN/LIN	yes	Internal 400 Program 400-5000	COM	180/220
21834				Vss/COM	
2184	IN/SD	yes	Internal 400 Program 400-5000	COM	680/270
21844				Vss/COM	

### Typical Connection



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High side floating absolute voltage	-0.3	620 (Note 1)	V	
V <sub>S</sub>	High side floating supply offset voltage	V <sub>B</sub> - 20	V <sub>B</sub> + 0.3		
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3		
V <sub>CC</sub>	Low side and logic fixed supply voltage	-0.3	20 (Note 1)		
V <sub>LO</sub>	Low side output voltage	-0.3	V <sub>CC</sub> + 0.3		
DT	Programmable deadtime pin voltage (IRS21844 only)	V <sub>SS</sub> - 0.3	V <sub>CC</sub> + 0.3		
V <sub>IN</sub>	Logic input voltage (IN & $\overline{SD}$ )	V <sub>SS</sub> - 0.3	V <sub>CC</sub> + 0.3		
V <sub>SS</sub>	Logic ground (IRS21844 only)	V <sub>CC</sub> - 20	V <sub>CC</sub> + 0.3		
dV <sub>S</sub> /dt	Allowable offset supply voltage transient	—	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25 °C	(8-lead PDIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
		(14-lead PDIP)	—	1.6	
		(14-lead SOIC)	—	1.0	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	(8-lead PDIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
		(14-lead PDIP)	—	75	
		(14-lead SOIC)	—	120	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-50	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

Note 1: All supplies are fully tested at 25 V and an internal 20 V clamp exists for each supply.

## Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> and V<sub>SS</sub> offset rating are tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High side floating supply absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High side floating supply offset voltage	Note 2	600	
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low side and logic fixed supply voltage	10	20	
V <sub>LO</sub>	Low side output voltage	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic input voltage (IN & $\overline{SD}$ )	V <sub>SS</sub>	V <sub>CC</sub>	
DT	Programmable deadtime pin voltage (IRS21844 only)	V <sub>SS</sub>	V <sub>CC</sub>	
V <sub>SS</sub>	Logic ground (IRS21844 only)	-5	5	
T <sub>A</sub>	Ambient temperature	-40	125	°C

Note 2: Logic operational for V<sub>S</sub> of -5 V to +600 V. Logic state held for V<sub>S</sub> of -5 V to -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$ ,  $V_{SS} = \text{COM}$ ,  $C_L = 1000\text{ pF}$ ,  $T_A = 25^\circ\text{ C}$ ,  $DT = V_{SS}$  unless otherwise specified.

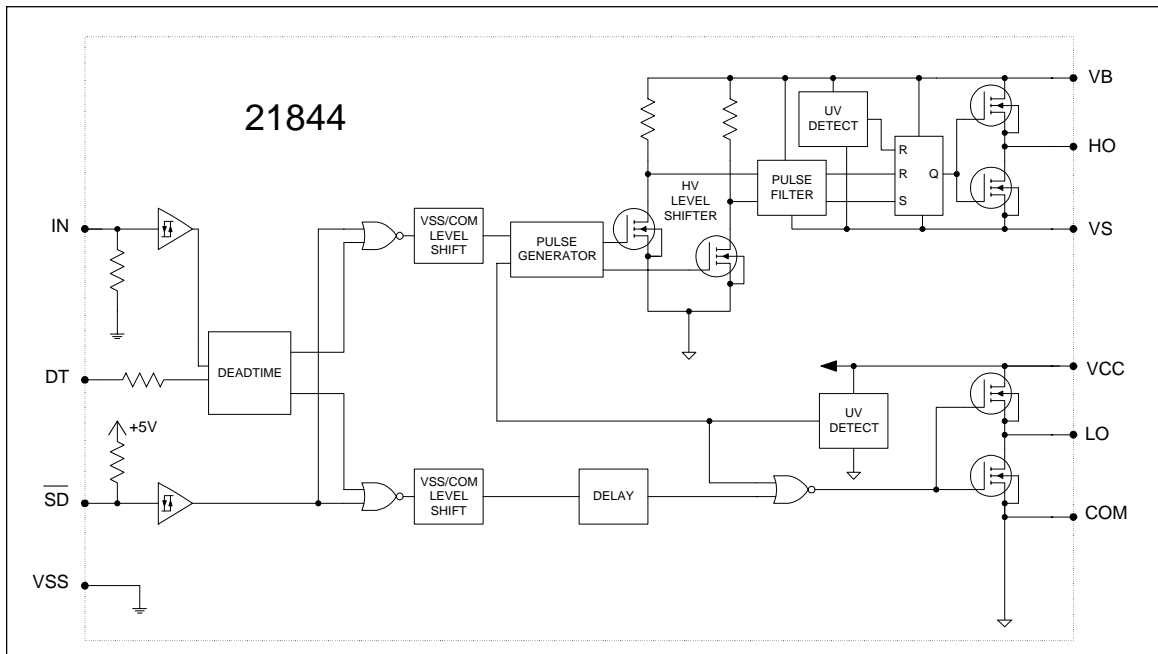
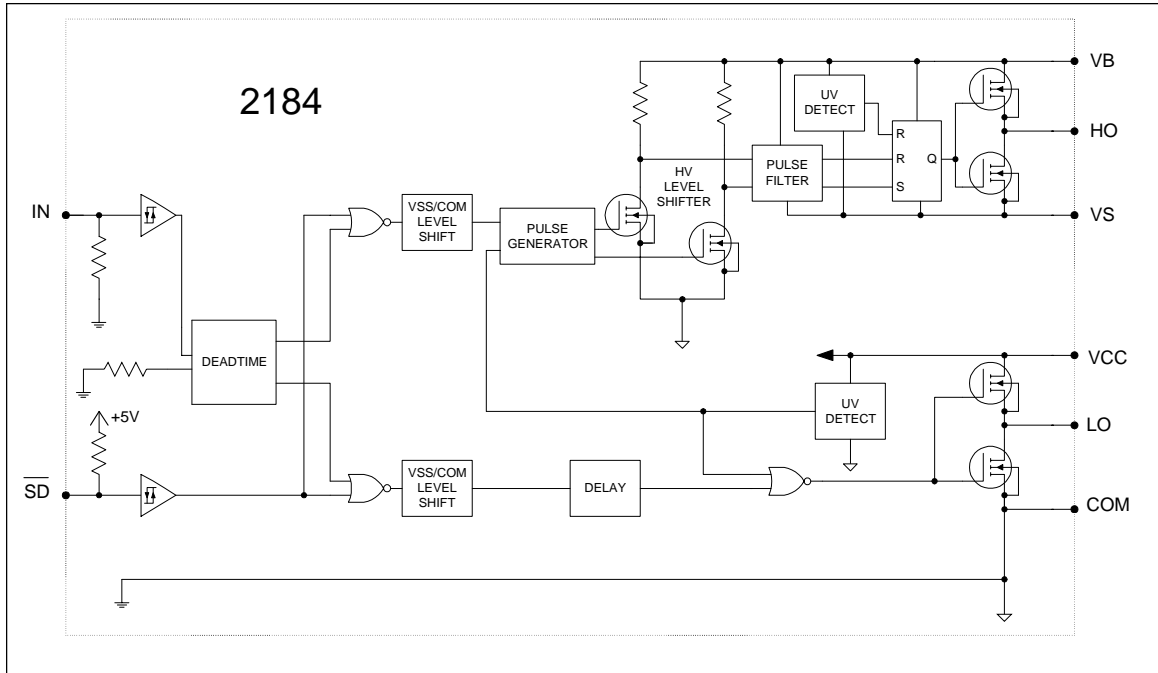
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	680	900	ns	$V_S = 0\text{ V}$
$t_{off}$	Turn-off propagation delay	—	270	400		$V_S = 0\text{ V}$ or $600\text{ V}$
$t_{sd}$	Shut-down propagation delay	—	180	270		
MTon	Delay matching, HS & LS turn-on	—	0	90		
MToff	Delay matching, HS & LS turn-off	—	0	40		
$t_r$	Turn-on rise time	—	40	60		$V_S = 0\text{ V}$
$t_f$	Turn-off fall time	—	20	35		
DT	Deadtime: LO turn-off to HO turn-on (DT <sub>LO-HO</sub> ) & HO turn-off to LO turn-on (DT <sub>HO-LO</sub> )	280	400	520	μs	$R_{DT} = 0\ \Omega$
		4	5	6		$R_{DT} = 200\text{ k}\Omega$
MDT	Deadtime matching = $DT_{LO} - HO - DT_{HO-LO}$	—	0	50	ns	$R_{DT} = 0\ \Omega$
		—	0	600		$R_{DT} = 200\text{ k}\Omega$

## Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$ ,  $V_{SS} = \text{COM}$ ,  $DT = V_{SS}$  and  $T_A = 25^\circ\text{ C}$  unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$ , and  $I_{IN}$  parameters are referenced to  $V_{SS}/\text{COM}$  and are applicable to the respective input leads: IN and SD. The  $V_O$ ,  $I_O$ , and  $R_{on}$  parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" input voltage for HO & logic "0" for LO	2.5	—	—	V	$V_{CC} = 10\text{ V}$ to $20\text{ V}$
$V_{IL}$	Logic "0" input voltage for HO & logic "1" for LO	—	—	0.8		
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold	2.5	—	—		
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold	—	—	0.8		
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	—	1.2		$I_O = 0\text{ A}$
$V_{OL}$	Low level output voltage, $V_O$	—	—	0.2		$I_O = 20\text{ mA}$
$I_{LK}$	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600\text{ V}$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	20	60	150	mA	$V_{IN} = 0\text{ V}$ or $5\text{ V}$
$I_{QCC}$	Quiescent $V_{CC}$ supply current	0.4	1.0	1.6		
$I_{IN+}$	Logic "1" input bias current	—	25	60	μA	$IN = 5\text{ V}$ , $\overline{SD} = 0\text{ V}$
$I_{IN-}$	Logic "0" input bias current	—	—	1.0		$IN = 0\text{ V}$ , $\overline{SD} = 5\text{ V}$
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold	8.0	8.9	9.8	V	
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold	7.4	8.2	9.0		
$V_{CCUVH}$ $V_{BSUVH}$	Hysteresis	0.3	0.7	—		
$I_{O+}$	Output high short circuit pulsed current	1.4	1.9	—	A	$V_O = 0\text{ V}$ , $PW \leq 10\ \mu\text{s}$
$I_{O-}$	Output low short circuit pulsed current	1.8	2.3	—		$V_O = 15\text{ V}$ , $PW \leq 10\ \mu\text{s}$

## Functional Block Diagrams



## Lead Definitions

Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO (referenced to COM for IRS2184 and VSS for IRS21844)
$\overline{SD}$	Logic input for shutdown (referenced to COM for IRS2184 and VSS for IRS21844)
DT	Programmable deadtime lead, referenced to VSS. (IRS21844 only)
VSS	Logic ground (IRS21844 only)
$V_B$	High side floating supply
HO	High side gate drive output
$V_S$	High side floating supply return
$V_{CC}$	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

## Lead Assignments

<p>8-Lead PDIP</p>	<p>8-Lead SOIC</p>
<b>IRS2184PbF</b>	<b>IRS2184SPbF</b>
<p>14-Lead PDIP</p>	<p>14-Lead SOIC</p>
<b>IRS21844PbF</b>	<b>IRS21844SPbF</b>

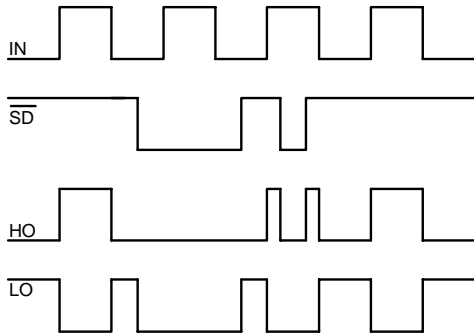


Figure 1. Input/Output Timing Diagram

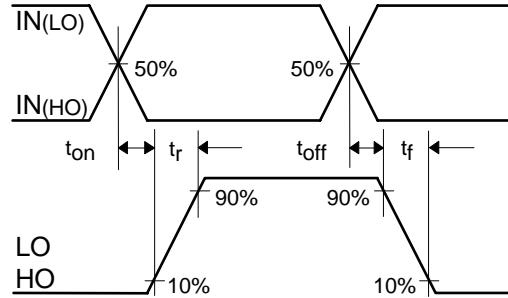


Figure 2. Switching Time Waveform Definitions

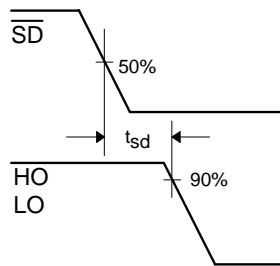


Figure 3. Shutdown Waveform Definitions

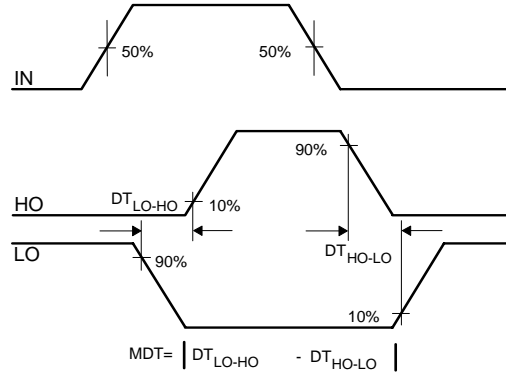


Figure 4. Deadtime Waveform Definitions

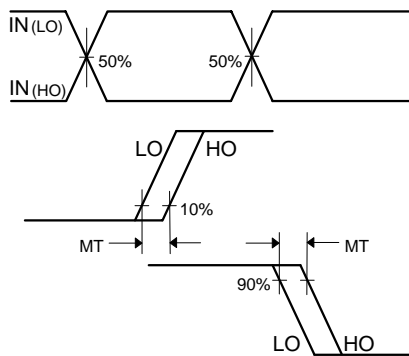
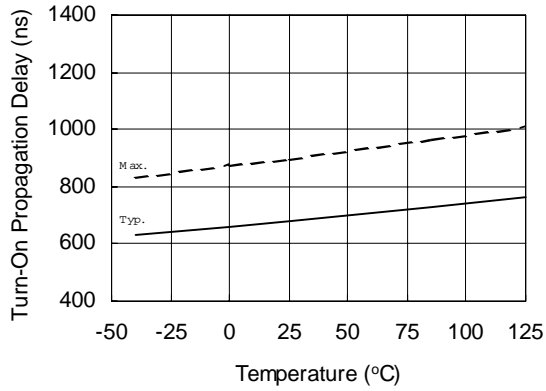
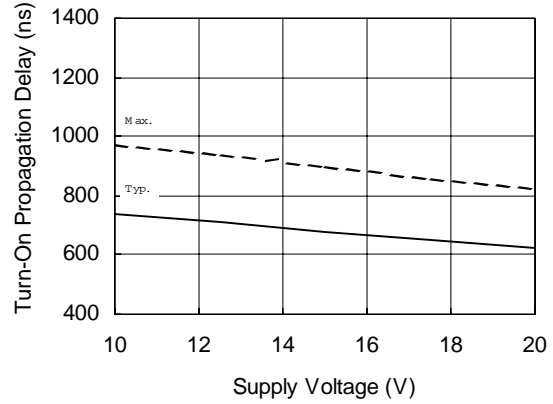


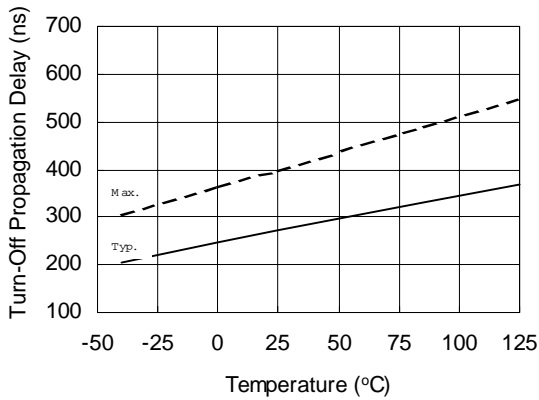
Figure 5. Delay Matching Waveform Definitions



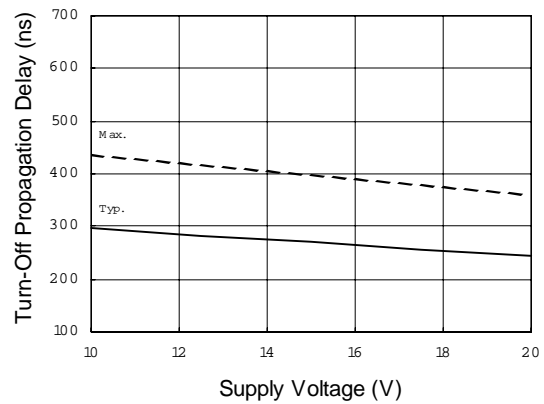
**Figure 4A. Turn-On Propagation Delay vs. Temperature**



**Figure 4B. Turn-On Propagation Delay vs. Supply Voltage**



**Figure 5A. Turn-Off Propagation Delay vs. Temperature**



**Figure 5B. Turn-Off Propagation Delay vs. Supply Voltage**

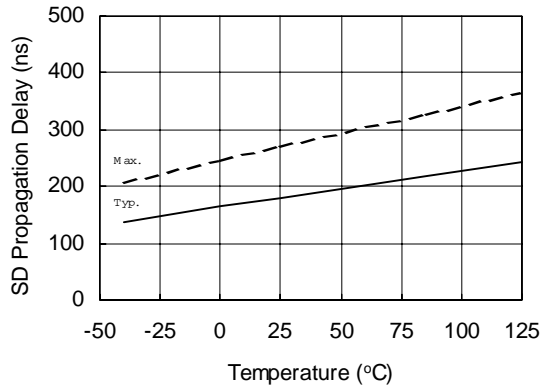


Figure 6A. SD Propagation Delay vs. Temperature

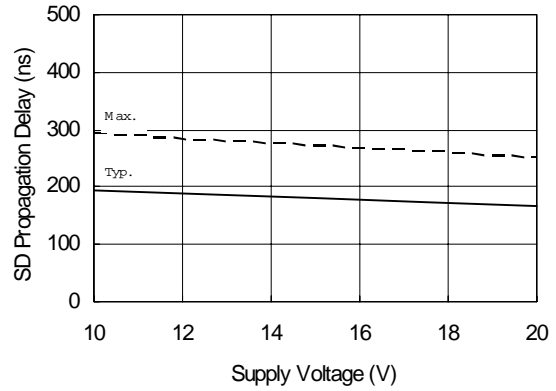


Figure 6B. SD Propagation Delay vs. Supply Voltage

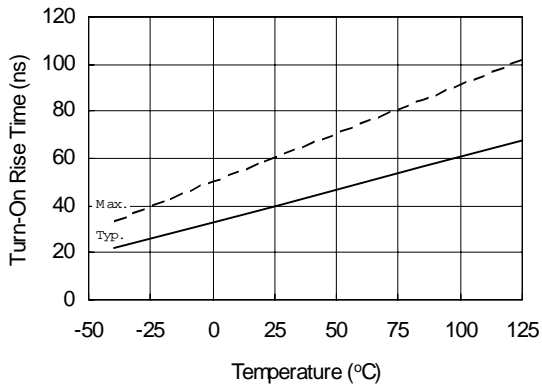


Figure 7A. Turn-On Rise Time vs. Temperature

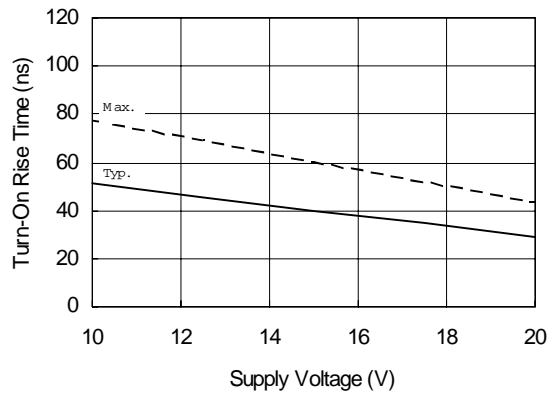
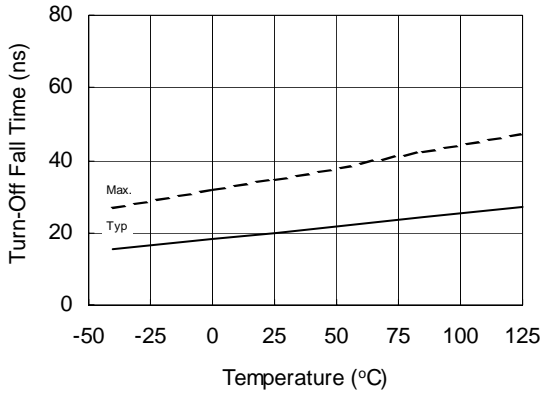
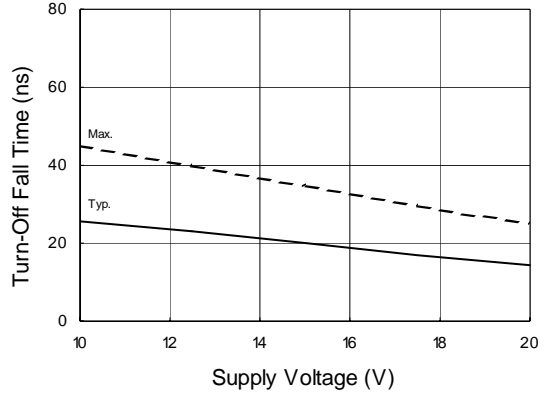


Figure 7B. Turn-On Rise Time vs. Supply Voltage

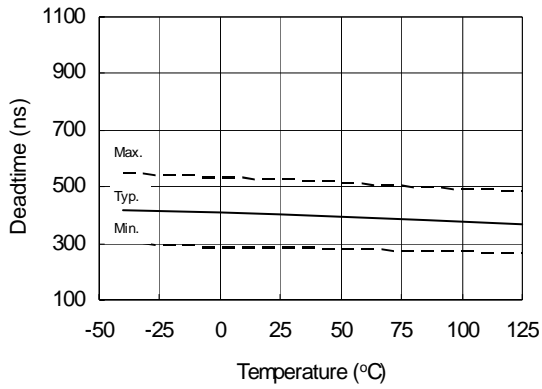




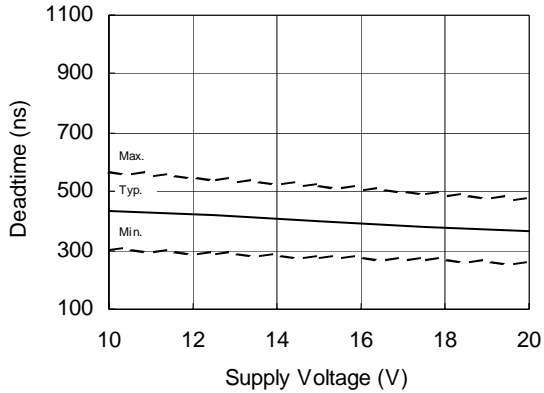
**Figure 8A. Turn-Off Fall Time vs. Temperature**



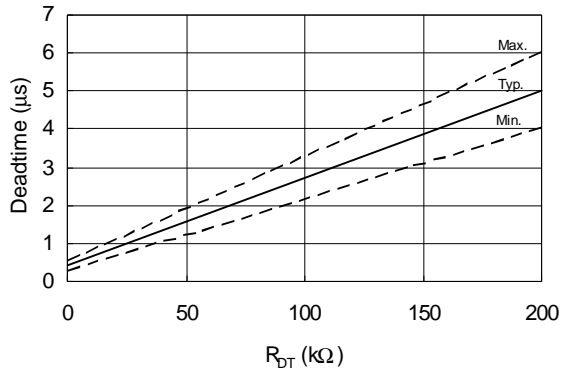
**Figure 8B. Turn-Off Fall Time vs. Supply Voltage**



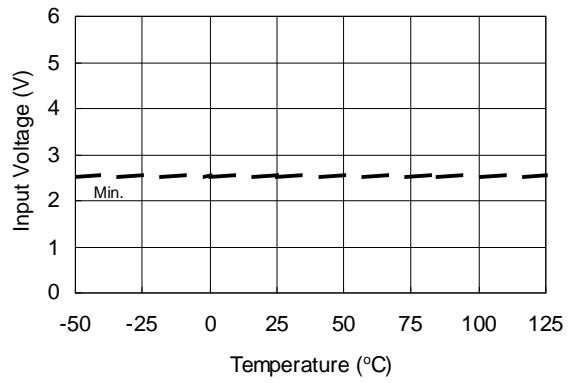
**Figure 9A. Deadtime vs. Temperature**



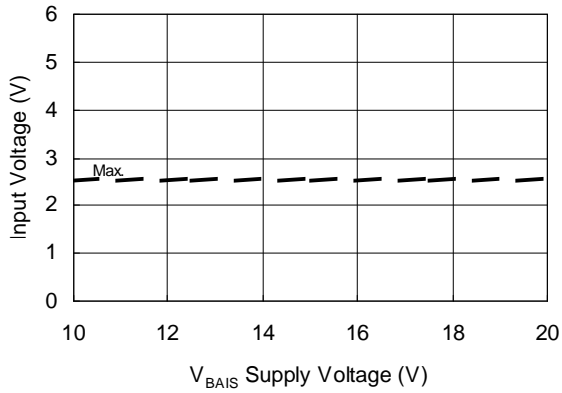
**Figure 9B. Deadtime vs. Supply Voltage**



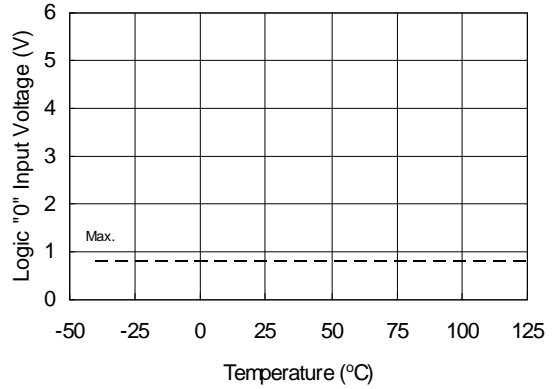
**Figure 9C. Deadtime vs.  $R_{DT}$**



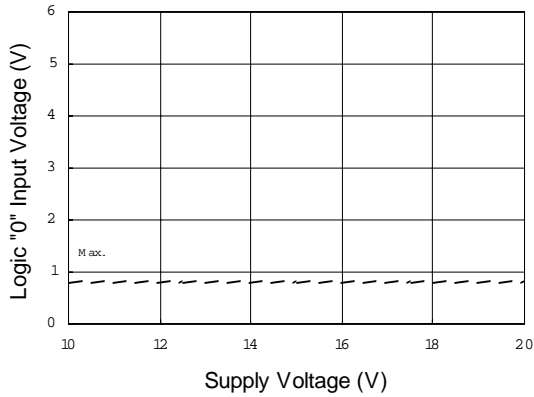
**Figure 10A. Logic "1" Input Voltage vs. Temperature**



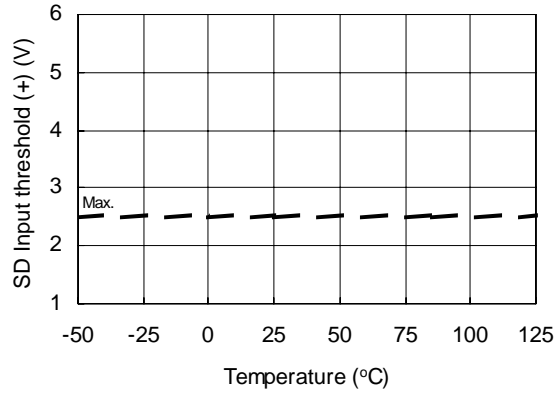
**Figure 10B. Logic "1" Input Voltage vs. Supply Voltage**



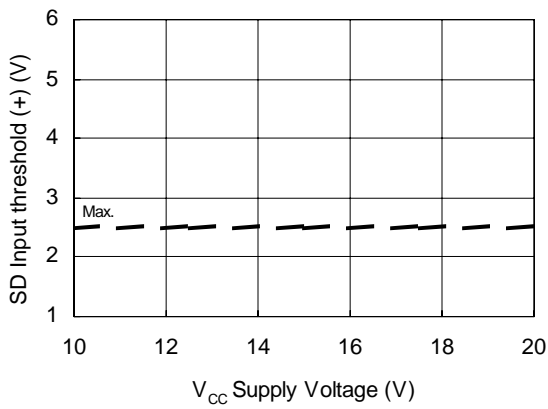
**Figure 11A. Logic "0" Input Voltage vs. Temperature**



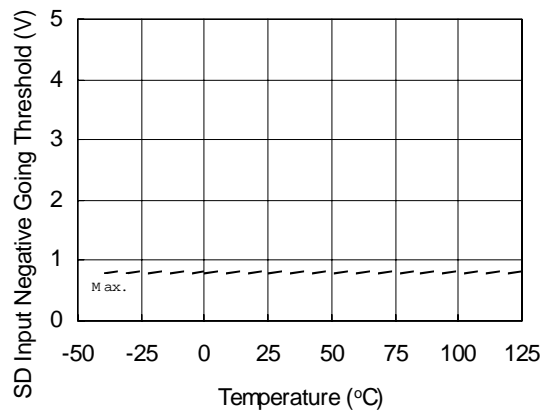
**Figure 11B. Logic "0" Input Voltage vs. Supply Voltage**



**Figure 12A. SD input positive going threshold (+) vs. Temperature**



**Figure 12B. SD input positive going threshold (+) vs. Supply Voltage**



**Figure 13A. SD Input Negative Going Threshold vs. Temperature**

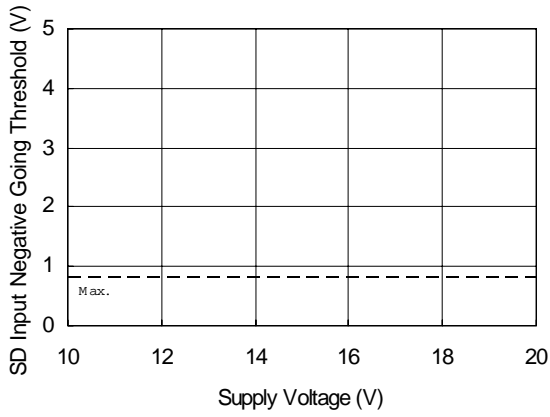


Figure 13B. SD Input Negative Going Threshold vs. Supply Voltage

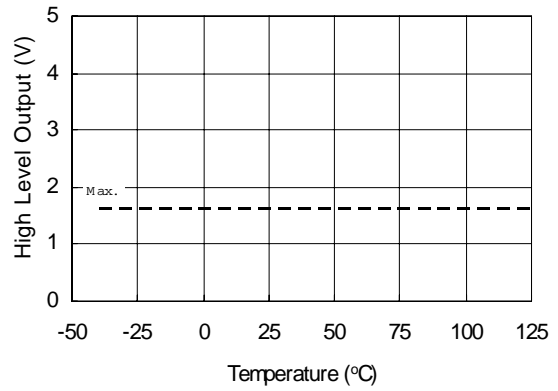


Figure 14A. High Level Output vs. Temperature

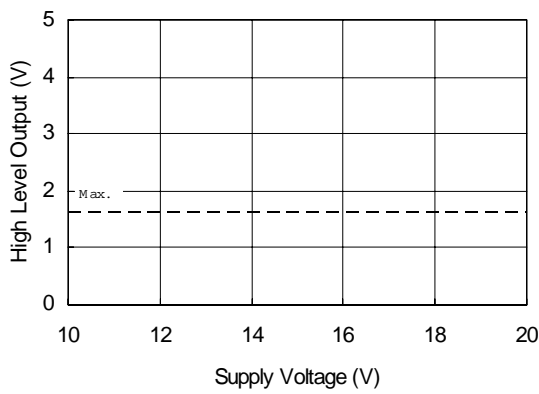


Figure 14B. High Level Output vs. Supply Voltage

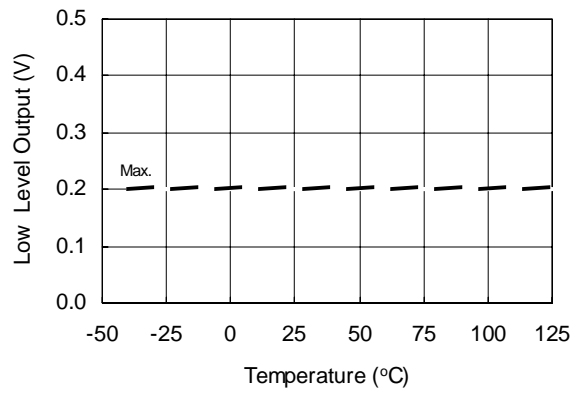


Figure 15A. Low Level Output vs. Temperature

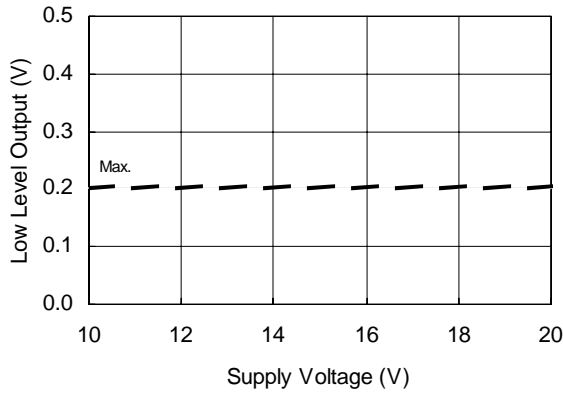


Figure 15B. Low Level Output vs. Supply Voltage

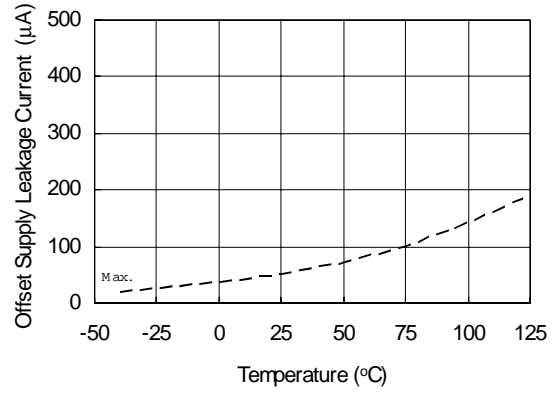


Figure 16A. Offset Supply Leakage Current vs. Temperature

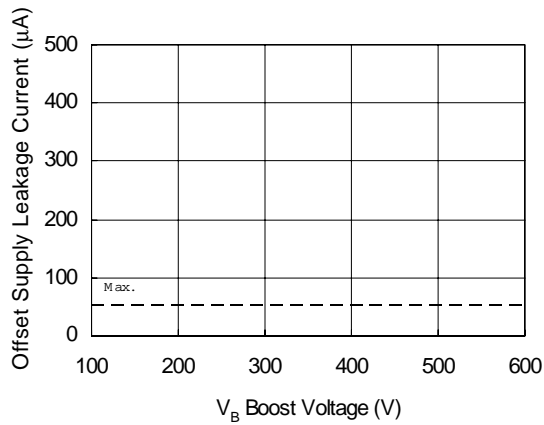


Figure 16B. Offset Supply Leakage Current vs. V<sub>B</sub> Boost Voltage

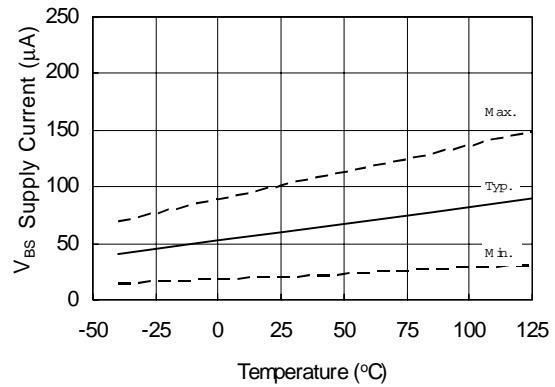
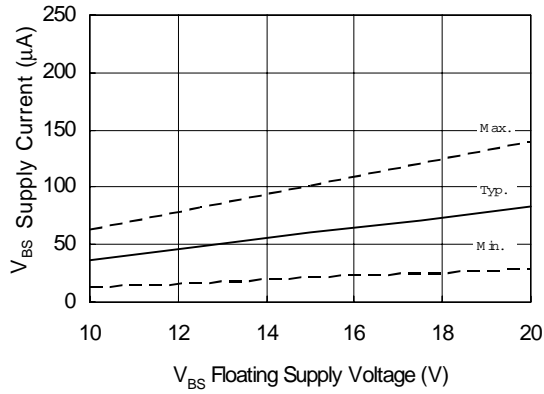
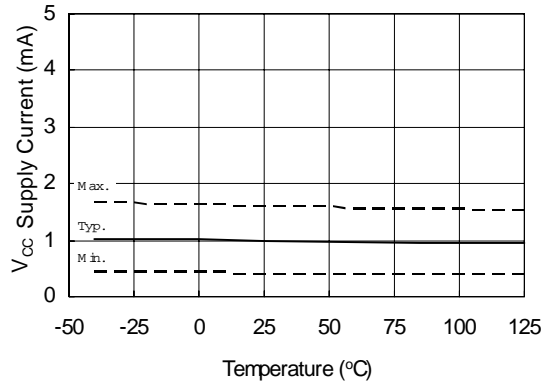


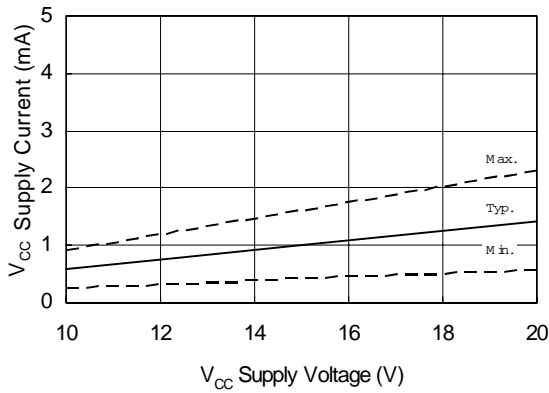
Figure 17A. V<sub>BS</sub> Supply Current vs. Temperature



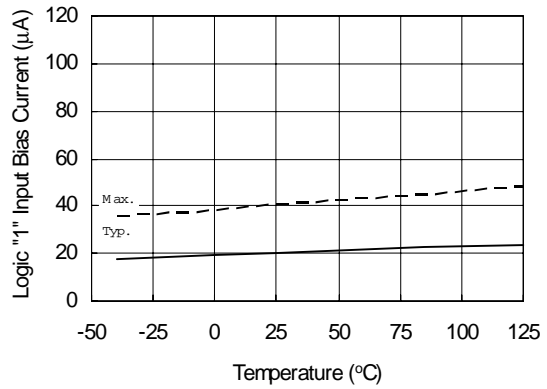
**Figure 17B.  $V_{BS}$  Supply Current vs.  $V_{BS}$  Floating Supply Voltage**



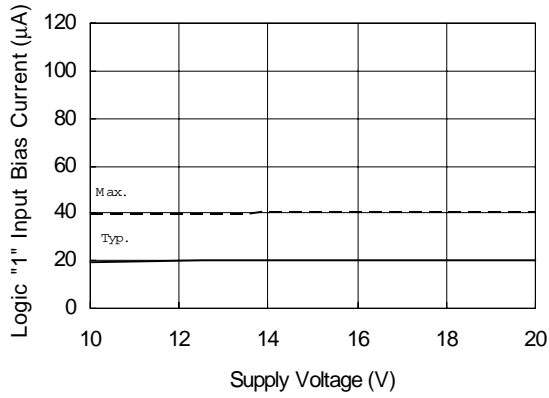
**Figure 18A.  $V_{CC}$  Supply Current vs. Temperature**



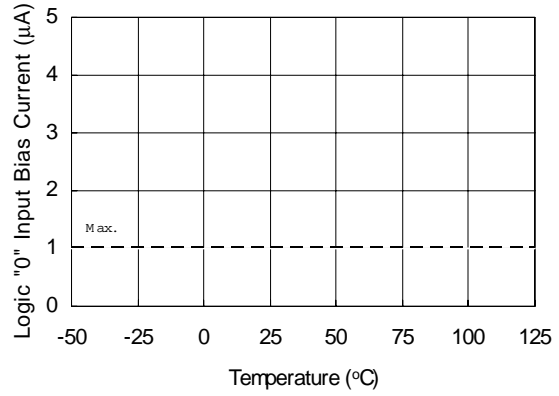
**Figure 18B.  $V_{CC}$  Supply Current vs.  $V_{CC}$  Supply Voltage**



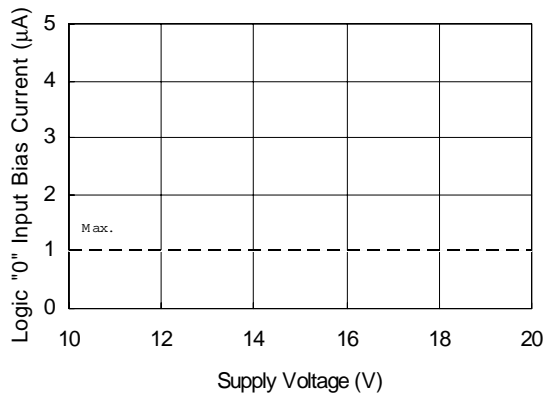
**Figure 19A. Logic "1" Input Bias Current vs. Temperature**



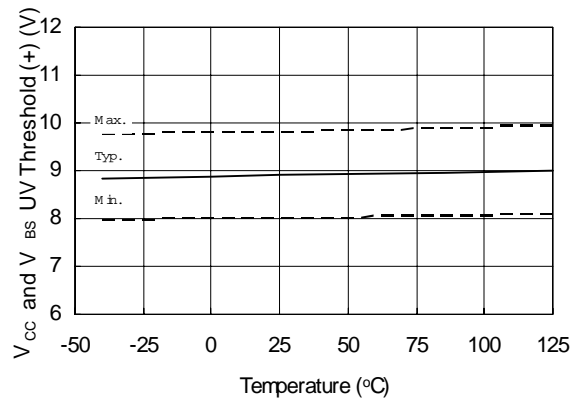
**Figure 19B. Logic "1" Input Bias Current vs. Supply Voltage**



**Figure 20A. Logic "0" Input Bias Current vs. Temperature**



**Figure 20B. Logic "0" Input Bias Current vs. Supply Voltage**



**Figure 21.  $V_{CC}$  and  $V_{BS}$  Undervoltage Threshold (+) vs. Temperature**

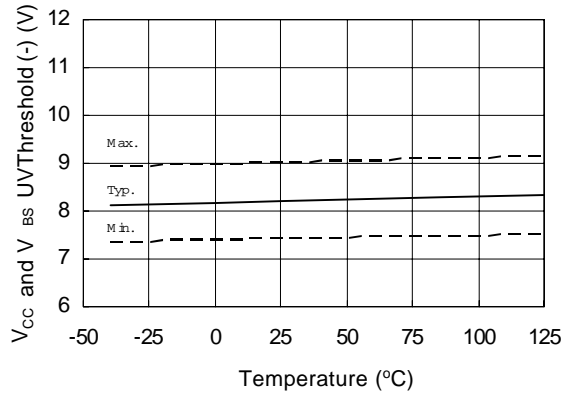


Figure 22.  $V_{CC}$  and  $V_{BS}$  Undervoltage Threshold (-) vs. Temperature

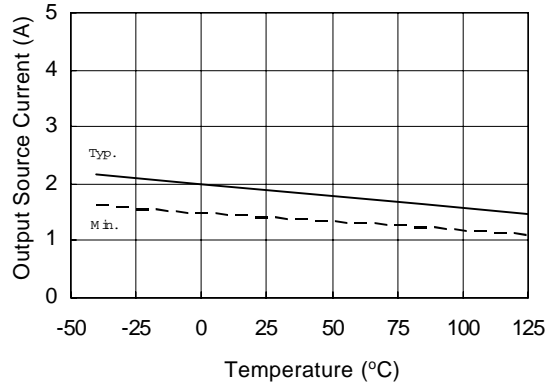


Figure 23A. Output Source Current vs. Temperature

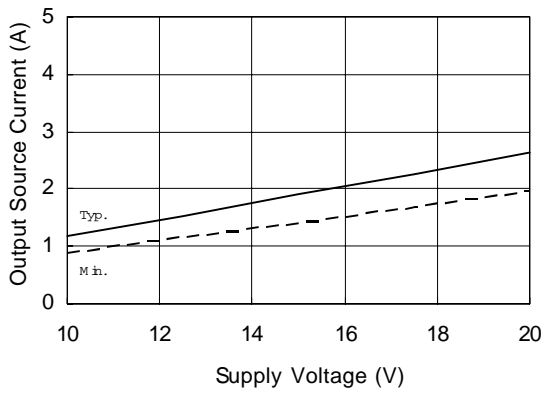


Figure 23B. Output Source Current vs. Supply Voltage

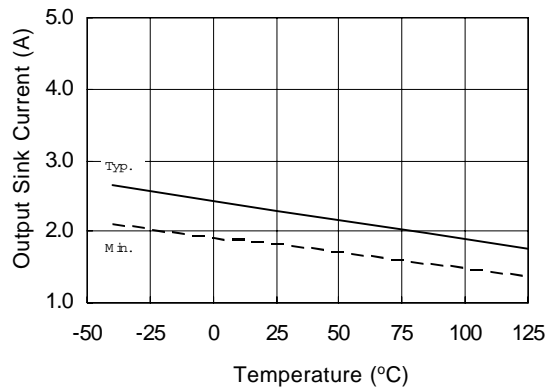
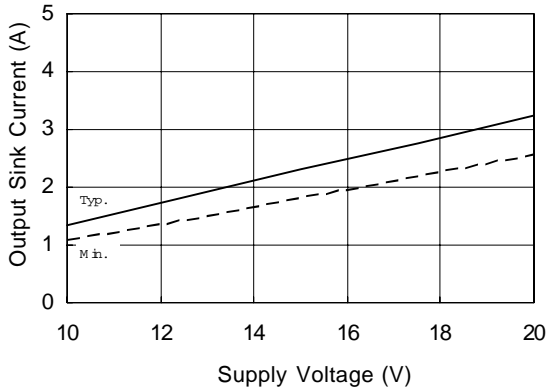


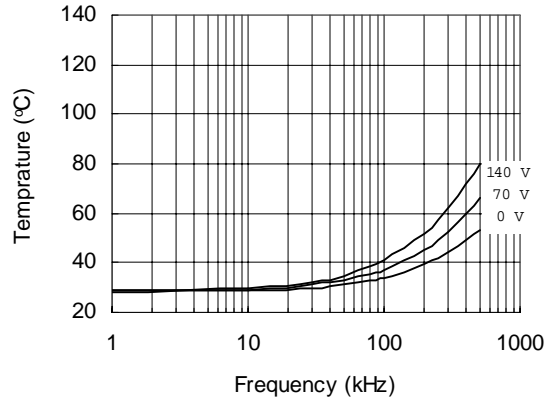
Figure 24A. Output Sink Current vs. Temperature



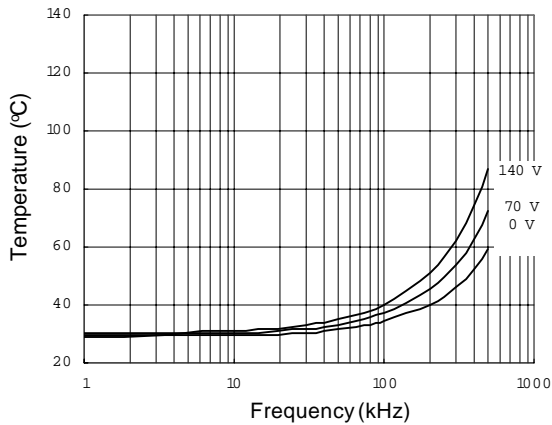
# IRS2184/IRS21844(S)PbF



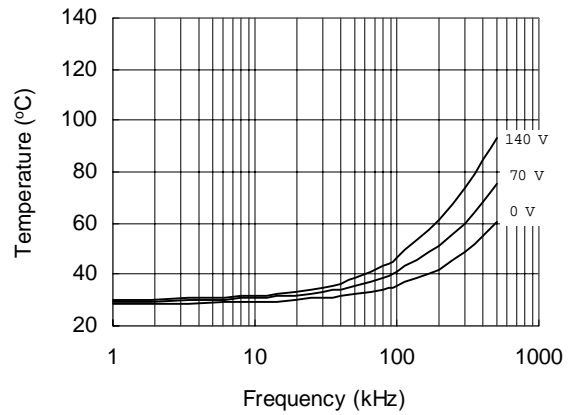
**Figure 24B. Output Sink Current vs. Supply Voltage**



**Figure 21. IRS2181 vs. Frequency (IRFBC20),  $R_{gate}=33 \Omega$ ,  $V_{CC}=15 V$**

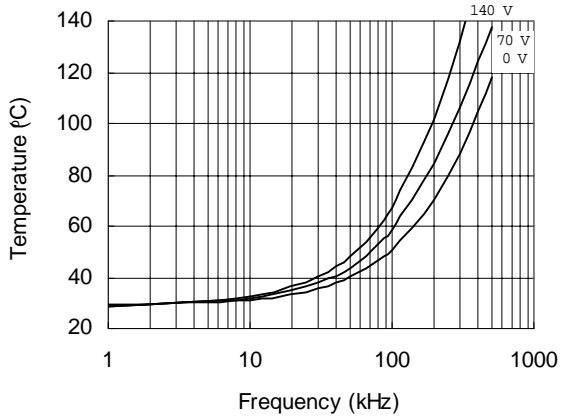


**Figure 22. IRS2181 vs. Frequency (IRFBC30),  $R_{gate}=22 \Omega$ ,  $V_{CC}=15 V$**

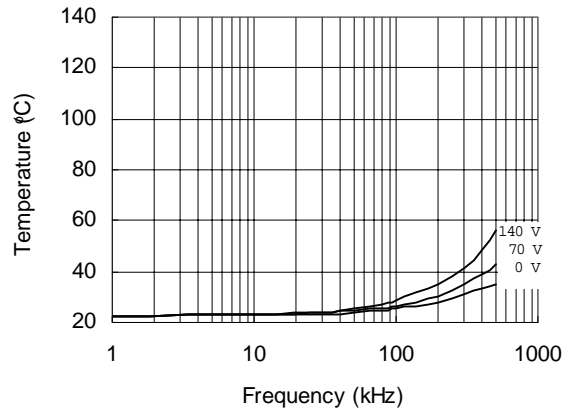


**Figure 23. IRS2181 vs. Frequency (IRFBC40),  $R_{gate}=15 \Omega$ ,  $V_{CC}=15 V$**

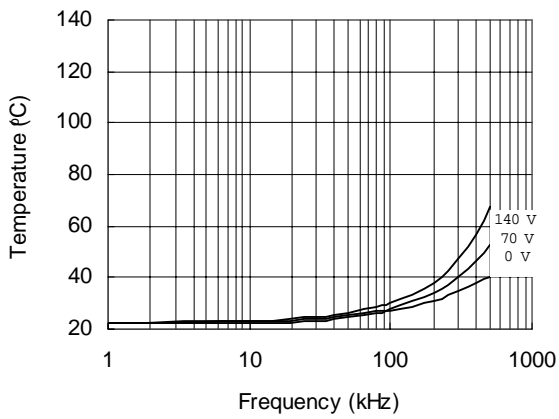
# IRS2184/IRS21844(S)PbF



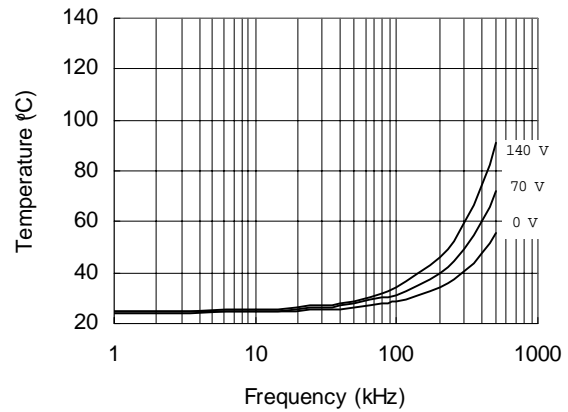
**Figure 24. IRS2181 vs. Frequency (IRFPE50),  
 $R_{gate}=10 \Omega$ ,  $V_{CC}=15 V$**



**Figure 25. IRS21814 vs. Frequency (IRFBC20),  
 $R_{gate}=33 \Omega$ ,  $V_{CC}=15 V$**



**Figure 26. IRS21814 vs. Frequency (IRFBC30),  
 $R_{gate}=22 \Omega$ ,  $V_{CC}=15 V$**



**Figure 27. IRS21814 vs. Frequency (IRFBC40),  
 $R_{gate}=15 \Omega$ ,  $V_{CC}=15 V$**

# IRS2184/IRS21844(S)PbF

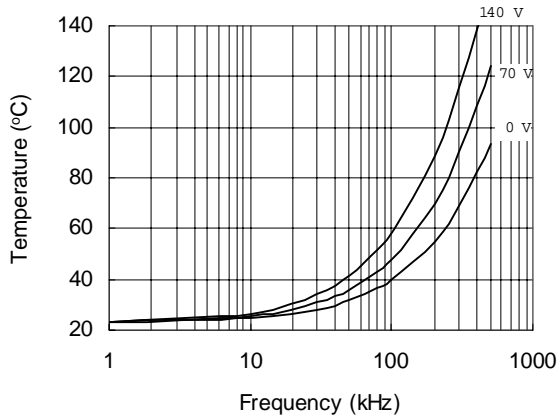


Figure 28. IRS21814 vs. Frequency (IRFPE50),  
 $R_{gate}=10 \Omega$ ,  $V_{CC}=15 V$

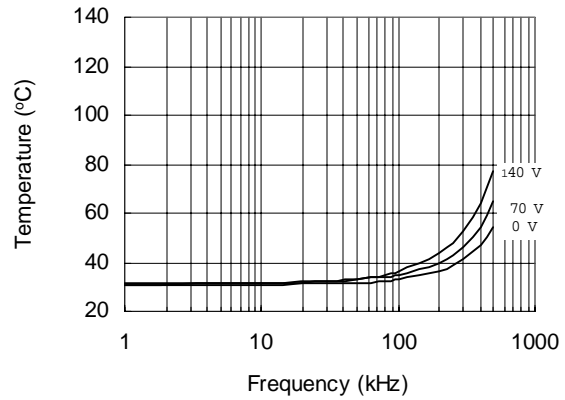


Figure 29. IRS2181S vs. Frequency (IRFBC20),  
 $R_{gate}=33 \Omega$ ,  $V_{CC}=15 V$

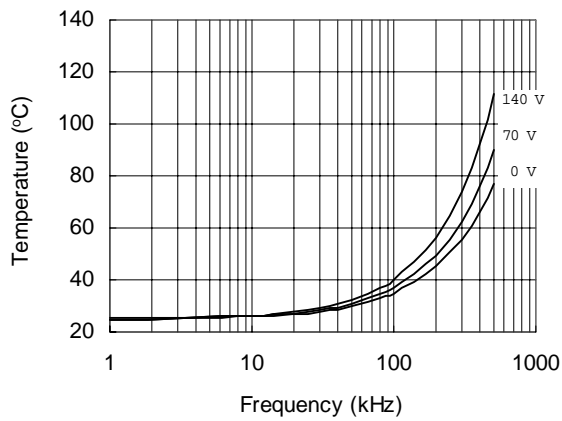


Figure 30. IRS2181S vs. Frequency (IRFBC30),  
 $R_{gate}=22 \Omega$ ,  $V_{CC}=15 V$

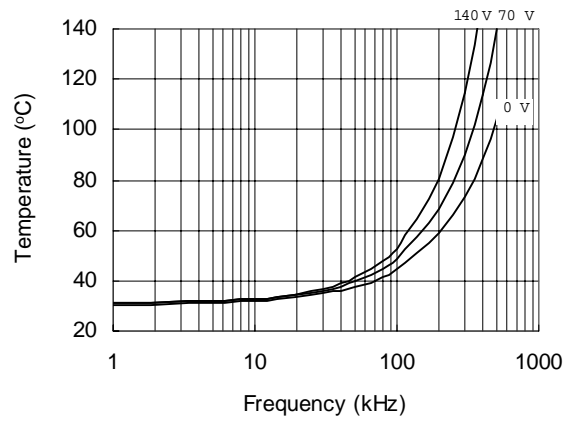
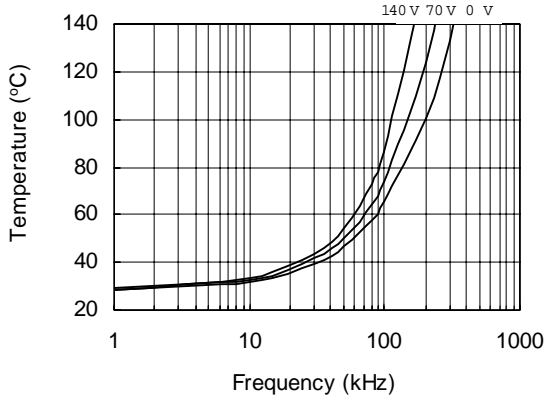
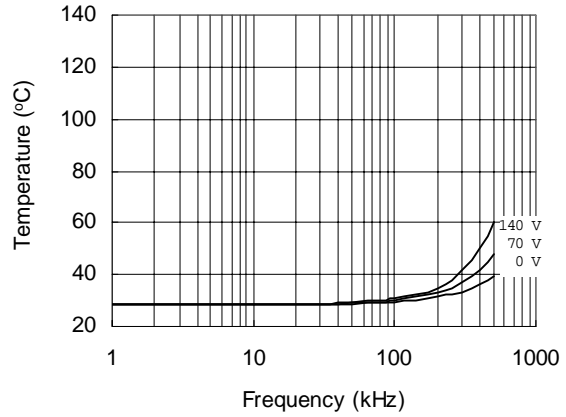


Figure 31. IRS2181S vs. Frequency (IRFBC40),  
 $R_{gate}=15 \Omega$ ,  $V_{CC}=15 V$

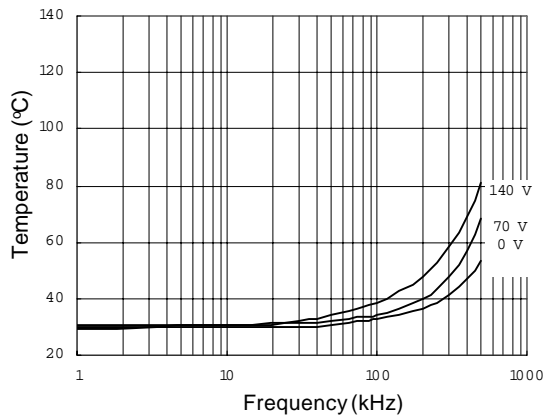
# IRS2184/IRS21844(S)PbF



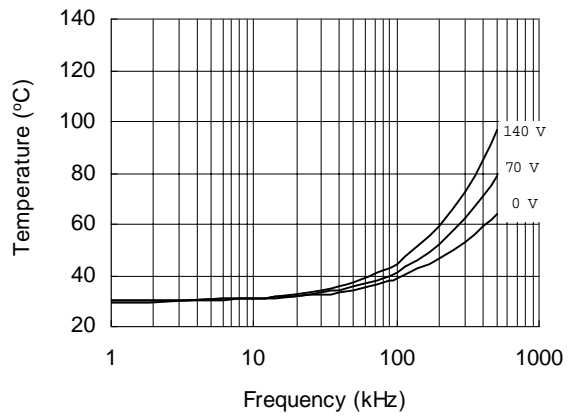
**Figure 32. IRS2181S vs. Frequency (IRFPE50),  
 $R_{gate}=10 \Omega$ ,  $V_{CC}=15 V$**



**Figure 33. IRS21814S vs. Frequency (IRFBC20),  
 $R_{gate}=33 \Omega$ ,  $V_{CC}=15 V$**

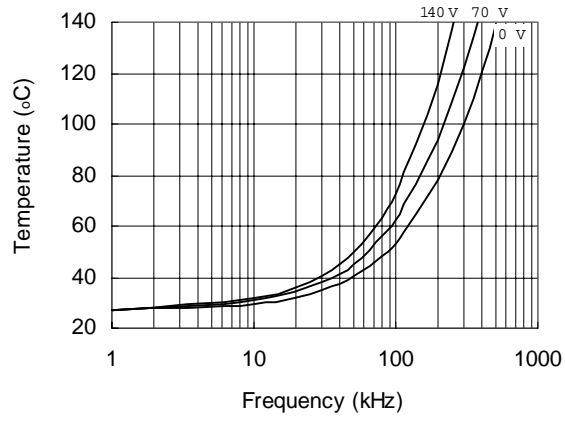


**Figure 34. IRS21814S vs. Frequency (IRFBC30),  
 $R_{gate}=22 \Omega$ ,  $V_{CC}=15 V$**



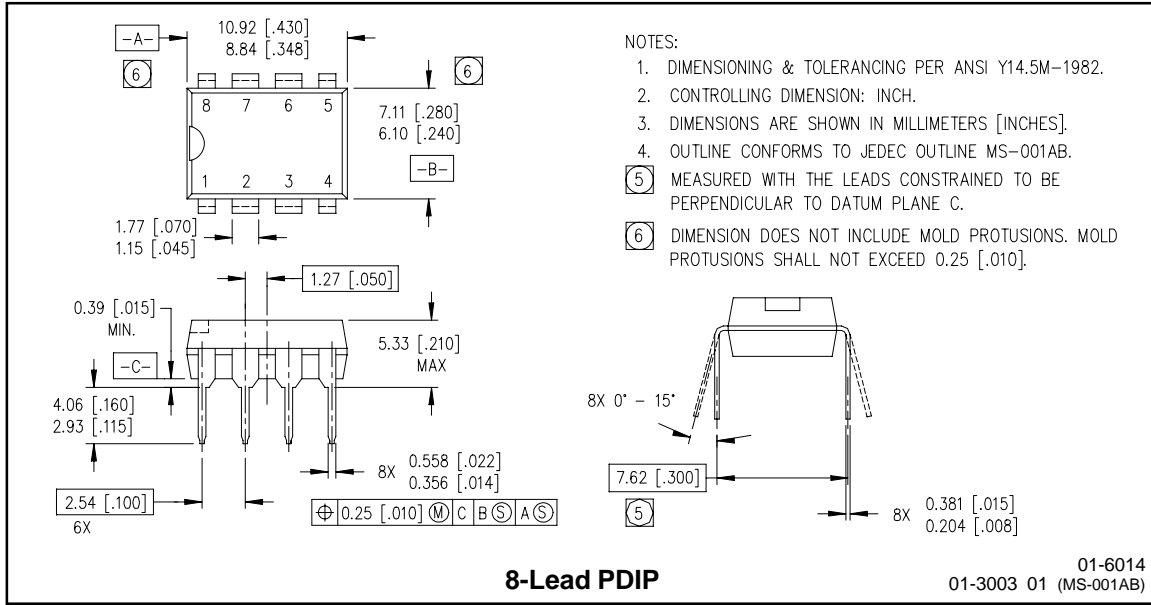
**Figure 35. IRS21814S vs. Frequency (IRFBC40),  
 $R_{gate}=15 \Omega$ ,  $V_{CC}=15 V$**

# IRS2184/IRS21844(S)PbF

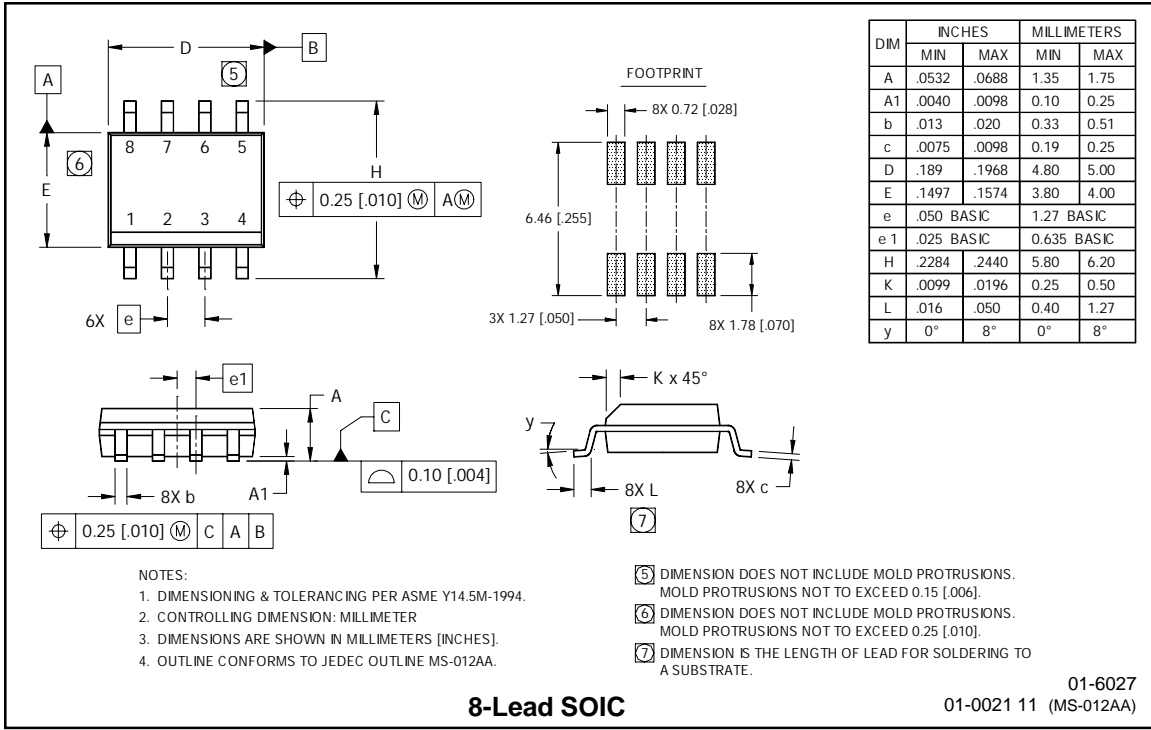


**Figure 36. IRS21814S vs. Frequency (IRFPE50),  
 $R_{gate}=10 \Omega$ ,  $V_{CC}=15 V$**

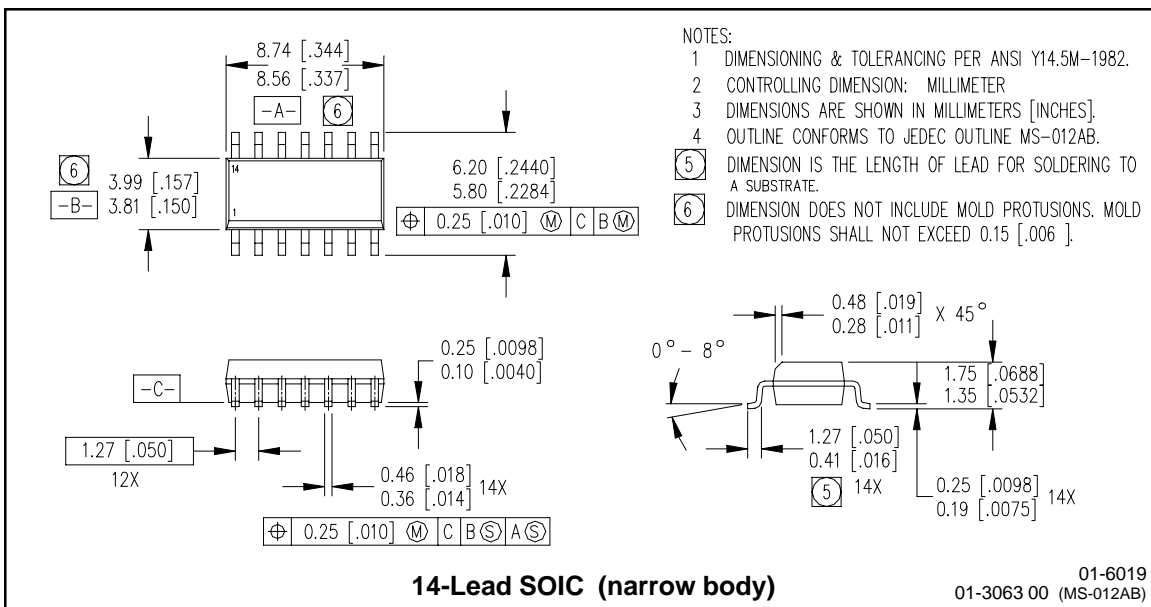
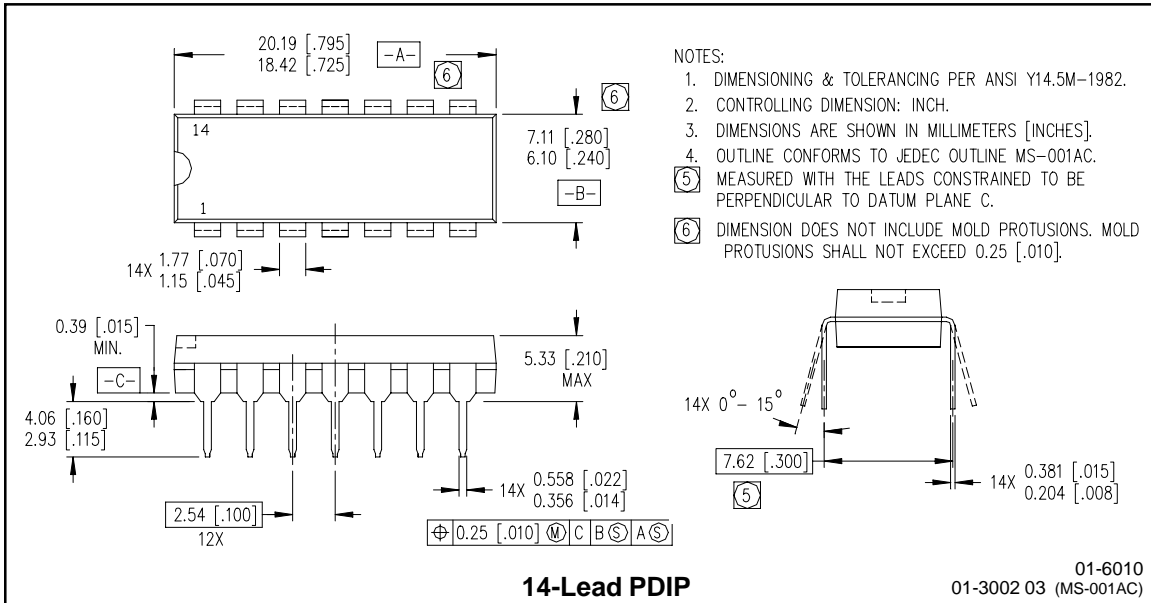
## Cast Outlines



- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
  - ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
  - ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

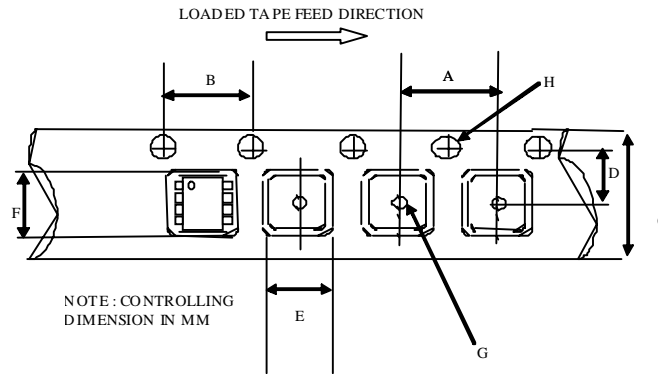


# IRS2184/IRS21844(S)PbF



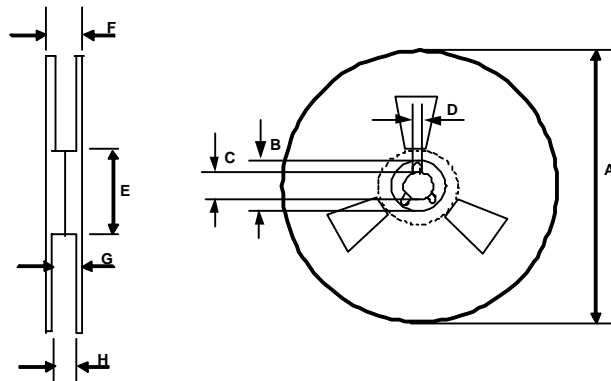
# IRS2184/IRS21844(S)PbF

## Tape & Reel 8-lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

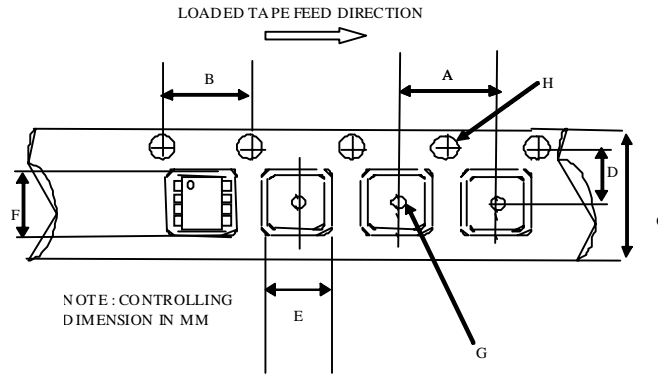


REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

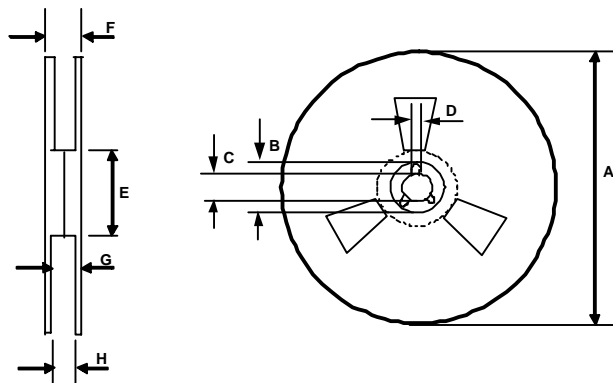


## Tape & Reel 14-lead SOIC



CARRIER TAPE DIMENSION FOR 14SOICN

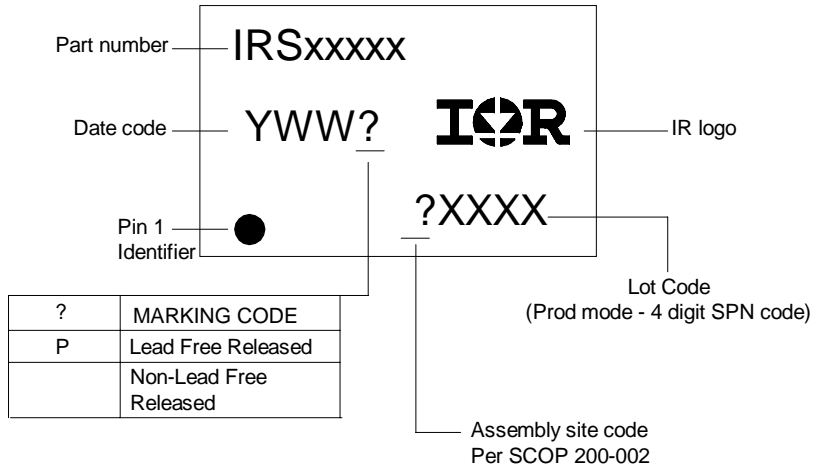
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 14SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

- |                                       |   |
|---------------------------------------|---|
| 8-Lead PDIP IRS2184PbF                | 14-Lead PDIP IR2S1844PbF                |
| 8-Lead SOIC IRS2184SPbF               | 14-Lead SOIC IRS21844SPbF               |
| 8-Lead SOIC Tape & Reel IRS2184STRPbF | 14-Lead SOIC Tape & Reel IRS21844STRPbF |