FAIRCHILD
SEMICONDUCTOR TM

March 1996

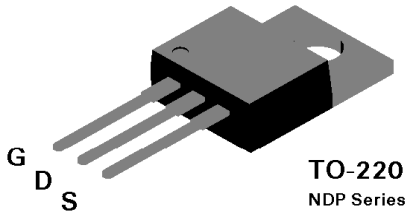
NDP7050 / NDB7050
N-Channel Enhancement Mode Field Effect Transistor

General Description

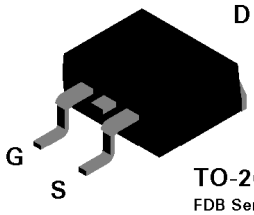
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

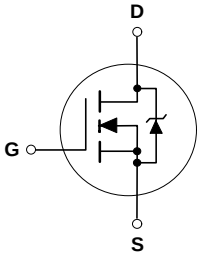
- 75A, 50V. $R_{DS(ON)}$ = 0.013Ω @ V_{GS}=10V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
FDB Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP7050	NDB7050	Units
V_{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage (R_{GS} ≤ 1 MΩ)	50		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive (t_p < 50 µs)	± 40		
I_D	Drain Current - Continuous	75		A
	- Pulsed	225		
P_D	Maximum Power Dissipation @ T_C = 25°C	150		W
	Derate above 25°C	1		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 75 A			550	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				75	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0 V			250	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	2.8	4	V
		T_J = 125°C	1.4	2.1	3.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 40 A		0.01	0.013	Ω
		T_J = 125°C		0.015	0.023	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	75			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 37.5 A	15	39		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		2960	3600	pF
C_{oss}	Output Capacitance			1130	1600	pF
C_{rss}	Reverse Transfer Capacitance			380	800	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 75 A, V_{GS} = 10 V, R_{GEN} = 5 Ω		17	30	nS
t_r	Turn - On Rise Time			128	400	nS
$t_{D(off)}$	Turn - Off Delay Time			54	80	nS
t_f	Turn - Off Fall Time			90	200	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 75 A, V_{GS} = 10 V		100	115	nC
Q_{gs}	Gate-Source Charge			14.5		nC
Q_{gd}	Gate-Drain Charge			51		nC

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				75	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				225	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 37.5 A (Note 1)		0.9	1.3	V
		T_J = 125°C		0.84	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 75 A, dI_F/dt = 100 A/µs		80	150	ns
I_{rr}	Reverse Recovery Current		2	4.8	10	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

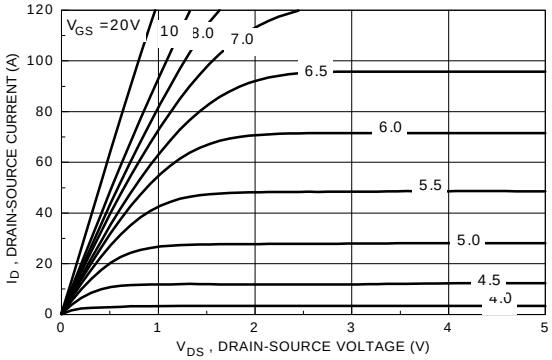


Figure 1. On-Region Characteristics.

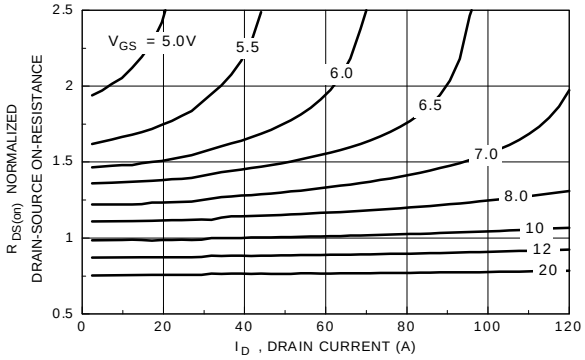


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

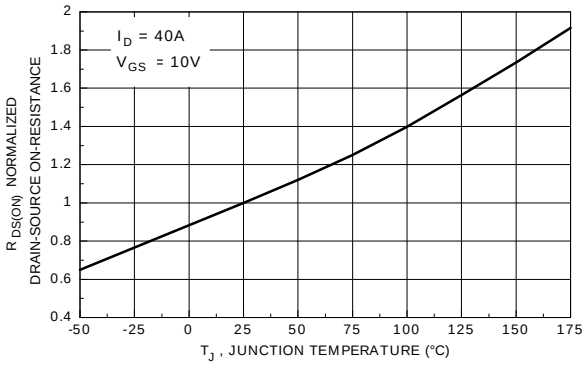


Figure 3. On-Resistance Variation with Temperature.

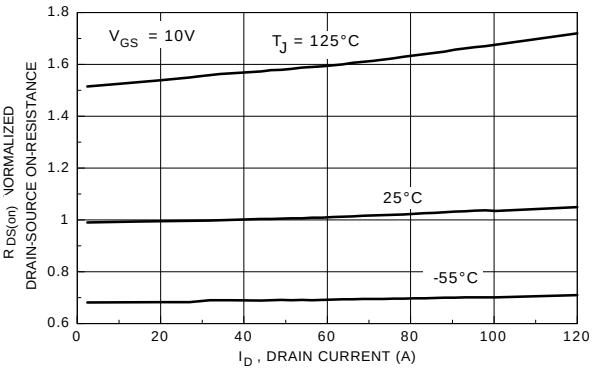


Figure 4. On-Resistance Variation with Drain Current and Temperature.

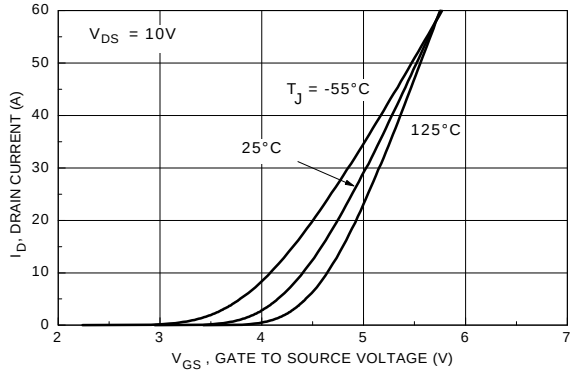


Figure 5. Transfer Characteristics.

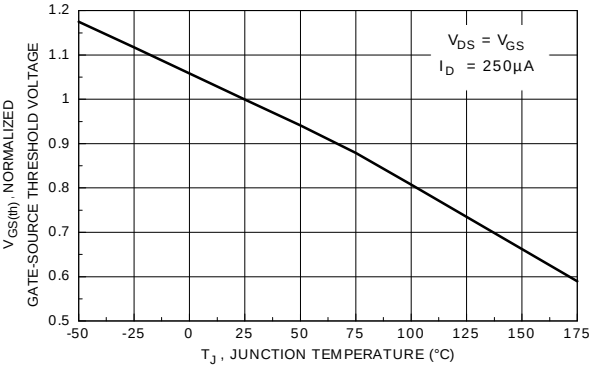
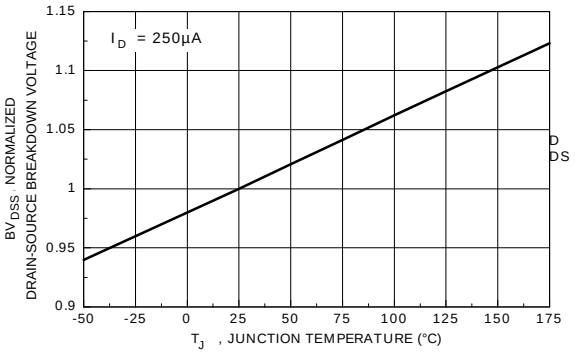
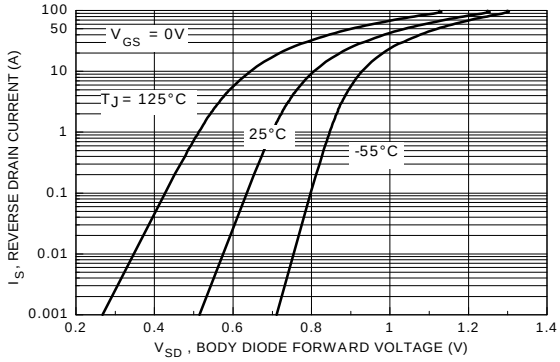
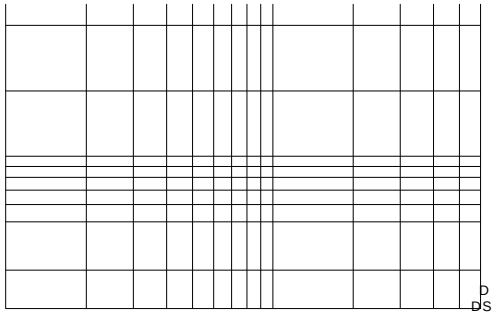
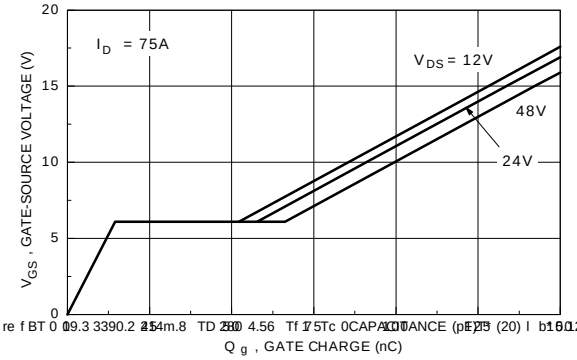


Figure 6. Gate Threshold Variation with Temperature.


I_D = 250µA
BV_{DSS}, NORMALIZED
DRAIN-SOURCE BREAKDOWN VOLTAGE
1.15
1.1
1.05
1
0.95
0.9
-50 -25 0 25 50 75 100 125 150 175
T_J , JUNCTION TEMPERATURE (°C)


V_{GS} = 0V
T_J = 125°C
25°C
-55°C
I_S, REVERSE DRAIN CURRENT (A)
100
50
10
1
0.1
0.01
0.001
0.2 0.4 0.6 0.8 1 1.2 1.4
V_{SD} , BODY DIODE FORWARD VOLTAGE (V)


1 2 5 10 20 30


I_D = 75A
V_{DS} = 12V
48V
24V
V_{GS} , GATE-SOURCE VOLTAGE (V)
20
15
10
5
0
0 5 10 15 20 25 30
Q_g , GATE CHARGE (nC)

Typical Electrical Characteristics (continued)

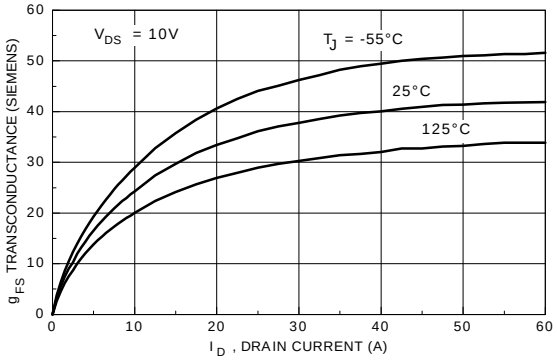


Figure 13. Transconductance Variation with Drain Current and Temperature.

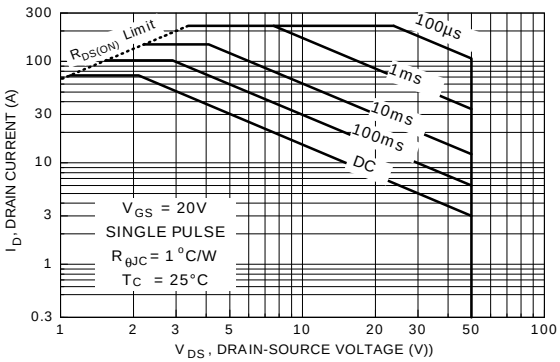


Figure 14. Maximum Safe Operating Area.

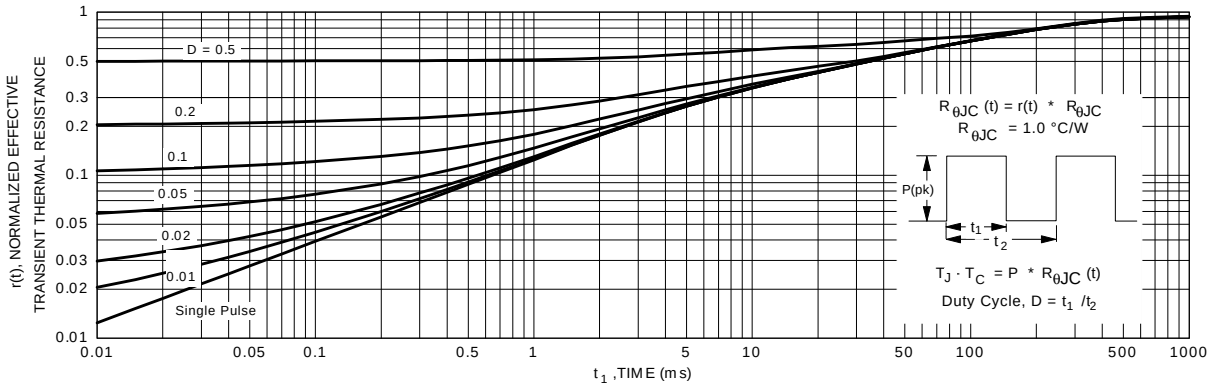
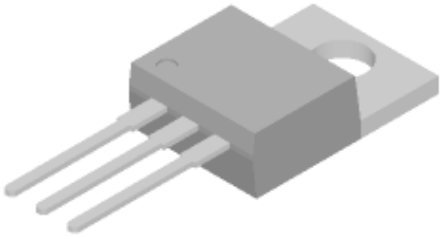


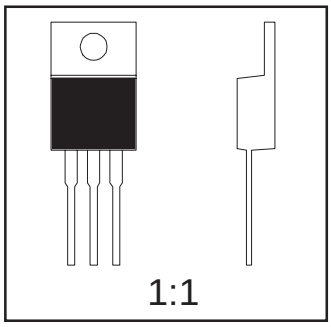
Figure 15. Transient Thermal Response Curve.


530mm
mm
units maximum
FSCIN
FS852
NDP4060L
FS852
NDP4060L

TO-220 Tape and Reel Data and Package Dimensions, continued

TO-220 (FS PKG Code 37)

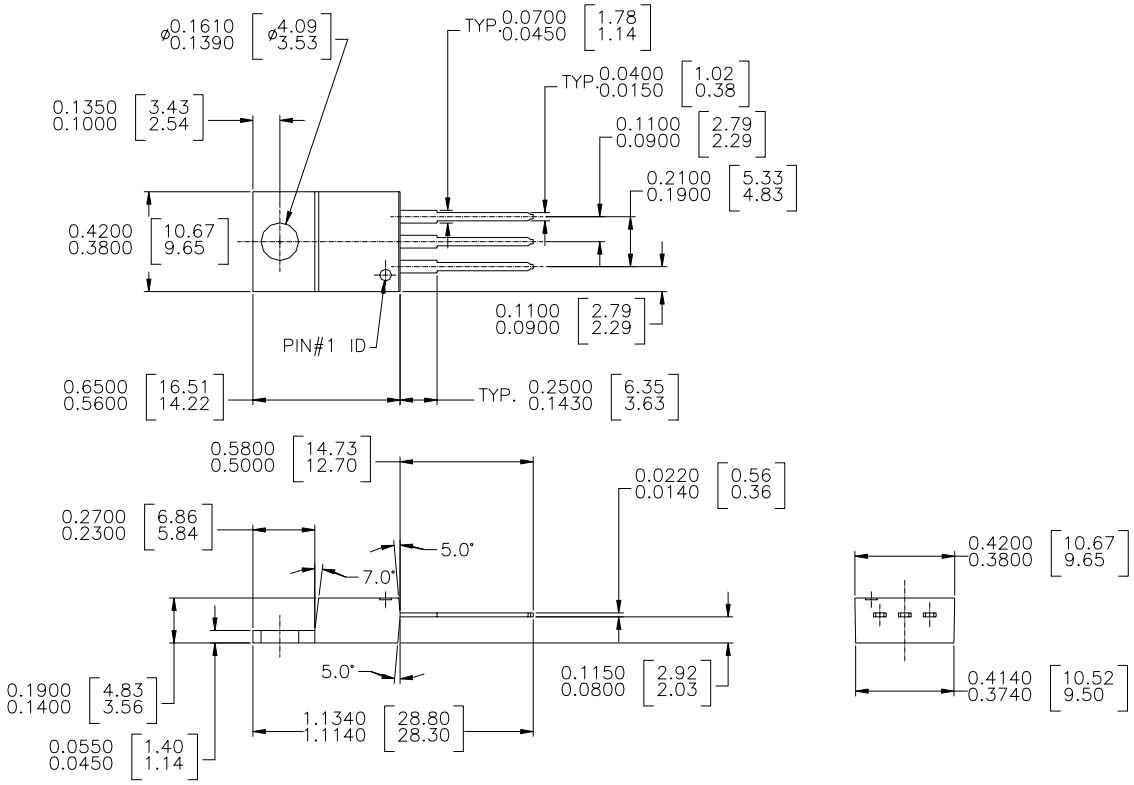




Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 1.4378



NOTE : UNLESS OTHERWISE SPECIFIED

TO 220 3 LEAD

1. STANDARD LEAD FINISH :
200 MICROINCHES / 5.08 MICRON MINIMUM
LEAD / TIN 15/85 ON OLIN 194 COPPER OR EQUIVALENT

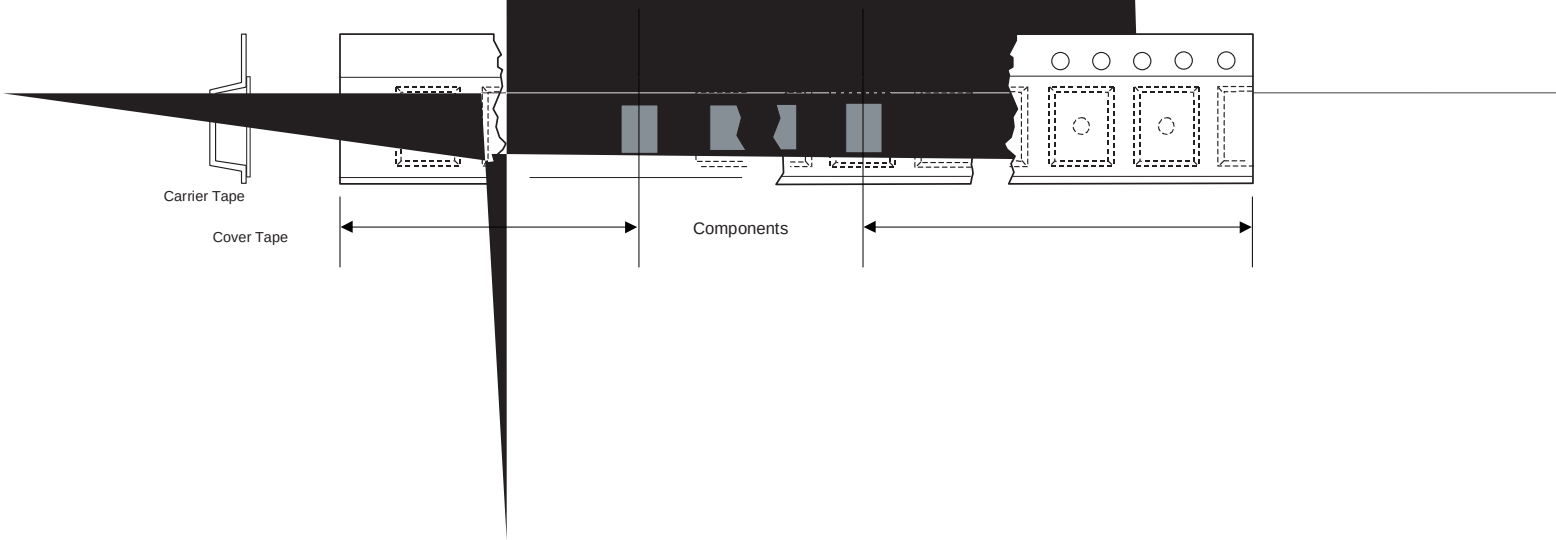
2. DIMENSION BASED ON JEDEC STANDARD TO-220
VARIATION AB, ISSUE J, DATED 3/24/87

TO-263AB/D^{2}PAK Packagi
Configuration: Figure 1.0

TO-263AB/D^{2}PAK Packaging Information		
Packaging Option		

Note/Comments		

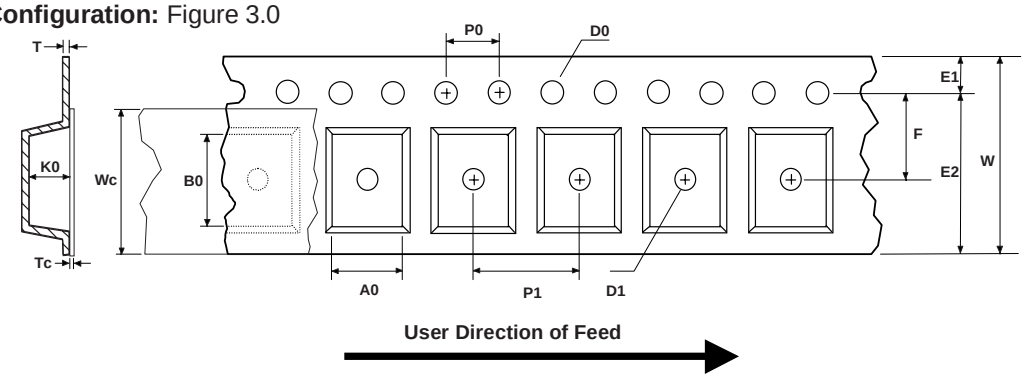
TO-263AB/D^{2}PAK Tape Lea
Configuration: Figure 2.0



TO-263AB/D²PAK Tape and Reel Data and Package Dimensions, continued

TO-263AB/D²PAK Embossed Carrier Tape

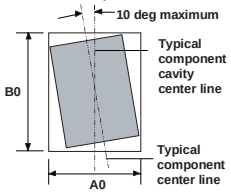
Configuration: Figure 3.0



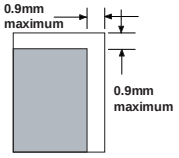
Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
TO263AB/ D²PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Sketch A (Side or Front Sectional View)
Component Rotation



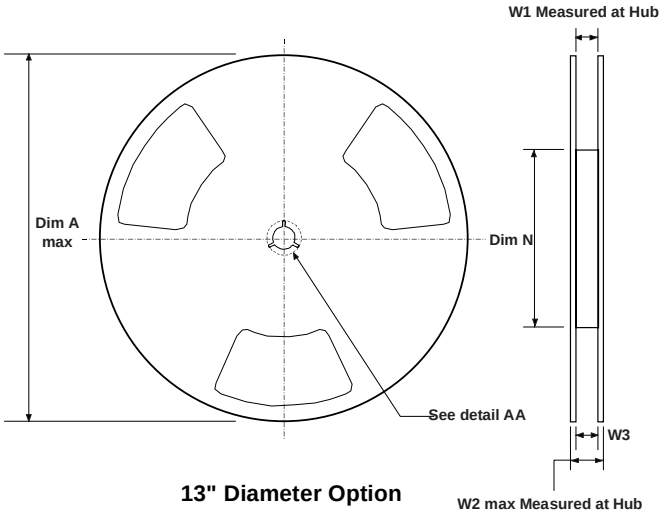
Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

TO-263AB/D²PAK Reel Configuration:

Figure 4.0

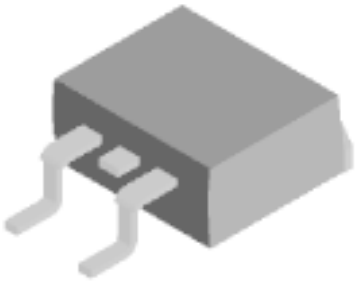


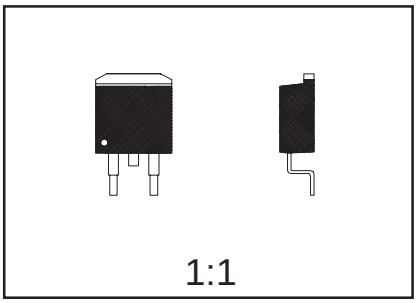
13" Diameter Option

Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
24mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.961 +0.078/-0.000 24.4 +2/0	1.197 30.4	0.941 – 0.1.079 23.9 – 27.4

TO-263AB/D²PAK Tape and Reel Data and Package Dimensions, continued

TO-263AB/D²PAK (FS PKG Code 45)

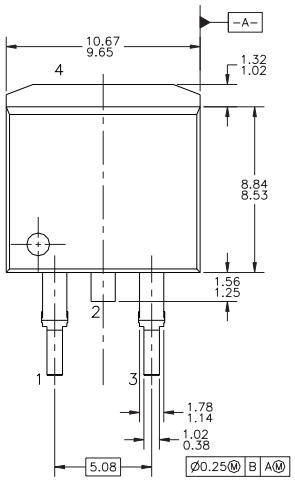


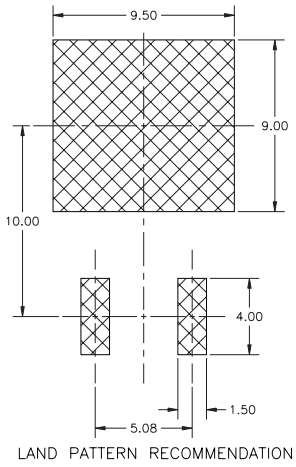


Scale 1:1 on letter size paper

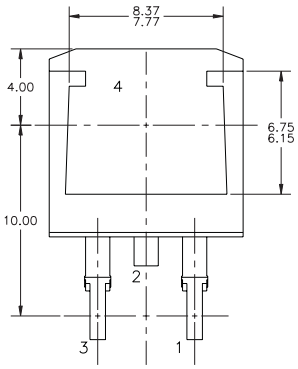
Dimensions shown below are in:
inches [millimeters]

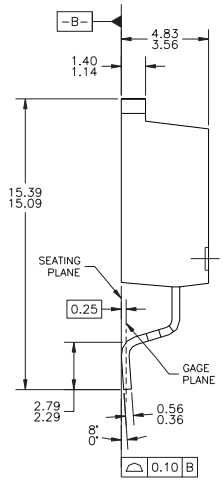
Part Weight per unit (gram): 1.4378





LAND PATTERN RECOMMENDATION





NOTES: UNLESS OTHERWISE SPECIFIED
A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) STANDARD LEAD FINISH:
200 MICROINCHES / 5.08 MICROMETERS MIN.
LEAD/TIN 15/85 ON OLIN 194 COPPER OR EQUIVALENT.
C) MAXIMUM VERTICAL BURR ON HEATSINK NOT TO EXCEED 0.003 INCH / 0.05mm.
D) NO PACKAGE CHIPS, CRACKS OR SURFACE IDENTIFICATION ALLOWED AFTER FORMING.
E) REFERENCE JEDEC, TO-263, ISSUE C, VARIATION AB, DATED 2/92.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™
CoolFET™
CROSSVOLT™
E^2CMOS^{TM}
FACT™
FACT Quiet Series™
FAST®
FASTr™
GTO™
HiSeC™
ISOPLANAR™
MICROWIRE™
POP™
PowerTrench™
QFET™
QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
TinyLogic™
UHC™
VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.