1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

The data flash ROM (2 KB X 2 blocks) is embedded.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Outline

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

<table>
<tr><th colspan="2">Item</th><th>Performance</th></tr>
<tr><td rowspan="5">CPU</td><td>Number of basic instructions</td><td>89 instructions</td></tr>
<tr><td>Shortest instruction execution time</td><td>62.5 ns (f(X$_{IN}$) = 16 MHz, V$_{CC}$ = 3.0 to 5.5 V)
100 ns (f(X$_{IN}$) = 10 MHz, V$_{CC}$ = 2.7 to 5.5 V)</td></tr>
<tr><td>Operating mode</td><td>Single-chip</td></tr>
<tr><td>Address space</td><td>1M bytes</td></tr>
<tr><td>Memory capacity</td><td>See Table 1.2 "Product List"</td></tr>
<tr><td rowspan="8">Peripheral function</td><td>Interrupt</td><td>Internal: 9 factors, External: 5 factors,
Software: 4 factors, Priority level: 7 levels</td></tr>
<tr><td>Watchdog timer</td><td>15 bits x 1 (with prescaler)
Reset start function selectable</td></tr>
<tr><td>Timer</td><td>Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel,
Timer Z: 8 bits x 1 channel
(Each timer equipped with 8-bit prescaler)
Timer C: 16 bits x 1 channel
    Input capture circuit</td></tr>
<tr><td>Serial Interface</td><td>•1 channel
 Clock synchronous, UART
•1 channel
 UART</td></tr>
<tr><td>A/D converter</td><td>10-bit A/D converter: 1 circuit, 8 channels</td></tr>
<tr><td>Clock generation circuit</td><td>2 circuits
 •Main clock generation circuit (Equipped with a built-in feedback resistor)
 •On-chip oscillator</td></tr>
<tr><td>Oscillation stop detection function</td><td>Stop detection of main clock oscillation</td></tr>
<tr><td>Port</td><td>Input/Output: 22 (including LED drive port), Input: 2
(LED drive I/O port: 8)</td></tr>
<tr><td rowspan="2">Electrical characteristics</td><td>Power supply voltage</td><td>V$_{CC}$ = 3.0 to 5.5 V (f(X$_{IN}$) = 16 MHz)
V$_{CC}$ = 2.7 to 5.5 V (f(X$_{IN}$) = 10 MHz)</td></tr>
<tr><td>Power consumption</td><td>Typ. 8mA (V$_{CC}$ = 5.0 V, (f(X$_{IN}$) = 16MHz, High-speed mode)
Typ. 5mA (V$_{CC}$ = 3.0 V, (f(X$_{IN}$) = 10MHz, High-speed mode)
Typ. 35μA (V$_{CC}$ = 3.0 V, Wait mode, Peripheral clock stops)
Typ. 0.7μA (V$_{CC}$ = 3.0 V, Stop mode)</td></tr>
<tr><td rowspan="2">Flash memory</td><td>Program/erase voltage</td><td>V$_{CC}$ = 2.7 to 5.5 V</td></tr>
<tr><td>Number of program/erase</td><td>10,000 times (Data area)
1,000 times (Program area)</td></tr>
<tr><td colspan="2">Operating ambient temperature</td><td>-20 to 85 °C
-40 to 85 °C (D-version)</td></tr>
<tr><td colspan="2">Package</td><td>32-pin plastic mold LQFP</td></tr>
</table>

RENESAS

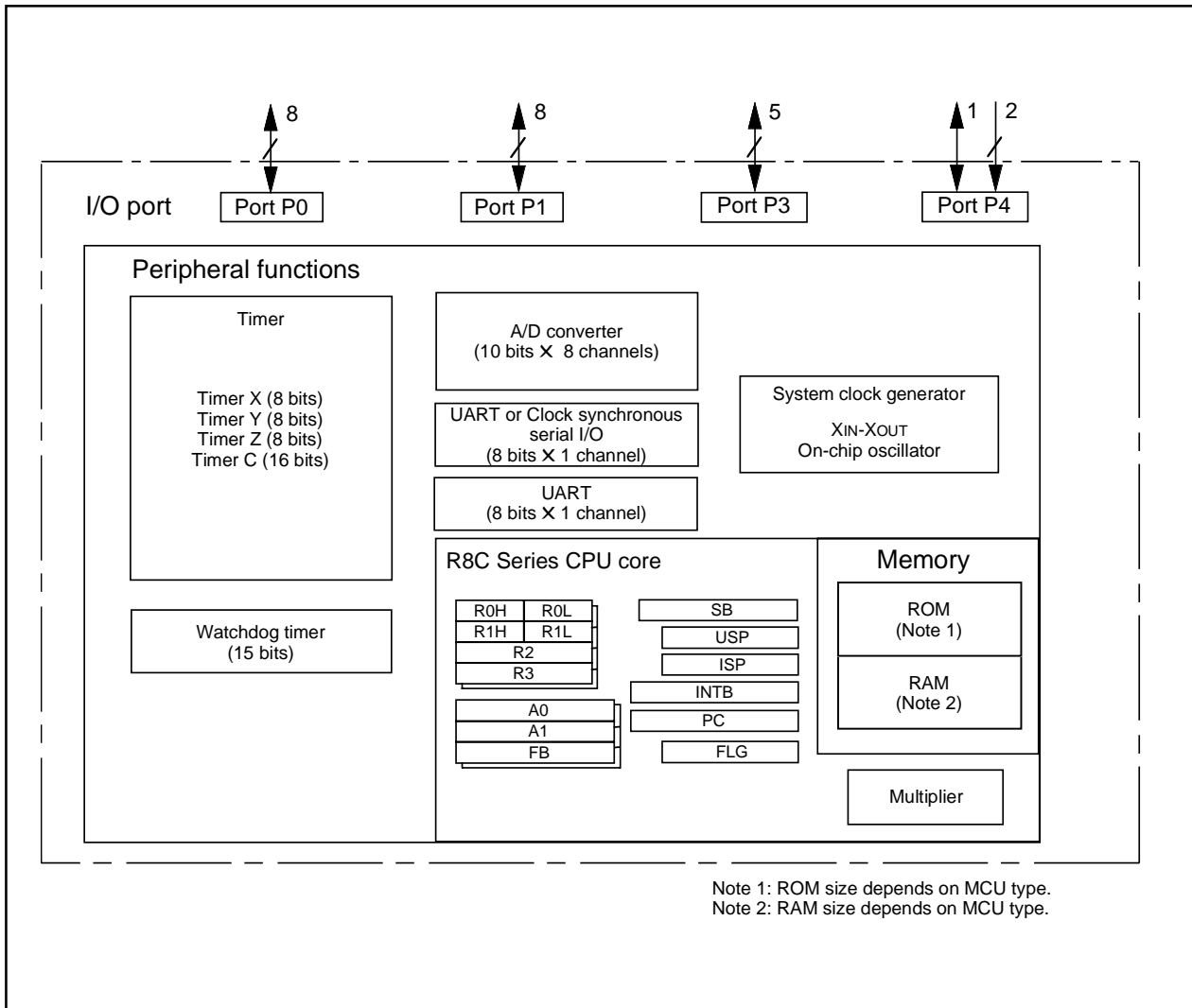## 1.3 Block Diagram

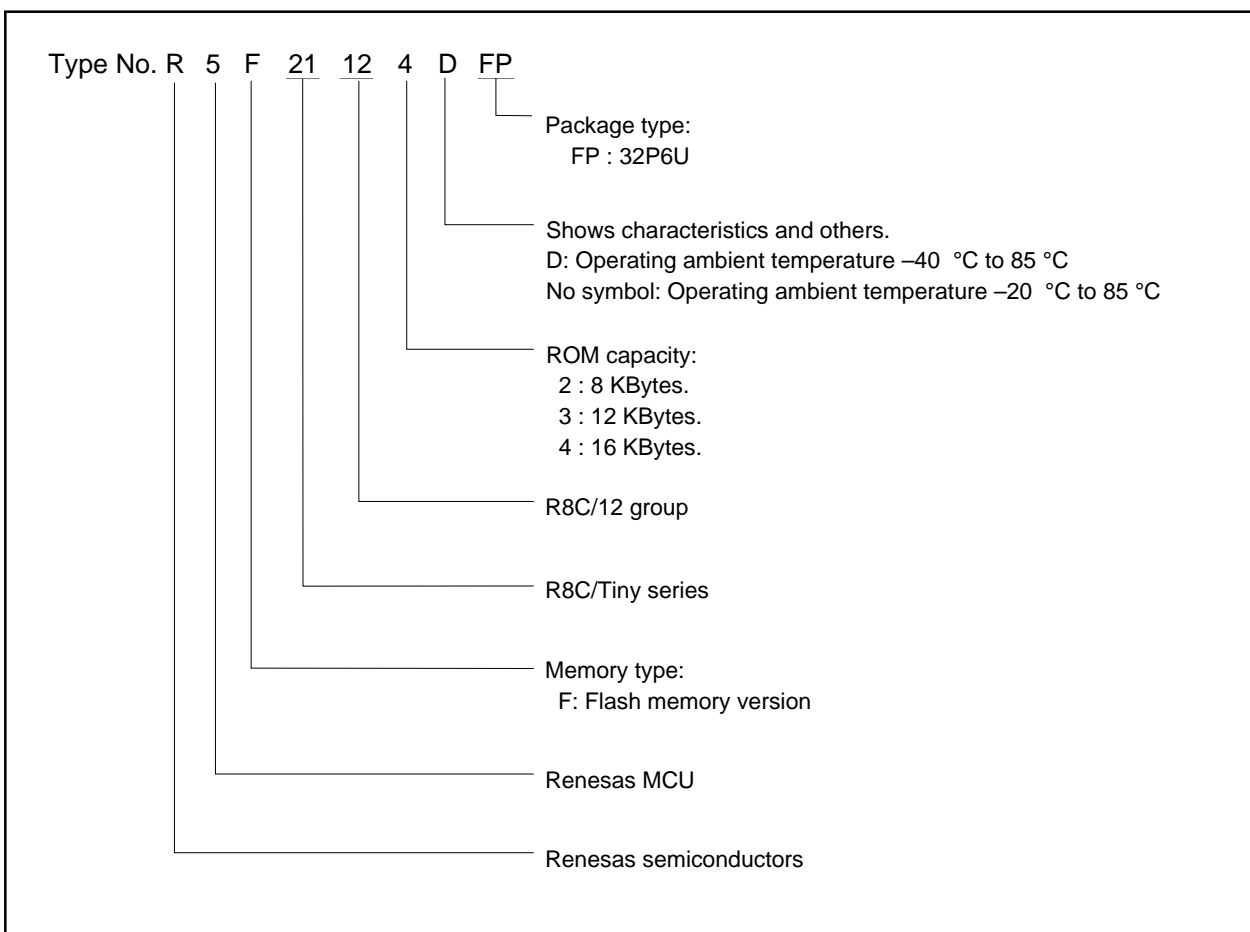Figure 1.1. shows this MCU block diagram.

Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the products.

Table 1.2 Product List

As of September 2004

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program area	Data area			
R5F21122FP	8K bytes	2K bytes x 2	512 bytes	32P6U-A	Flash memory version
R5F21123FP	12K bytes	2K bytes x 2	768 bytes	32P6U-A	
R5F21124FP	16K bytes	2K bytes x 2	1K bytes	32P6U-A	
R5F21122DFP	8K bytes	2K bytes x 2	512 bytes	32P6U-A	D version
R5F21123DFP	12K bytes	2K bytes x 2	768 bytes	32P6U-A	
R5F21124DFP	16K bytes	2K bytes x 2	1K bytes	32P6U-A	

```
Type No. R   5   F   21  12   4   D  FP

                                    │   Package type:
                                    │      FP : 32P6U
                                    │
                                 │  Shows characteristics and others.
                                 │  D: Operating ambient temperature –40 °C to 85 °C
                                 │  No symbol: Operating ambient temperature –20 °C to 85 °C
                                 │
                             │      ROM capacity:
                             │       2 : 8 KBytes.
                             │       3 : 12 KBytes.
                             │       4 : 16 KBytes.
                             │
                         │          R8C/12 group
                         │
                     │              R8C/Tiny series
                     │
                 │                  Memory type:
                 │                     F: Flash memory version
                 │
             │                      Renesas MCU
             │
         │                          Renesas semiconductors
```

Figure 1.2 Type No., Memory Size, and Package

RENESAS

1.5 Pin Configuration

Figure 1.3 shows the pin configuration (top view).

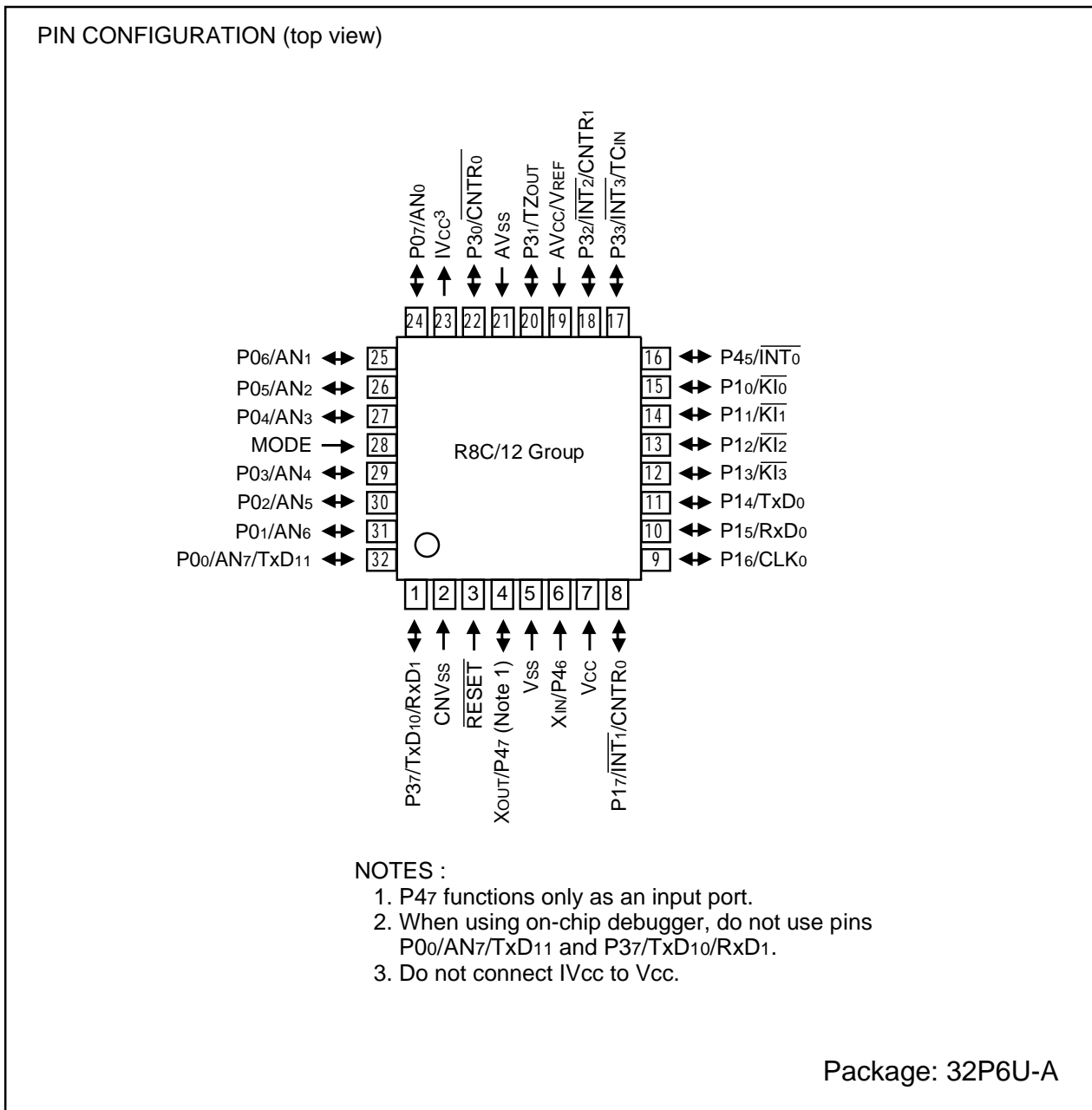PIN CONFIGURATION (top view)

R8C/12 Group

Top pins (left to right, 24–17):
P07/AN0, IVcc[3], P30/CNTR0, AVss, P31/TZout, AVcc/VREF, P32/INT2/CNTR1, P33/INT3/TCIN

Left pins (top to bottom, 25–32):
P06/AN1 — 25
P05/AN2 — 26
P04/AN3 — 27
MODE — 28
P03/AN4 — 29
P02/AN5 — 30
P01/AN6 — 31
P00/AN7/TxD11 — 32

Right pins (top to bottom, 16–9):
16 — P45/INT0
15 — P10/KI0
14 — P11/KI1
13 — P12/KI2
12 — P13/KI3
11 — P14/TxD0
10 — P15/RxD0
9 — P16/CLK0

Bottom pins (left to right, 1–8):
P37/TxD10/RxD1, CNVss, RESET, Xout/P47 (Note 1), Vss, Xin/P46, Vcc, P17/INT1/CNTR0

NOTES :
1. P47 functions only as an input port.
2. When using on-chip debugger, do not use pins
   P00/AN7/TxD11 and P37/TxD10/RxD1.
3. Do not connect IVcc to Vcc.

Package: 32P6U-A

Figure 1.3 Pin Configuration (Top View)

RENESAS

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 μF). Do not connect to Vcc.
Analog power supply input	AVcc, AVss	I	These are power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss.
Reset input	$\overline{\text{RESET}}$	I	"L" on this input resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor.
MODE	MODE	I	Connect this pin to Vcc via a resistor.
Main clock input	X_{IN}	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the X_{IN} and X_{OUT} pins. To use an externally derived clock, input it to the X_{IN} pin and leave the X_{OUT} pin open.
Main clock output	X_{OUT}	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT}}_0$ to $\overline{\text{INT}}_3$	I	These are $\overline{\text{INT}}$ interrupt pins.
Key input interrupt	$\overline{\text{KI}}_0$ to $\overline{\text{KI}}_3$	I	These are key input interrupt pins.
Timer X	$CNTR_0$	I/O	This is the timer X I/O pin.
	$\overline{CNTR_0}$	O	This is the timer X output pin.
Timer Y	$CNTR_1$	I/O	This is the timer Y I/O pin.
Timer Z	TZ_{OUT}	O	This is the timer Z output pin.
Timer C	TC_{IN}	I	This is the timer C input pin.
Serial interface	CLK_0	I/O	This is a transfer clock I/O pin.
	RxD_0, RxD_1	I	These are serial data input pins.
	TxD_0, TxD_{10}, TxD_{11}	O	These are serial data output pins.
Reference voltage input	V_{REF}	I	This is a reference voltage input pin for A/D converter. Connect the V_{REF} pin to Vcc.
A/D converter	AN_0 to AN_7	I	These are analog input pins for A/D converter.
I/O port	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P3_0$ to $P3_3$, $P3_7$, $P4_5$	I/O	These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. $P1_0$ to $P1_7$ also function as LED drive ports.
Input port	$P4_6$, $P4_7$	I	These are input only pins.

RENESAS

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.
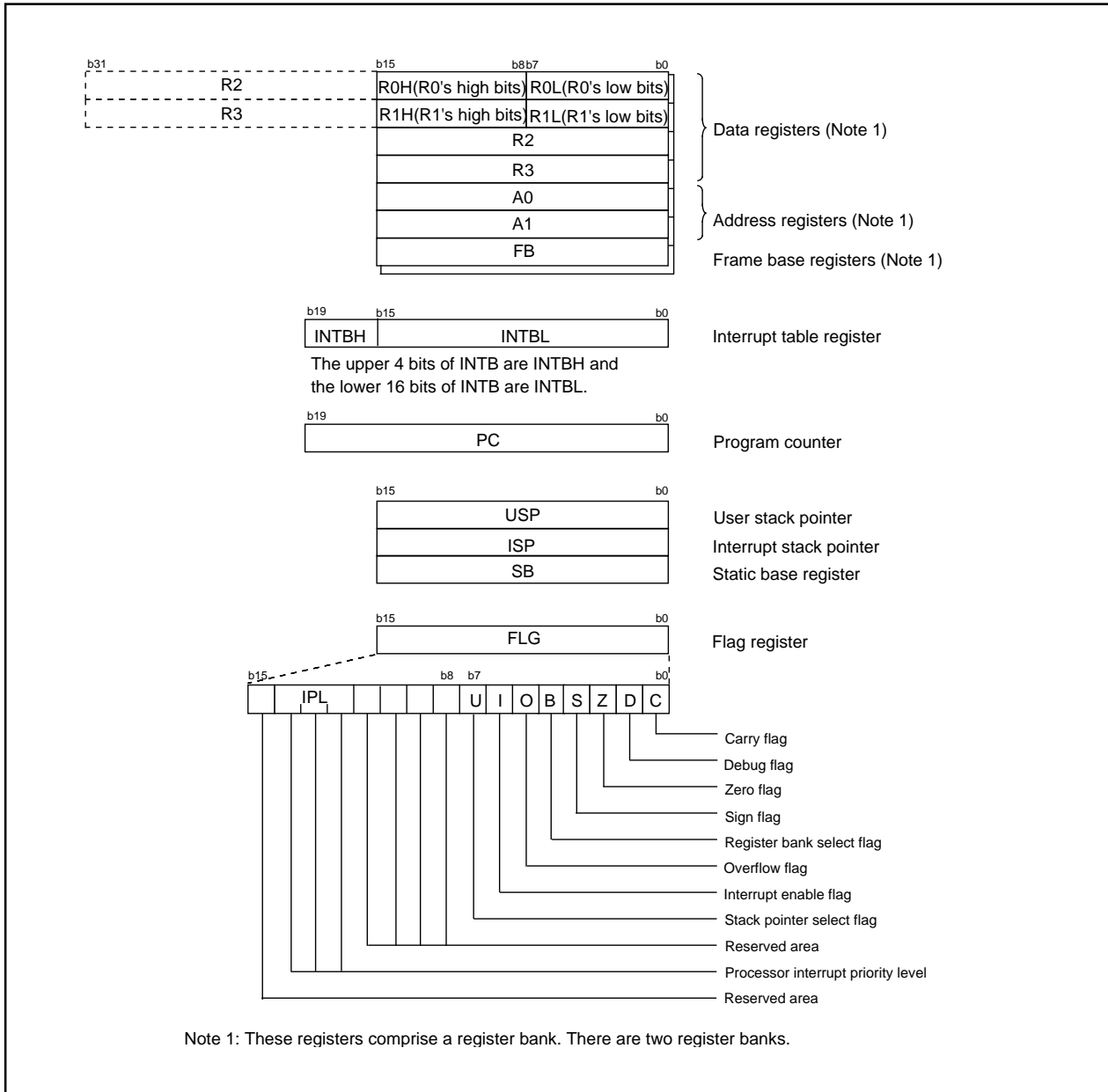

Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

RENESAS

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.
Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0" ; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.
Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".
The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

RENESAS

3. Memory

Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 00000_{16} to $FFFFF_{16}$.

The internal ROM (program area) is allocated in a lower address direction beginning with address $0FFFF_{16}$. For example, a 16-Kbyte internal ROM is allocated to the addresses from $0C000_{16}$ to $0FFFF_{16}$. The fixed interrupt vector table is allocated to the addresses from $0FFDC_{16}$ to $0FFFF_{16}$. Therefore, store the start address of each interrupt routine here.

The internal ROM (data area) is allocated to the addresses from 02000_{16} to $02FFF_{16}$.

The internal RAM is allocated in an upper address direction beginning with address 00400_{16}. For example, a 1-Kbyte internal RAM is allocated to the addresses from 00400_{16} to $007FF_{16}$. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

Special function registers (SFR) are allocated to the addresses from 00000_{16} to $002FF_{16}$. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.

NOTES :
1. The data flash ROM block A (2K bytes) and block B (2K bytes) are shown.
2. Blank spaces are reserved. No access is allowed.

Type name	Internal ROM		Internal RAM	
	Size	Address 0YYYY$_{16}$	Size	Address 0XXXX$_{16}$
R5F21124FP, R5F21124DFP	16K bytes	$0C000_{16}$	1K bytes	$007FF_{16}$
R5F21123FP, R5F21123DFP	12K bytes	$0D000_{16}$	768 bytes	$006FF_{16}$
R5F21122FP, R5F21122DFP	8K bytes	$0E000_{16}$	512 bytes	$005FF_{16}$

Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After reset
0000_{16}			
0001_{16}			
0002_{16}			
0003_{16}			
0004_{16}	Processor mode register 0	PM0	$XXXX0X00_2$
0005_{16}	Processor mode register 1	PM1	$00XXX0X0_2$
0006_{16}	System clock control register 0	CM0	01101000_2
0007_{16}	System clock control register 1	CM1	00100000_2
0008_{16}			
0009_{16}	Address match interrupt enable register	AIER	$XXXXXX00_2$
$000A_{16}$	Protect register	PRCR	$00XXX000_2$
$000B_{16}$			
$000C_{16}$	Oscillation stop detection register	OCD	00000100_2
$000D_{16}$	Watchdog timer reset register	WDTR	XX_{16}
$000E_{16}$	Watchdog timer start register	WDTS	XX_{16}
$000F_{16}$	Watchdog timer control register	WDC	$000XXXXX_2$
0010_{16}	Address match interrupt register 0	RMAD0	00_{16}
0011_{16}			00_{16}
0012_{16}			$X0_{16}$
0013_{16}			
0014_{16}	Address match interrupt register 1	RMAD1	00_{16}
0015_{16}			00_{16}
0016_{16}			$X0_{16}$
0017_{16}			
0018_{16}			
0019_{16}			
$001A_{16}$			
$001B_{16}$			
$001C_{16}$			
$001D_{16}$			
$001E_{16}$	$\overline{INT0}$ input filter select register	INT0F	$XXXXX000_2$
$001F_{16}$			
0020_{16}			
0021_{16}			
0022_{16}			
0023_{16}			
0024_{16}			
0025_{16}			
0026_{16}			
0027_{16}			
0028_{16}			
0029_{16}			
$002A_{16}$			
$002B_{16}$			
$002C_{16}$			
$002D_{16}$			
$002E_{16}$			
$002F_{16}$			
0030_{16}			
0031_{16}			
0032_{16}			
0033_{16}			
0034_{16}			
0035_{16}			
0036_{16}			
0037_{16}			
0038_{16}			
0039_{16}			
$003A_{16}$			
$003B_{16}$			
$003C_{16}$			
$003D_{16}$			
$003E_{16}$			
$003F_{16}$			

NOTES :
  1. The blank areas are reserved and cannot be used by users.

  X : Undefined

Table 4.2 SFR Information(2)[1]

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆			
0049₁₆			
004A₁₆			
004B₁₆			
004C₁₆			
004D₁₆	Key input interrupt control register	KUPIC	XXXXX0002
004E₁₆	A/D conversion interrupt control register	ADIC	XXXXX0002
004F₁₆			
0050₁₆			
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055₁₆	INT2 interrupt control register	INT2IC	XXXXX0002
0056₁₆	Timer X interrupt control register	TXIC	XXXXX0002
0057₁₆	Timer Y interrupt control register	TYIC	XXXXX0002
0058₁₆	Timer Z interrupt control register	TZIC	XXXXX0002
0059₁₆	INT1 interrupt control register	INT1IC	XXXXX0002
005A₁₆	INT3 interrupt control register	INT3IC	XXXXX0002
005B₁₆	Timer C interrupt control register	TCIC	XXXXX0002
005C₁₆			
005D₁₆	INT0 interrupt control register	INT0IC	XX00X0002
005E₁₆			
005F₁₆			
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

NOTES :
  1.The blank areas are reserved and cannot be used by users.

X : Undefined

Table 4.3 SFR Information(3)[1]

Address	Register	Symbol	After reset
0080₁₆	Timer Y, Z mode register	TYZMR	00₁₆
0081₁₆	Prescaler Y	PREY	FF₁₆
0082₁₆	Timer Y secondary	TYSC	FF₁₆
0083₁₆	Timer Y primary	TYPR	FF₁₆
0084₁₆	Timer Y, Z waveform output control register	PUM	00₁₆
0085₁₆	Prescaler Z	PREZ	FF₁₆
0086₁₆	Timer Z secondary	TZSC	FF₁₆
0087₁₆	Timer Z primary	TZPR	FF₁₆
0088₁₆			
0089₁₆			
008A₁₆	Timer Y, Z output control register	TYZOC	00₁₆
008B₁₆	Timer X mode register	TXMR	00₁₆
008C₁₆	Prescaler X	PREX	FF₁₆
008D₁₆	Timer X register	TX	FF₁₆
008E₁₆	Timer count source setting register	TCSS	00₁₆
008F₁₆			
0090₁₆	Timer C register	TC	00₁₆
0091₁₆			00₁₆
0092₁₆			
0093₁₆			
0094₁₆			
0095₁₆			
0096₁₆	External input enable register	INTEN	00₁₆
0097₁₆			
0098₁₆	Key input enable register	KIEN	00₁₆
0099₁₆			
009A₁₆	Timer C control register 0	TCC0	00₁₆
009B₁₆	Timer C control register 1	TCC1	00₁₆
009C₁₆	Capture register	TM0	FF₁₆
009D₁₆			FF₁₆
009E₁₆			
009F₁₆			
00A0₁₆	UART0 transmit/receive mode register	U0MR	00₁₆
00A1₁₆	UART0 bit rate generator	U0BRG	XX₁₆
00A2₁₆	UART0 transmit buffer register	U0TB	XX₁₆
00A3₁₆			XX₁₆
00A4₁₆	UART0 transmit/receive control register 0	U0C0	00001000₂
00A5₁₆	UART0 transmit/receive control register 1	U0C1	00000010₂
00A6₁₆	UART0 receive buffer register	U0RB	XX₁₆
00A7₁₆			XX₁₆
00A8₁₆	UART1 transmit/receive mode register	U1MR	00₁₆
00A9₁₆	UART1 bit rate register	U1BRG	XX₁₆
00AA₁₆	UART1 transmit buffer register	U1TB	XX₁₆
00AB₁₆			XX₁₆
00AC₁₆	UART1 transmit/receive control register 0	U1C0	00001000₂
00AD₁₆	UART1 transmit/receive control register 1	U1C1	00000010₂
00AE₁₆	UART1 receive buffer register	U1RB	XX₁₆
00AF₁₆			XX₁₆
00B0₁₆	UART transmit/receive control register 2	UCON	00₁₆
00B1₁₆			
00B2₁₆			
00B3₁₆			
00B4₁₆			
00B5₁₆			
00B6₁₆			
00B7₁₆			
00B8₁₆			
00B9₁₆			
00BA₁₆			
00BB₁₆			
00BC₁₆			
00BD₁₆			
00BE₁₆			
00BF₁₆			

NOTES :
  1. The blank areas are reserved and cannot be used by users.

  X : Undefined

RENESAS

Table 4.4 SFR Information(4)[1]

Address	Register	Symbol	After reset
$00C0_{16}$	A/D register	AD	$XXXXXXXX_2$
$00C1_{16}$			$XXXXXXXX_2$
$00C2_{16}$			
$00C3_{16}$			
$00C4_{16}$			
$00C5_{16}$			
$00C6_{16}$			
$00C7_{16}$			
$00C8_{16}$			
$00C9_{16}$			
$00CA_{16}$			
$00CB_{16}$			
$00CC_{16}$			
$00CD_{16}$			
$00CE_{16}$			
$00CF_{16}$			
$00D0_{16}$			
$00D1_{16}$			
$00D2_{16}$			
$00D3_{16}$			
$00D4_{16}$	A/D control register 2	ADCON2	00_{16}
$00D5_{16}$			
$00D6_{16}$	A/D control register 0	ADCON0	$00000XXX_2$
$00D7_{16}$	A/D control register 1	ADCON1	00_{16}
$00D8_{16}$			
$00D9_{16}$			
$00DA_{16}$			
$00DB_{16}$			
$00DC_{16}$			
$00DD_{16}$			
$00DE_{16}$			
$00DF_{16}$			
$00E0_{16}$	Port P0 register	P0	XX_{16}
$00E1_{16}$	Port P1 register	P1	XX_{16}
$00E2_{16}$	Port P0 direction register	PD0	00_{16}
$00E3_{16}$	Port P1 direction register	PD1	00_{16}
$00E4_{16}$			
$00E5_{16}$	Port P3 register	P3	XX_{16}
$00E6_{16}$			
$00E7_{16}$	Port P3 direction register	PD3	00_{16}
$00E8_{16}$	Port P4 register	P4	XX_{16}
$00E9_{16}$			
$00EA_{16}$	Port P4 direction register	PD4	00_{16}
$00EB_{16}$			
$00EC_{16}$			
$00ED_{16}$			
$00EE_{16}$			
$00EF_{16}$			
$00F0_{16}$			
$00F1_{16}$			
$00F2_{16}$			
$00F3_{16}$			
$00F4_{16}$			
$00F5_{16}$			
$00F6_{16}$			
$00F7_{16}$			
$00F8_{16}$			
$00F9_{16}$			
$03FA_{16}$			
$00FB_{16}$			
$00FC_{16}$	Pull-up control register 0	PUR0	$00XX0000_2$
$00FD_{16}$	Pull-up control register 1	PUR1	$XXXXXX0X_2$
$00FE_{16}$	Port P1 drive capacity control register	DRR	00_{16}
$00FF_{16}$			
$01B3_{16}$	Flash memory control register 4	FMR4	01000000_2
$01B4_{16}$			
$01B5_{16}$	Flash memory control register 1	FMR1	$1000000X_2$
$01B6_{16}$			
$01B7_{16}$	Flash memory control register 0	FMR0	00000001_2
$0FFFF_{16}$	Option function select register [2]	OFS	Note 2

X : Undefined

NOTES:
1. The blank areas, 0100_{16} to $01B2_{16}$ and $01B8_{16}$ to $02FF_{16}$ are reserved and cannot be used by users.
2. The watchdog timer control bit is assigned. Refer to "Figure11.2 OFS, WDC, WDTR and WDTS registers" of Hardware Manual for details

RENESAS

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Supply voltage	$V_{CC}=AV_{CC}$	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage	$V_{CC}=AV_{CC}$	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_{opr}=25 $^\circ$C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	$^\circ$C
T_{stg}	Storage temperature		-65 to 150	$^\circ$C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage			2.7		5.5	V
AV_{CC}	Analog supply voltage				V_{CC}[3]		V
V_{SS}	Supply voltage				0		V
AV_{SS}	Analog supply voltage				0		V
V_{IH}	"H" input voltage			0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage			0		0.2V_{CC}	V
$I_{OH(sum)}$	"H" peak all output currents	Sum of all pins' IOH (peak)				-60.0	mA
$I_{OH(peak)}$	"H" peak output current					-10.0	mA
$I_{OH(avg)}$	"H" average output current					-5.0	mA
$I_{OL(sum)}$	"L" peak all output currents	Sum of all pins' IOL (peak)				60	mA
$I_{OL(peak)}$	"L" peak output current	Except $P1_0$ to $P1_7$				10	mA
		$P1_0$ to $P1_7$	Drive ability HIGH			30	mA
			Drive ability LOW			10	mA
$I_{OL(avg)}$	"L" average output current	Except $P1_0$ to $P1_7$				5	mA
		$P1_0$ to $P1_7$	Drive ability HIGH			15	mA
			Drive ability LOW			5	mA
f (X_{IN})	Main clock input oscillation frequency		3.0V £ V_{CC} £ 5.5V	0		16	MHz
			2.7V £ V_{CC} < 3.0V	0		10	MHz

Note
 1: Referenced to V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
 2: The mean output current is the mean value within 100ms.
 3: Maintain V_{CC}=AV_{CC}

Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		Vref =Vcc			10	Bit
–	Absolute accuracy	10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V			±3	LSB
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V			±2	LSB
		10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=3.3V			±5	LSB
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=3.3V			±2	LSB
RLADDER	Ladder resistance		VREF=VCC	10		40	kΩ
tCONV	Conversion time	10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V	3.3			μs
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V	2.8			μs
VREF	Reference voltage				Vcc[4]		V
VIA	Analog input voltage			0		Vref	V
–	A/D operation clock frequency[2]	Without sample & hold		0.25		10	MHz
		With sample & hold		1.0		10	MHz

Note

 1: Referenced to VCC=AVCC=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.

 2: When fAD is 10 MHz more, divide the fAD and make A/D operation clock frequency (ØAD) lower than
    10 MHz.

 3: When the Vcc is less than 4.2V, divide the fAD and make A/D operation clock frequency (ØAD) lower than fAD/2.

 4: Maintain Vcc=Vref
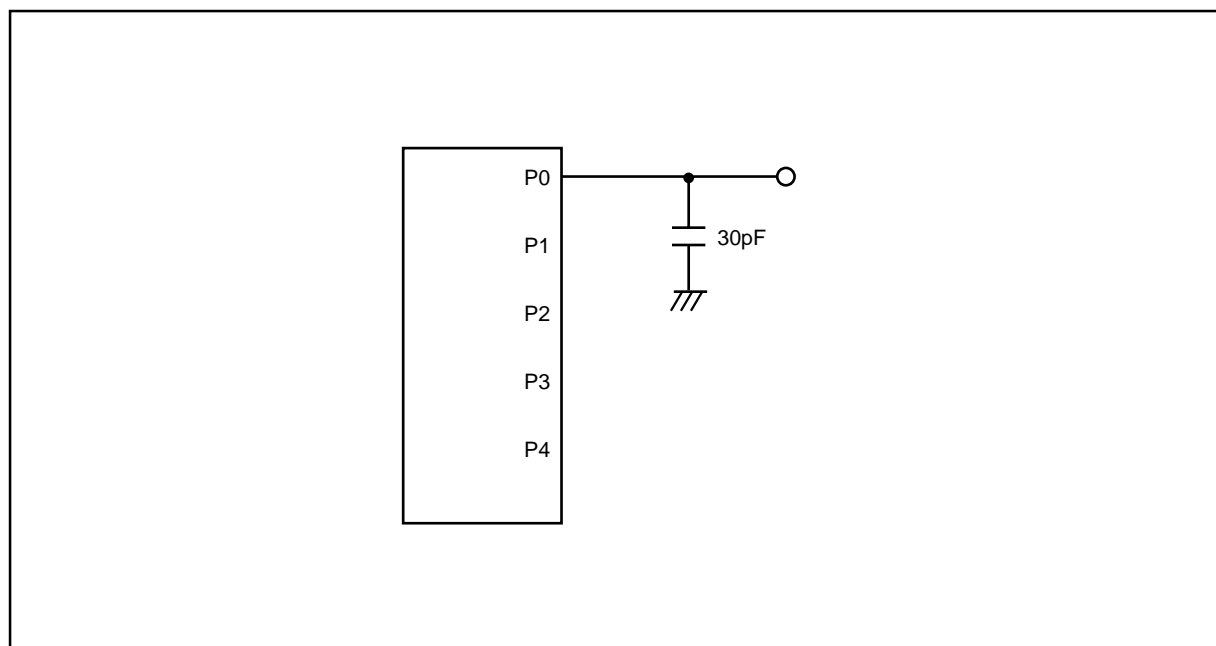
Figure 5.1 Port P0 to P4 measurement circuit

Table 5.4 Flash Memory (Program area) Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase cycle [2]		1,000 [3]	—	—	cycle
–	Byte program time	V_{CC} = 5.0 V at Topr = 25 °C	—	50	—	μs
–	Block erase time	V_{CC} = 5.0 V at Topr = 25 °C	—	0.4	—	s
$t_{d(SR-ES)}$	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program, Erase Temperature		0	—	60	°C
–	Data-retention duration	Topr = 55 °C	20	—	—	year

Table 5.5 Flash Memory (Data area Block A, Block B) Electrical Characteristics [4]

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase endurance[2]		10000 [3]	—	—	times
–	Byte program time(program/erase endurance ≤1000 times)	V_{CC} = 5.0 V at Topr = 25 °C	—	50	400	μs
–	Byte program time(program/erase endurance >1000 times)	V_{CC} = 5.0 V at Topr = 25 °C	—	65	—	μs
–	Block erase time(program/erase endurance ≤1000 times)	V_{CC} = 5.0 V at Topr = 25 °C	—	0.2	9	s
–	Block erase time(program/erase endurance >1000 times)	V_{CC} = 5.0 V at Topr = 25 °C	—	0.3	—	s
$t_{d(SR-ES)}$	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program/Erase Temperature		-20(-40)[8]	—	85	°C
–	Data-retention duration	Topr = 55 °C	20	—	—	year

Note
 1: Referenced to V_{CC}=AV_{CC}=2.7 to 5.5V at Topr = 0 to 60 °C unless otherwise specified.
 2: Definition of Program/Erase
    The cycle of Program/Erase shows a cycle for each block.
    If the program/erase number is "n" (n = 1,000, 10,000), "n" times erase can be performed for each block.
    For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.
    However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).
 3: Maximum numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.
 4: Table 16.5 applies for Block A or B when the Program/Erase cycles are more than 1000. The byte program time up to 1000 cycles are the same as that of the program area (see Table 5.4).
 5: To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.
 6: If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.
 7: Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
 8: -40 °C for D version.
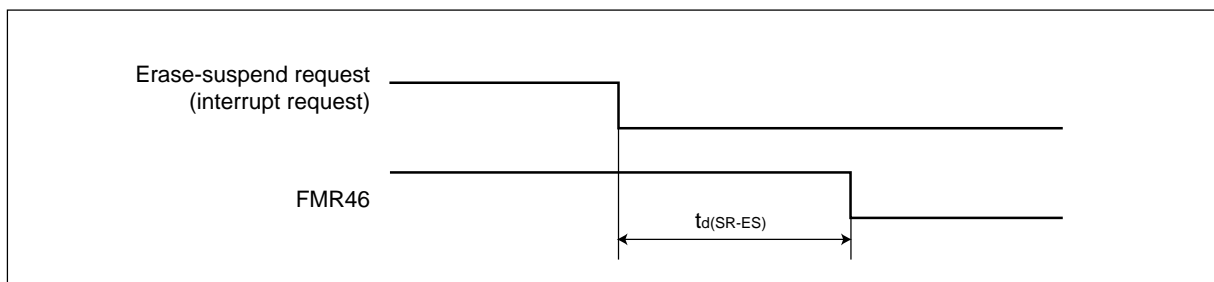
Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Min.	Standard Typ.	Max.	Unit
td(P-R)	Time for internal power supply stabilization during powering-on[2]				2	ms
td(R-S)	STOP release time[3]				150	µs

Note

1: The measuring condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.

2: This shows the waiting time until the internal power supply generating circuit is stabilized during powering-on.

3: This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

Table 5.7 Electrical Characteristics (1)   [Vcc=5V]

Symbol	Parameter		Measuring condition		Min.	Standard Typ.	Max.	Unit
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-5mA		Vcc-2.0		Vcc	V
			I_{OH}=-200µA		Vcc-0.3		Vcc	V
		X_{OUT}	Drive capacity HIGH	I_{OH}=-1 mA	Vcc-2.0		Vcc	V
			Drive capacity LOW	I_{OH}=-500µA	Vcc-2.0		Vcc	V
V_{OL}	"L" output voltage	P10 to P17 Except X_{OUT}	I_{OH}= 5 mA				2.0	V
			I_{OH}= 200 µA				0.45	V
		P10 to P17	Drive capacity HIGH	I_{OL}= 15 mA			2.0	V
			Drive capacity LOW	I_{OL}= 5 mA			2.0	V
			Drive capacity LOW	I_{OL}= 200 µA			0.45	V
		X_{OUT}	Drive capacity HIGH	I_{OL}= 1 mA			2.0	V
			Drive capacity LOW	I_{OL}=500 µA			2.0	V
$V_{T+}-V_{T-}$	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1			0.2		1.0	V
		RESET			0.2		2.2	V
I_{IH}	"H" input current		V_I=5V				5.0	µA
I_{IL}	"L" input current		V_I=0V				-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	X_{IN}				1.0		MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0			V

Note

1 : Referenced to Vcc=AVcc=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=20MHz unless otherwise specified.

RENESAS

Table 5.8 Electrical Characteristics (2)   [Vcc=5V]

Symbol	Parameter	Measuring condition		Min.	Standard Typ.	Max.	Unit
I_{CC}	Power supply current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss	High-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz No division		8	14	mA
			X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz No division		5		mA
		Medium-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8		3		mA
			X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8		2		mA
		On-chip oscillator mode	Main clock off On-chip oscillator on=125 kHz Division by 8		470	900	μA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation		40	80	μA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off		38	76	μA
		Stop mode	Main clock off On-chip oscillator off CM10="1" Peripheral clock off		0.8	3.0	μA

Note

1: The power supply current measuring is executed using the measuring program on frash memory.

2: Timer Y is operated with timer mode.

RENESAS

Timing requirements (Unless otherwise noted: Vcc = 5V, Vss = 0V at Ta = 25 °C) [Vcc=5V]

Table 5.9 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	62.5		ns
tWH(XIN)	XIN input HIGH pulse width	30		ns
tWL(XIN)	XIN input LOW pulse width	30		ns

Table 5.10 CNTR0 input, CNTR1 input, $\overline{\text{INT2}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	100		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	40		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	40		ns

Table 5.11 TCIN input, $\overline{\text{INT3}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	400 [1]		ns
tWH(TCIN)	TCIN input HIGH pulse width	200 [2]		ns
tWL(TCIN)	TCIN input LOW pulse width	200 [2]		ns

NOTES
1 : When using the Timer C capture function, adjust the cycle time above (1/ Timer C count source frequency x 3).
2 : When using the Timer C capture function, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.12 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	200		ns
tW(CKH)	CLKi input HIGH pulse width	100		ns
tW(CKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	35		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.13 External interrupt $\overline{\text{INT0}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{\text{INT0}}$ input HIGH pulse width	250 [1]		ns
tW(INL)	$\overline{\text{INT0}}$ input LOW pulse width	250 [2]		ns

NOTES
1 : When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2 : When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

RENESAS
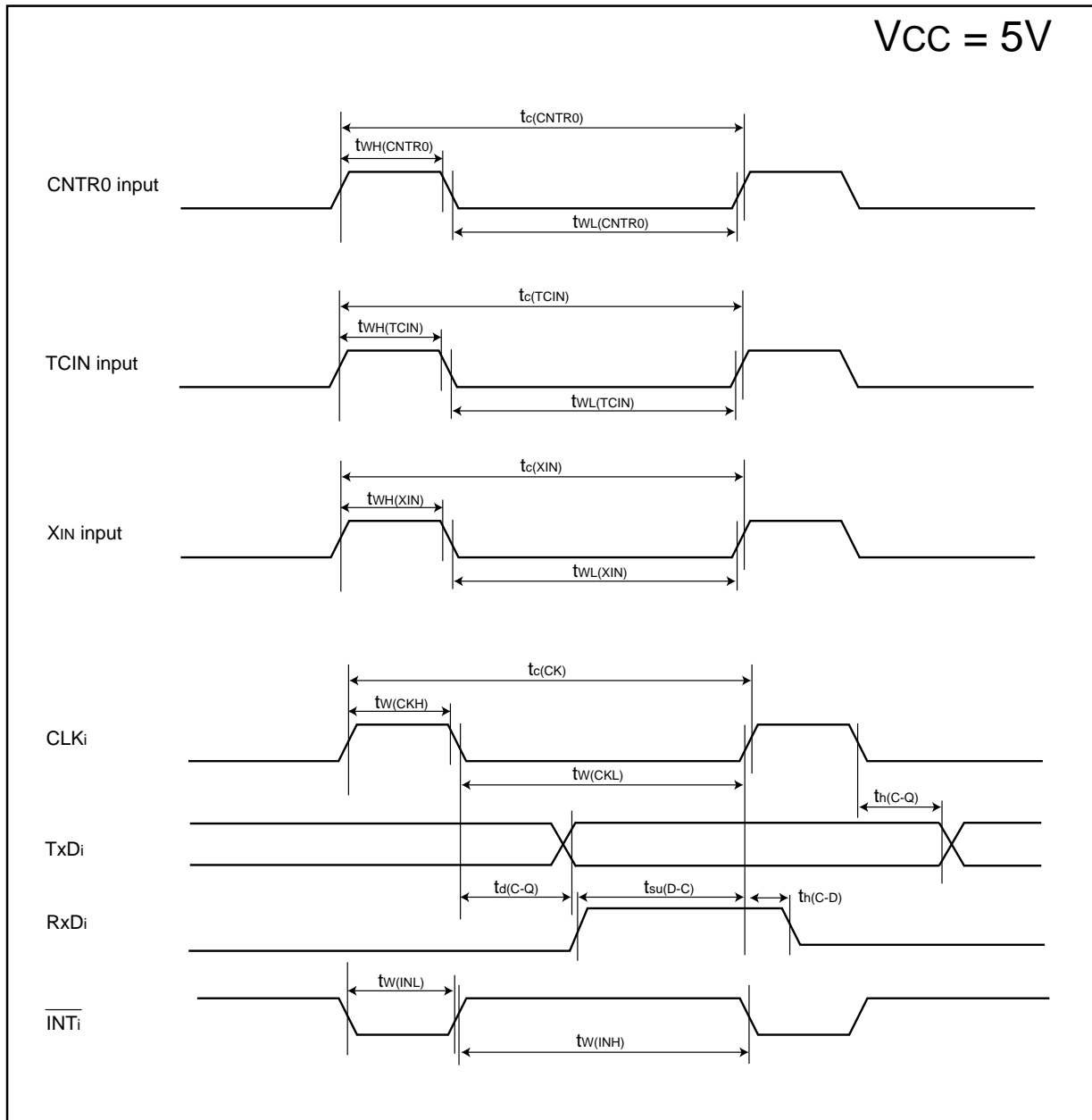
Figure 5.3 Vcc=5V timing diagram

Table 5.14 Electrical Characteristics (3)   [Vcc=3V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-1mA		Vcc-0.5		Vcc	V
		X_{OUT}	Drive capacity HIGH	I_{OH}=-0.1 mA	Vcc-0.5		Vcc	V
			Drive capacity LOW	I_{OH}=-50 μA	Vcc-0.5		Vcc	V
V_{OL}	"L" output voltage	P10 to P17 Except X_{OUT}	I_{OH}= 1 mA				0.5	V
		P10 to P17	Drive capacity HIGH	I_{OL}= 2 mA			0.5	V
			Drive capacity LOW	I_{OL}= 1 mA			0.5	V
		X_{OUT}	Drive capacity HIGH	I_{OL}= 0.1 mA			0.5	V
			Drive capacity LOW	I_{OL}=50 μAs			0.5	V
V_{T+}-V_{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1			0.2		0.8	V
		RESET			0.2		1.8	V
I_{IH}	"H" input current		V_I=3V				4.0	μA
I_{IL}	"L" input current		V_I=0V				-4.0	μA
R_{PULLUP}	Pull-up resistance		V_I=0V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	X_{IN}				3.0		MΩ
f_{RING}	On-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0			V

Note

1 : Referenced to V_{CC}=AV_{CC}=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

RENESAS

Table 5.15 Electrical Characteristics (4)   [Vcc=3V]

Symbol	Parameter	Measuring condition		Min.	Standard Typ.	Max.	Unit
I_{CC}	Power supply current (V$_{CC1}$=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V$_{SS}$	High-speed mode	X$_{IN}$=16 MHz (square wave) On-chip oscillator on=125 kHz No division		7	12	mA
			X$_{IN}$=10 MHz (square wave) On-chip oscillator on=125 kHz No division		5		mA
		Medium-speed mode	X$_{IN}$=16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8		2.5		mA
			X$_{IN}$=10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8		1.6		mA
		On-chip oscillator mode	Main clock off On-chip oscillator on=125 kHz Division by 8		420	800	μA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation		37	74	μA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off		35	70	μA
		Stop mode	Main clock off On-chip oscillator off CM10="1" Peripheral clock off		0.7	3.0	μA

Note
 1: The power supply current measuring is executed using the measuring program on frash memory.
 2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: Vcc = 3V, Vss = 0V at Ta = 25 °C) [Vcc=3V]

Table 5.16 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	100		ns
tWH(XIN)	XIN input HIGH pulse width	40		ns
tWL(XIN)	XIN input LOW pulse width	40		ns

Table 5.17 CNTR0 input, CNTR1 input, INT2 input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	300		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	120		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	120		ns

Table 5.18 TCIN input, INT3 input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	1200 [1]		ns
tWH(TCIN)	TCIN input HIGH pulse width	600 [2]		ns
tWL(TCIN)	TCIN input LOW pulse width	600 [2]		ns

NOTES
 1 : When using the Timer C capture function, adjust the cycle time above (1/ Timer C count source frequency x 3).
 2 : When using the Timer C capture function, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.19 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	300		ns
tW(CKH)	CLKi input HIGH pulse width	150		ns
tW(CKL)	CLKi input LOW pulse width	150		ns
td(C-Q)	TxDi output delay time		160	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	55		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.20 External interrupt INT0 input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	INT0 input HIGH pulse width	380 [1]		ns
tW(INL)	INT0 input LOW pulse width	380 [2]		ns

NOTES
 1 : When selecting the digital filter by the INT0 input filter select bit, use the INT0 input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
 2 : When selecting the digital filter by the INT0 input filter select bit, use the INT0 input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
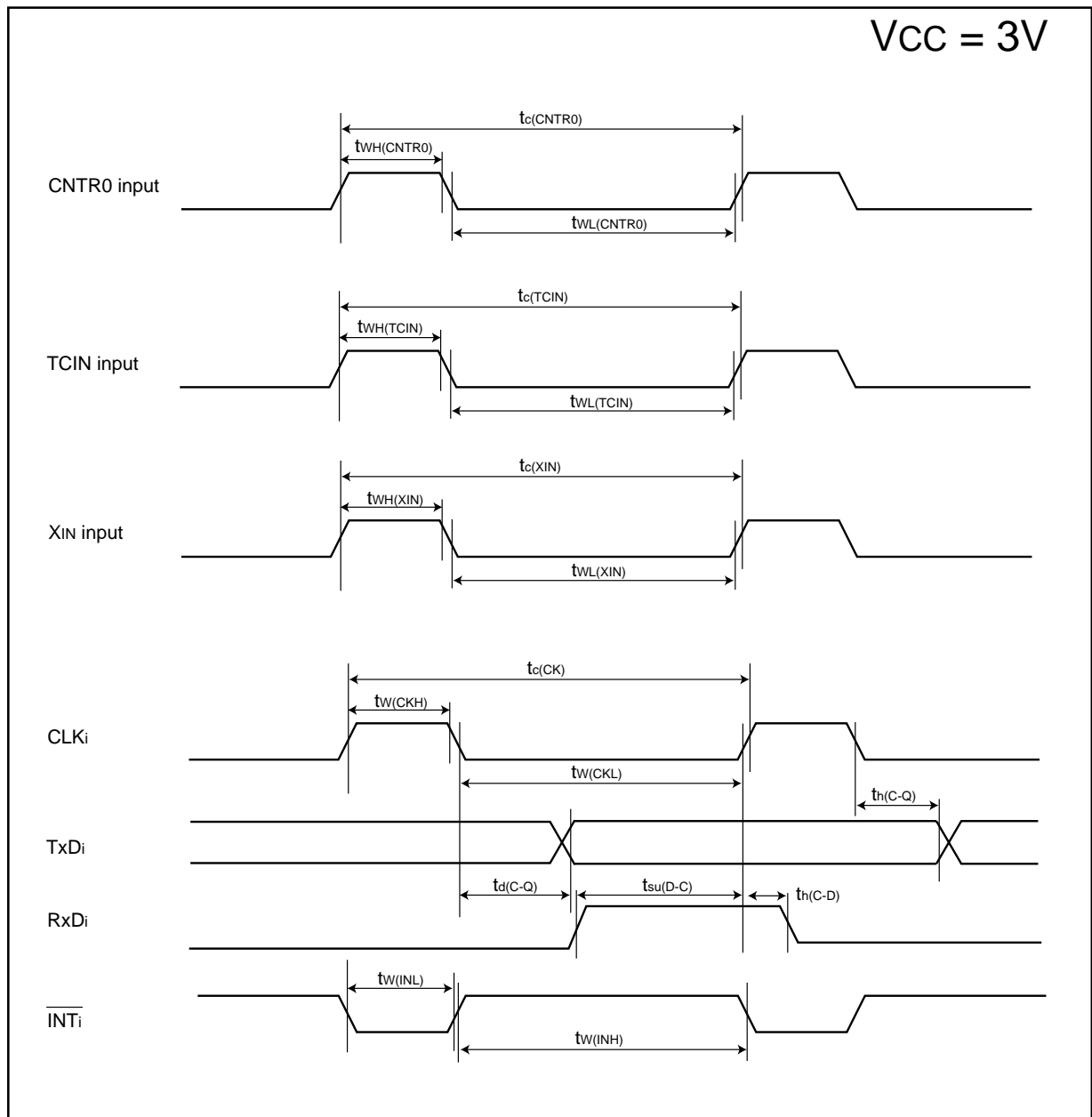
Figure 5.4 Vcc=3V timing diagram

Package Dimensions

32P6U-A

Plastic 32pin 7×7mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-0707-0.80	—		Cu Alloy
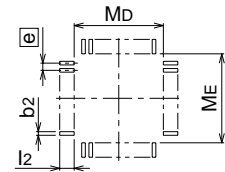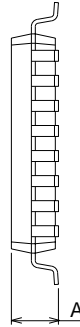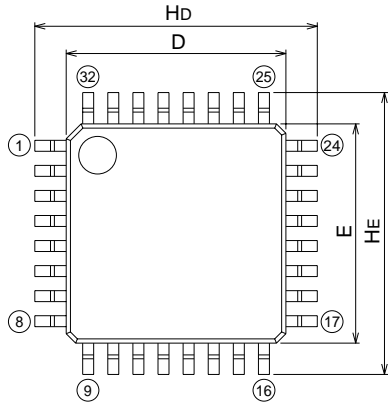
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	—	0.8	—
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.3	0.5	0.7
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.2
y	—	—	0.1
θ	0¡	—	10¡
b2	—	0.5	—
l2	1.0	—	—
MD	—	7.4	—
ME	—	7.4	—

Detail F

RENESAS
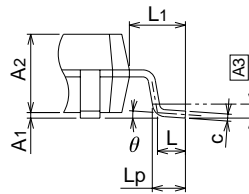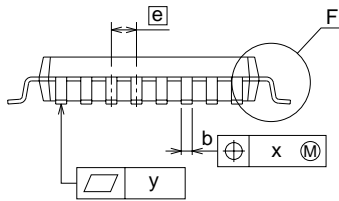
REVISION HISTORY	R8C/12 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Oct 28, 2003		First edition issued
0.20	Dec05, 2003	16	Table 16.5 revised
1.00	Sep30, 2004	All pages	Words standardized (on-chip oscillator, serial interface, A/D)
		2	Table 1.1 revised
		5	Figure 1.3, NOTES 3 added
		6	Table 1.3 revised
		9	Figure 3.1, NOTES added
		10-13	One body sentence in chapter 4 added ; Titles of Table 4.1 to 4.4 added
		12	Table 4.3 revised ; Table 4.4 revised
		14	Table 5.2 revised
		15	Table 5.3 revised
		16	Table 5.4 and 5.5 revised
		17	Table 5.7 revised
		18	Table 5.8 revised
		19	Table 5.13 revised
		21	Table 5.14 revised
		22	Table 5.15 revised
		23	Table 5.17 revised

RENESAS

RENESAS SALES OFFICES   http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001