

## 4-BIT X 16-WORD FIFO REGISTER

## FEATURES

- Independent asynchronous inputs and outputs
- Expandable in either direction
- Reset capability
- Status indicators on inputs and outputs
- 3-state outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT40105 are high-speed Si-gate CMOS devices and are pin compatible with the "40105" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40105 are first-in/first-out (FIFO) "elastic" storage registers that can store sixteen 4-bit words. The "40105" is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems. Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripples through to the output end, the status of the first control flip-flop (data-in ready output - DIR) indicates if the FIFO is full, and the status of the last flip-flop (data-out ready output - DOR) indicates if the FIFO

(continued on next page)

| SYMBOL                                 | PARAMETER  | CONDITIONS                                      | TYPICAL |     | UNIT |
|--|--|---|---------|-----|------|
|  |  |   | HC      | HCT |      |
| t <sub>PHL</sub> /<br>t <sub>PLH</sub> | propagation delay<br>MR to DIR, DOR<br>S $\bar{O}$ to Q <sub>n</sub> | C <sub>L</sub> = 15 pF<br>V <sub>CC</sub> = 5 V | 16      | 15  | ns   |
|  |  |   | 37      | 35  | ns   |
| t <sub>PHL</sub>                       | propagation delay<br>SI to DIR<br>S $\bar{O}$ to DOR                 |   | 16      | 18  | ns   |
|  |  |   | 17      | 18  | ns   |
| f <sub>max</sub>                       | maximum clock frequency  |   | 33      | 31  | MHz  |
| C <sub>I</sub>                         | input capacitance  |   | 3.5     | 3.5 | pF   |
| C <sub>PD</sub>                        | power dissipation<br>capacitance per package                         | notes 1 and 2                                   | 134     | 145 | pF   |

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

C<sub>L</sub> = output load capacitance in pF

f<sub>o</sub> = output frequency in MHz

V<sub>CC</sub> = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

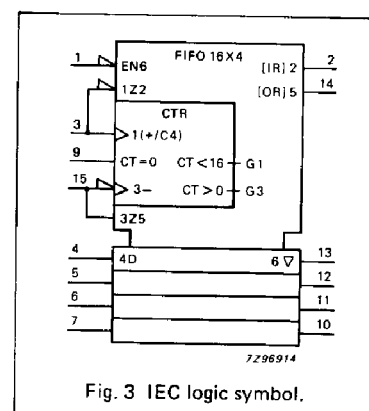
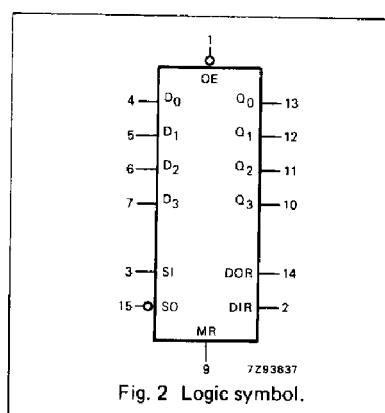
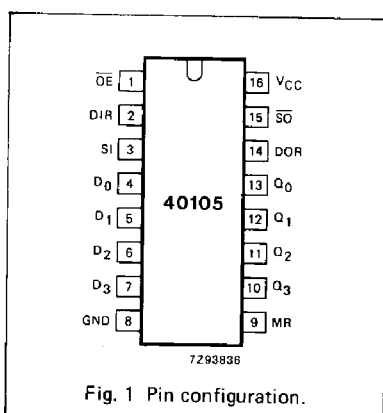
## PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

## PIN DESCRIPTION

| PIN NO.        | SYMBOL                           | NAME AND FUNCTION                             |
|----------------|----------------------------------|---|
| 1              | $\bar{O}E$                       | output enable input (active LOW)              |
| 2              | DIR                              | data-in ready output                          |
| 3              | SI                               | shift-in input (LOW-to-HIGH, edge-triggered)  |
| 4, 5, 6, 7     | D <sub>0</sub> to D <sub>3</sub> | parallel data inputs                          |
| 8              | GND                              | ground (0 V)                                  |
| 9              | MR                               | asynchronous master reset input (active HIGH) |
| 13, 12, 11, 10 | Q <sub>0</sub> to Q <sub>3</sub> | 3-state data outputs                          |
| 14             | DOR                              | data-out ready output                         |
| 15             | S $\bar{O}$                      | shift-out input (HIGH-to-LOW, edge-triggered) |
| 16             | V <sub>CC</sub>                  | positive supply voltage                       |



**GENERAL DESCRIPTION**

contains data. As the earliest data is removed from the bottom of the data stack (output end), all data entered later will automatically ripple toward the output.

**INPUTS AND OUTPUTS****Data inputs (D<sub>0</sub> to D<sub>3</sub>)**

As there is no weighting of the inputs, any input can be assigned as the MSB. The size of the FIFO memory can be reduced from the 4 x 16 configuration, i.e. 3 x 16, down to 1 x 16, by tying unused data input pins to V<sub>CC</sub> or GND.

**Data outputs (Q<sub>0</sub> to Q<sub>3</sub>)**

As there is no weighting of the outputs, any output can be assigned as the MSB. The size of the FIFO memory can be reduced from the 4 x 16 configuration as described for data inputs. In a reduced format, the unused data output pins must be left open circuit.

**Master-reset (MR)**

When MR is HIGH, the control functions within the FIFO are cleared, and data content is declared invalid. The data-in-ready (DIR) flag is set HIGH and the data-out-ready (DOR) flag is set LOW. The output stage remains in the state of the last word that was shifted out, or in the random state existing at power-up.

**Status flag outputs (DIR, DOR)**

Indication of the status of the FIFO is given by two status flags, data-in-ready (DIR) and data-out-ready (DOR):

- DIR = HIGH indicates the input stage is empty and ready to accept valid data;
- DIR = LOW indicates that the FIFO is full or that a previous shift-in operation is not complete (busy);
- DOR = HIGH assures valid data is present at the outputs Q<sub>0</sub> to Q<sub>3</sub> (does not indicate that new data is awaiting transfer into the output stage);
- DOR = LOW indicates the output stage is busy or there is no valid data.

**Shift-in control (SI)**

Data is loaded into the input stage on a LOW-to-HIGH transition of SI. It also triggers an automatic data transfer process (ripple through). If SI is held HIGH during reset, data will be loaded at the falling edge of the MR signal.

**Shift-out control (S<sub>O</sub>)**

A HIGH-to-LOW transition of S<sub>O</sub> causes the DOR flags to go LOW. A HIGH-to-LOW transition of S<sub>O</sub> causes

upstream data to move into the output stage, and empty locations to move towards the input stage (bubble-up).

**Output enable ( $\overline{OE}$ )**

The outputs Q<sub>0</sub> to Q<sub>3</sub> are enabled when  $\overline{OE}$  = LOW. When  $\overline{OE}$  = HIGH the outputs are in the high impedance OFF-state.

**FUNCTIONAL DESCRIPTION****Data input**

Following power-up, the master-reset (MR) input is pulsed HIGH to clear the FIFO memory (see Fig. 8). The data-in-ready flag (DIR = HIGH) indicates that the FIFO input stage is empty and ready to receive data. When DIR is valid (HIGH), data present at D<sub>0</sub> to D<sub>3</sub> can be shifted-in using the SI control input. With SI = HIGH, data is shifted into the input stage and a busy indication is given by DIR going LOW.

The data remains at the first location in the FIFO until DIR is set to HIGH and data moves through the FIFO to the output stage, or to the last empty location. If the FIFO is not full after the SI pulse, DIR again becomes valid (HIGH) to indicate that space is available in the FIFO. The DIR flag remains LOW if the FIFO is full (see Fig. 6). The SI pulse must be made LOW in order to complete the shift-in process.

With the FIFO full, SI can be held HIGH until a shift-out (S<sub>O</sub>) pulse occurs. Then, following a shift-out of data, an empty location appears at the FIFO input and DIR goes HIGH to allow the next data to be shifted-in. This remains at the first FIFO location until SI goes LOW (see Fig. 7).

**Data transfer**

After data has been transferred from the input stage of the FIFO following SI = LOW, data moves through the FIFO asynchronously and is stacked at the output end of the register. Empty locations appear at the input end of the FIFO as data moves through the device.

**Data output**

The data-out-ready flag (DOR = HIGH) indicates that there is valid data at the output (Q<sub>0</sub> to Q<sub>3</sub>). The initial master-reset at power-on (MR = HIGH) sets DOR to LOW (see Fig. 8). After MR = LOW, data shifted into the FIFO moves through to the output stage causing DOR to go HIGH. As the DOR flag goes HIGH, data can be shifted-out using the S<sub>O</sub> control input. With S<sub>O</sub> = HIGH, data in the output stage is shifted out and a busy indication is given by DOR going LOW. When S<sub>O</sub> is made LOW, data moves through the FIFO

to fill the output stage and an empty location appears at the input stage. When the output stage is filled DOR goes HIGH, but if the last of the valid data has been shifted-out leaving the FIFO empty the DOR flag remains LOW (see Fig. 9). With the FIFO empty, the last word that was shifted-out is latched at the output Q<sub>0</sub> to Q<sub>3</sub>.

With the FIFO empty, the S<sub>O</sub> input can be held HIGH until the SI control input is used. Following an SI pulse, data moves through the FIFO to the output stage, resulting in the DOR flag pulsing HIGH and as shift-out of data occurring. The S<sub>O</sub> control must be made LOW before additional data can be shifted-out (see Fig. 10).

**High-speed burst mode**

If it is assumed that the shift-in/shift-out pulses are not applied until the respective status flags are valid, it follows that the shift-in/shift-out rates are determined by the status flags. However, without the status flags a high-speed burst mode can be implemented. In this mode, the burst-in/burst-out rates are determined by the pulse widths of the shift-in/shift-out inputs and burst rates of 35 MHz can be obtained. Shift pulses can be applied without regard to the status flags but shift-in pulses that would overflow the storage capacity of the FIFO are not allowed (see Figs 11 and 12).

**Expanded format**

With the addition of a logic gate, the FIFO is easily expanded to increase word length (see Fig. 17). The basic operation and timing are identical to a single FIFO, with the exception of an additional gate delay on the flag outputs. If during application, the following occurs:

- SI is held HIGH when the FIFO is empty, some additional logic is required to produce a composite DIR pulse (see Figs 7 and 18).

Due to the part-to-part spread of the ripple through time, the SI signals of FIFO<sub>A</sub> and FIFO<sub>B</sub> will not always coincide and the AND-gate will not produce a composite flag signal. The solution is given in Fig. 18.

The "40105" is easily cascaded to increase the word capacity and no external components are needed. In the cascaded configuration, all necessary communications and timing are performed by the FIFOs. The intercommunication speed is determined by the minimum flag pulse widths and the flag delays. The data rate of cascaded devices is typically 25 MHz. Word-capacity can be expanded to and beyond 32-words x 4-bits (see Fig. 19).

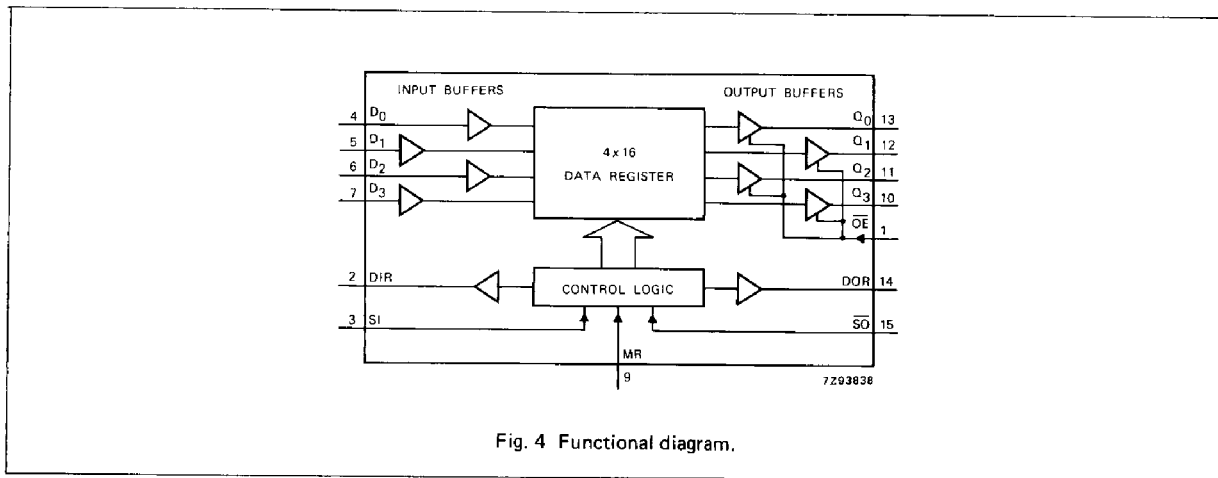


Fig. 4 Functional diagram.

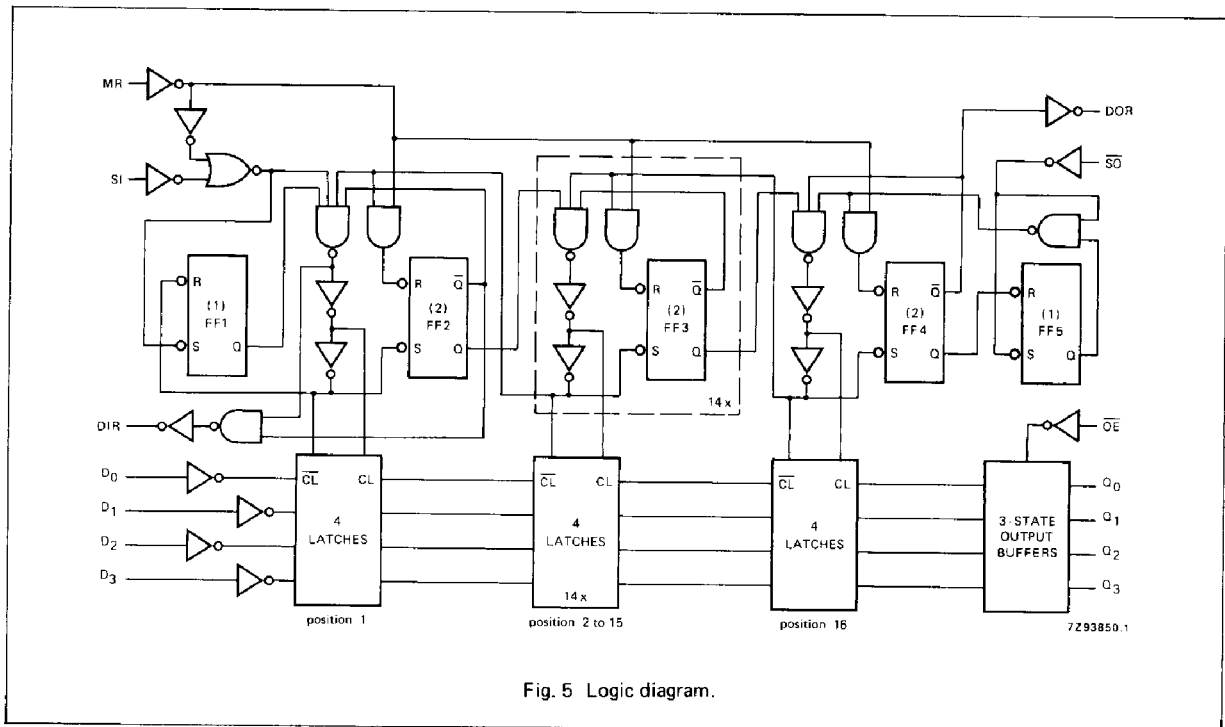


Fig. 5 Logic diagram.

**Notes to Fig. 5**

(see control flip-flops)

- (1) LOW on  $\bar{S}$  input of FF1 and FF5 will set Q output to HIGH independent of state on  $\bar{R}$  input.
- (2) LOW on  $\bar{R}$  input of FF2, FF3 and FF4 will set Q output to LOW independent of state on  $\bar{S}$  input.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications."

Output capability: standard

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                                 | PARAMETER   | T <sub>amb</sub> (°C) |                   |                    |                 |                    |                 | UNIT               | TEST CONDITIONS      |                   |         |
|--|---|-----------------------|-------------------|--------------------|-----------------|--------------------|-----------------|--------------------|----------------------|-------------------|---------|
|  |   | 74HC                  |                   |                    |                 |                    |                 |                    | V <sub>CC</sub><br>V | WAVEFORMS         |         |
|  |   | +25                   |                   |                    | -40 to +85      |                    | -40 to +125     |                    |                      |                   |         |
|  |   | min.                  | typ.              | max.               | min.            | max.               | min.            |                    |                      |                   | max.    |
| t <sub>PHL</sub> /<br>t <sub>PLH</sub> | propagation delay<br>MR to DIR, DOR                     |                       | 52<br>19<br>15    | 175<br>35<br>30    |                 | 220<br>44<br>37    |                 | 265<br>53<br>45    | ns                   | 2.0<br>4.5<br>6.0 | Fig. 8  |
| t <sub>PHL</sub>                       | propagation delay<br>SI to DIR                          |                       | 52<br>19<br>15    | 210<br>42<br>36    |                 | 265<br>53<br>45    |                 | 315<br>63<br>54    | ns                   | 2.0<br>4.5<br>6.0 | Fig. 6  |
| t <sub>PHL</sub>                       | propagation delay<br>SO to DOR                          |                       | 55<br>20<br>16    | 210<br>42<br>36    |                 | 265<br>53<br>45    |                 | 315<br>63<br>54    | ns                   | 2.0<br>4.5<br>6.0 | Fig. 9  |
| t <sub>PHL</sub> /<br>t <sub>PLH</sub> | propagation delay<br>SO to Q <sub>n</sub>               |                       | 116<br>42<br>34   | 400<br>80<br>68    |                 | 500<br>100<br>85   |                 | 600<br>120<br>102  | ns                   | 2.0<br>4.5<br>6.0 | Fig. 14 |
| t <sub>PLH</sub>                       | propagation delay/<br>ripple through delay<br>SI to DOR |                       | 564<br>205<br>165 | 2000<br>400<br>340 |                 | 2500<br>500<br>425 |                 | 3000<br>600<br>510 | ns                   | 2.0<br>4.5<br>6.0 | Fig. 10 |
| t <sub>PLH</sub>                       | propagation delay/<br>bubble-up delay<br>SO to DIR      |                       | 701<br>255<br>204 | 2500<br>500<br>425 |                 | 3125<br>625<br>532 |                 | 3750<br>750<br>638 | ns                   | 2.0<br>4.5<br>6.0 | Fig. 7  |
| t <sub>PZH</sub> /<br>t <sub>PZL</sub> | 3-state output enable time<br>OE to Q <sub>n</sub>      |                       | 41<br>15<br>12    | 150<br>30<br>26    |                 | 190<br>38<br>33    |                 | 225<br>45<br>38    | ns                   | 2.0<br>4.5<br>6.0 | Fig. 16 |
| t <sub>PHZ</sub> /<br>t <sub>PLZ</sub> | 3-state output disable time<br>OE to Q <sub>n</sub>     |                       | 41<br>15<br>12    | 140<br>28<br>24    |                 | 175<br>35<br>30    |                 | 210<br>42<br>36    | ns                   | 2.0<br>4.5<br>6.0 | Fig. 16 |
| t <sub>THL</sub> /<br>t <sub>TLH</sub> | output transition time                                  |                       | 19<br>7<br>6      | 75<br>15<br>13     |                 | 95<br>19<br>16     |                 | 110<br>22<br>19    | ns                   | 2.0<br>4.5<br>6.0 | Fig. 14 |
| t <sub>w</sub>                         | SI pulse width<br>HIGH or LOW                           | 80<br>16<br>14        | 19<br>7<br>6      |                    | 100<br>20<br>17 |                    | 120<br>24<br>20 |                    | ns                   | 2.0<br>4.5<br>6.0 | Fig. 6  |
| t <sub>w</sub>                         | SO pulse width<br>HIGH or LOW                           | 120<br>24<br>20       | 39<br>14<br>11    |                    | 150<br>30<br>26 |                    | 180<br>36<br>31 |                    | ns                   | 2.0<br>4.5<br>6.0 | Fig. 9  |
| t <sub>w</sub>                         | DIR pulse width<br>HIGH                                 | 12<br>6<br>5          | 58<br>21<br>17    | 180<br>36<br>31    | 10<br>5<br>4    | 225<br>45<br>38    | 10<br>5<br>4    | 270<br>54<br>46    | ns                   | 2.0<br>4.5<br>6.0 | Fig. 7  |
| t <sub>w</sub>                         | DOR pulse width<br>LOW                                  | 12<br>6<br>5          | 55<br>20<br>16    | 170<br>34<br>29    | 10<br>5<br>4    | 215<br>43<br>37    | 10<br>5<br>4    | 255<br>51<br>43    | ns                   | 2.0<br>4.5<br>6.0 | Fig. 9  |

## AC CHARACTERISTICS FOR 74HC (Cont'd)

| SYMBOL           | PARAMETER  | T <sub>amb</sub> (°C) |                   |      |                 |      |                 | UNIT | TEST CONDITIONS      |                   |                      |
|------------------|--|-----------------------|-------------------|------|-----------------|------|-----------------|------|----------------------|-------------------|----------------------|
|                  |  | 74HC                  |                   |      |                 |      |                 |      | V <sub>CC</sub><br>V | WAVEFORMS         |                      |
|                  |  | +25                   |                   |      | -40 to +85      |      | -40 to +125     |      |                      |                   |                      |
|                  |  | min.                  | typ.              | max. | min.            | max. | min.            |      |                      |                   | max.                 |
| t <sub>w</sub>   | MR pulse width<br>HIGH   | 80<br>16<br>14        | 22<br>8<br>6      |      | 100<br>20<br>17 |      | 120<br>24<br>20 |      | ns                   | 2.0<br>4.5<br>6.0 | Fig. 8               |
| t <sub>rem</sub> | removal time<br>MR to SI                                       | 50<br>10<br>9         | 14<br>5<br>4      |      | 65<br>13<br>11  |      | 75<br>15<br>13  |      | ns                   | 2.0<br>4.5<br>6.0 | Fig. 15              |
| t <sub>su</sub>  | set-up time<br>D <sub>n</sub> to SI                            | -5<br>-5<br>-5        | -39<br>-14<br>-11 |      | -5<br>-5<br>-5  |      | -5<br>-5<br>-5  |      | ns                   | 2.0<br>4.5<br>6.0 | Fig. 13              |
| t <sub>h</sub>   | hold time<br>D <sub>n</sub> to SI                              | 125<br>25<br>21       | 44<br>16<br>13    |      | 155<br>31<br>26 |      | 190<br>38<br>32 |      | ns                   | 2.0<br>4.5<br>6.0 | Fig. 13              |
| f <sub>max</sub> | maximum pulse frequency<br>SI, SO using flags or<br>burst mode | 3.6<br>18<br>21       | 10<br>30<br>36    |      | 2.8<br>14<br>16 |      | 2.4<br>12<br>14 |      | MHz                  | 2.0<br>4.5<br>6.0 | Figs 6, 9, 11 and 12 |
| f <sub>max</sub> | maximum pulse frequency<br>SI, SO cascaded                     | 3.6<br>18<br>21       | 10<br>30<br>36    |      | 2.8<br>14<br>16 |      | 2.4<br>12<br>14 |      | MHz                  | 2.0<br>4.5<br>6.0 | Figs 6 and 9         |

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT           | UNIT LOAD<br>COEFFICIENT |
|-----------------|--------------------------|
| $\overline{OE}$ | 0.75                     |
| SI              | 0.40                     |
| D <sub>n</sub>  | 0.30                     |
| MR              | 1.50                     |
| SO              | 0.40                     |

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

| SYMBOL            | PARAMETER  | $T_{amb}$ (°C) |      |      |            |      |             |      | UNIT | TEST CONDITIONS |                      |
|-------------------|--|----------------|------|------|------------|------|-------------|------|------|-----------------|----------------------|
|                   |  | 74HCT          |      |      |            |      |             |      |      | $V_{CC}$<br>V   | WAVEFORMS            |
|                   |  | +25            |      |      | -40 to +85 |      | -40 to +125 |      |      |                 |                      |
|                   |  | min.           | typ. | max. | min.       | max. | min.        | max. |      |                 |                      |
| $t_{PHL}/t_{PLH}$ | propagation delay<br>MR to DIR, DOR                            |                | 18   | 35   |            | 44   |             | 53   | ns   | 4.5             | Fig. 8               |
| $t_{PHL}$         | propagation delay<br>SI to DIR                                 |                | 21   | 42   |            | 53   |             | 63   | ns   | 4.5             | Fig. 6               |
| $t_{PHL}$         | propagation delay<br>SO to DOR                                 |                | 20   | 42   |            | 53   |             | 63   | ns   | 4.5             | Fig. 9               |
| $t_{PHL}/t_{PLH}$ | propagation delay<br>SO to $Q_n$                               |                | 40   | 80   |            | 100  |             | 120  | ns   | 4.5             | Fig. 14              |
| $t_{PLH}$         | propagation delay/<br>ripple through delay<br>SI to DOR        |                | 188  | 400  |            | 500  |             | 600  | ns   | 4.5             | Fig. 10              |
| $t_{PLH}$         | propagation delay/<br>bubble-up delay<br>SO to DIR             |                | 244  | 500  |            | 625  |             | 750  | ns   | 4.5             | Fig. 7               |
| $t_{pZH}/t_{pZL}$ | 3-state output enable time<br>$\overline{OE}$ to $Q_n$         |                | 18   | 35   |            | 44   |             | 53   | ns   | 4.5             | Fig. 16              |
| $t_{pHZ}/t_{pLZ}$ | 3-state output disable time<br>$\overline{OE}$ to $Q_n$        |                | 15   | 30   |            | 38   |             | 45   | ns   | 4.5             | Fig. 16              |
| $t_{THL}/t_{TLH}$ | output transition time   |                | 7    | 15   |            | 19   |             | 22   | ns   | 4.5             | Fig. 14              |
| $t_W$             | SI pulse width<br>HIGH or LOW                                  | 16             | 6    |      | 20         |      | 24          |      | ns   | 4.5             | Fig. 6               |
| $t_W$             | SO pulse width<br>HIGH or LOW                                  | 16             | 7    |      | 20         |      | 24          |      | ns   | 4.5             | Fig. 9               |
| $t_W$             | DIR pulse width<br>HIGH or LOW                                 | 6              | 20   | 34   | 5          | 43   | 5           | 51   | ns   | 4.5             | Fig. 7               |
| $t_W$             | DOR pulse width<br>HIGH or LOW                                 | 6              | 19   | 34   | 5          | 43   | 5           | 51   | ns   | 4.5             | Fig. 9               |
| $t_W$             | MR pulse width<br>HIGH   | 16             | 7    |      | 20         |      | 24          |      | ns   | 4.5             | Fig. 8               |
| $t_{rem}$         | removal time<br>MR to SI                                       | 15             | 7    |      | 19         |      | 22          |      | ns   | 4.5             | Fig. 15              |
| $t_{su}$          | set-up time<br>$D_n$ to SI                                     | -5             | -14  |      | -4         |      | -4          |      | ns   | 4.5             | Fig. 13              |
| $t_h$             | hold time<br>$D_n$ to SI                                       | 27             | 16   |      | 34         |      | 41          |      | ns   | 4.5             | Fig. 13              |
| $f_{max}$         | maximum pulse frequency<br>SI, SO using flags or<br>burst mode |                | 28   |      | 12         |      | 10          |      | MHz  | 4.5             | Figs 6, 9, 11 and 12 |
| $f_{max}$         | maximum pulse frequency<br>SI, SO cascaded                     |                | 28   |      | 12         |      | 10          |      | MHz  | 4.5             | Figs 6 and 9         |

AC WAVEFORMS

Shifting in sequence FIFO empty to FIFO full

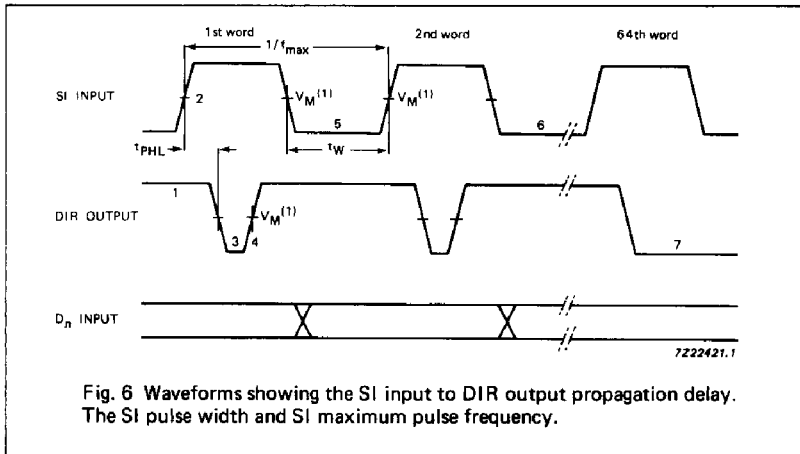


Fig. 6 Waveforms showing the SI input to DIR output propagation delay. The SI pulse width and SI maximum pulse frequency.

Notes to Fig. 6

1. DIR initially HIGH; FIFO is prepared for valid data.
2. SI set HIGH; data loaded into input stage.
3. DIR drops LOW, input stage "busy".
4. DIR goes HIGH, status flag indicates FIFO prepared for additional data; data from first location "ripple through".
5. SI set LOW; necessary to complete shift-in process.
6. Repeat process to load 2nd word through to 16th word into FIFO.
7. DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

With FIFO full; SI held HIGH in anticipation of empty location

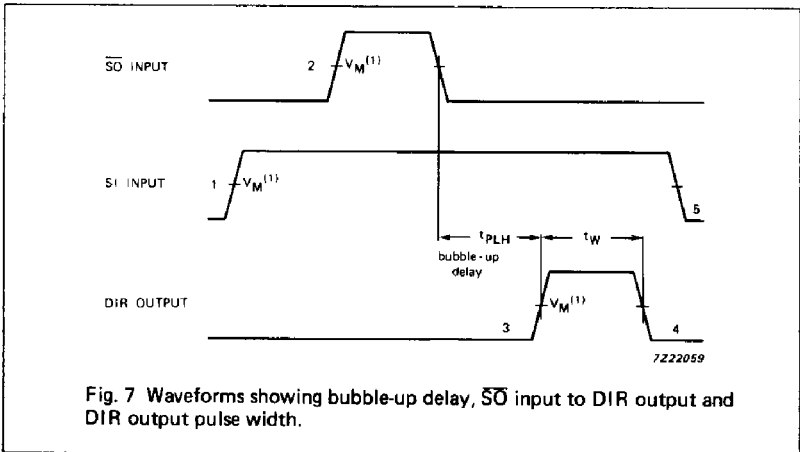


Fig. 7 Waveforms showing bubble-up delay, S0 input to DIR output and DIR output pulse width.

Notes to Fig. 7

1. FIFO is initially, shift-in is held HIGH.
2. S0 pulse; data in the output stage is unloaded, "bubble-up process of empty locations begins".
3. DIR HIGH; when empty location reached input stage, flag indicates FIFO is prepared for data input.
4. DIR returns to LOW; FIFO is full again.
5. SI brought LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full.

AC WAVEFORMS

Master reset applied with FIFO full

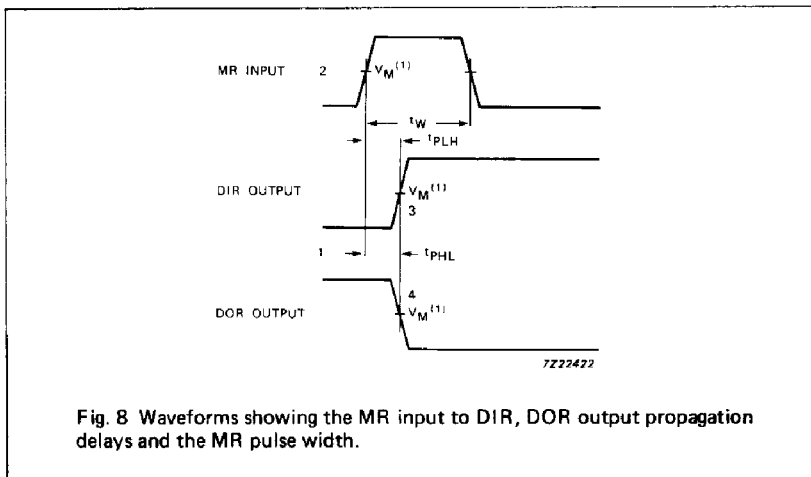


Fig. 8 Waveforms showing the MR input to DIR, DOR output propagation delays and the MR pulse width.

Notes to Fig. 8

1. DIR LOW, output ready HIGH; assume FIFO is full.
2. MR pulse HIGH; clears FIFO.
3. DIR goes HIGH; flag indicates input prepared for valid data.
4. DOR drops LOW; flag indicates FIFO empty.

Shifting out sequence; FIFO full to FIFO empty

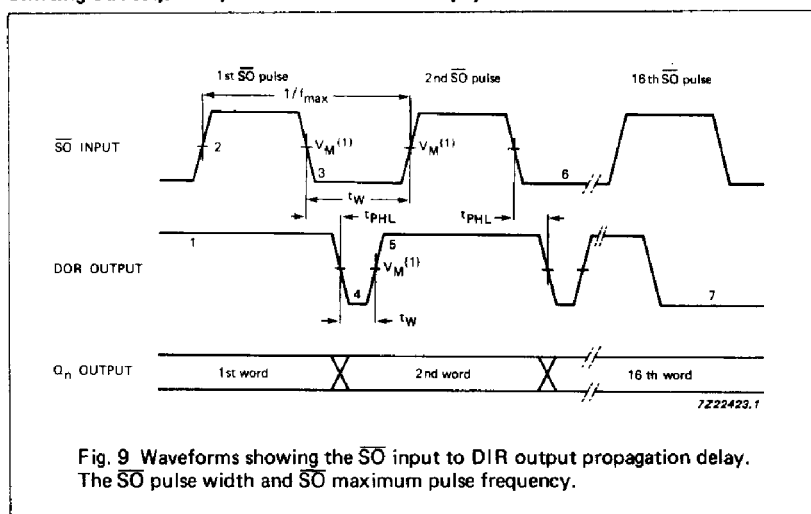


Fig. 9 Waveforms showing the  $\overline{S0}$  input to DIR output propagation delay. The  $\overline{S0}$  pulse width and  $\overline{S0}$  maximum pulse frequency.

Notes to Fig. 9

1. DOR HIGH; no data transfer in progress, valid data is present at output stage.
2.  $\overline{S0}$  set HIGH.
3.  $\overline{S0}$  is set LOW; data in the input stage is unloaded, and new data replaces it as empty location "bubbles-up" to input stage.
4. DOR drops LOW; output stage "busy".
5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay.
6. Repeat process to unload the 3rd through to the 16th word from FIFO.
7. DOR remains LOW; FIFO is empty.



With FIFO empty;  $\overline{S\bar{O}}$  is held HIGH in anticipation

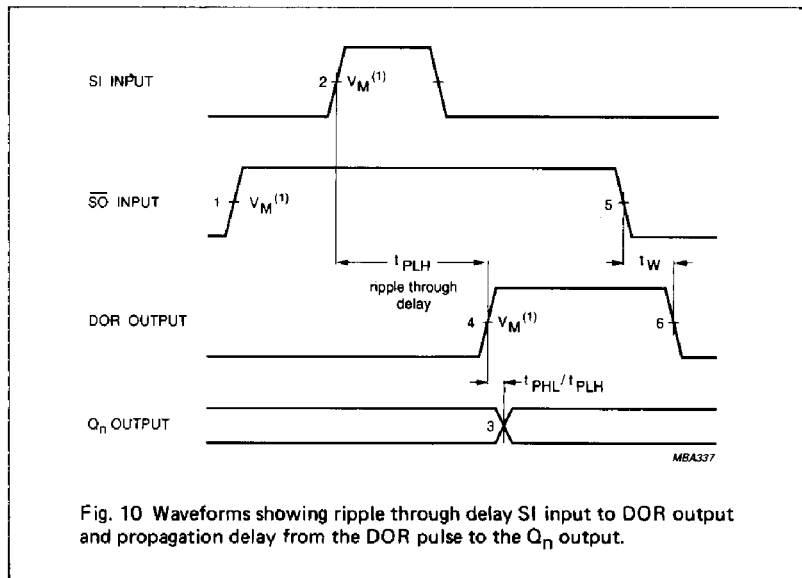


Fig. 10 Waveforms showing ripple through delay SI input to DOR output and propagation delay from the DOR pulse to the  $Q_n$  output.

Notes to Fig. 10

1. FIFO is initially empty,  $\overline{S\bar{O}}$  is held HIGH.
2. SI pulse; loads data into FIFO and initiates ripple through process.
3. DOR flag signals the arrival of valid data at the output stage.
4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the  $Q_n$  output.
5.  $\overline{S\bar{O}}$  set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.
6. DOR goes LOW; FIFO is empty again.

Shift-in operation; high-speed burst mode

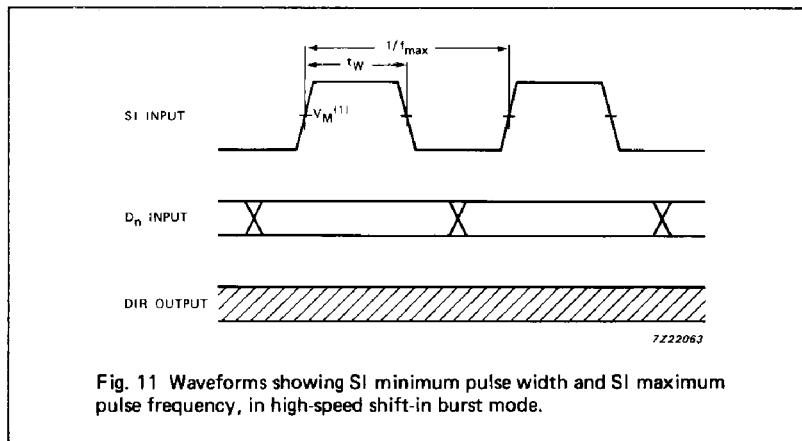


Fig. 11 Waveforms showing SI minimum pulse width and SI maximum pulse frequency, in high-speed shift-in burst mode.

Note to Fig. 11

In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored.

AC WAVEFORMS

Shift-out operation; high-speed burst mode

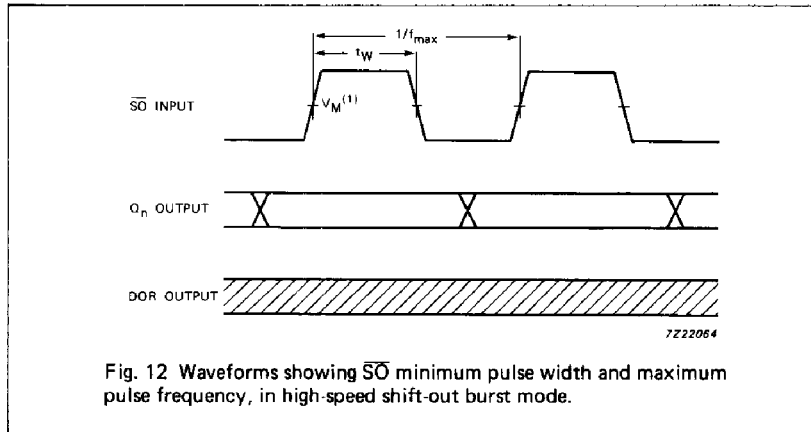


Fig. 12 Waveforms showing  $\overline{S0}$  minimum pulse width and maximum pulse frequency, in high-speed shift-out burst mode.

Note to Fig. 12

In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a don't care condition and a  $\overline{S0}$  pulse can be applied without regard to the flag.

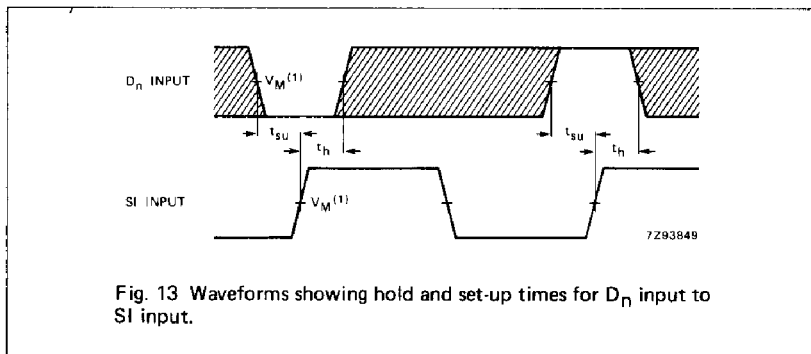


Fig. 13 Waveforms showing hold and set-up times for  $D_n$  input to SI input.

Note to Fig. 13

The shaded areas indicate when the input is permitted to change for predictable output performance.

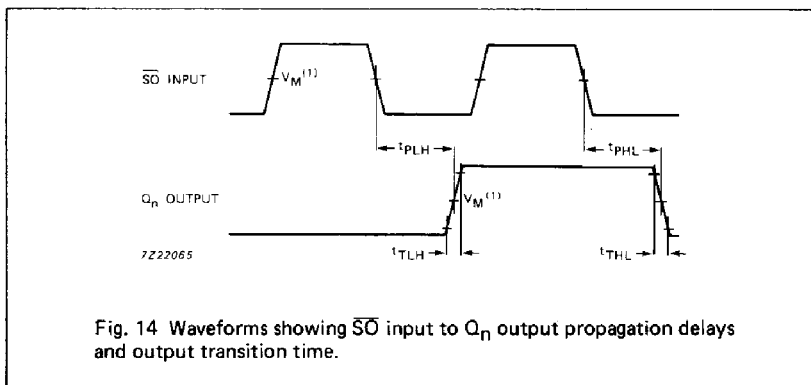


Fig. 14 Waveforms showing  $\overline{S0}$  input to  $Q_n$  output propagation delays and output transition time.

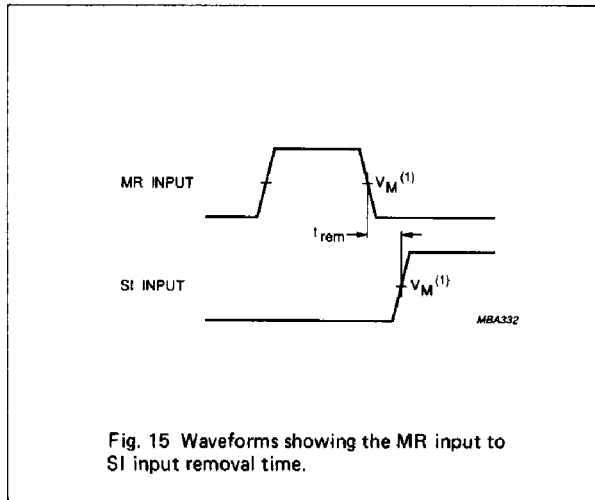


Fig. 15 Waveforms showing the MR input to SI input removal time.

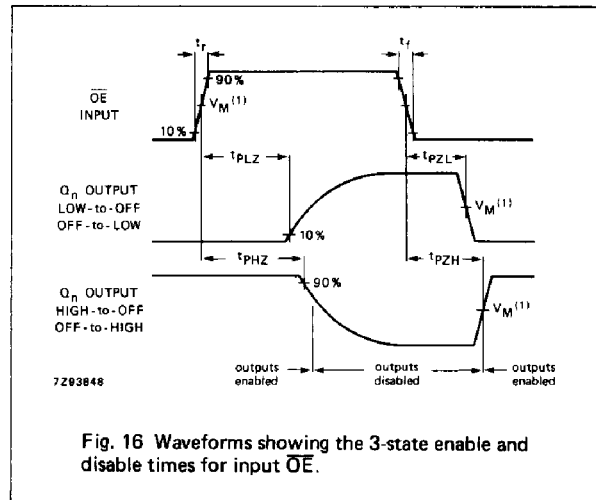


Fig. 16 Waveforms showing the 3-state enable and disable times for input OE.

**Note to AC waveforms**

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

**APPLICATION INFORMATION**

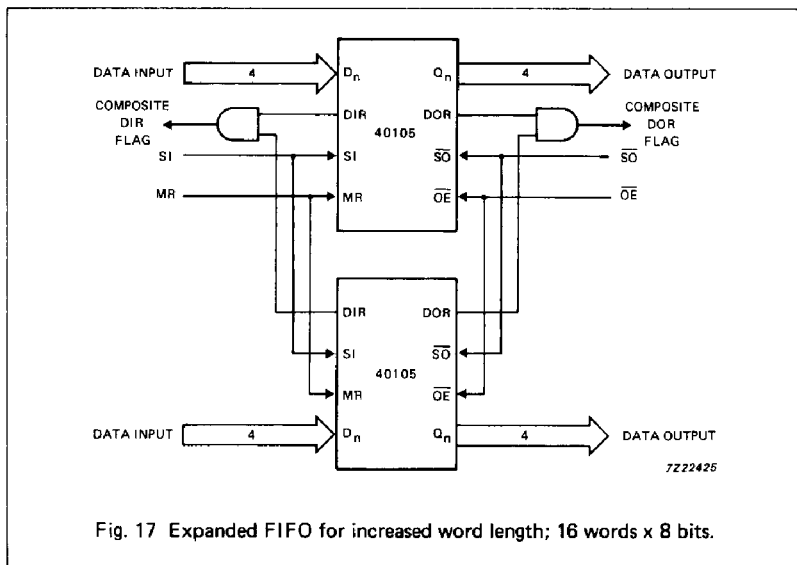


Fig. 17 Expanded FIFO for increased word length; 16 words x 8 bits.

**Note to Fig. 17**

The PC74HC/HCT40105 is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

APPLICATION INFORMATION

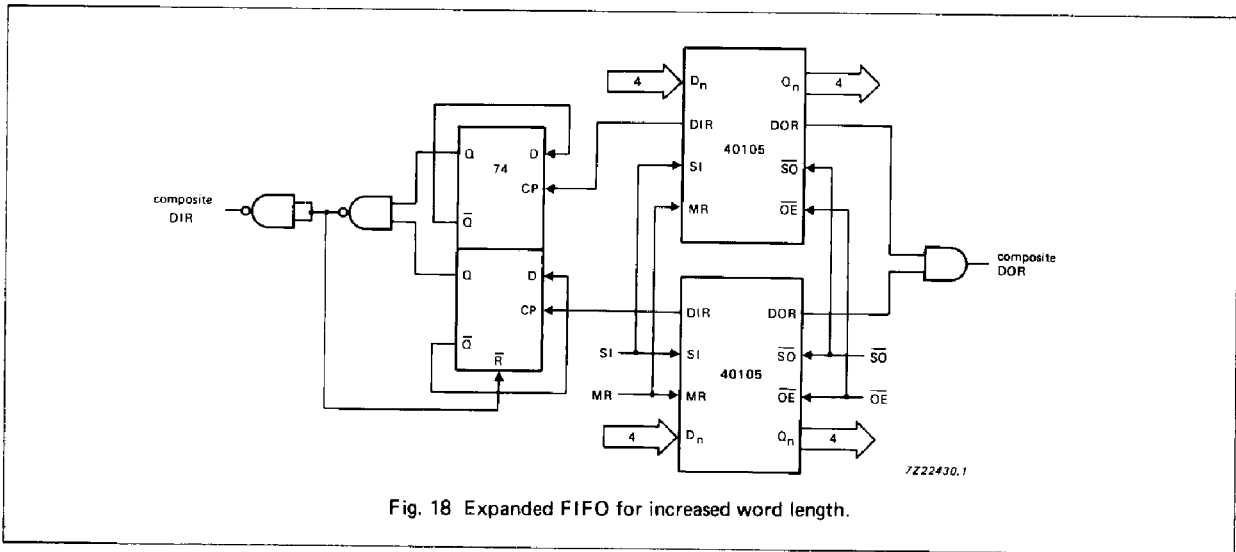


Fig. 18 Expanded FIFO for increased word length.

Note to Fig. 18

This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started (see Fig. 7).

Expanded format

Fig. 19 shows two cascaded FIFOs providing a capacity of 32 words x 4 bits.

Fig. 20 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are initially empty. After a rippled through delay, data arrives at the output of FIFOA. Due to SOA being HIGH, a DORA pulse is generated. The requirements of SIB and DINB are satisfied by the DORA pulse width and the timing between the rising edge of DORA and QnA. After a second ripple through delay, data arrives at the output of FIFOB.

Fig. 21 shows the signals on the nodes of both FIFOs after the application of a SOB pulse, when both FIFOs are initially full. After a bubble-up delay a DIRB pulse is generated, which acts as a SOA pulse for FIFOA. One word is transferred from the output of FIFOA to the input of FIFOB. The requirements of the SOA pulse for FIFOA is satisfied by the pulse width of DORB. After a second bubble-up delay an empty space arrives at DINB, at which time DIRA goes HIGH.

Fig. 22 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.

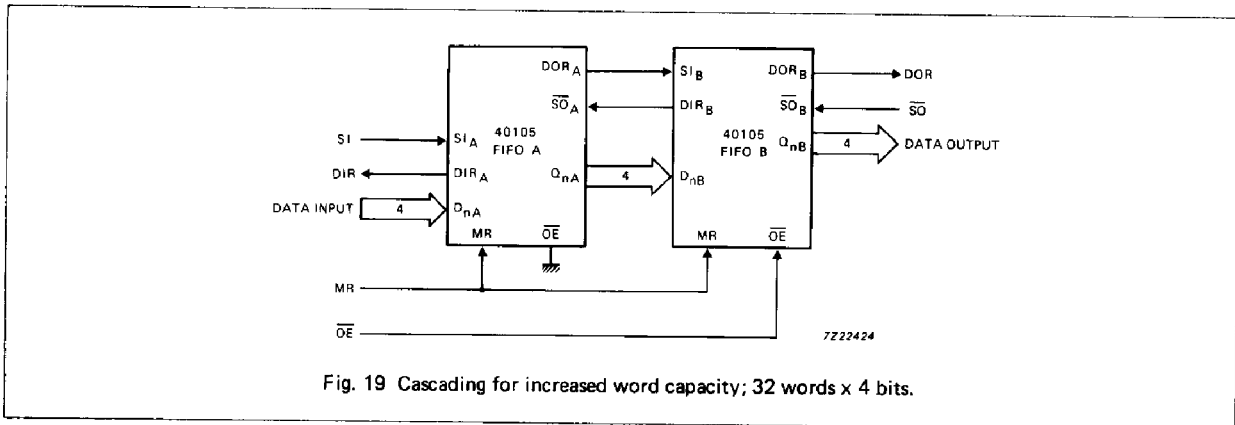


Fig. 19 Cascading for increased word capacity; 32 words x 4 bits.

Note to Fig. 19

The PC74HC/HCT40105 is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figs 17 and 19 demonstrate the intercommunication timing between FIFOA and FIFOB. Fig. 22 gives an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

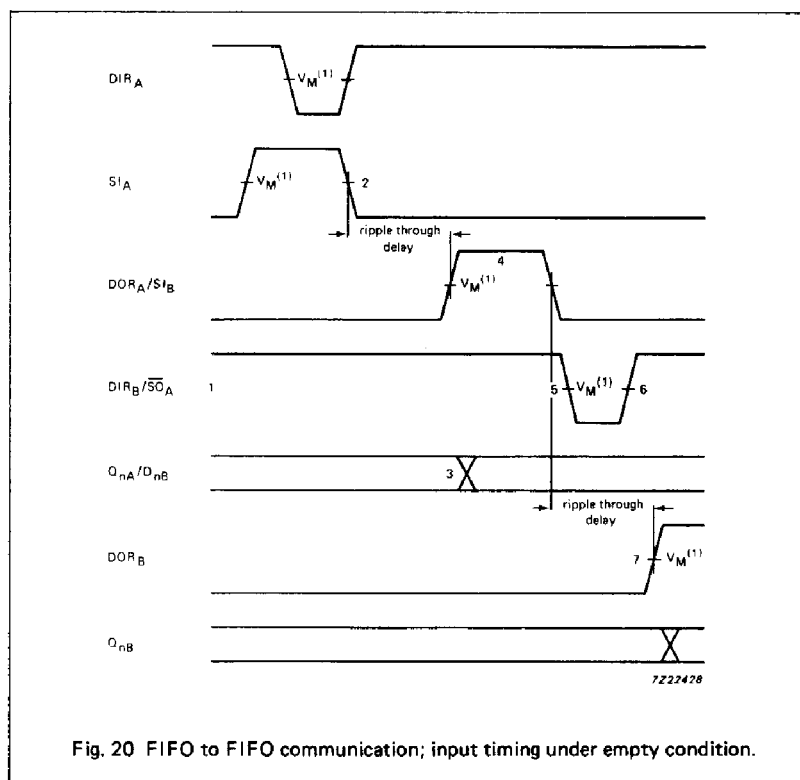


Fig. 20 FIFO to FIFO communication; input timing under empty condition.

**Notes to Fig. 20**

1. FIFO<sub>A</sub> and FIFO<sub>B</sub> initially empty,  $\overline{SO}_A$  held HIGH in anticipation of data.
2. Load one word into FIFO<sub>A</sub>;  $SI$  pulse applied, results in  $DIR$  pulse.
3. Data out <sub>A</sub>/data in <sub>B</sub> transition; valid data arrives at FIFO<sub>A</sub> output stage after a specified delay of the DOR flag, meeting data input set-up requirements of FIFO<sub>B</sub>.
4.  $DOR_A$  and  $SI_B$  pulse HIGH; (ripple through delay after  $SI_A$  LOW) data is unloaded from FIFO<sub>A</sub> as a result of the data output ready pulse, data is shifted into FIFO<sub>B</sub>.
5.  $DIR_B$  and  $\overline{SO}_A$  go LOW; flag indicates input stage of FIFO<sub>B</sub> is busy, shift-out of FIFO<sub>A</sub> is complete.
6.  $DIR_B$  and  $\overline{SO}_A$  go HIGH automatically; the input stage of FIFO<sub>B</sub> is again able to receive data,  $\overline{SO}$  is held HIGH in anticipation of additional data.
7.  $DOR_B$  goes HIGH; (ripple through delay after  $SI_B$  LOW) valid data is present one propagation delay later at the FIFO<sub>B</sub> output stage.

APPLICATION INFORMATION

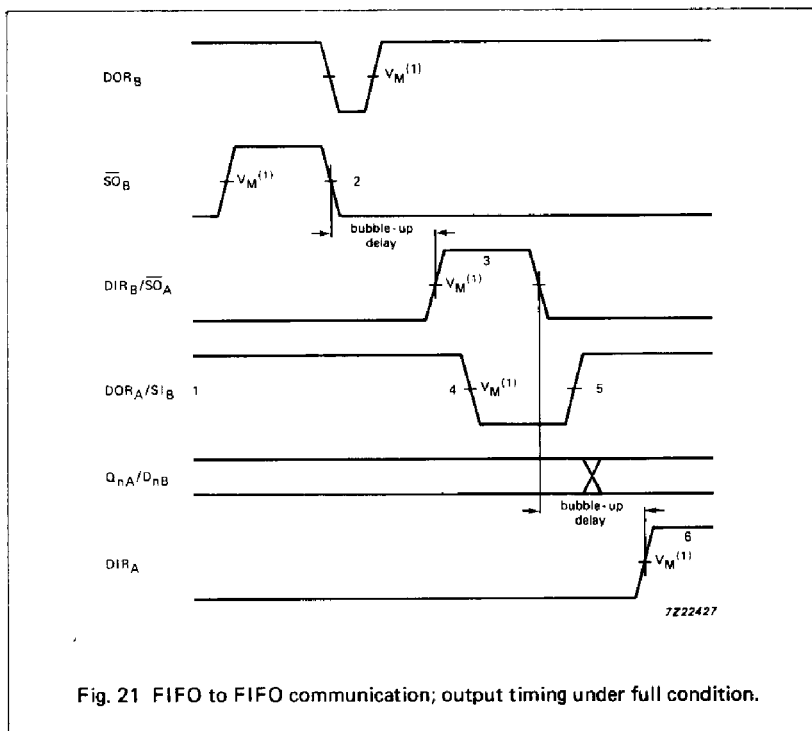


Fig. 21 FIFO to FIFO communication; output timing under full condition.

Notes to Fig. 21

1. FIFO<sub>A</sub> and FIFO<sub>B</sub> initially full, S<sub>I</sub><sub>B</sub> held HIGH in anticipation of shifting in new data as empty location bubbles-up.
2. Unload one word from FIFO<sub>B</sub>; S<sub>O</sub><sub>B</sub> pulse applied, results in DOR pulse.
3. DIR<sub>B</sub> and S<sub>O</sub><sub>A</sub> pulse HIGH; (bubble-up delay after S<sub>O</sub><sub>B</sub> LOW) data is loaded into FIFO<sub>B</sub> as a result of the DIR pulse, data is shifted out of FIFO<sub>A</sub>.
4. DOR<sub>A</sub> and S<sub>I</sub><sub>B</sub> go LOW; flag indicates the output stage of FIFO<sub>A</sub> is busy, shift-in to FIFO<sub>B</sub> is complete.
5. DOR<sub>A</sub> and S<sub>I</sub><sub>B</sub> go HIGH; flag indicates valid data is again available at FIFO<sub>A</sub> output stage, S<sub>I</sub><sub>B</sub> is held HIGH, awaiting bubble-up of empty location.
6. DIR<sub>A</sub> goes HIGH; (bubble-up delay after S<sub>O</sub><sub>A</sub> LOW) an empty location is present at input stage of FIFO<sub>A</sub>.

Note to application waveforms

- (1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.  
 HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

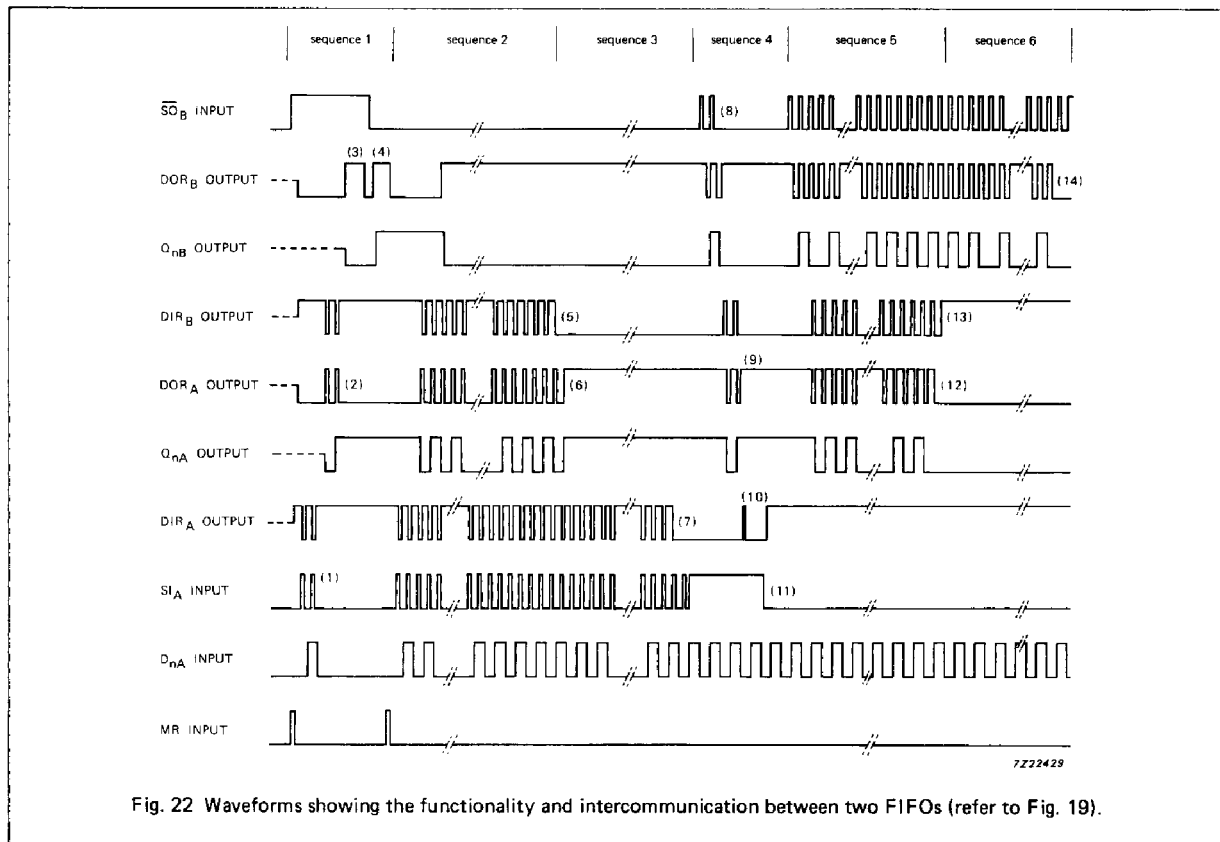


Fig. 22 Waveforms showing the functionality and intercommunication between two FIFOs (refer to Fig. 19).

**Note to Fig. 22**

**Sequence 1 (Both FIFOs empty, starting shift-in process):**

After a MR pulse has been applied FIFO<sub>A</sub> and FIFO<sub>B</sub> are empty. The DOR flags of FIFO<sub>A</sub> and FIFO<sub>B</sub> go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data.  $\overline{S0}_B$  is held HIGH and two  $SIA$  pulses are applied (1). These pulses allow two data words to ripple through to the output stage of FIFO<sub>B</sub> (2). When data arrives at the output of FIFO<sub>B</sub>, a  $DOR_B$  pulse is generated (3). When  $\overline{S0}_B$  goes LOW, the first bit is shifted out and a second bit ripples through to the output after which  $DOR_B$  goes HIGH (4).

**Sequence 2 (FIFO<sub>B</sub> runs full):**

After the MR pulse, a series of 16  $SIA$  pulses are applied. When 16 words are shifted in,  $DIR_B$  remains LOW due to FIFO<sub>B</sub> being full (5).  $DOR_A$  goes LOW due to FIFO<sub>A</sub> being empty.

**Sequence 3 (FIFO<sub>A</sub> runs full):**

When 17 words are shifted in,  $DOR_A$  remains HIGH due to valid data remaining at the output of FIFO<sub>A</sub>.  $Q_{nA}$  remains HIGH, being the polarity of the 17th data word (6). After the 32th  $SIA$  pulse,  $DIR$  remains LOW and both FIFOs are full (7). Additional pulses have no effect.

**Sequence 4 (Both FIFOs full, starting shift-out process):**

$SIA$  is held HIGH and two  $\overline{S0}_B$  pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of FIFO<sub>B</sub>, and proceed to FIFO<sub>A</sub> (9). When the first empty location arrives at the input of FIFO<sub>A</sub>, a  $DIR_A$  pulse is generated (10) and a new word is shifted into FIFO<sub>A</sub>.  $SIA$  is made LOW and now the second empty location reaches the input stage of FIFO<sub>A</sub>, after which  $DIR_A$  remains HIGH (11).

**Sequence 5 (FIFO<sub>A</sub> runs empty):**

At the start of sequence 5 FIFO<sub>A</sub> contains 15 valid words due to two words being shifted out and one word being shifted in in sequence 4. An additional series of  $\overline{S0}_B$  pulses are applied. After 15  $\overline{S0}_B$  pulses, all words from FIFO<sub>A</sub> are shifted into FIFO<sub>B</sub>.  $DOR_A$  remains LOW (12).

**Sequence 6 (FIFO<sub>B</sub> runs empty):**

After the next  $\overline{S0}_B$  pulse,  $DIR_B$  remains HIGH due to the input stage of FIFO<sub>B</sub> being empty (13). After another 15  $\overline{S0}_B$  pulses,  $DOR_B$  remains LOW due to both FIFOs being empty (14). Additional  $\overline{S0}_B$  pulses have no effect. The last word remains available at the output  $Q_n$ .