dsPIC33FJ128GP804 and PIC24HJ128GP504

dsPIC33FJ128GP804 and PIC24HJ128GP504 PIM Information Sheet for Graphics Applications

The dsPIC33FJ128GP804 and PIC24HJ128GP504 Graphics Plug-In-Modules (PIMs) demonstrate the capabilities of the dsPIC33FJ128GP804 Digital Signal Controller (DSC) and the PIC24HJ128GP504 Microcontroller (MCU) using the Explorer 16 Development Board and the PICtail™ Plus Daughter Boards for graphics.

These PIMs support the Microchip Graphics Library with the following PICtail™ Plus boards:

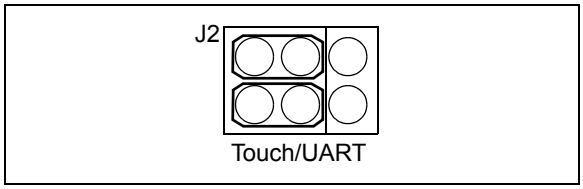
- Graphics LCD Controller PICtail™ Plus SSD1926 Board
- Graphics PICtail™ Plus Daughter Board

In addition, these PIMs also extend parallel port support to the LCD display on the Explorer 16 Development Board.

The pin schematics for the graphics PIMs are different from that of the dsPIC33FJ128GP804 and PIC24HJ128GP504 general purpose PIMs. These graphics PIMs do not support other PICtail™ Plus Daughter Boards such as the Audio PICtail™ Plus Daughter Board and the Thermal/Linear Intelligent Sensor PICtail™ Plus Daughter Board. For additional compatibility details refer the schematics of the respective PICtail™ Plus Daughter Boards.

For a typical application using the TFT with a touch screen, connect pin 2 and pin 3 on jumper J2 to use the touch screen signals for touch sense, as shown in Figure 1.

FIGURE 1: TFT JUMPER SETTING



To use the UART channel to download the image files from PC, connect pin 1 and pin 3 on jumper J2, as shown in Figure 2.

FIGURE 2: UART JUMPER SETTING

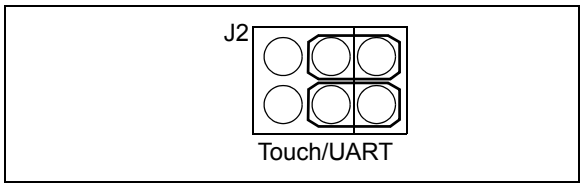


Table 1 provides the mapping of the 44 pins on the device to the 100-pin socket. The schematics for the 100-pin header and 44-pin device are provided in Figure 3 and Figure 4.

TABLE 1: 44-PIN TO 100-PIN PINOUT

Device Pin #	dsPIC33FJ128GP804 and PIC24HJ128GP504	PIM Pin #	Functional Description
1	SDA1/RP9/CN21/PMD3/RB9	99	PMPD3
2	RP22/CN18/PMA1/RC6	43	ALH
3	RP23/CN17/PMA0/RC7	44	ALL
4	RP24/CN20/PMA5/RC8	96	YU
5	RP25/CN19/PMA6/RC9	97	XL
6	VSS	15	Vss
7	VCAP/VDDCORE	85	VDDCORE
8	PGED2/RP10/CN16/PMD2/RB10	98	PMPD2
9	PGEC2/RP11/CN15/PMD1/RB11	94	PMPD1
10	AN12/RP12/CN14/PMD0/RB12	93	PMPD0
11	AN11/RP13/CN13/PMRD/RB13	82	PMPRD
12	TMS/PMA10/RA10	8	POWER
13	TCK/PMA7/RA7	77	WAIT
14	AN10/DAC1LP/RTCC/RP14/ CN12/PMWR/RB14	81	PMPWR
15	AN9/DAC1LN/RP15/CN11/RB15	70	CS
16	AVSS	36	AVSS
17	AVDD	30	AVDD
18	$\overline{\text{MCLR}}$	13	$\overline{\text{MCLR}}$
19	AN0/VREF+/CN2/RA0	79	EEPROM CS
20	AN1/VREF-/CN3/RA1	7	RS
21	PGED1/AN2/C2IN-/RP0/CN4/RB0	27	PGD
22	PGEC1/AN3/C2IN+/RP1/CN5/RB1	26	PGC
23	AN4/C1IN-/RP2/CN6/RB2	34/39(1)	YD/UART_RX(1)
24	AN5/C1IN+/RP3/CN7/RB3	35/50(1)	XR/UART_TX(1)
25	AN6/DAC1RM/RP16/CN8/RC0	12	EEPROM SDO
26	AN7/DAC1LM/RP17/CN9/RC1	11	EEPROM SDI
27	AN8/CVREF/RP18/PMA2/CN10/RC2	10	EEPROM SCK
28	VDD	62	VDD
29	VSS	65	VSS
30	OSC1/CLKI/CN30/RA2	63	OSCI
31	OSC2/CLKO/CN29/RA3	64	OSCO
32	TDO/PMA8/RA8	76	FLASH CS1
33	SOSCI/RP4/CN1/RB4	72	BUZZER
34	SOSCO/T1CK/CN0/RA4	6	RST
35	TDI/PMA9/RA9	71	FLASH CS2
36	RP19/CN28/PMBE/RC3	78	BE
37	RP20/CN25/PMA5/RC4	95	A16
38	RP21/CN26/PMA3/RC5	1	A17
39	VSS	31	VSS
40	VDD	2	VDD
41	PGED3/ASDA1/RP5/CN27/PMD7/RB5	5	PMPD7
42	PGEC3/ASCL1/RP6/CN24/PMD6/RB6	4	PMPD6
43	INT0/RP7/CN23/PMD5/RB7	3	PMPD5
44	SCL1/RP8/CN22/PMD4/RB8	100	PMPD4

Note 1: The pin function is based on the J2 jumper setting (see Figure 1 and Figure 2).

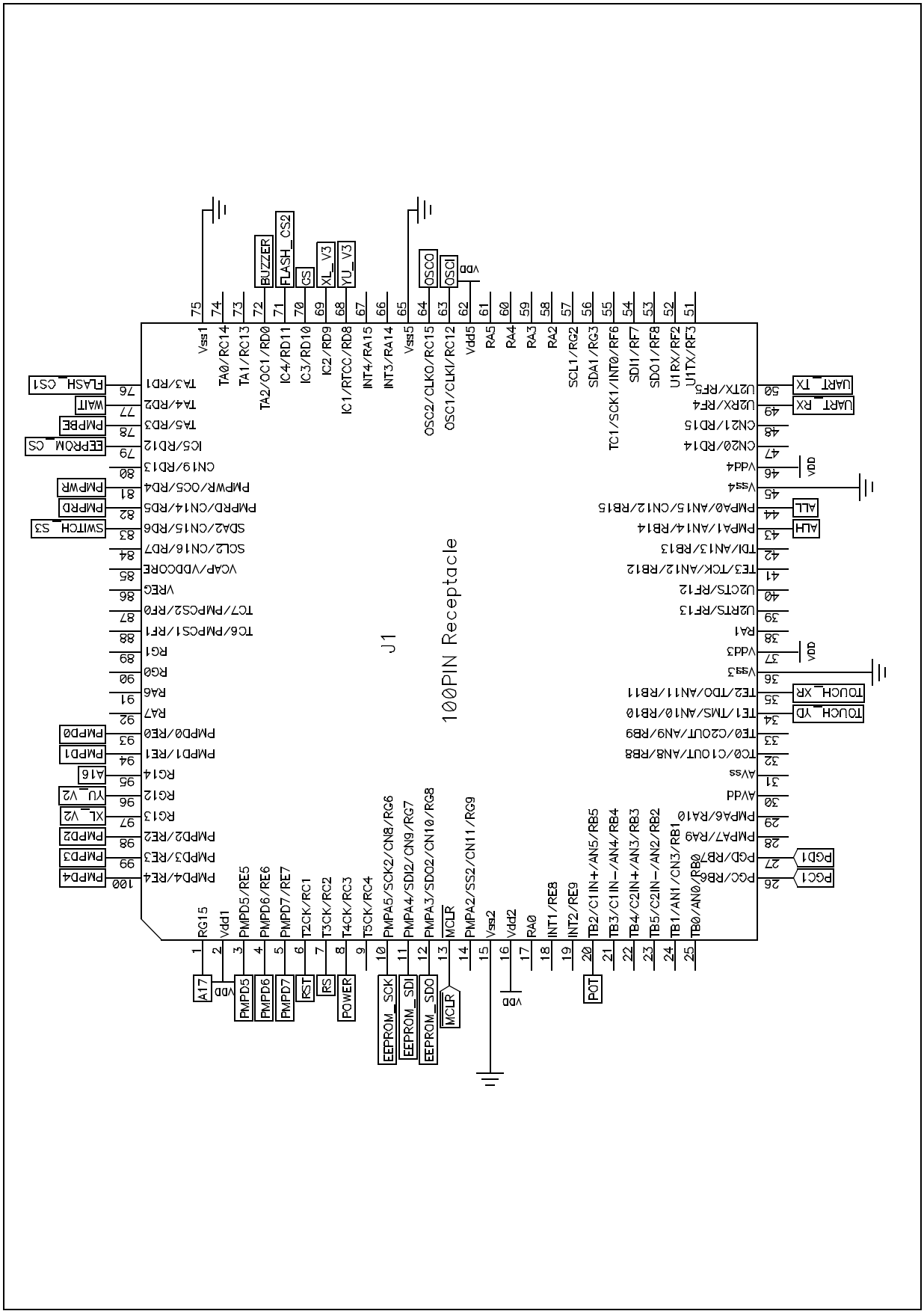


FIGURE 3: 100-PIN HEADER SCHEMATIC

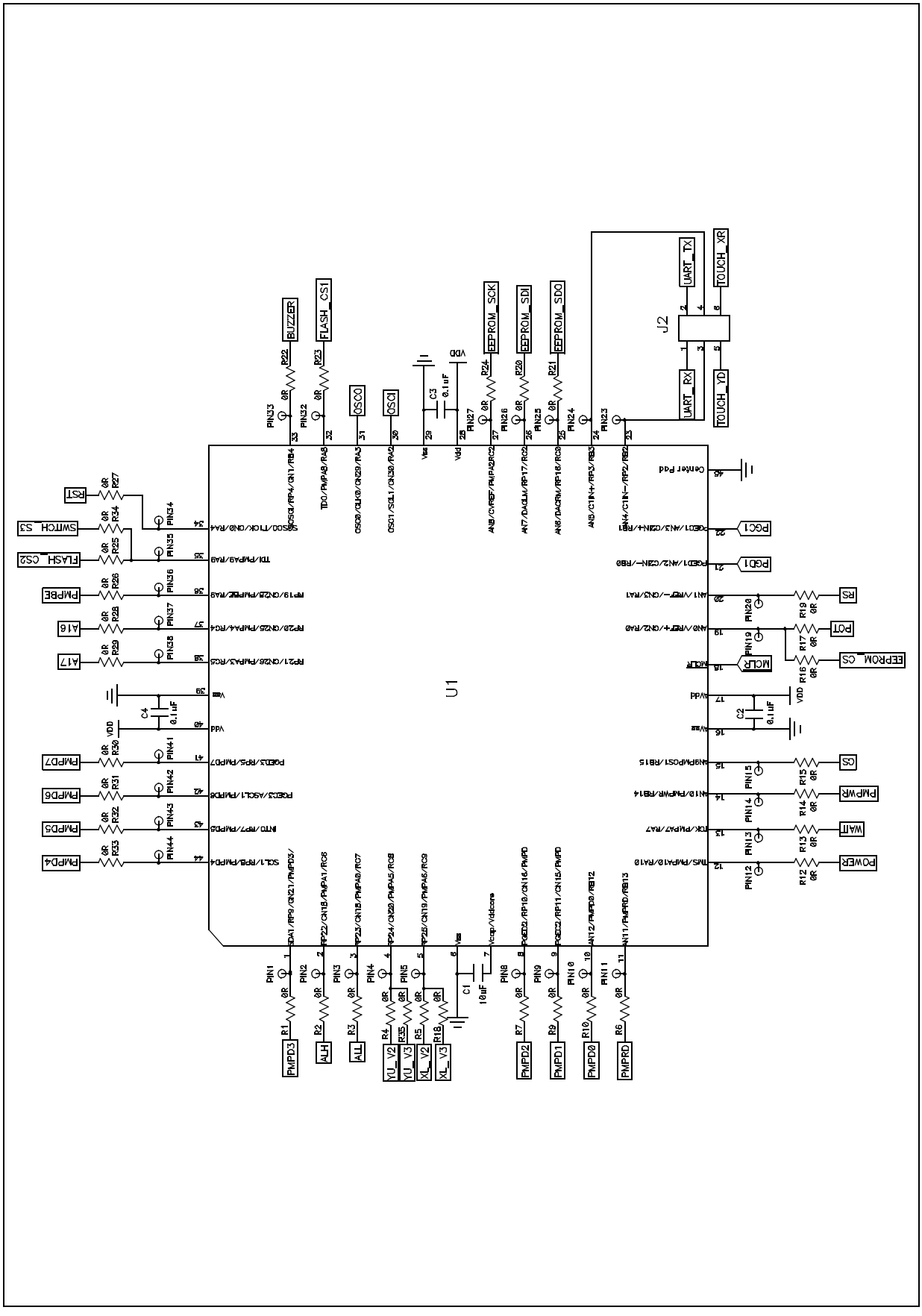


FIGURE 4: 44-PIN DEVICE SCHEMATIC

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