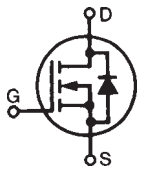
IXYS

Linear L2™ Power MOSFET w/Extended FBSOA

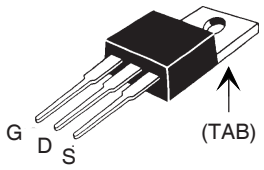
IXTH15N50L2
IXTP15N50L2

V_{DSS} = 500V
I_{D25} = 15A
$R_{DS(on)}$ ≤ 480mΩ

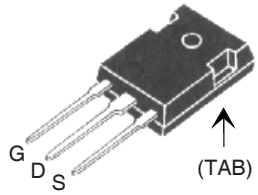
N-Channel Enhancement Mode
Avalanche Rated



TO-220 (IXTP)



TO-247 (IXTH)



G = Gate D = Drain
S = Source TAB = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	500	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	500	V
V_{GSS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	15	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	35	A
I_A	T_C = 25°C	15	A
E_{AS}	T_C = 25°C	750	mJ
P_D	T_C = 25°C	300	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10s	260	°C
M_d	Mounting Torque	1.13/10	Nm/lb.in.
Weight	TO-220	3.0	g
	TO-247	6.0	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250μA	2.5		4.5	V
I_{GSS}	V_{GS} = ± 20V, V_{DS} = 0V			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			25	μA
	T_J = 125°C			200	μA
$R_{DS(on)}$	V_{GS} = 10V, $I_D = 0.5 \bullet I_{D25}$, Note 1			480	mΩ

Features

- Designed for Linear Operation
- International Standard Packages
- Avalanche Rated
- Guaranteed FBSOA at 75°C

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- Solid State Circuit Breakers
- Soft Start Controls
- Linear Amplifiers
- Programmable Loads
- Current Regulators

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 10V, I_D = 0.5 • I_{D25}, Note 1	4.5	6.3	8.0	S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		4080		pF
C_{oss}			265		pF
C_{rss}			68		pF
$t_{d(on)}$	**Resistive Switching Times**		38		ns
t_r	V_{GS} = 10V, 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		73		ns
$t_{d(off)}$	R_G = 10Ω (External)		110		ns
t_f			65		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		123		nC
Q_{gs}			20		nC
Q_{gd}			72		nC
R_{thJC}				0.42	°C/W
R_{thCS}	(TO-220)		0.50		°C/W
	(TO-247)		0.21		°C/W

Safe Operating Area Specification

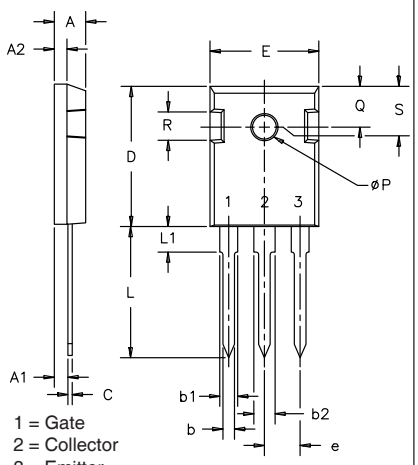
Symbol	Test Conditions	Min.	Typ.	Max.	
SOA	V_{DS} = 400V, I_D = 0.375A, T_C = 75°C, tp = 2s	150			W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			15	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			60	A
V_{SD}	I_F = 15A, V_{GS} = 0V, Note 1			1.5	V
t_{rr}	I_F = 15A, -di/dt = 100A/μs, V_R = 100V, V_{GS} = 0V		570		ns

Note 1: Pulse test, t ≤ 300μs; duty cycle, d ≤ 2%.

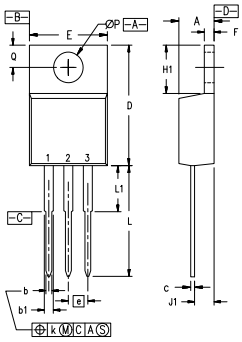
TO-247 (IXTH) AD Outline



1 = Gate
2 = Collector
3 = Emitter
Tab = Collector

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.209	4.7	5.3
A_1	.087	.102	2.2	2.54
A_2	.059	.098	2.2	2.6
b	.040	.055	1.0	1.4
b_1	.065	.084	1.65	2.13
b_2	.113	.123	2.87	3.12
C	.016	.031	.4	.8
D	.819	.845	20.80	21.46
E	.610	.640	15.75	16.26
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1		.177		4.50
øP	.140	.144	3.55	3.65
Q	.212	.244	5.4	6.2
R	.170	.216	4.32	5.49
S	.242 BSC		6.15 BSC	

TO-220 (IXTP) Outline



Pins: 1 - Gate 2 - Drain
3 - Source 4 - Drain

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
øP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

Fig. 1. Output Characteristics @ 25ºC

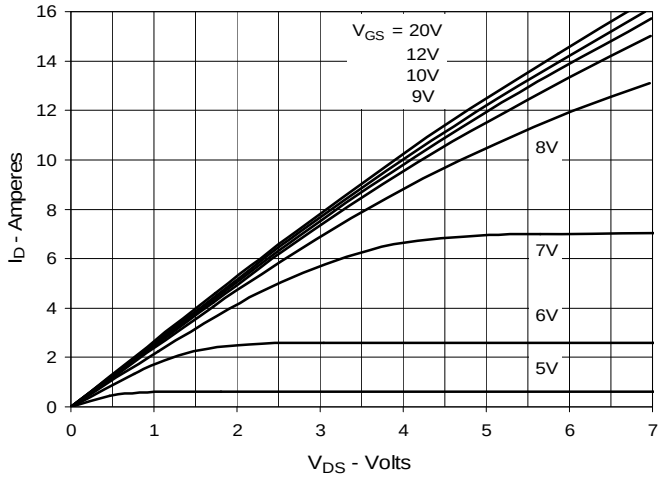


Fig. 2. Extended Output Characteristics @ 25ºC

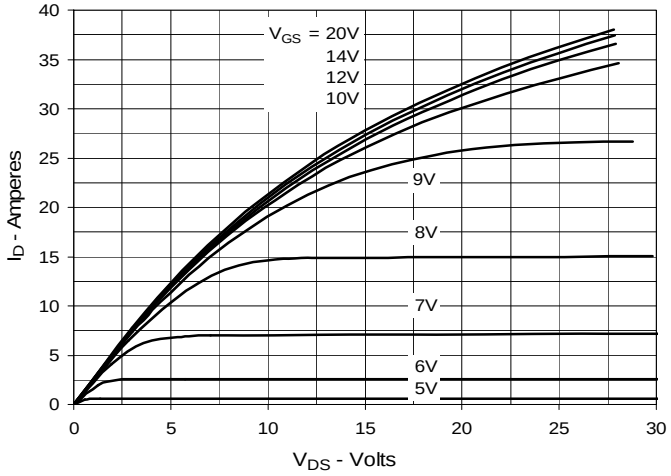


Fig. 3. Output Characteristics @ 125ºC

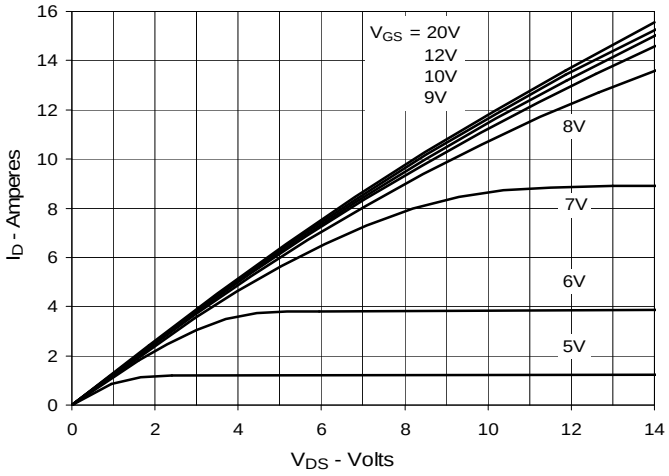


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 7.5A Value vs. Junction Temperature

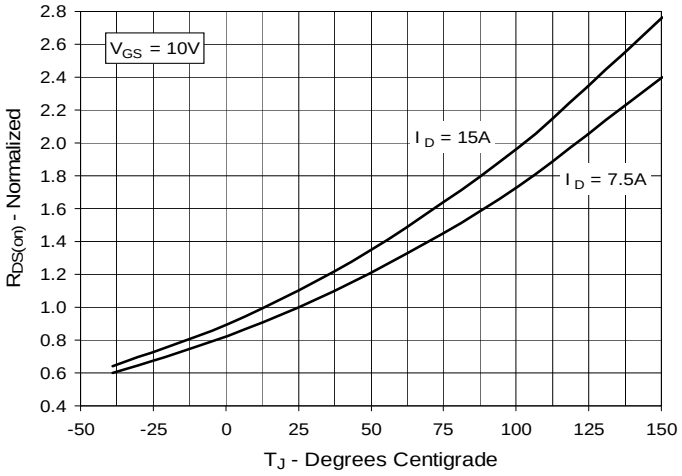


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 7.5A Value vs. Drain Current

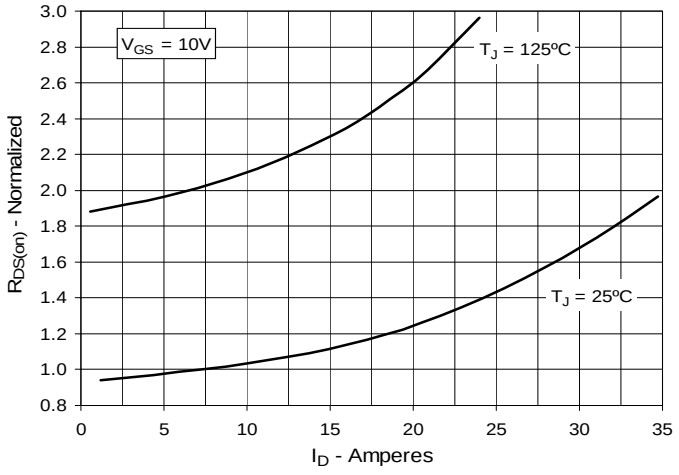


Fig. 6. Maximum Drain Current vs. Case Temperature

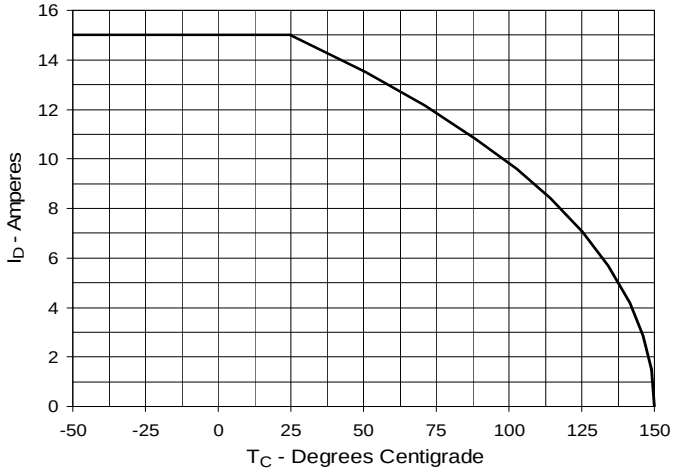


Fig. 7. Input Admittance

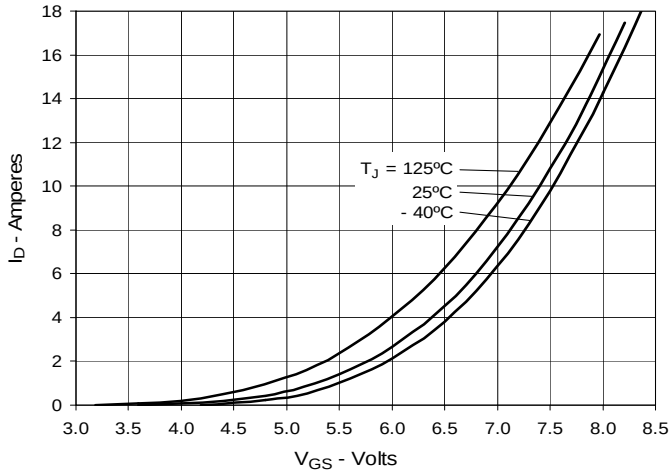


Fig. 8. Transconductance

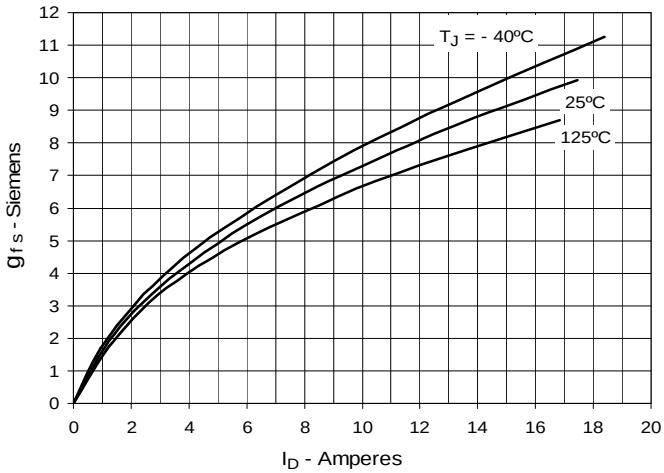


Fig. 9. Forward Voltage Drop of Intrinsic Diode

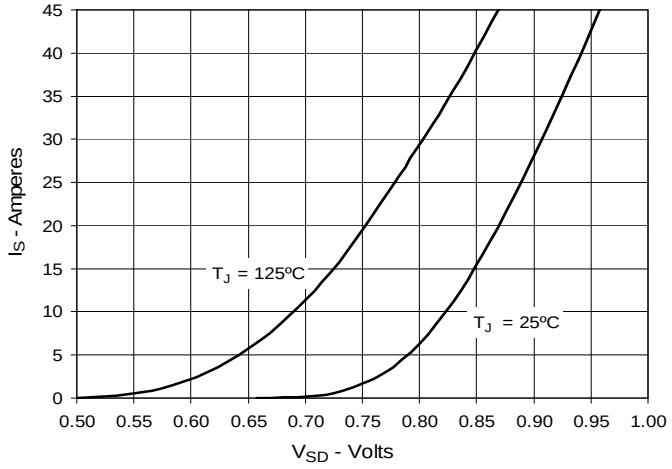


Fig. 10. Gate Charge

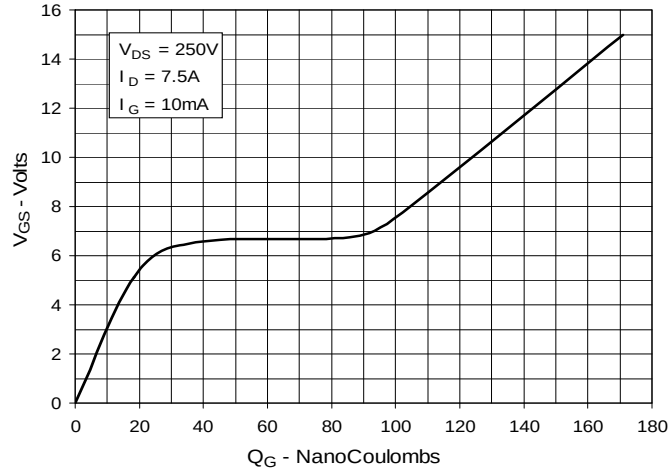


Fig. 11. Capacitance

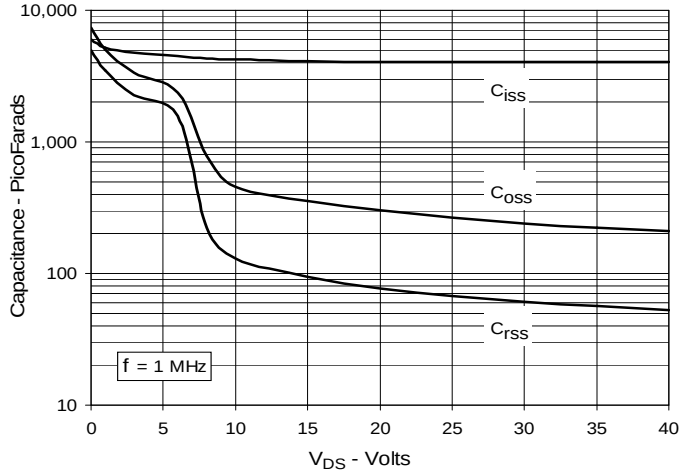


Fig. 12. Maximum Transient Thermal Impedance

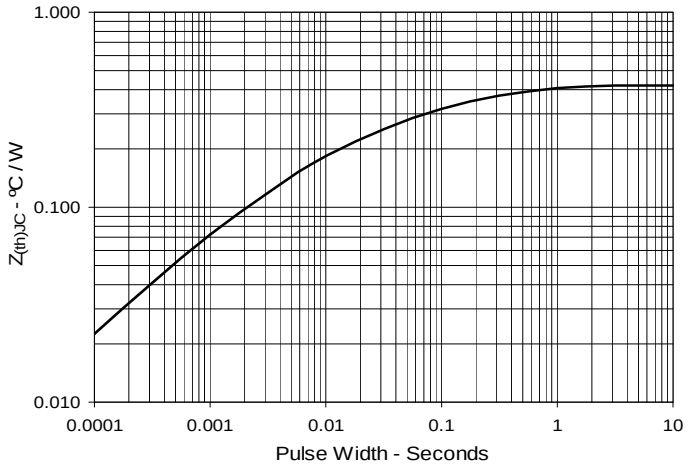


Fig. 13. Forward-Bias Safe Operating Area @ T_C = 25ºC

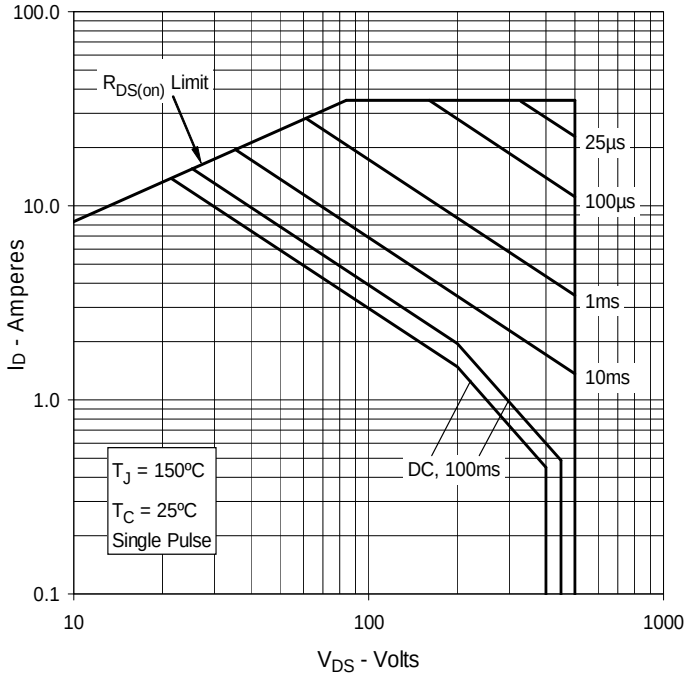


Fig. 14. Forward-Bias Safe Operating Area @ T_C = 75ºC