ACPL-P481/W481

Inverted Logic, High CMR Optocoupler for Intelligent Power Modules and IGBT/MOSFET Gate Drive

Data Sheet

Description

The high-speed ACPL-P481/W481 optocoupler contains a GaAsP LED, photo detector and a Schmitt trigger that eliminates the need for external waveform conditioning circuits.

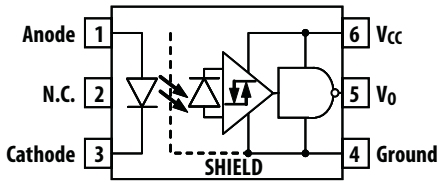
The totem pole output eliminates the need for a pull-up resistor. An Intelligent Power Module, Power MOSFET or IGBT can be driven directly.

Propagation delay difference between devices has been minimized to maximize inverter efficiency through reduced switching dead time.

Applications

- IPM Interface Isolation
- Isolated IGBT/MOSFET Gate Drive
- AC and Brushless DC Motor Drives
- Industrial Inverters
- General Digital Isolation

Functional Diagram



Note: A 0.1 µF bypass capacitor must be connected between pins 4 and 6.

Truth Table (Positive Logic)

LED	V_O
ON	LOW
OFF	HIGH

Features

- Inverted output type (totem pole output)
- Performance Specified for Common IPM Applications Over Industrial Temperature Range.
- Short Maximum Propagation Delays
- Minimized Pulse Width Distortion (PWD)
- Very High Common Mode Rejection (CMR)
- Hysteresis
- Available in Stretched SO-6 Package.
- Package Clearance/Creepage at 8 mm (ACPL-W481)
- Safety Approval: (pending)
  - UL Recognized with 3750 V_{rms} for 1 minute per UL1577.
  - CSA Approved.
  - IEC/EN/DIN EN 60747-5-5 Approved with V_{IORM} = 891 V_{peak} for ACPL-P481 and V_{IORM} = 1140 V_{peak} for ACPL-W481, under option 060.

Specifications

- Wide Operating Temperature Range: –40°C to 100°C.
- Maximum Propagation Delay t_{PHL} / t_{PLH} = 350 ns
- Maximum Pulse Width Distortion (PWD) = 250 ns.
- Propagation Delay Difference: Min. –100 ns, Max. 250 ns
- Wide Operating V_{CC} Range: 4.5 V to 20 V
- 20 kV/µs Minimum Common Mode Rejection (CMR) at V_{CM} = 1000 V.

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

ACPL-P481/W481 is UL recognized with 3750/5000 Vrms for 1 minute respectively per UL 1577.

Part number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-P481 ACPL-W481	-000E	Stretched SO-6	X			100 per tube
	-500E		X	X		1000 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an ordering part number.

Example 1:

ACPL-P481-560E: Stretched SO-6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and RoHS compliant.

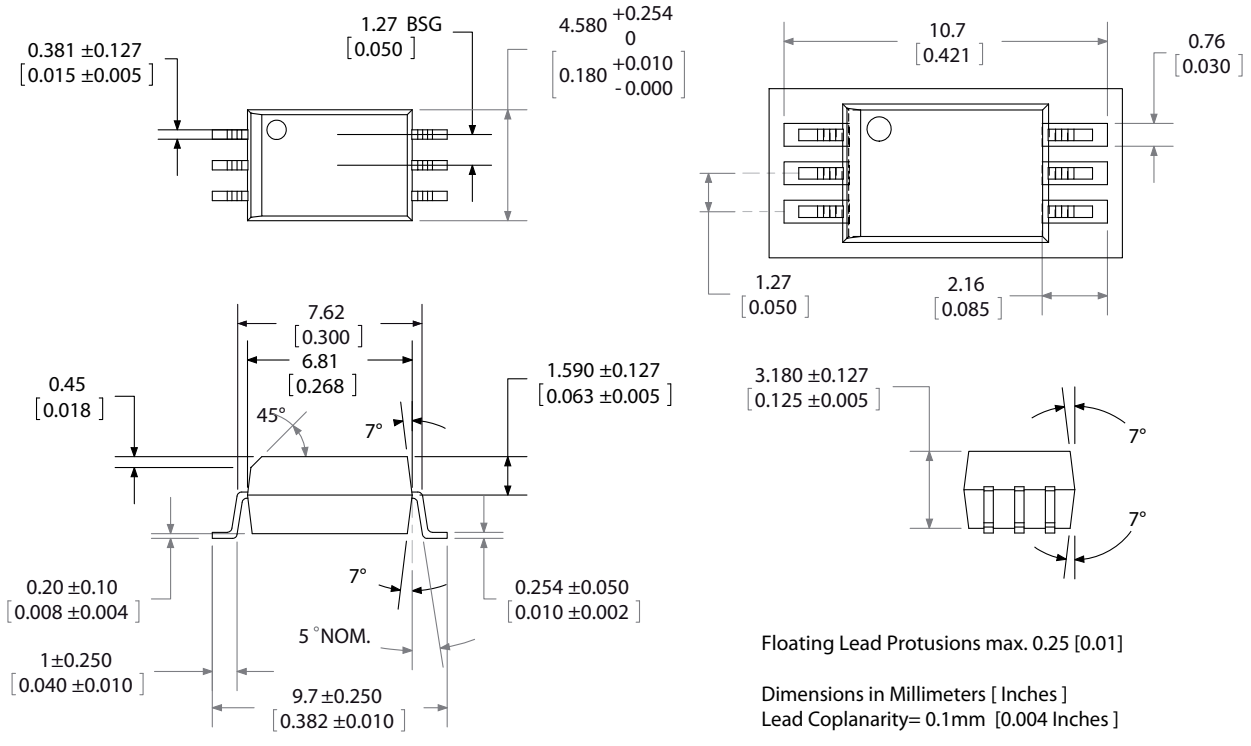
Example 2:

ACPL-P481-000E: Stretched SO-6 Surface Mount package in tube packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

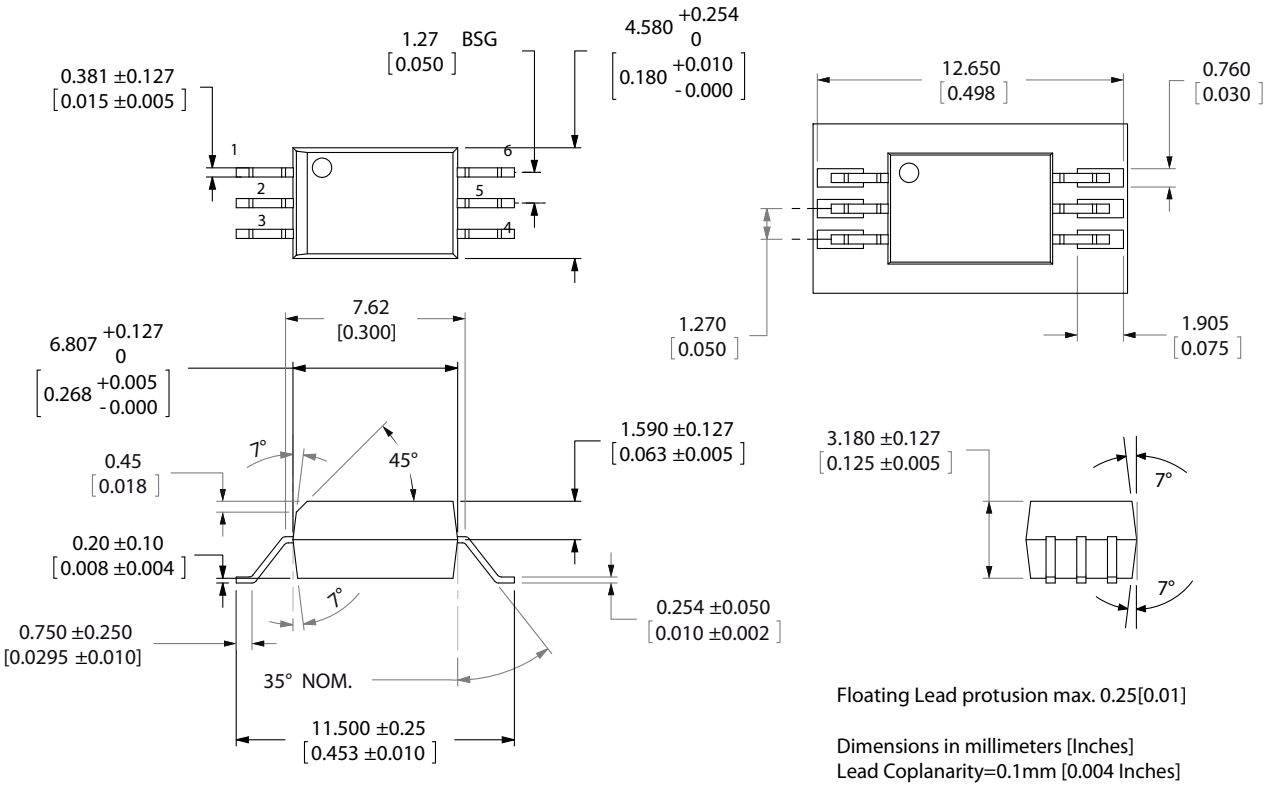
ACPL-P481 Stretched SO-6 Package, 7 mm clearance



Floating Lead Protusions max. 0.25 [0.01]

Dimensions in Millimeters [Inches]
Lead Coplanarity= 0.1mm [0.004 Inches]

ACPL-W481 Stretched SO-6 Package, 8 mm clearance



Recommended Pb-Free IR Profile

The recommended reflow profile is per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACPL-P481/W481 is pending approval by the following organizations:

IEC/EN/DIN EN 60747-5-5 (Option 060 only)

Approved with Maximum Working Insulation Voltage V_{IORM} = 891 V_{peak} for ACPL-P481 and V_{IORM} = 1140 V_{peak} for ACPL-W481

UL

Approval under UL 1577, component recognition program up to
V_{ISO} = 3750 V_{RMS}. File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

Table 1. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (ACPL-P481/W481 Option 060)

Description	Symbol	ACPL-P481	ACPL-W481	Unit
Installation Classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 150 Vrms for rated mains voltage ≤ 300 Vrms for rated mains voltage ≤ 600 Vrms		 I – IV I – III I – II	 I – IV I – III I – II	
Climatic Classification		55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	891	1140	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1670	2137	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6=V_{PR}, Type and Sample Test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	1426	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	8000	V_{peak}
Safety-limiting Values – maximum values allowed in the event of a failure.				
Case Temperature	T_S	175	175	°C
Input Current	$I_{S, INPUT}$	230	230	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under the Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2), for a detailed description of Method a and Method b partial discharge test profiles.

Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-P481	ACPL-W481	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	100	°C	
Average Input Current	$I_{F(avg)}$		10	mA	
Peak Transient Input Current (< 1 μs pulse width, 300 pps) (< 200 μs pulse width, < 1% duty cycle)	$I_{F(tran)}$		 1.0 40	 A mA	
Reverse Input Voltage	V_R		5	V	
Average Output Current	I_O		25	mA	
Supply Voltage	V_{CC}	0	25	V	
Output Voltage	V_O	-0.5	25	V	
Total Package Power Dissipation	P_T		210	mW	1
Solder Reflow Temperature Profile		See Reflow Thermal Profile			

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Power Supply Voltage	V_{CC}	4.5	20	V	2
Forward Input Current (OFF)	$I_{F(OFF)}$	6	10	mA	
Forward Input Voltage (ON)	$V_{F(ON)}$	–	0.8	V	
Operating Temperature	T_A	-40	100	°C	

Table 5. Electrical Specifications

Over recommended operating conditions T_A = -40 °C to 100 °C, V_{CC} = +4.5 V to 20 V, $I_{F(ON)}$ = 6 mA to 10 mA, $V_{F(OFF)}$ = 0 V to 0.8 V, unless otherwise specified. All typicals at T_A = 25 °C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Logic Low Output Voltage	V_{OL}			0.3	V	I_{OL} = 3.5 mA	1, 3	
				0.5		I_{OL} = 6.5 mA		
Logic High Output Voltage	V_{OH}	V_{CC}-1.8	V_{CC} - 0.9		V	I_{OH} = -3.5 mA	2, 3, 7	
		V_{CC}-2.5	V_{CC} - 1.2			I_{OH} = -6.5 mA		
Output Leakage Current ($V_O = V_{CC}$ + 0.5 V)	I_{OHH}			100	µA	V_{CC} = 5 V, V_F = 0 V		
				500	µA	V_{CC} = 20 V, V_F = 0 V		
Logic Low Supply Current	I_{CCL}		1.9	3.0	mA	V_{CC} = 5.5 V, I_F = 10 mA, I_O = 0mA		
			2.0	3.0	mA	V_{CC} = 20 V, I_F = 10 mA, I_O = 0mA		
Logic High Supply Current	I_{CCH}		1.5	2.5	mA	V_{CC} = 5.5 V, V_F = 0 V, I_O = 0mA		
			1.6	2.5	mA	V_{CC} = 20 V, V_F = 0 V, I_O = 0mA		
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	$V_O = V_{CC}$ = 5.5 V, I_F = 10 mA		3
		50			mA	$V_O = V_{CC}$ = 20 V, I_F = 10 mA		
Logic High Short Circuit Output Current	I_{OSH}			-25	mA	V_{CC} = 5.5 V, V_F = 0 V, V_O = GND		3
				-50	mA	V_{CC} = 20 V, V_F = 0 V, V_O = GND		
Input Forward Voltage	V_F		1.5	1.7	V	T_A = 25°C, I_F = 6 mA	4	
				1.85	V	I_F = 6 mA		
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$		1.7		mV/°C	I_F = 6 mA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		4

Table 6. Switching Specifications

Over recommended operating conditions T_A = -40 °C to 100 °C, V_{CC} = +4.5 V to 20 V, $I_{F(ON)}$ = 6 mA to 10 mA, $V_{F(OFF)}$ = 0 V to 0.8 V, unless otherwise specified. All typicals at T_A = 25 °C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		110	350	ns	With Peaking Capacitor	5, 6	6
Propagation Delay Time to Logic High Output Level	t_{PLH}		140	350	ns	With Peaking Capacitor	5, 6	6
Pulse Width Distortion	$\lvert t_{PHL} - t_{PLH} \rvert$ = PWD			250	ns			9
Propagation Delay Difference Between Any Two Parts	PDD	-100		250	ns			10
Output Rise Time (10-90%)	t_r		16		ns		5, 8	
Output Fall Time (90-10%)	t_f		20		ns		5, 8	
Logic High Common Mode Transient Immunity	$\lvert CM_H \rvert$	20			kV/µs	$\lvert V_{CM} \rvert$ = 1000 V, V_F = 0 V, V_{CC} = 5 V, T_A = 25°C	9	7
Logic Low Common Mode Transient Immunity	$\lvert CM_L \rvert$	20			kV/µs	$\lvert V_{CM} \rvert$ = 1000 V, I_F = 6.0 mA, V_{CC} = 5 V, T_A = 25°C	9	7

Table 7. Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750 (ACPL-P481) 5000 (ACPL-W481)			V_{rms}	RH < 50%, t = 1 min. T_A = 25°C		5, 8
Input-Output Resistance	R_{I-O}		10^{12}			V_{I-O} = 500 V_{dc}		5
Input-Output Capacitance	C_{I-O}		0.6			f = 1 MHz, V_{I-O} = 0 V_{dc}		5

* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable).

Notes:
1. Derate total package power dissipation, P_T, linearly above 70°C free-air temperature at a rate of 4.5 mW/°C.
2. Detector requires a VCC of 4.5V or higher for stable operation as output might be unstable if VCC is lower than 4.5V. Be sure to check the power ON/OFF operation other than the supply current.
3. Duration of output short circuit time should not exceed 10 ms.
4. Input capacitance is measured between pin 1 and pin 3.
5. Device considered a two-terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.
6. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the leading edge of the output pulse.
7. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state, V_O > 2.0 V. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state, V_O < 0.8 V.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for one second (leakage detection current limit, I_{I-O} <= 5 μA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.
9. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
10. Use of a 0.1 μF bypass capacitor connected between pins 4 and 6 is recommended.
11. The difference between t_{PLH} and t_{PHL} between any two devices under the same test condition.

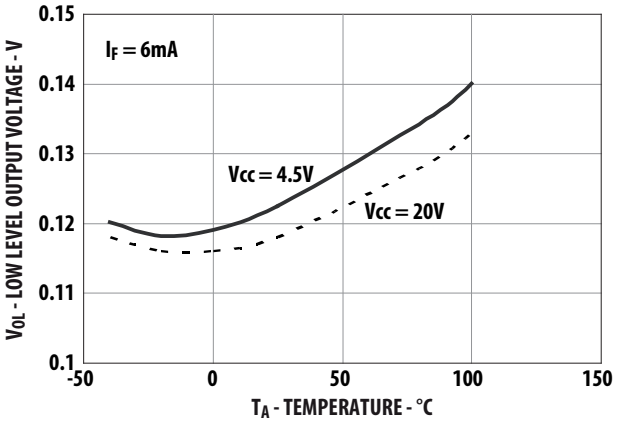


Figure 1. Typical Logic Low Output Voltage vs. Temperature

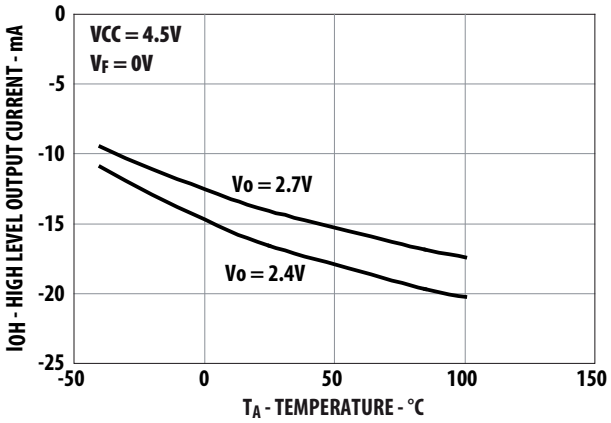


Figure 2. Typical Logic High Output Current vs. Temperature

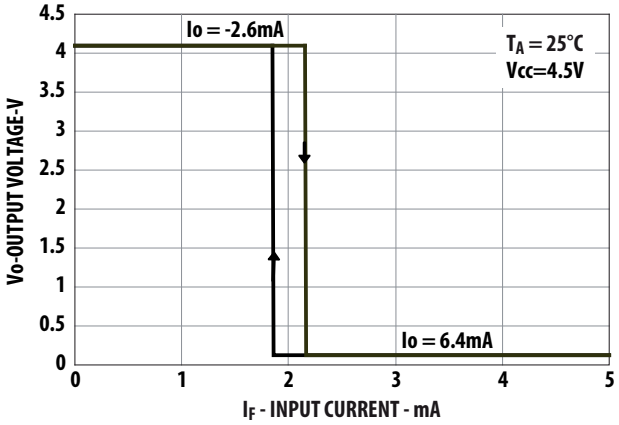


Figure 3. Typical Output Voltage vs. Forward Input Current

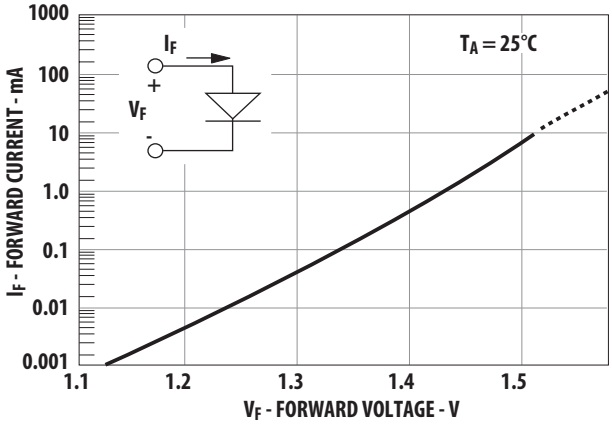
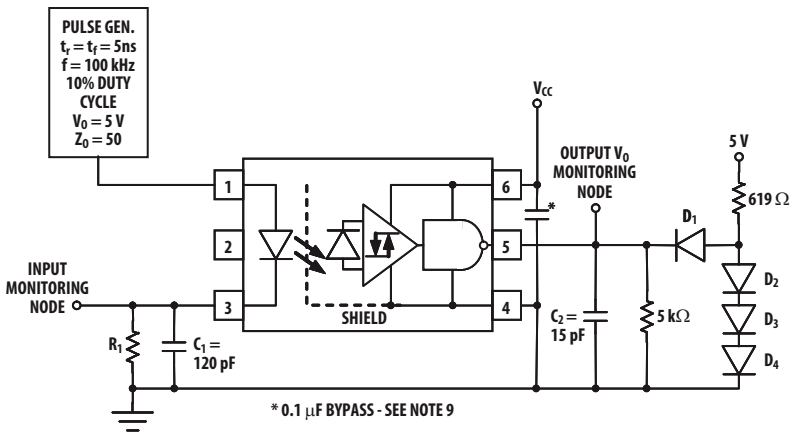


Figure 4. Typical Input Diode Forward Characteristic



THE PROBE AND JIG CAPACITANCES ARE INCLUDED IN C_1 AND C_2.

R_1	660 Ω	330 Ω
$I_{F(ON)}$	6 mA	10 mA

ALL DIODES ARE EITHER 1N916 OR 1N3064

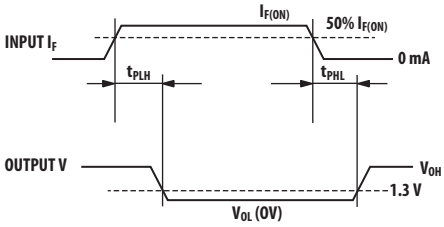


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

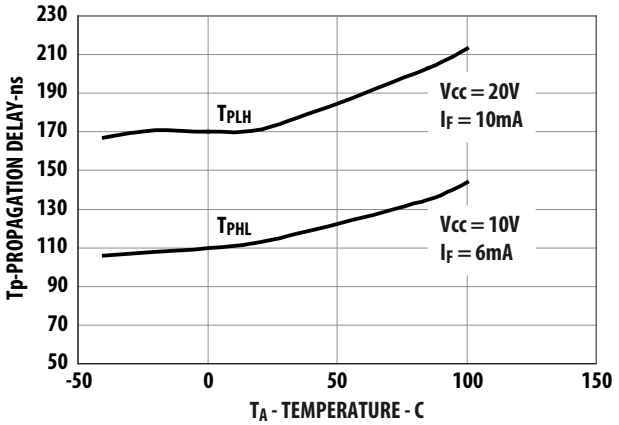


Figure 6. Typical Propagation Delays vs. Temperature.

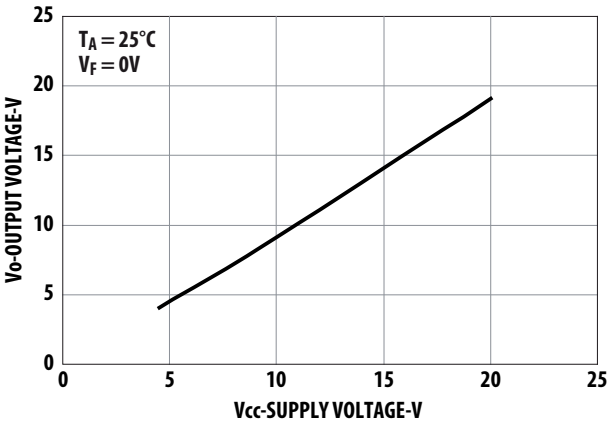


Figure 7. Typical Logic High Output Voltage vs. Supply Voltage

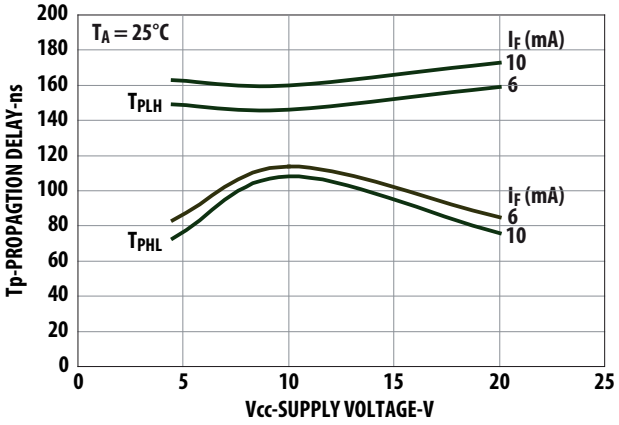
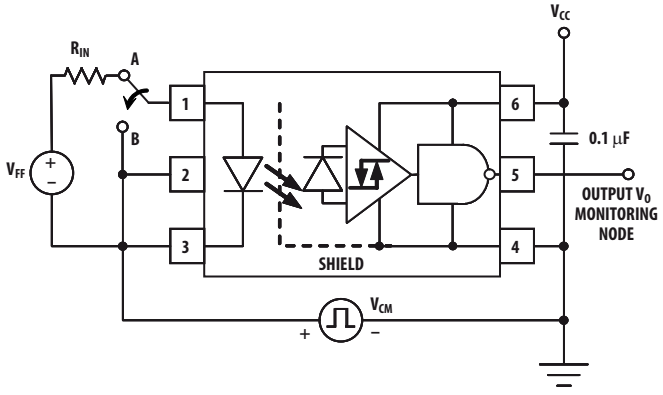


Figure 8. Typical Propagation Delay vs. Supply Voltage



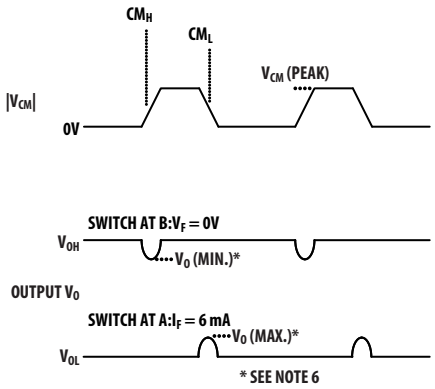


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

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