FINAL | COM'L: -5/7/B/B-2/A, 10/2 | MIL: -10/12/15/B/A

PAL20R8 Family

24-Pin TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As fast as 5 ns maximum propagation delay**
- **Popular 24-pin architectures: 20L8, 20R8, 20R6, 20R4**
- **Programmable replacement for high-speed TTL logic**
- **Power-up reset for initialization**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **24-pin SKINNYDIP and 28-pin PLCC packages save space**

GENERAL DESCRIPTION

The PAL20R8 Family (PAL20L8, PAL20R8, PAL20R6, PAL20R4) includes the PAL20R8-5 Series which is ideal for high-performance applications. The PAL20R8 Family is provided in the standard 24-pin DIP and 28-pin PLCC pinouts.

The devices provide user programmable logic for replacing conventional SSI/LSI gates and flip-flops at a reduced chip cost.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

— Variable input/output pin ratio
— Programmable three-state outputs
— Registers with feedback

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to Vcc or GND.

AMD's FusionPLD program allows PAL20R8 Family designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

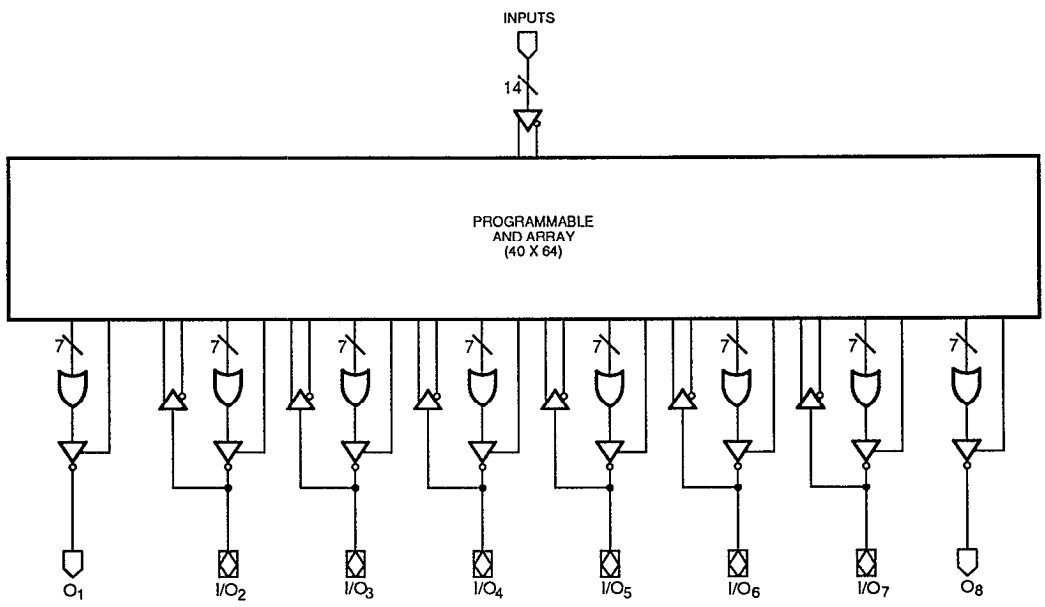
PRODUCT SELECTOR GUIDE

Device	Dedicated Inputs	Outputs	Product Terms/Output	Feedback	Enable
PAL20L8	14	6 comb. 2 comb.	7 7	I/O –	prog. prog.
PAL20R8	12	8 reg.	8	reg.	pin
PAL20R6	12	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL20R4	12	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

Publication# 16490 Rev. C Amendment/0
Issue Date: October 1994

BLOCK DIAGRAMS

PAL20L8



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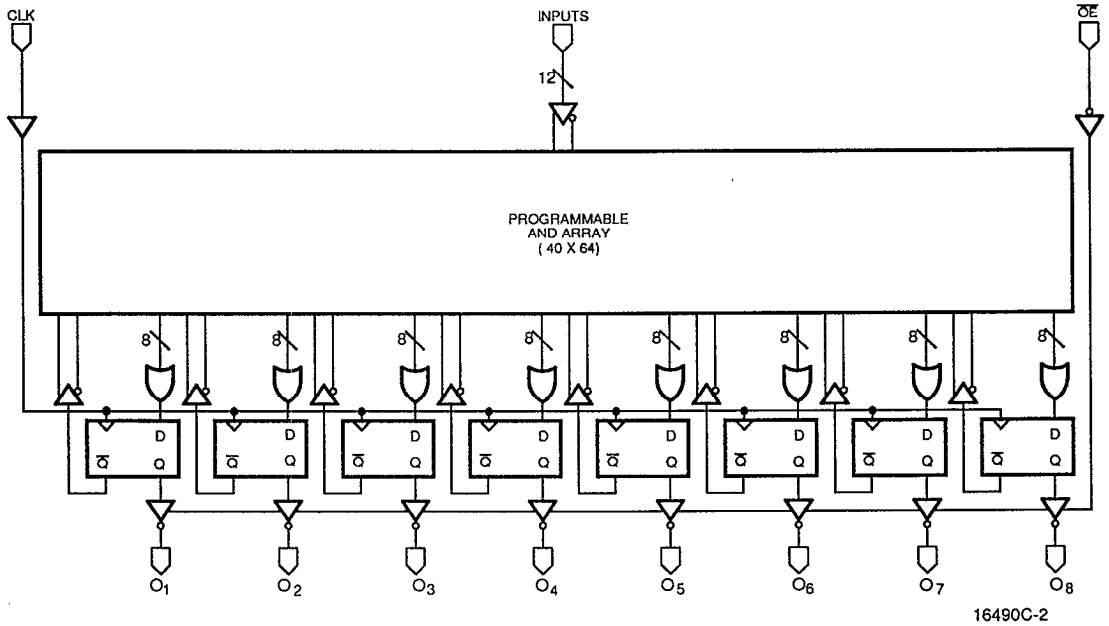
PAL20R8



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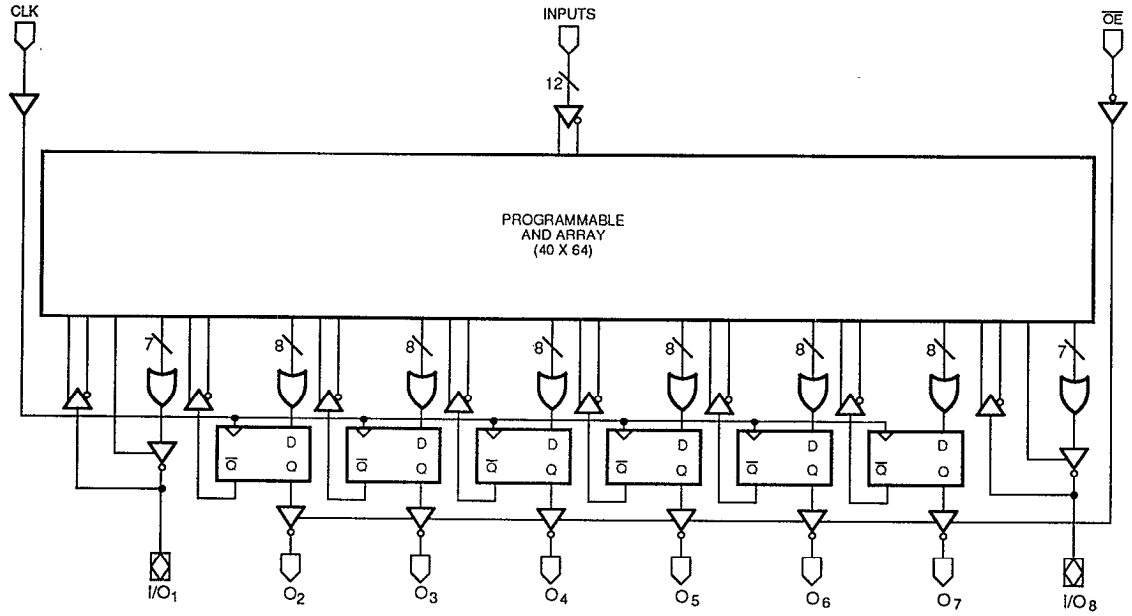
BLOCK DIAGRAMS

PAL20R6



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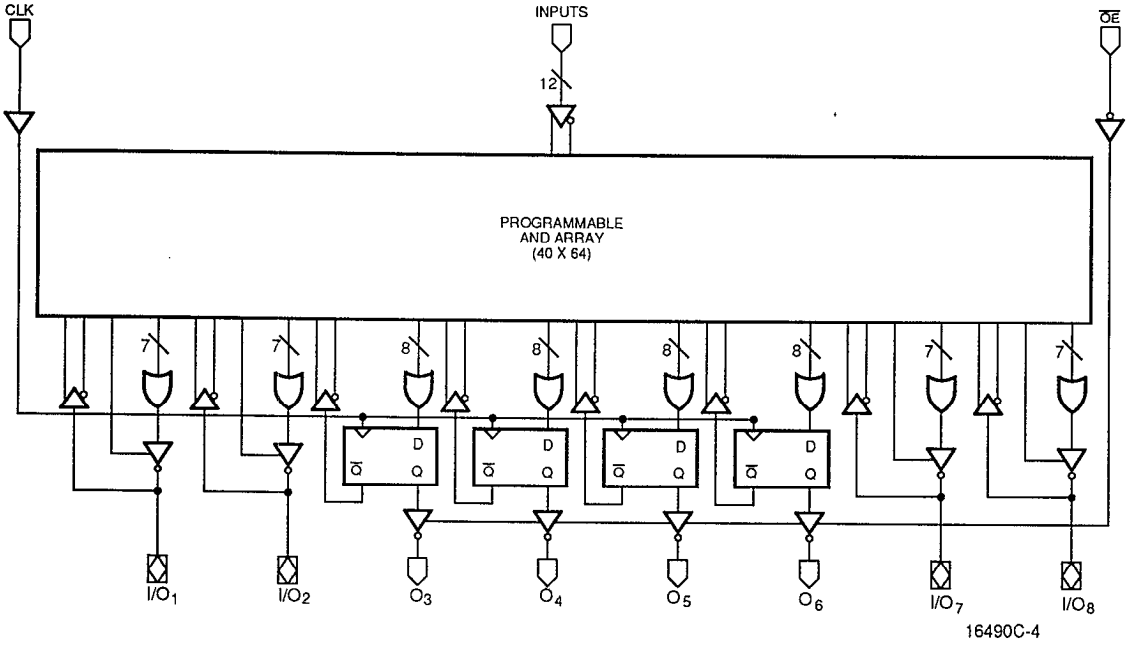
PAL20R4

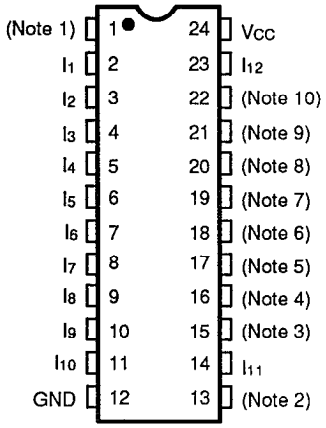


16490C-4

CONNECTION DIAGRAMS

Top View

SKINNYDIP/FLATPACK

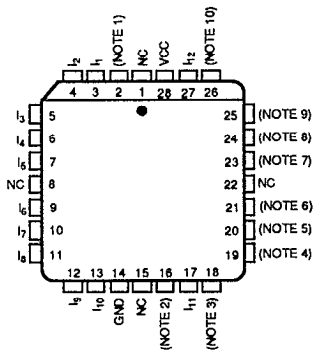


16490C-5

Note: *Pin 1 is marked for orientation.*

PLCC/LCC

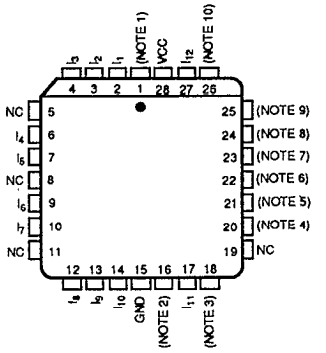
JEDEC: Applies to -5, -7(-12/10 mil), -10(-15 mil), B-2 Series Only



16490C-6

PLCC

Applies to B and A Series Only



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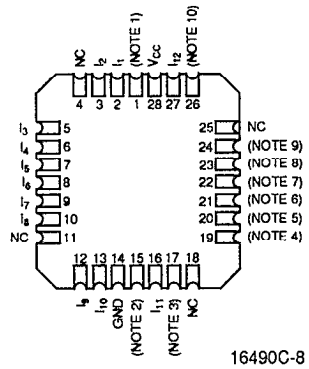
LCC

Applies to B and A Series Only



16490C-8

Note	20L8	20R8	20R6	20R4
1	I_0	CLK	CLK	CLK
2	I_{13}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	I/O_7
10	O_8	O_8	I/O_8	I/O_8

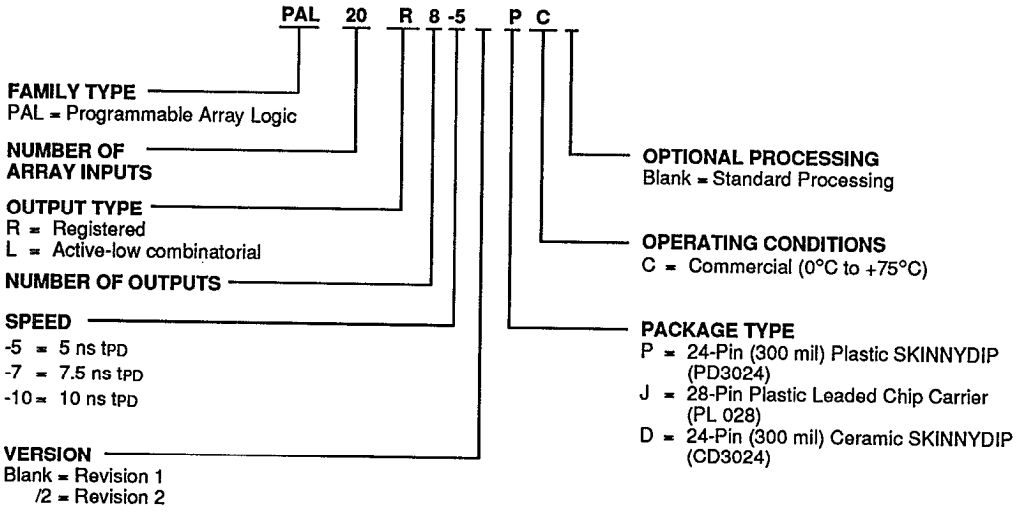
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
O = Output
$\overline{OE}$ = Output Enable
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PAL20L8-5	PC, JC
PAL20R8-5	
PAL20R6-5	
PAL20R4-5	
PAL20L8-10/2	
PAL20R8-10/2	
PAL20R6-10/2	
PAL20R4-10/2	
PAL20L8-7	PC, JC, DC
PAL20R8-7	
PAL20R6-7	
PAL20R4-7	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

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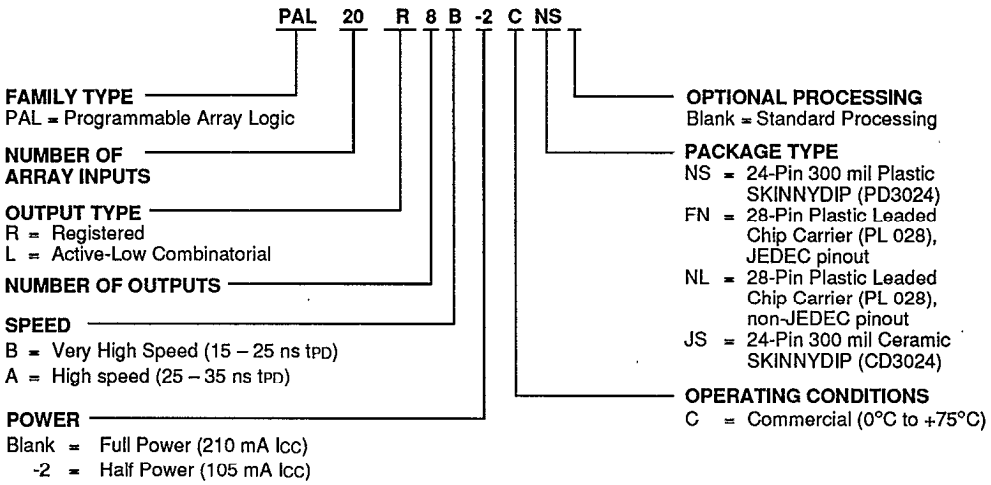


Valid Combinations		
PAL20L8	B-2	CNS, CFN, CJS
PAL20R8	B, A	CNS, CNL, CJS
PAL20R6		
PAL20R4		

Valid Combinations

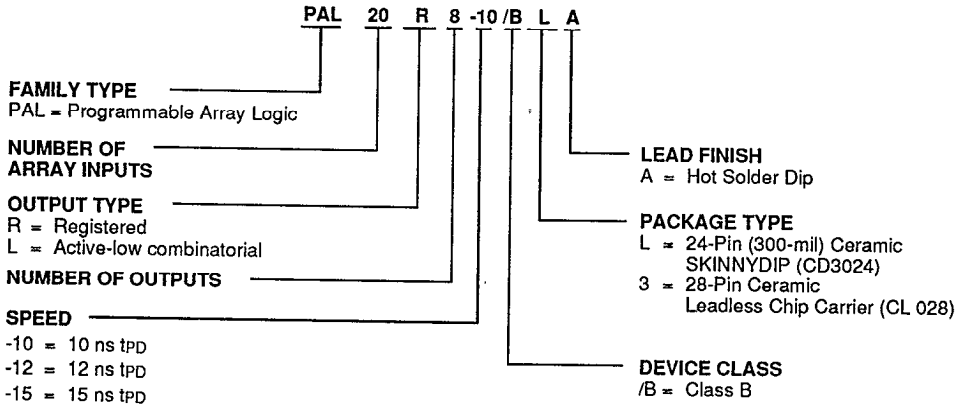
Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: *Marked with MMI logo.*

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL20L8	-10, -12, -15	/BLA, /B3A
PAL20R8		
PAL20R6		
PAL20R4		

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A Tests consist of Subgroups:
1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

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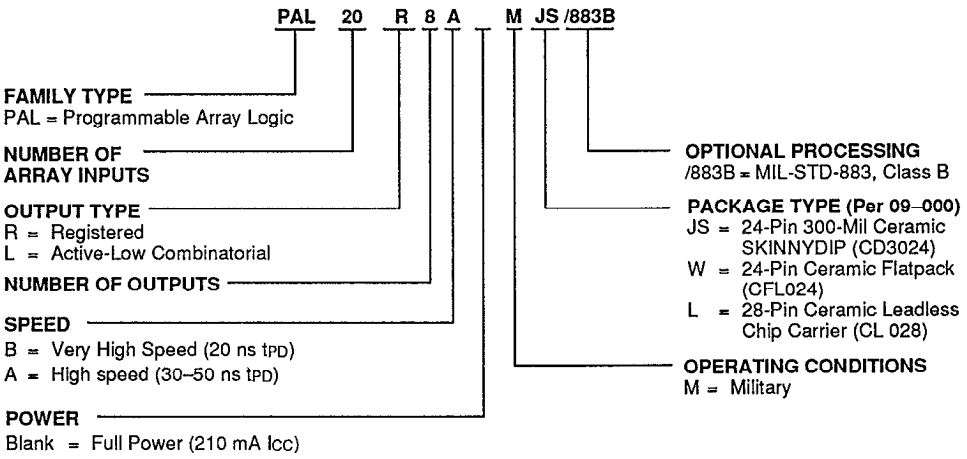


Valid Combinations		
PAL20L8	B, A	MJS/883B, MW/883B, ML/883B
PAL20R8		
PAL20R6		
PAL20R4		

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: *Marked with MMI logo.*

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

Standard 24-Pin PAL Family

The standard 24-pin PAL family is comprised of four different devices, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Using any of a number of development packages, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The registered devices have twelve dedicated input lines, and each combinatorial output is an I/O pin. The PAL20L8 has fourteen dedicated input lines, and only six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to Vcc or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL20R8 Family will be HIGH due to the active-low outputs. The Vcc rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the AMD marked 20R8, 20R6, and 20R4 devices can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL20R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is intact.

Quality and Testability

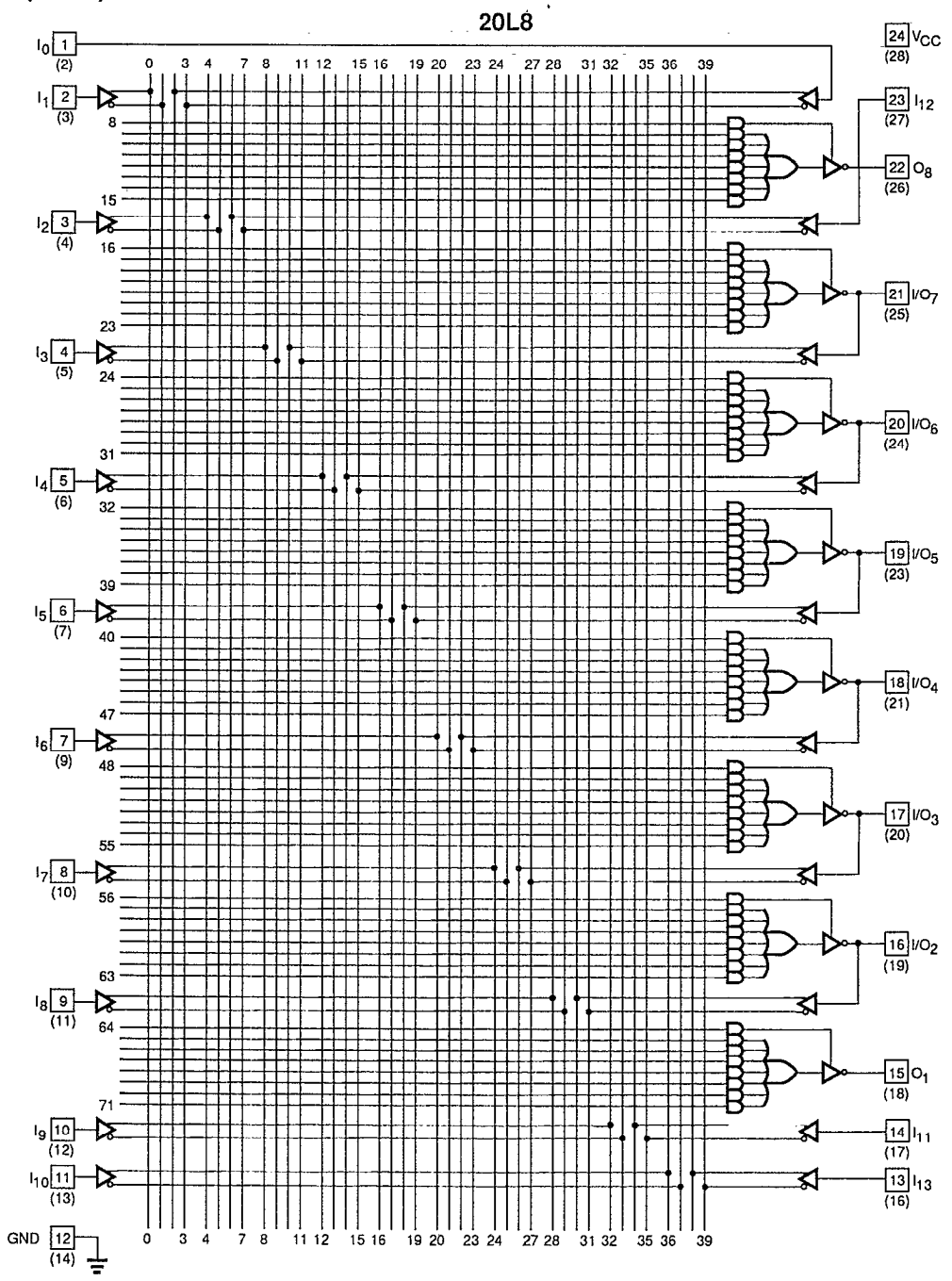
The PAL20R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The PAL20R8-5, -7 and 10/2 are fabricated with AMD's oxide isolated process. The array connections are formed with highly reliable PtSi fuses. The PAL20R8B, B-2, and A series are fabricated with AMD's trench-isolated bipolar process. The array connections are formed with proven TiW fuses. These processes reduce parasitic capacitances and minimum geometries to provide higher performance.

LOGIC DIAGRAM

DIP (PLCC) Pinouts



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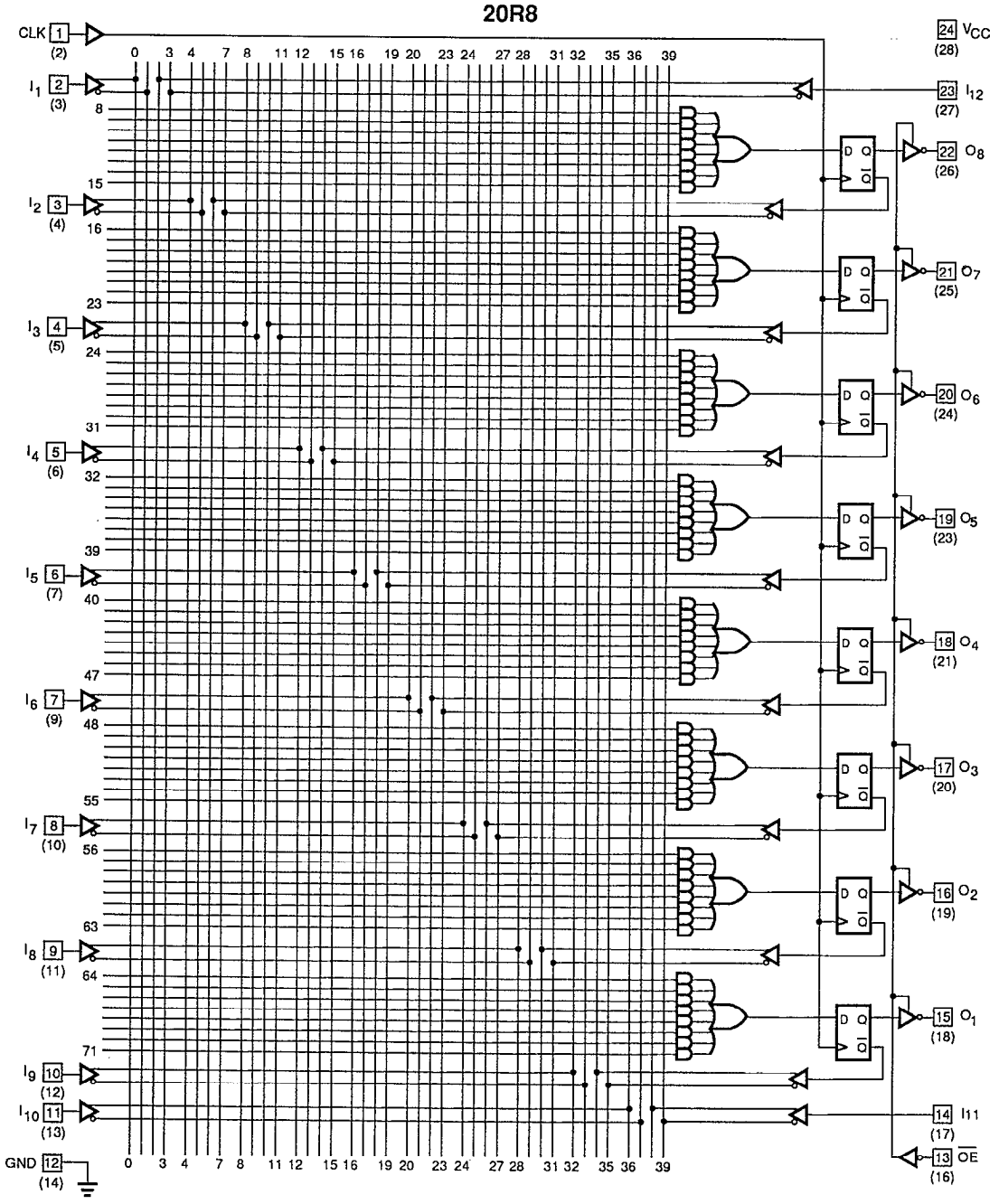
LOGIC DIAGRAM

DIP (PLCC) Pinouts



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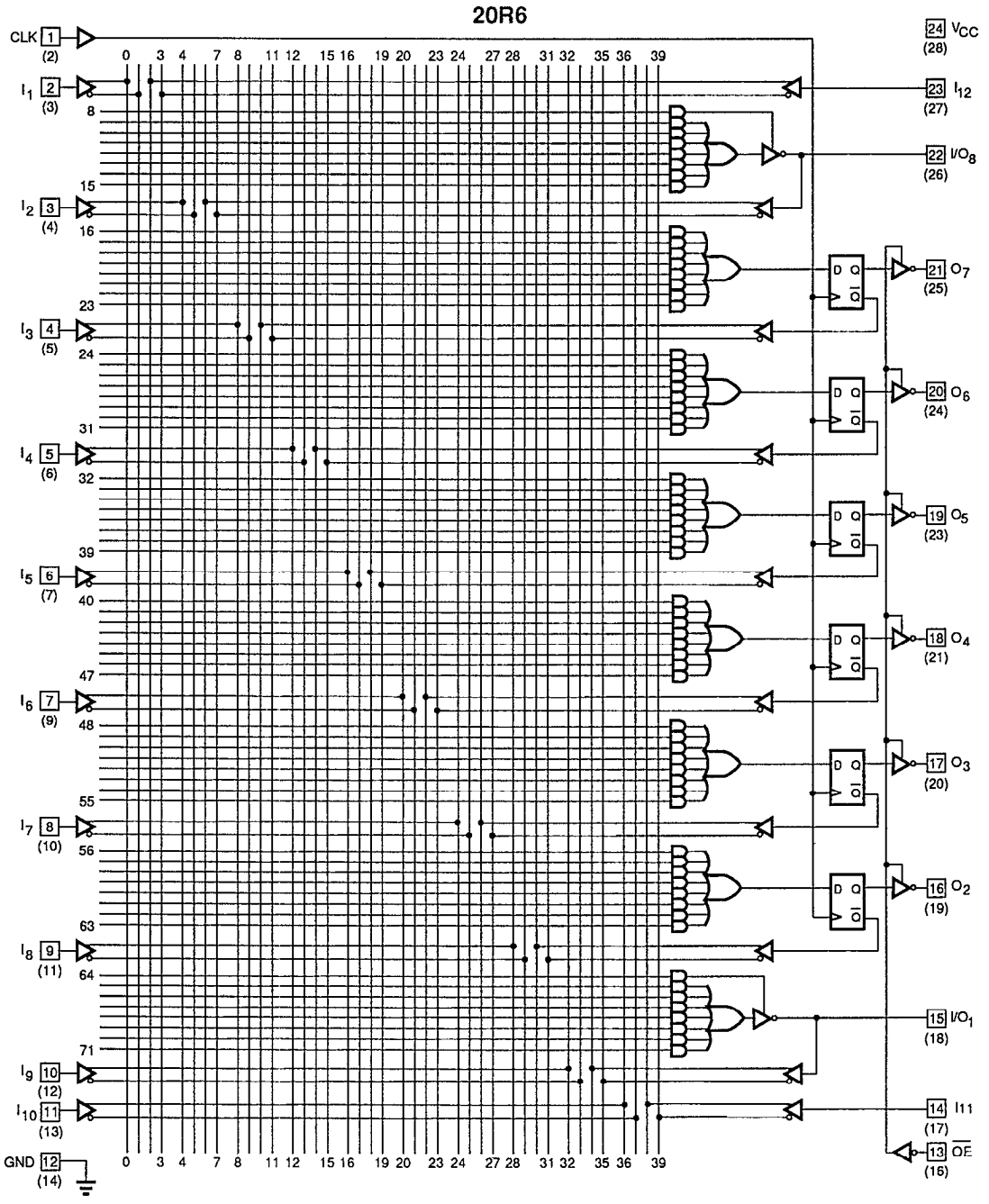
LOGIC DIAGRAM

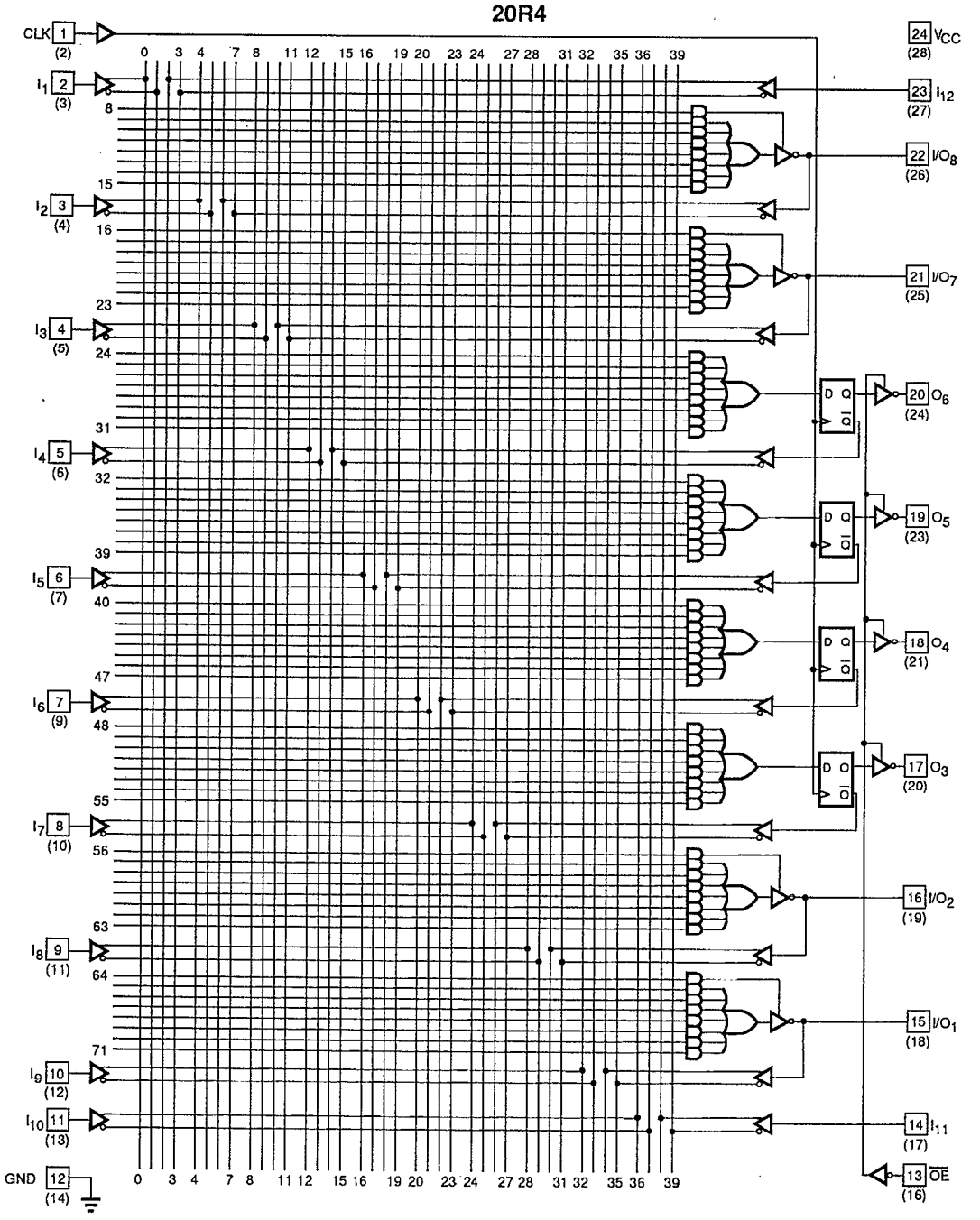
DIP (PLCC) Pinouts



16490C-11

LOGIC DIAGRAM

DIP (PLCC) Pinouts



16490C-12

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with
Power Applied ..... −55°C to +125°C

Supply Voltage with
Respect to Ground ..... −0.5 V to +7.0 V

DC Input Voltage ..... −1.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... −0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min		−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		210	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4		15	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					12	ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			12		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		45		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					12	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6, 20R4		18	ns
t_{ER}	Input to Output Disable Using Product Term Control					15	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

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t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{WL}	Clock Width	LOW			15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback (f_{CNT})			28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6, 20R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *Calculated from measured f_{MAX} internal.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*