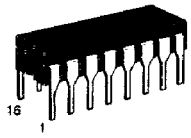
MOTOROLA

MC14512B

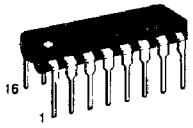
8-CHANNEL DATA SELECTOR

The MC14512B is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Diode Protection on All Inputs
- Single Supply Operation
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

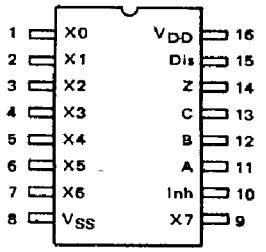
T_A = −55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

PIN ASSIGNMENT



TRUTH TABLE

C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
X	X	X	1	0	0
X	X	X	X	1	High Impedance

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	−3.0 −0.64 −1.6 −4.2	— — — —	−2.4 −0.51 −1.3 −3.4	−4.2 −0.88 −2.25 −8.8	— — — —	−1.7 −0.36 −0.9 −2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.8 μA/kHz) f + I_{DD} I_T = (1.6 μA/kHz) f + I_{DD} I_T = (2.4 μA/kHz) f + I_{DD}							μAdc
Three-State Leakage Current	I_{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C, See Figure 1)

Characteristic	Symbol	V_{DD}	All Types		Unit
			Typ #	Max	
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	5.0 10 15	100 50 40	200 100 80	ns
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	t_{PLH}	5.0 10 15	330 125 85	650 250 170	ns
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	t_{PHL}	5.0 10 15	330 125 85	650 250 170	ns
3-State Output Delay Times (Figure 3) "1" or "0" to High Z, and High Z to "1" or "0"	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	5.0 10 15	60 35 30	150 100 75	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

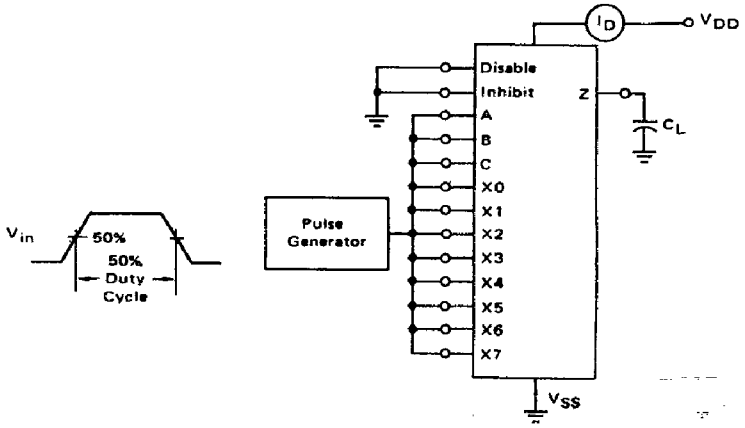
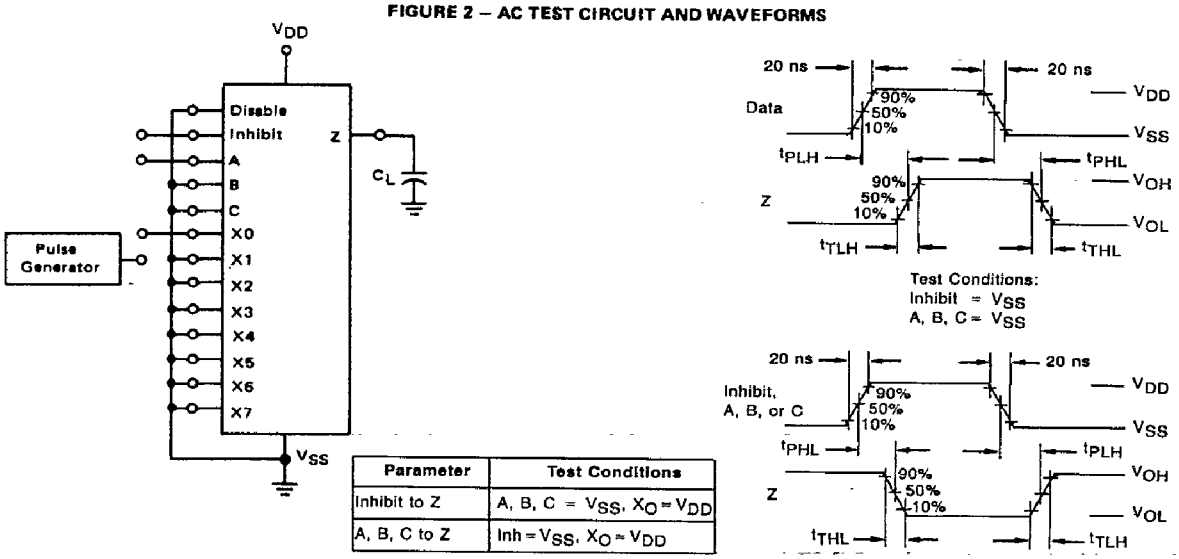
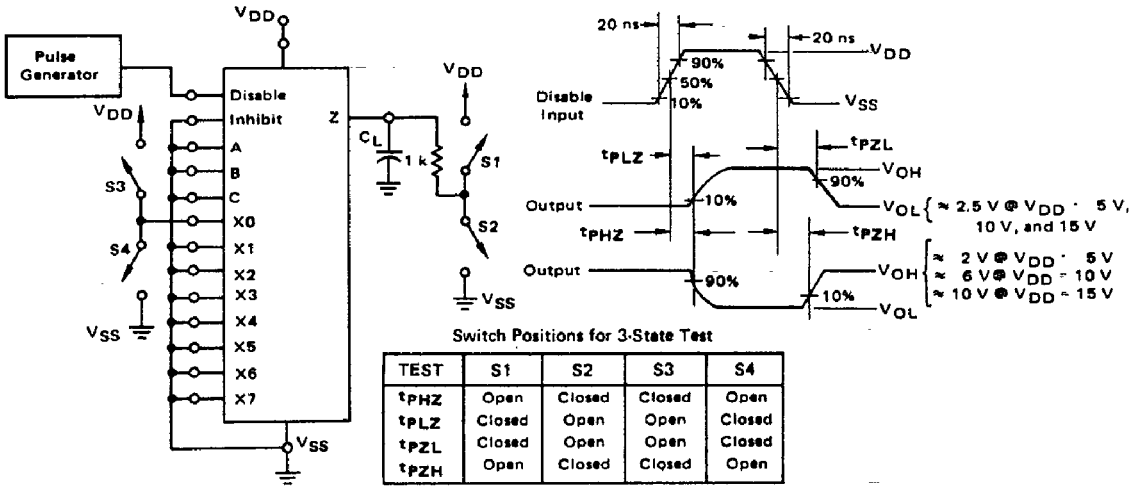


FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



Parameter	Test Conditions
Inhibit to Z	A, B, C = V_{SS}, X_O = V_{DD}
A, B, C to Z	Inh = V_{SS}, X_O = V_{DD}

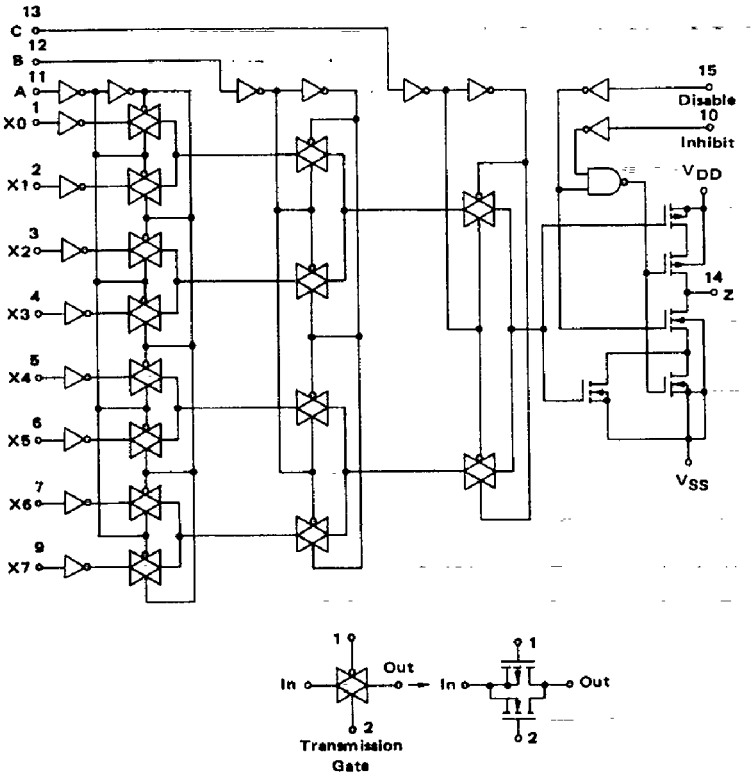
FIGURE 3 – 3-STATE AC TEST CIRCUIT AND WAVEFORM

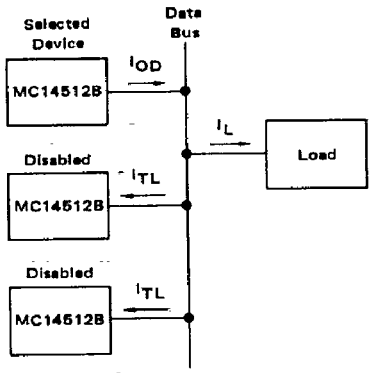


Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

LOGIC DIAGRAM





3-STATE MODE OF OPERATION

Output terminals of several MC14512B 8-Bit Data Selectors can be connected to a single data bus as shown. One MC14512B is selected by the 3-state control, and the remaining devices are disabled into a high-impedance "off" state. The number of 8-bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I_{OD}, 3-state or disable output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic state of the bus line.

MOTOROLA

MC14513B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

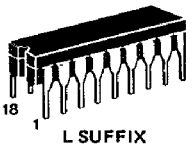
BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER WITH RIPPLE BLANKING

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

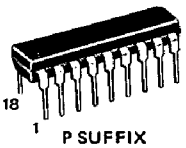
The MC14513B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and has output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. The Ripple Blanking Input (RBI) and Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Binary Input
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Capability
- Adds Ripple Blanking In, Ripple Blanking Out to MC14511B
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.



L SUFFIX
CERAMIC PACKAGE
CASE 726



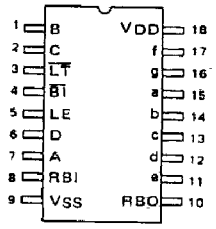
P SUFFIX
PLASTIC PACKAGE
CASE 707

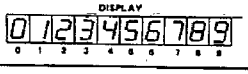
ORDERING INFORMATION

MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

T_A = −55°C to + 125°C for all packages

PIN ASSIGNMENT





MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	T_A	−55 to +125	°C
Power Dissipation, per Package†	P_D	500	mW
Storage Temperature Range	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output‡	P_{OHmax}	50	mW

‡ $P_{OHmax} = I_{OH}(V_{DD} - V_{OH})$

*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: − 12 mW/°C From 100°C To 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (see Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

INPUTS								OUTPUTS								
RBI	LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	RBO	a	b	c	d	e	f	g	DISPLAY
X	X	X	0	X	X	X	X	†	1	1	1	1	1	1	1	8
X	X	0	1	X	X	X	X	†	0	0	0	0	0	0	0	Blank
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	0	1	1	0	0	0	0	0	1	1	1	1	1	1	0	0
X	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0	1
X	0	1	1	0	0	1	0	0	1	1	0	1	1	0	1	2
X	0	1	1	0	0	1	1	0	1	1	1	1	0	0	1	3
X	0	1	1	0	1	0	0	0	0	1	1	0	0	1	1	4
X	0	1	1	0	1	0	1	0	1	0	1	1	0	1	1	5
X	0	1	1	0	1	1	0	0	1	0	1	1	1	1	1	6
X	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	7
X	0	1	1	1	0	0	0	0	1	1	1	1	1	1	1	8
X	0	1	1	1	0	0	1	0	1	1	1	1	0	1	1	9
X	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	1	1	1	X	X	X	X	‡	*							*

X = Don't Care
‡ RBO = RBI (D C B A) indicated by other rows of table
* Depends upon the BCD code previously applied when LE = 0

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage — Segment Outputs "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.1	—	4.1	5.0	—	4.1	—	Vdc
		10	9.1	—	9.1	10	—	9.1	—	
		15	14.1	—	14.1	15	—	14.1	—	
Output Voltage — RBO Output "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage # "0" Level (V_O = 3.8 or 0.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
(V_O = 8.8 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.8 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
(V_O = 0.5 or 3.8 Vdc) "1" Level	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 8.8 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.8 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Voltage — Segments	V_{OH}									Vdc
(I_{OH} = 0 mA) Source		5.0	4.1	—	4.1	4.57	—	4.1	—	
(I_{OH} = 5.0 mA)			—	—	—	4.24	—	—	—	
(I_{OH} = 10 mA)			3.9	—	3.9	4.12	—	3.5	—	
(I_{OH} = 15 mA)			—	—	—	3.94	—	—	—	
(I_{OH} = 20 mA)			3.4	—	3.4	3.70	—	3.0	—	
(I_{OH} = 25 mA)			—	—	—	3.54	—	—	—	
(I_{OH} = 0 mA)		10	9.1	—	9.1	9.58	—	9.1	—	Vdc
(I_{OH} = 5.0 mA)			—	—	—	9.26	—	—	—	
(I_{OH} = 10 mA)			9.0	—	9.0	9.17	—	8.6	—	
(I_{OH} = 15 mA)			—	—	—	9.04	—	—	—	
(I_{OH} = 20 mA)			8.6	—	8.6	8.90	—	8.2	—	
(I_{OH} = 25 mA)			—	—	—	8.75	—	—	—	
(I_{OH} = 0 mA)		15	14.1	—	14.1	14.59	—	14.1	—	Vdc
(I_{OH} = 5.0 mA)			—	—	—	14.27	—	—	—	
(I_{OH} = 10 mA)			14	—	14	14.18	—	13.6	—	
(I_{OH} = 15 mA)			—	—	—	14.07	—	—	—	
(I_{OH} = 20 mA)			13.6	—	13.6	13.95	—	13.2	—	
(I_{OH} = 25 mA)			—	—	—	13.80	—	—	—	

(continued)

ELECTRICAL CHARACTERISTICS — continued (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Drive Current — RBO Output										
(V_{OH} = 2.5 V) Source	I_{OH}	5.0	−0.40	—	−0.32	−0.64	—	−0.22	—	mAdc
(V_{OH} = 9.5 V)		10	−0.21	—	−0.17	−0.34	—	−0.12	—	
(V_{OH} = 13.5 V)		15	−0.81	—	−0.66	−1.30	—	−0.46	—	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.18	—	0.15	0.29	—	0.10	—	mAdc
(V_{OL} = 0.5 V)		10	0.47	—	0.38	0.75	—	0.26	—	
(V_{OL} = 1.5 V)		15	1.80	—	1.50	2.90	—	1.0	—	
Output Drive Current — Segments	I_{OL}									mAdc
(V_{OL} = 0.4 V) Sink		5.0	0.64	—	0.51	088	—	0.36	—	
(V_{OL} = 0.5 V)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 V)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) V_{in} = 0 or V_{DD}, I_{out} = 0 μA	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.9 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.8 μA/kHz) f + I_{DD}							
		15	I_T = (5.7 μA/kHz) f + I_{DD}							

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

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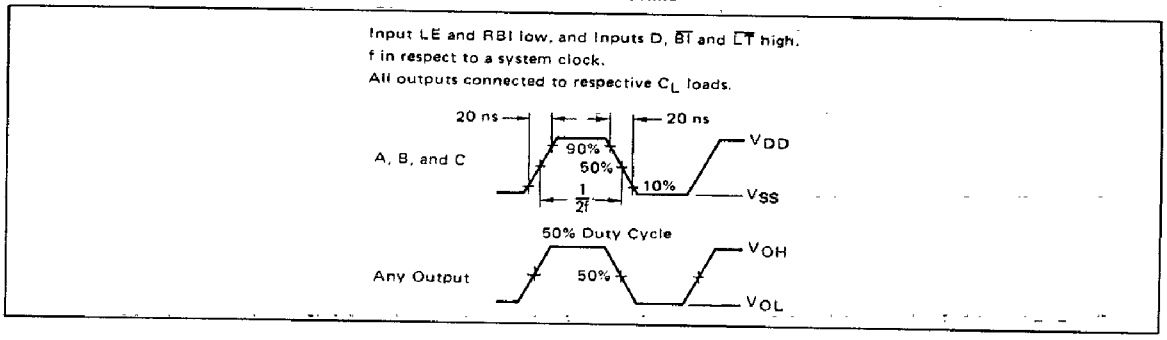
FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS



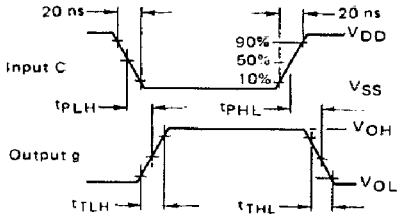
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise Time Segment Outputs	t_{TLH}					ns
		5.0	–	40	80	
		10		30	60	
		15		25	50	
Output Rise Time RBO Output	t_{TLH}					ns
		5.0		480	960	
		10		240	480	
		15		190	380	
Output Fall Time–Segment Outputs*	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 50 ns		5.0	–	125	250	
t_{THL} = (0.75 ns/pF) C_L + 37.5 ns		10	–	75	150	
t_{THL} = (0.55 ns/pF) C_L + 37.5 ns		15	–	65	130	
Output Fall Time – RBO Outputs	t_{THL}					ns
t_{THL} = (3.25 ns/pF) C_L + 107.5 ns		5.0	–	270	540	
t_{THL} = (1.35 ns/pF) C_L + 67.5 ns		10	–	135	270	
t_{THL} = (0.95 ns/pF) C_L + 62.5 ns		15	–	110	220	
Propagation Delay Time–A, B, C, D Inputs*	t_{PLH}					ns
t_{PLH} = (0.40 ns/pF) C_L + 620 ns		5.0		640	1280	
t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns		10	–	250	500	
t_{PLH} = (0.20 ns/pF) C_L + 165 ns		15	–	175	350	
t_{PHL} = (1.3 ns/pF) C_L + 655 ns	t_{PHL}	5.0	–	720	1440	ns
t_{PHL} = (0.60 ns/pF) C_L + 260 ns		10	–	290	580	
t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns		15	–	200	400	
Propagation Delay Time–RBI and BI Inputs*	t_{PLH}					ns
t_{PLH} = (1.05 ns/pF) C_L + 547.5 ns		5.0	–	600	750	
t_{PLH} = (0.45 ns/pF) C_L + 177.5 ns		10	–	200	300	
t_{PLH} = (0.30 ns/pF) C_L + 135 ns		15	–	150	220	
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns	t_{PHL}	5.0	–	485	970	ns
t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns		10	–	200	400	
t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns		15	–	160	320	
Propagation Delay Time–$\overline{LT}$ Input*	t_{PLH}					ns
t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns		5.0	–	313	625	
t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns		10	–	125	250	
t_{PLH} = (0.20 ns/pF) C_L + 80 ns		15	–	90	180	
t_{PHL} = (1.3 ns/pF) C_L + 248 ns	t_{PHL}	5.0	–	313	625	ns
t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns		10	–	125	250	
t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns		15	–	90	180	
Setup Time	t_{su}	5.0	100	–	–	ns
		10	40	–		
		15	30	–	–	
Hold Time	t_h	5.0	60	–	–	ns
		10	40	–	–	
		15	30	–	–	
Latch Enable Pulse Width	$t_{WL(LE)}$	5.0	520	260	–	ns
		10	220	110		
		15	130	65	–	

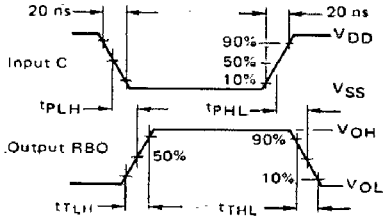
*The formulas given are for the typical characteristics only.

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS

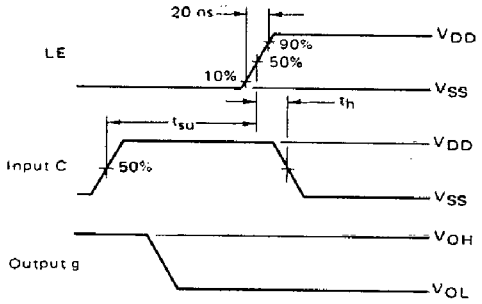
a. Data Propagation Delay: Inputs RBI, D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high



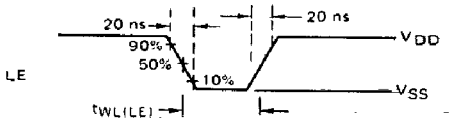
b. Inputs A, B, D and LE low, and Inputs RBI, $\overline{BI}$ and $\overline{LT}$ high.



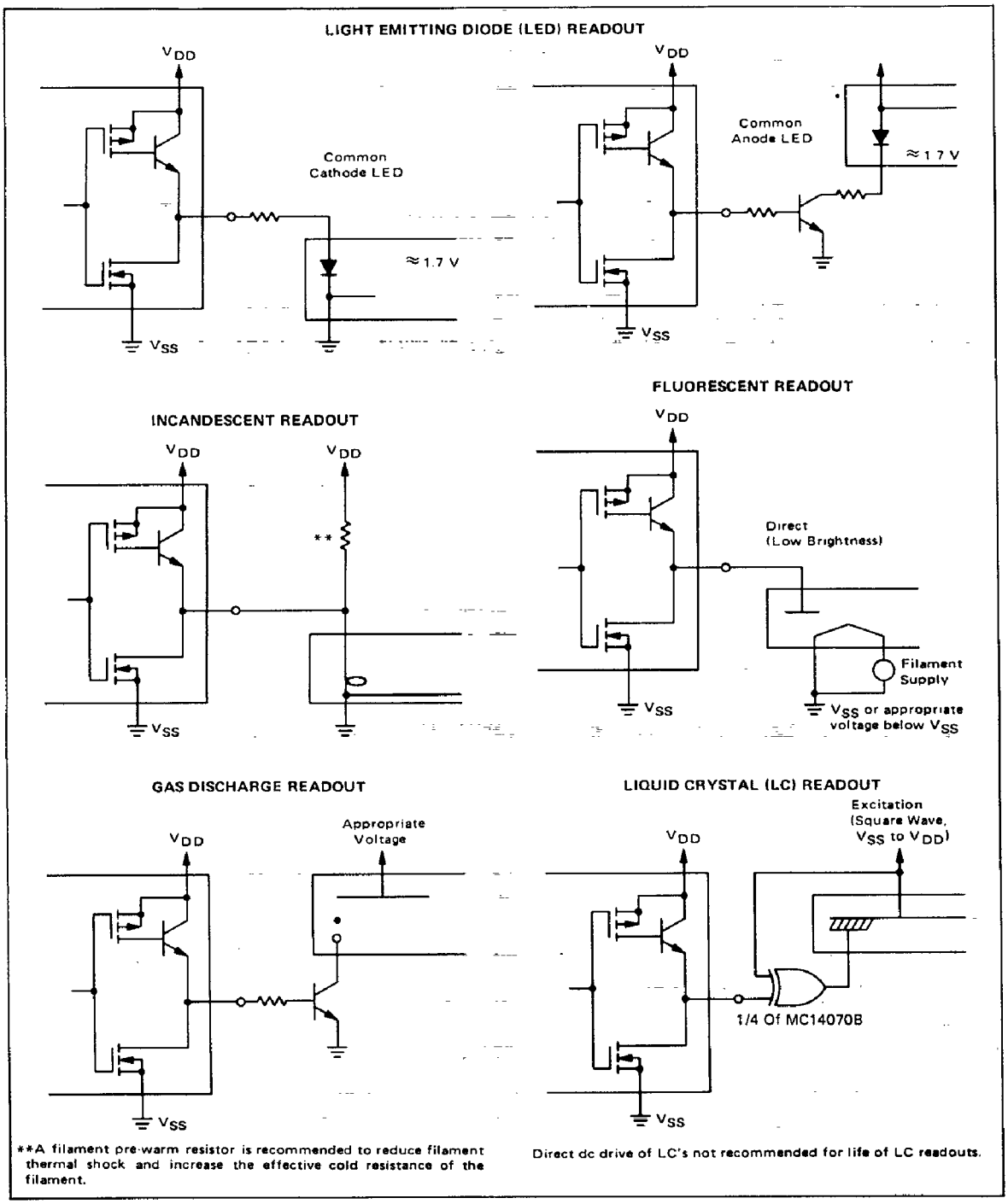
c. Setup and Hold Times Input RBI and D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



d. Pulse Width. Data DCBA strobed into latches.



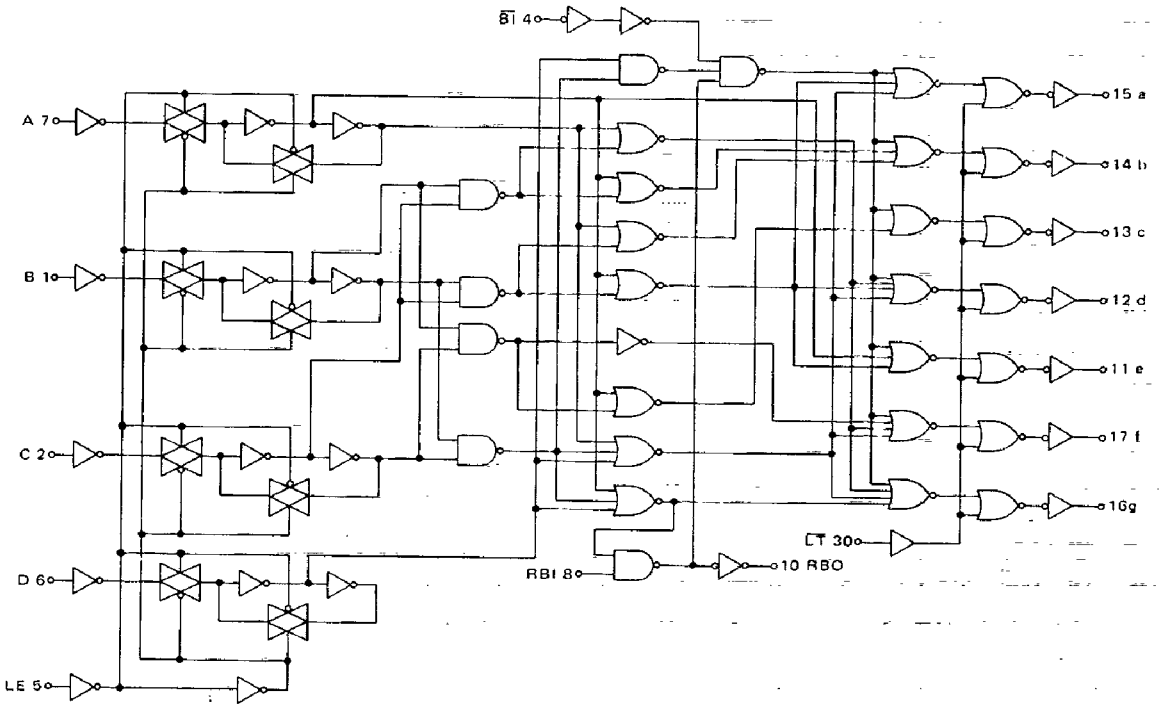
CONNECTIONS TO VARIOUS DISPLAY READOUTS



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

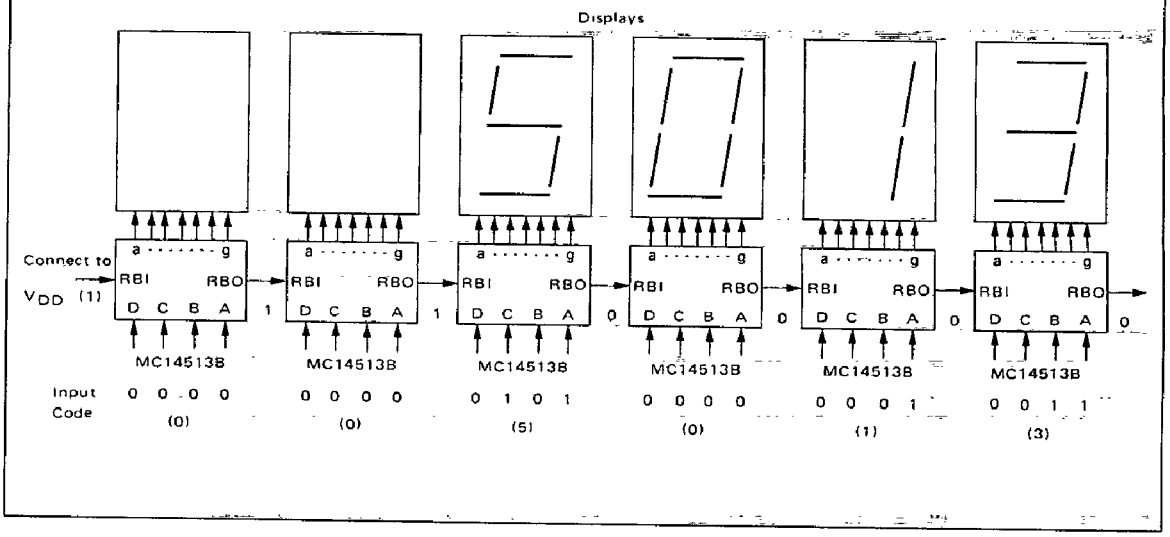
Direct dc drive of LC's not recommended for life of LC readouts.

LOGIC DIAGRAM



TYPICAL APPLICATIONS FOR RIPPLE BLANKING

LEADING EDGE ZERO SUPPRESSION



TYPICAL APPLICATIONS FOR RIPPLE BLANKING (Cont)

TRAILING EDGE ZERO SUPPRESSION