MOTOROLA

MC14516B

BINARY UP/DOWN COUNTER

The MC14516B synchronous up/down binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure.

This counter can be preset by applying the desired value, in binary, to the Preset inputs (P0, P1, P2, P3) and then bringing the Preset Enable (PE) high. The direction of counting is controlled by applying a high (for up counting) or a low (for down counting) to the UP/DOWN input. The state of the counter changes on the positive transition of the clock input.
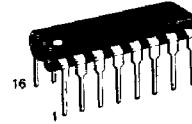
Cascading can be accomplished by connecting the Carry Out to the Carry In of the next stage while clocking each counter in parallel. The outputs (Q0, Q1, Q2, Q3) can be reset to a low state by applying a high to the reset (R) pin.

This CMOS counter finds primary use in up/down and difference counting. Other applications include: (1) Frequency synthesizer applications where low power dissipation and/or high noise immunity is desired, (2) Analog-to-digital and digital-to-analog conversions, and (3) Magnitude and sign generation.
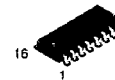
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design — Count Occurs on Positive Going Edge of Clock
- Single Pin Reset
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky Load Over the Rated Temperature Range

L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

TRUTH TABLE

Carry In	Up/Down	Preset Enable	Reset	Clock	Action
1	X	0	0	X	No Count
0	1	0	0	⌐	Count Up
0	0	0	0	⌐	Count Down
X	X	1	0	X	Preset
X	X	X	1	X	Reset

X = Don't Care

Note: When counting up, the Carry Out signal is normally high and is low only when Q0 through Q3 are high and Carry In is low. When counting down, Carry Out is low only when Q0 through Q3 and Carry In are low.

BLOCK DIAGRAM

1 ○—	PE	Q0 —○ 6
5 ○—	Carry In	
9 ○—	Reset	Q1 —○ 11
10 ○—	Up/Down	
15 ○—	Clock	Q2 —○ 14
4 ○—	P0	
12 ○—	P1	Q3 —○ 2
13 ○—	P2	
3 ○—	P3	Carry Out —○ 7

V_{DD} = Pin 16
V_{SS} = Pin 8

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V$_{SS}$)

Characteristic	Symbol	V$_{DD}$ Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V$_{in}$ = V$_{DD}$ or 0	V$_{OL}$	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V$_{in}$ = 0 or V$_{DD}$	V$_{OH}$	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V$_O$ = 4.5 or 0.5 Vdc) (V$_O$ = 9.0 or 1.0 Vdc) (V$_O$ = 13.5 or 1.5 Vdc)	V$_{IL}$	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V$_O$ = 0.5 or 4.5 Vdc) (V$_O$ = 1.0 or 9.0 Vdc) (V$_O$ = 1.5 or 13.5 Vdc)	V$_{IH}$	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V$_{OH}$ = 2.5 Vdc) Source (V$_{OH}$ = 4.6 Vdc) (V$_{OH}$ = 9.5 Vdc) (V$_{OH}$ = 13.5 Vdc)	I$_{OH}$	5.0 5.0 10 15	−3.0 −0.64 −1.6 −4.2	— — — —	−2.4 −0.51 −1.3 −3.4	−4.2 −0.88 −2.25 −8.8	— — — —	−1.7 −0.36 −0.9 −2.4	— — — —	mAdc
(V$_{OL}$ = 0.4 Vdc) Sink (V$_{OL}$ = 0.5 Vdc) (V$_{OL}$ = 1.5 Vdc)	I$_{OL}$	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I$_{in}$	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V$_{in}$ = 0)	C$_{in}$	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I$_{DD}$	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C$_L$ = 50 pF on all outputs, all buffers switching)	I$_T$	5.0 10 15	\multicolumn{6}{c}{I$_T$ = (0.58 μA/kHz) f + I$_{DD}$ I$_T$ = (1.20 μA/kHz) f + I$_{DD}$ I$_T$ = (1.70 μA/kHz) f + I$_{DD}$}						μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
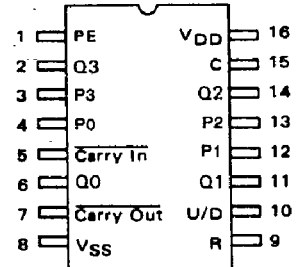
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I$_T$ is in μA (per package), C$_L$ in pF, V = (V$_{DD}$ − V$_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

PIN ASSIGNMENT

Pin	Name		Name	Pin
1	PE		V$_{DD}$	16
2	Q3		C	15
3	P3		Q2	14
4	P0		P2	13
5	Carry In		P1	12
6	Q0		Q1	11
7	Carry Out		U/D	10
8	V$_{SS}$		R	9

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SWITCHING CHARACTERISTICS* ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD}	All Types Min	All Types Typ #	All Types Max	Unit
Output Rise and Fall Time t_{TLH}, $t_{THL} = (1.5$ ns/pF$)$ $C_L + 25$ ns t_{TLH}, $t_{THL} = (0.75$ ns/pF$)$ $C_L + 12.5$ ns t_{TLH}, $t_{THL} = (0.55$ ns/pF$)$ $C_L + 9.5$ ns	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q t_{PLH}, $t_{PHL} = (1.7$ ns/pF$)$ $C_L + 230$ ns t_{PLH}, $t_{PHL} = (0.66$ ns/pF$)$ $C_L + 97$ ns t_{PLH}, $t_{PHL} = (0.5$ ns/pF$)$ $C_L + 75$ ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	315 130 100	630 260 200	ns
Clock to Carry Out t_{PLH}, $t_{PHL} = (1.7$ ns/pF$)$ $C_L + 230$ ns t_{PLH}, $t_{PHL} = (0.66$ ns/pF$)$ $C_L + 97$ ns t_{PLH}, $t_{PHL} = (0.5$ ns/pF$)$ $C_L + 75$ ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	315 130 100	630 260 200	ns
Carry In to Carry Out t_{PLH}, $t_{PHL} = (1.7$ ns/pF$)$ $C_L + 230$ ns t_{PLH}, $t_{PHL} = (0.66$ ns/pF$)$ $C_L + 97$ ns t_{PLH}, $t_{PHL} = (0.5$ ns/pF$)$ $C_L + 75$ ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	180 80 60	360 160 120	ns
Preset or Reset to Q t_{PLH}, $t_{PHL} = (1.7$ ns/pF$)$ $C_L + 230$ ns t_{PLH}, $t_{PHL} = (0.66$ ns/pF$)$ $C_L + 97$ ns t_{PLH}, $t_{PHL} = (0.5$ ns/pF$)$ $C_L + 75$ ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	315 130 100	630 360 200	ns
Preset or Reset to Carry Out t_{PLH}, $t_{PHL} = (1.7$ ns/pF$)$ $C_L + 465$ ns t_{PLH}, $t_{PHL} = (0.66$ ns/pF$)$ $C_L + 192$ ns t_{PLH}, $t_{PHL} = (0.5$ ns/pF$)$ $C_L + 125$ ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	550 225 150	1100 450 300	ns
Reset Pulse Width	t_W	5.0 10 15	380 200 160	190 100 80	— — —	ns
Clock Pulse Width	t_{WH}	5.0 10 15	350 170 140	200 100 75	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.0 6.0 8.0	1.5 3.0 4.0	MHz
Preset or Reset Removal Time The Preset or Reset signal must be low prior to a positive-going transition of the clock.	t_{rem}	5.0 10 15	650 230 180	325 115 90	— — —	ns
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5 4	µs
Setup Time Carry In to Clock	t_{su}	5.0 10 15	260 120 100	130 60 50	— — —	ns
Hold Time Clock to Carry In	t_h	5.0 10 15	0 20 20	−60 −20 0	— — —	ns
Setup Time Up/Down to Clock	t_{su}	5.0 10 15	500 200 150	250 100 75	— — —	ns
Hold Time Clock to Up/Down	t_h	5.0 10 15	−70 −10 0	−160 −60 −40	— — —	ns
Setup Time Pn to PE	t_{su}	5.0 10 15	−40 −30 −25	−120 −70 −50	— — —	ns
Hold Time PE to Pn	t_h	5.0 10 15	480 420 420	240 210 210	— — —	ns
Preset Enable Pulse Width	t_{WH}	5.0 10 15	200 100 80	100 50 40	— — —	ns

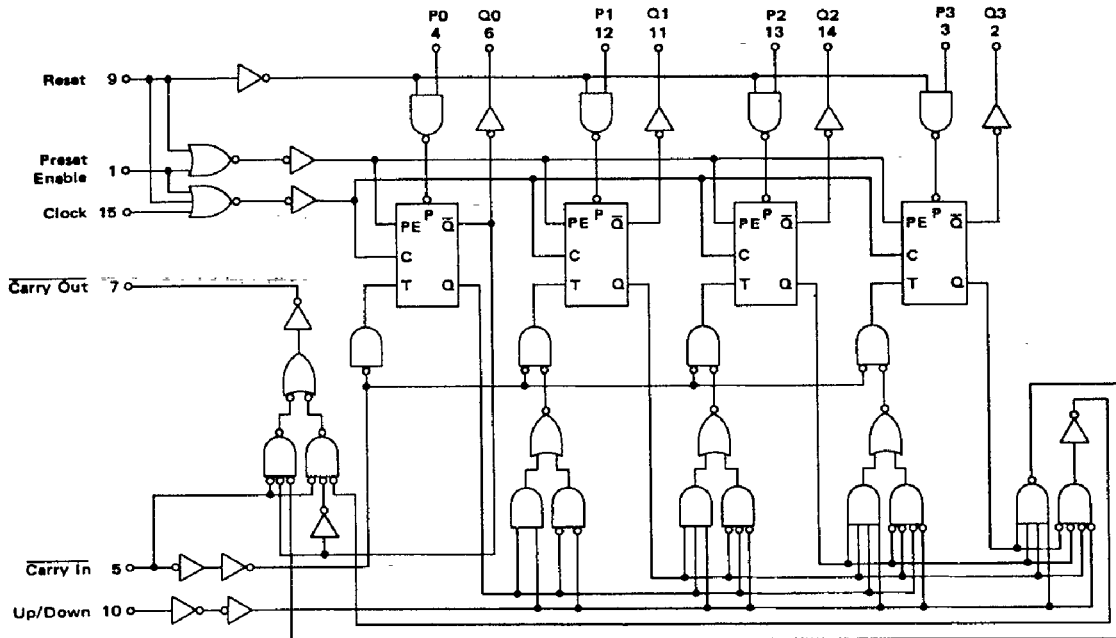*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
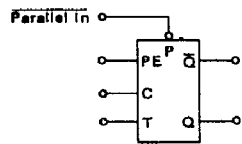
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FIGURE 1 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM
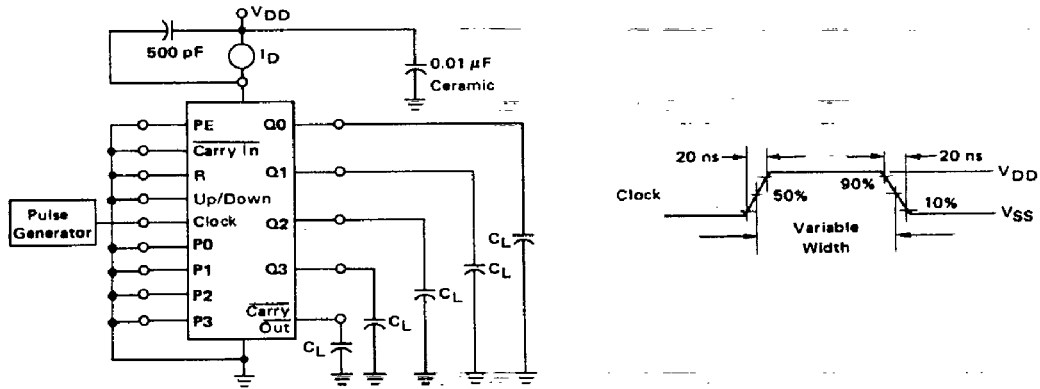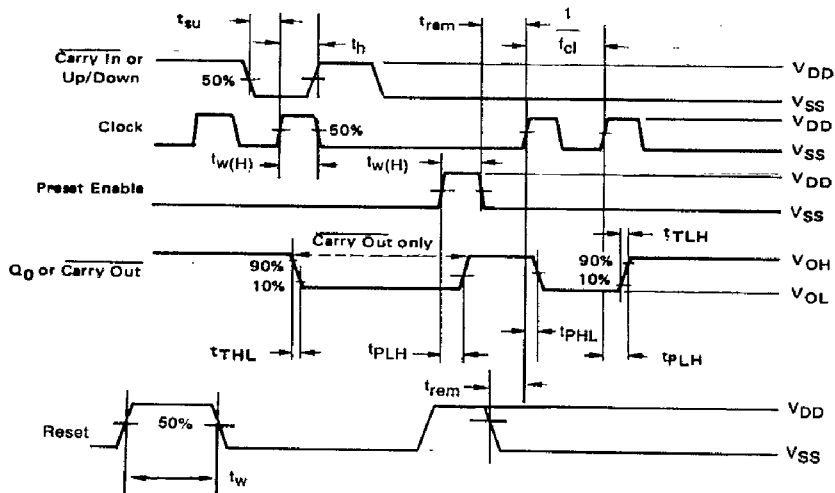

LOGIC DIAGRAM

TOGGLE FLIP-FLOP

FLIP-FLOP FUNCTIONAL TRUTH TABLE

PRESET ENABLE	CLOCK	T	Q_{n+1}
1	X	X	Parallel In
0	⌐⌐	0	Q_n
0	⌐⌐	1	$\bar{Q}_n$
0	⌐⌐	X	Q_n

X = Don't Care

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FIGURE 2 — SWITCHING TIME WAVEFORMS

PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3, Preset Inputs (Pins 4, 12, 13, 3) — Data on these inputs is loaded into the counter when PE is taken high.

Carry In, (Pin 5) — This active-low input is used when cascading stages. Carry In is usually connected to Carry Out of the previous stage. While high, Clock is inhibited.

Clock, (Pin 15) — Binary data is incremented or decremented, depending on the direction of count, on the positive transition of this input.

OUTPUTS

Q0, Q1, Q2, Q3, Binary outputs (Pins 6, 11, 14, 2) — Binary data is present on these outputs with Q0 corresponding to the least significant bit.

Carry Out, (Pin 7) — Used when cascading stages, Carry Out is usually connected to Carry In of the next stage. This synchronous output is active low and may also be used to indicate terminal count.

CONTROLS

PE, Preset Enable, (Pin 1) — Asynchronously loads data on the Preset Inputs. This pin is active high and inhibits the clock when high.

R, Reset, (Pin 9) — Asynchronously resets the Q outputs to a low state. This pin is active high and inhibits the clock when high.

Up/Down, (Pin 10) — Controls the direction of count, high for up count, low for down count.
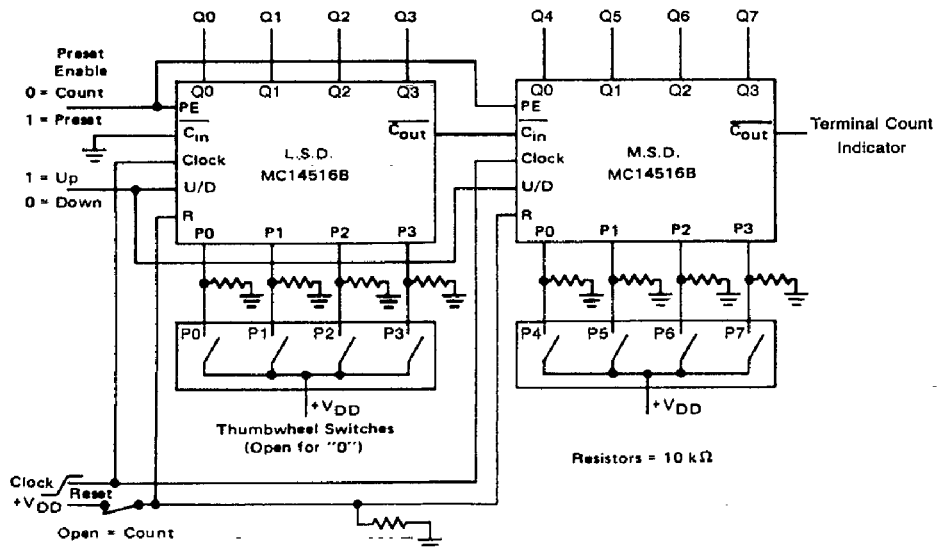
SUPPLY PINS

V_{SS}, Negative Supply Voltage, (Pin 8) — This pin is usually connected to ground.

V_{DD}, Positive Supply Voltage, (Pin 16) — This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.
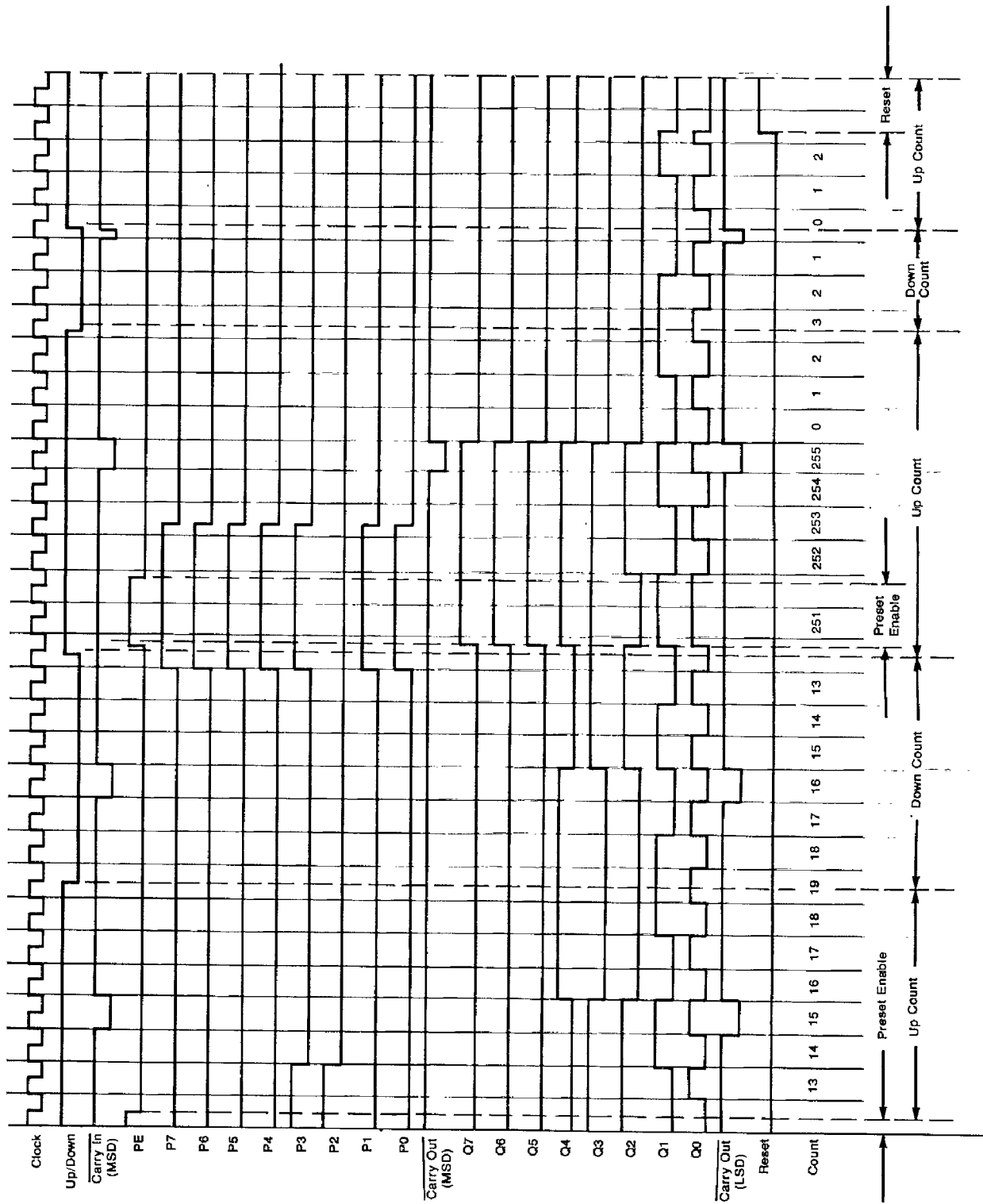
FIGURE 3 — PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER

Note: The Least Significant Digit (L.S.D.) counts from a preset value once Preset Enable (PE) goes low. The Most Significant Digit (M.S.D.) is disabled while $\overline{C_{in}}$ is high. When the count of the L.S.D. reaches 0 (count down mode) or reaches 15 (count up mode), $\overline{C_{out}}$ goes low for one complete clock cycle, thus allowing the next counter to decrement/increment one count. (See Timing Diagram) The L.S.D. now counts through another cycle (15 clock pulses) and the above cycle is repeated.

TIMING DIAGRAM FOR THE PRESETTABLE
CASCADED 8-BIT UP/DOWN COUNTER

Clock
Up/Down
Carry In (MSD)
PE
P7
P6
P5
P4
P3
P2
P1
P0
Carry Out (MSD)
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
Carry Out (LSD)
Reset
Count

Reset

Up Count

Down Count

Up Count

Preset Enable

Down Count

Up Count

Preset Enable

2 1 0 1 2 3 2 1 0 255 254 253 252 251 13 14 15 16 17 18 19 18 17 16 15 14 13

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FIGURE 4 — PROGRAMMABLE CASCADED FREQUENCY DIVIDER
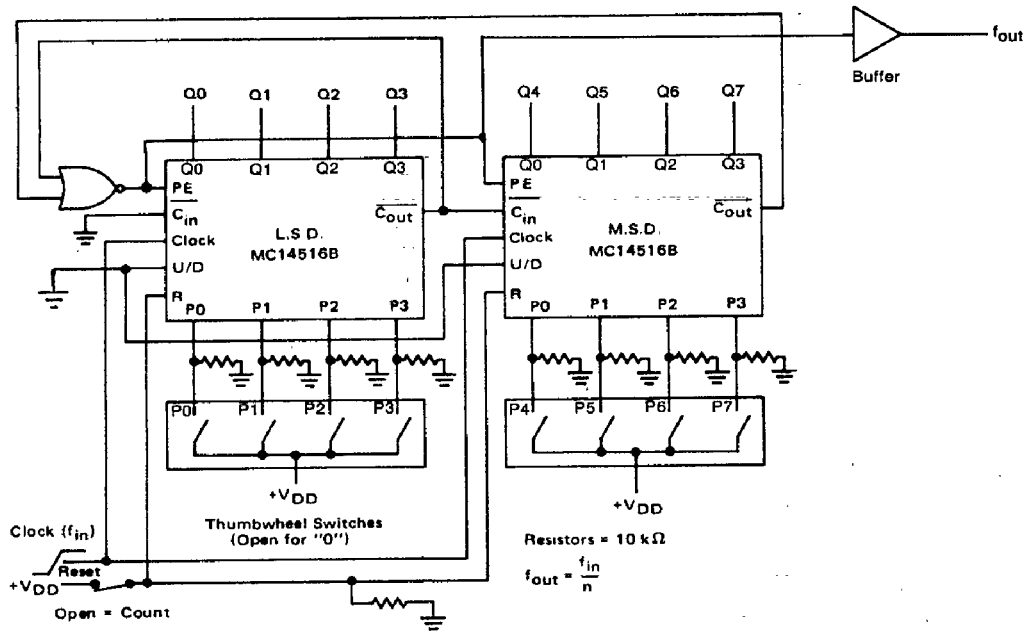
Note: The programmable frequency divider can be set by applying the desired divide ratio, in binary, to the preset inputs. For example, the maximum divide ratio of 255 may be obtained by applying a 1111 1111 to the preset inputs P0 to P7. For this divide operation, both counters should be configured in the count down mode. The divide ratio of zero is an undefined state and should be avoided.

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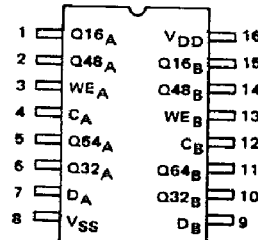L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP   Plastic
MC14XXXBCL   Ceramic
MC14XXXBDW   SOIC

$T_A = -55°$ to $125°C$ for all packages.

DUAL 64-BIT STATIC SHIFT REGISTER

The MC14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to $+18.0$	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to $+150$	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

PIN ASSIGNMENT

1 — Q16$_A$	V$_{DD}$ — 16
2 — Q48$_A$	Q16$_B$ — 15
3 — WE$_A$	Q48$_B$ — 14
4 — C$_A$	WE$_B$ — 13
5 — Q64$_A$	C$_B$ — 12
6 — Q32$_A$	Q64$_B$ — 11
7 — D$_A$	Q32$_B$ — 10
8 — V$_{SS}$	D$_B$ — 9

FUNCTIONAL TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
⌐	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
⌐	1	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
⌐⌐	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
⌐⌐	1	X	High Impedance	High Impedance	High Impedance	High Impedance

X = Don't Care

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	−3.0 −0.64 −1.6 −4.2	— — — —	−2.4 −0.51 −1.3 −3.4	−4.2 −0.88 −2.25 −8.8	— — — —	−1.7 −0.36 −0.9 −2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (4.2 μA/kHz) f + I_{DD} I_T = (8.8 μA/kHz) f + I_{DD} I_T = (13.7 μA/kHz) f + I_{DD}							μAdc
Three-State Leakage Current	I_{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* ($C_L = 50$ pF, $T_A = 25°C$)

| Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5\ ns/pF)\ C_L + 25\ ns$ $t_{TLH}, t_{THL} = (0.75\ ns/pF)\ C_L + 12.5\ ns$ $t_{TLH}, t_{THL} = (0.55\ ns/pF)\ C_L + 9.5\ ns$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7\ ns/pF)\ C_L + 390\ ns$ $t_{PLH}, t_{PHL} = (0.66\ ns/pF)\ C_L + 177\ ns$ $t_{PLH}, t_{PHL} = (0.5\ ns/pF)\ C_L + 115\ ns$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	475 210 140	770 300 215	ns
Clock Pulse Width	t_{WH}	5.0 10 15	330 125 100	170 75 60	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.0 6.7 8.3	1.5 4.0 5.3	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15		**See Note		—
Data to Clock Setup Time	t_{su}	5.0 10 15	0 10 15	−40 −15 0	— — —	ns
Data to Clock Hold Time	t_h	5.0 10 15	150 75 35	75 25 10	— — —	ns
Write Enable to Clock Setup Time	t_{su}	5.0 10 15	400 200 110	170 65 50	— — —	ns
Write Enable to Clock Release Time	t_{rel}	5.0 10 15	380 180 100	160 55 40	— — —	ns

* The formulas given are for the typical characteristics only at 25°C.
\# Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
** When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

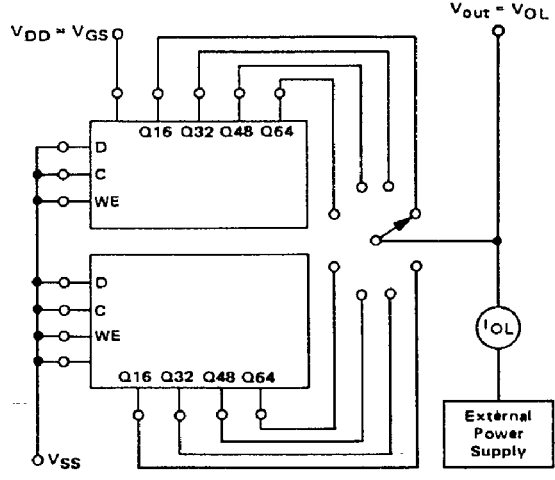**FIGURE 1 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM**
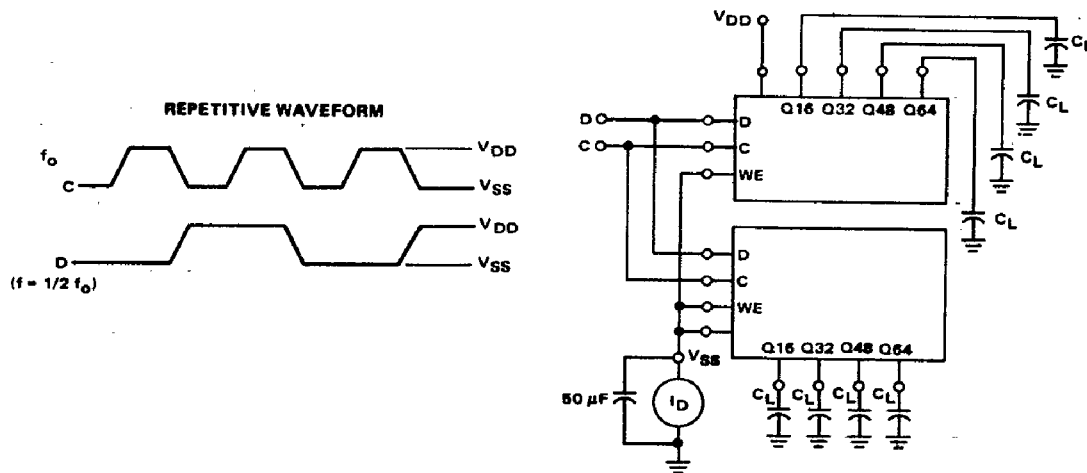
FIGURE 2 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT
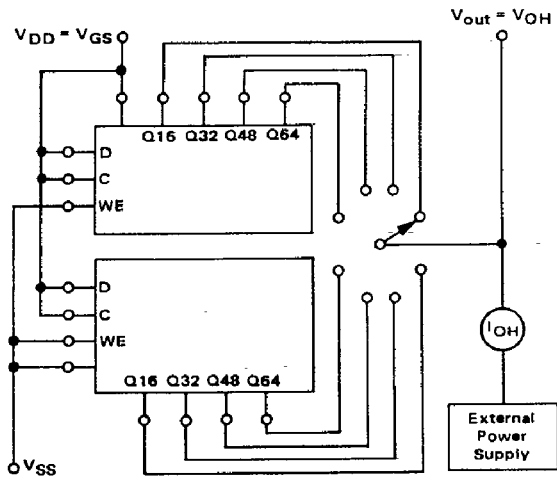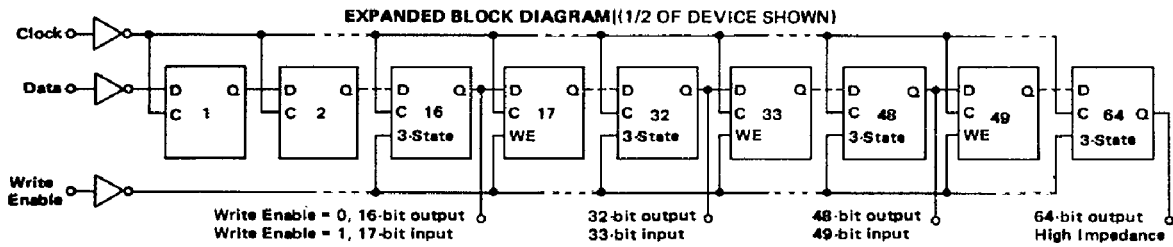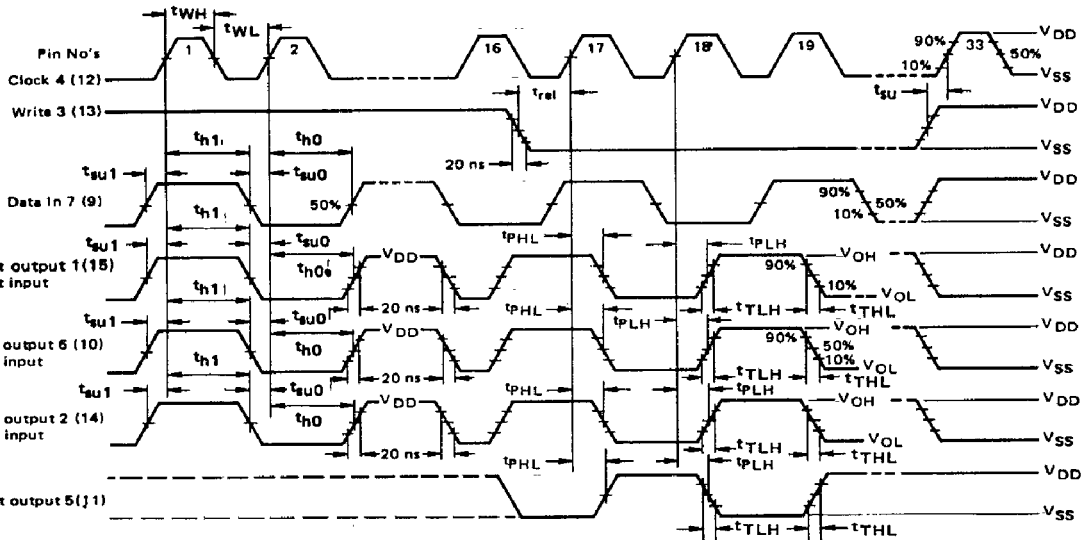

(Output being tested should be in the high-logic state).

FIGURE 3 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT

(Output being tested should be in the low-logic state).

FIGURE 4 – AC TEST WAVEFORMS

EXPANDED BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)

Write Enable = 0, 16-bit output
Write Enable = 1, 17-bit input

32-bit output
33-bit input

48-bit output
49-bit input

64-bit output
High Impedance

MOTOROLA

DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual bi-nary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with inter-changeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascad-ing multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition on Enable
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648
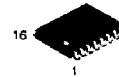
DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

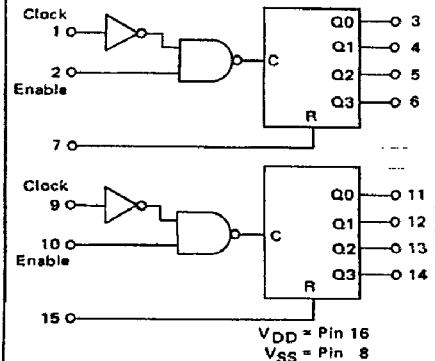MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A = −55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⌐	1	0	Increment Counter
0	⌐	0	Increment Counter
⌐	X	0	No Change
X	⌐	0	No Change
⌐	0	0	No Change
1	⌐	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

BLOCK DIAGRAM

Clock 1
Enable 2
7
Q0 → 3
Q1 → 4
Q2 → 5
Q3 → 6

Clock 9
Enable 10
15
Q0 → 11
Q1 → 12
Q2 → 13
Q3 → 14

V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precau-tions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.
Unused inputs must always be tied to an ap-propriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14518B•MC14520B

Characteristic	Symbol	V_{DD} Vdc	−55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level $(V_O = 4.5$ or 0.5 Vdc) $(V_O = 9.0$ or 1.0 Vdc) $(V_O = 13.5$ or 1.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level $(V_O = 0.5$ or 4.5 Vdc) $(V_O = 1.0$ or 9.0 Vdc) $(V_O = 1.5$ or 13.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current $(V_{OH} = 2.5$ Vdc) Source $(V_{OH} = 4.6$ Vdc) $(V_{OH} = 9.5$ Vdc) $(V_{OH} = 13.5$ Vdc)	I_{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mAdc
		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
$(V_{OL} = 0.4$ Vdc) Sink $(V_{OL} = 0.5$ Vdc) $(V_{OL} = 1.5$ Vdc)	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance $(V_{in} = 0)$	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.6\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (1.2\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (1.7\ \mu A/kHz)\ f + I_{DD}$							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
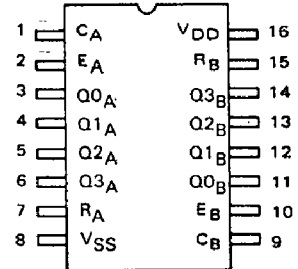
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.002.

PIN ASSIGNMENT

1	C_A	V_{DD}	16
2	E_A	R_B	15
3	$Q0_A$	$Q3_B$	14
4	$Q1_A$	$Q2_B$	13
5	$Q2_A$	$Q1_B$	12
6	$Q3_A$	$Q0_B$	11
7	R_A	E_B	10
8	V_{SS}	C_B	9

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$		5.0	—	100	200	
t_{TLH}, $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$		10	—	50	100	
t_{TLH}, $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q/Enable to Q						
t_{PLH}, $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$		5.0	—	280	560	
t_{PLH}, $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$		10	—	115	230	
t_{PLH}, $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$		15	—	80	160	
Reset to Q	t_{PHL}					ns
$t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$		5.0	—	330	650	
$t_{PHL} = (0.66 \text{ ns/pF}) C_L + 117 \text{ ns}$		10	—	130	230	
$t_{PHL} = (0.66 \text{ ns/pF}) C_L + 95 \text{ ns}$		15	—	90	170	
Clock Pulse Width	$t_{w(H)}$	5.0	200	100	—	ns
	$t_{w(L)}$	10	100	50	—	
		15	70	35	—	
Clock Pulse Frequency	f_{cl}	5.0	—	2.5	1.5	MHz
		10	—	6.0	3.0	
		15	—	8.0	4.0	
Clock or Enable Rise and Fall Time	t_{THL}, t_{TLH}	5.0	—	—	15	µs
		10	—	—	5	
		15	—	—	4	
Enable Pulse Width	$t_{WH(E)}$	5.0	440	220	—	ns
		10	200	100	—	
		15	140	70	—	
Reset Pulse Width	$t_{WH(R)}$	5.0	280	125	—	ns
		10	120	55	—	
		15	90	40	—	
Reset Removal Time	t_{rem}	5.0	−5	−45	—	ns
		10	15	−15	—	
		15	20	−5	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM
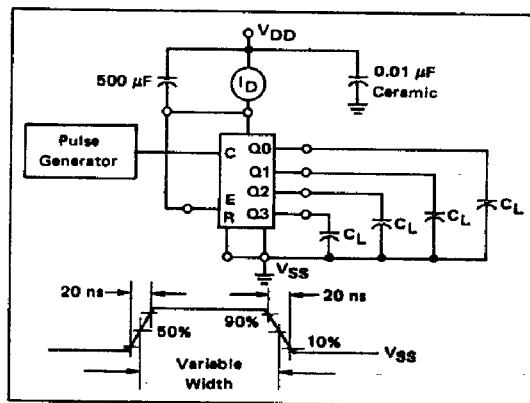
MC14518B•MC14520B
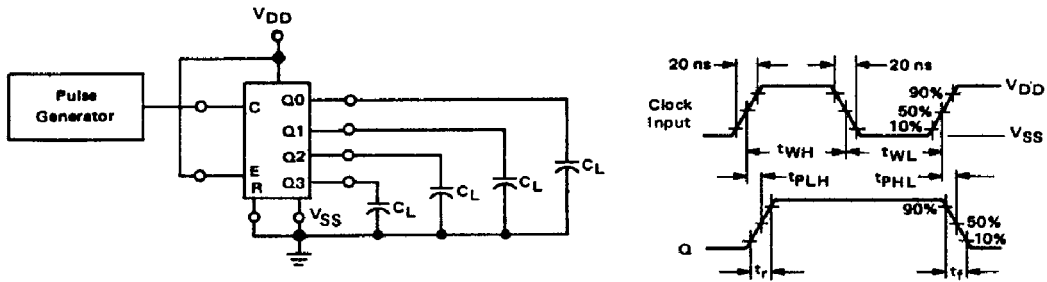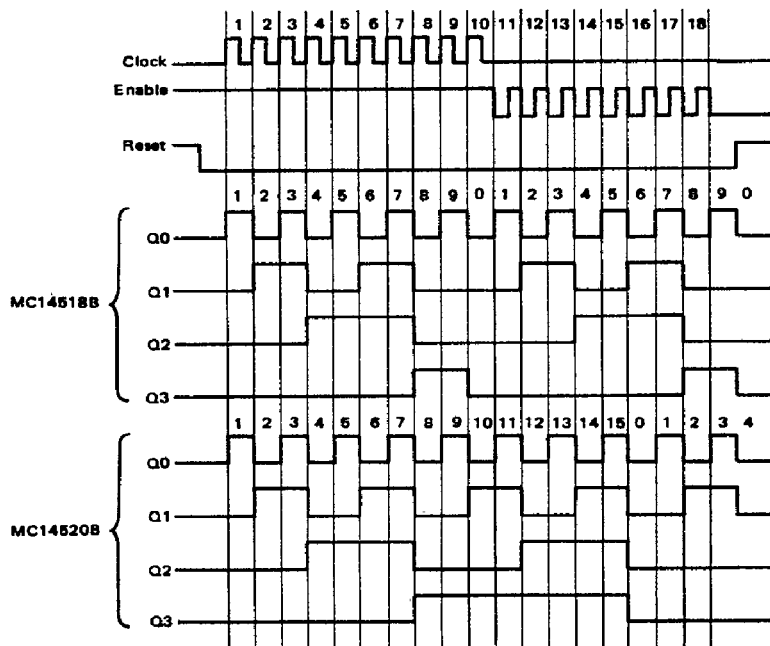
FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

FIGURE 3 — TIMING DIAGRAM

MC14518B•MC14520B

FIGURE 4 — DECADE COUNTER (MC14518B) LOGIC DIAGRAM
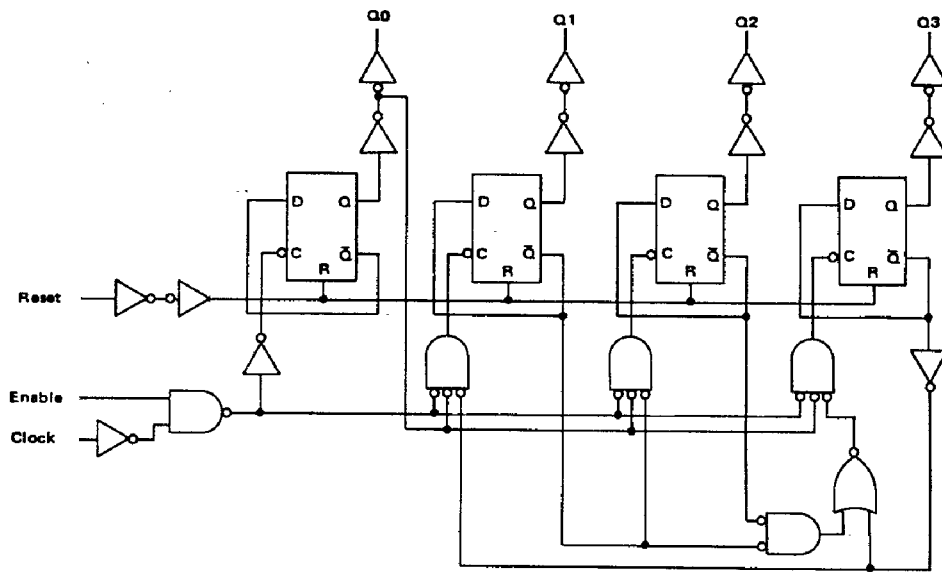**(1/2 OF DEVICE SHOWN)**

FIGURE 5 — BINARY COUNTER (MC14520B) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)

6-296